HX6639, a linear Hall-effect sensor, is composed of Hall sensor, linear amplifier and Totem-Pole output stage. It features low noise output, which makes it unnecessary to use external filtering. It also can provide increased temperature stability and accuracy. The linear Hall sensor has a wide operating temperature range of -40°C to +125°C, appropriate for commercial, consumer, and industrial environments.

The high sensitivity of Hall-effect sensor accurately tracks extremely weak changes in magnetic flux density. The linear sourcing output voltage is set by the supply voltage and in proportion of vary of the magnetic flux density. Typical operation current is 2.5 mA and operating voltage range is 2.8 volts to 6.0 volts. Trim version is available for an ultra low offset products.

The three package styles available provide magnetically optimized solutions for most applications. Package types SO is an SOT-23(1.1 mm nominal height), SQ is an QFN2020-3(0.5 mm nominal height), a miniature low-profile surface-mount package, while package UA is a three-lead ultra-mini SIP for through-hole mounting.

Features and Benefits

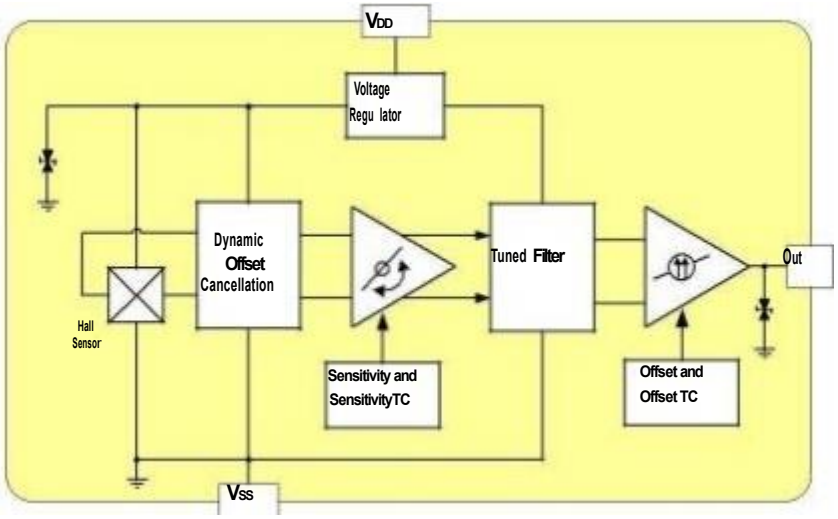
Operating Voltage Range: 2.8V~6.0V
Power consumption of 3.3mA at 5 V_{DC} for energy efficiency
Low-Noise Operation
Linear output for circuit design flexibility Totem-Pole for a stable and accurate output Responds to either positive or negative gauss
Magnetically Optimized Package for UA,SQ,SO Trim version is precise on offset
Robust ESD performance
RoHS compliant 2011/65/EU and Halogen Free

Applications

Current sensing Motor control Position sensing
Magnetic code reading
Rotary encoder
Ferrous metal detector
Vibration sensing
Liquid level sensing
Weight sensing

Part No.	Temperature Suffix	Package Type
HX6639IUA-A	I (-40°C to +105°C)	UA (TO92-3L)
HX6639IUA-B	I (-40°C to +105°C)	UA (TO92-3L)
HX6639IUA-C	I (-40°C to +105°C)	UA (TO92-3L)
HX6639IUA-D	I (-40°C to +105°C)	UA (TO92-3L)
HX6639ISQ-A	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISQ-B	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISQ-C	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISQ-D	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISO-A	I (-40°C to +105°C)	SO(SOT-23)
HX6639ISO-B	I (-40°C to +105°C)	SO(SOT-23)
HX6639ISO-C	I (-40°C to +105°C)	SO(SOT-23)
HX6639ISO-D	I (-40°C to +105°C)	SO(SOT-23)
HX6639IUA-A-T	I (-40°C to +105°C)	UA (TO92-3L)
HX6639IUA-B-T	I (-40°C to +105°C)	UA (TO92-3L)
HX6639IUA-C-T	I (-40°C to +105°C)	UA (TO92-3L)
HX6639IUA-D-T	I (-40°C to +105°C)	UA (TO92-3L)
HX6639ISQ-A-T	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISQ-B-T	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISQ-C-T	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISQ-D-T	I (-40°C to +105°C)	SQ (QFN2020-3)
HX6639ISO-A-T	I (-40°C to +105°C)	SO(SOT-23)
HX6639ISO-B-T	I (-40°C to +105°C)	SO(SOT-23)
HX6639ISO-C-T	I (-40°C to +105°C)	SO(SOT-23)
HX6639ISO-D-T	I (-40°C to +105°C)	SO(SOT-23)

Functional Diagram



Absolute Maximum Ratings At (Ta=25℃)

Characteristics		Values	Unit
Supply Voltage (***VDD***)		8	V
Reverse Voltage, (***VDDR***)		-0.5	V
Output Voltage,(***Vout***)		8	V
Output current, (***IOUT***)		5	mA
Operating Temperature Range, (***TA***)		-40 ~ +125	℃
Storage temperature Range, (***TS***)		-65 ~ +150	℃
Maximum Junction Temp,(TJ)		150	℃
Thermal Resistance	UA/SO/SQ	206/543/543	℃/W
	UA/SO/SQ	148/410/410	℃/W
Package Power Dissipation, (*PD*)	UA/SO/SQ	606/230/230	mW

***Note**: Do not apply reverse voltage to VDD and VOUT Pin, It may be caused for Miss function or damaged device.*

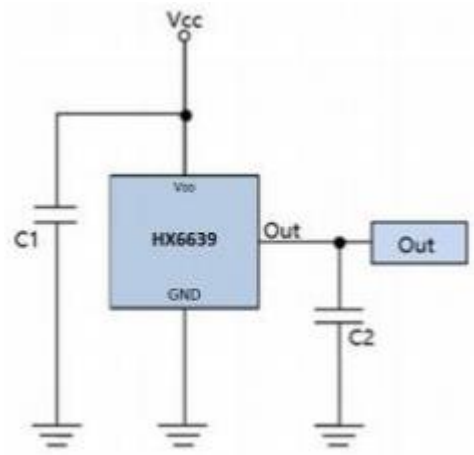
Electrical Specifications

DC Operating Parameters : T_A=+25℃, V_{CC}=5.0V

Parameters	Test Conditions		Min	Typ	Max	Units
Supply Voltage,(*VDD*)	Operating		2.8		6.0	V
Supply Current,(*IDD*)	B= 0 Gauss			3.3	5.0	mA
Output Current,(*IO*)	VDD > 3V		1.0	1.5		mA
Null Output Voltage,(*VNULL*)	A	B= 0 Gauss, (T Type)	2.375 (2.475)	2.5	2.625 (2.525)	V
	B	B= 0 Gauss, (T Type)	2.35 (2.45)	2.5	2.65 (2.55)	V
	C	B= 0 Gauss, (T Type)	2.325 (2.400)	2.5	2.675 (2.600)	V
	D	B= 0 Gauss, (T Type)	2.275 (2.375)	2.5	2.725 (2.625)	V
High Output Voltage, (*VOH*)	B> Max Magnetic Gauss			4.9	4.99	V

Low Output Voltage, (V_{OL})	B> Min Magnetic Gauss		0.01	0.1		V
Output Voltage Span,(V_{OS})				4.8		V
Output Referred Noise, (V_{ON})	Ta=25°C, output open			20		mV
Power-On Time, (T_P)					100	uS
Output Switch Time, (T_{SW})					150	uS
Output Switch Frequency, (F_{SW})			3			kHz
Magnetic Range Gauss	A			±600		Gauss
	B			±343		Gauss
	C			±240		Gauss
	D			±185		Gauss
Ratiometry Null output error, (R_{VON})	Operating voltage range relative to 5V			±1.5		%
Ratiometry Sensitivity error, (R_{SEN})	Operating voltage range relative to 5V			±1.5		%
Linearity, (*LIN*)	% of Span			±1.5		%
Sensitivity	A	Standard, (T type)	3.68 (3.80)	4.0	4.32 (4.20)	mV/G
	B	Standard, (T type)	6.44 (6.65)	7.0	7.56 (7.35)	mV/G
	C	Standard, (T type)	9.0 (9.5)	10.0	10.8 (10.5)	mV/G
	D	Standard, (T type)	11.7 (12.35)	13.0	14.3 (13.65)	mV/G
Sensitivity Temperature Coefficient, (TC_{Sens})	Ta=105°C, relative to Sens@25°C			±0.1		%/°C
Deltanull voltage,(ΔV_{ON})	Ta=105°C, relative to V_{ON} @25°C			20		mV
Electro-Static Discharge	HBM		4			KV

Typical application circuit

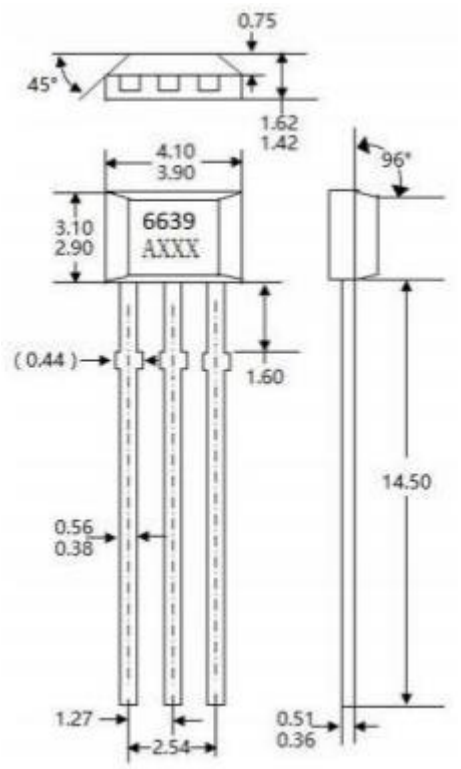


C1 : 1nF/10V
C2 : 10nF/10V

Sensor Location, Package Dimension and Marking

Package

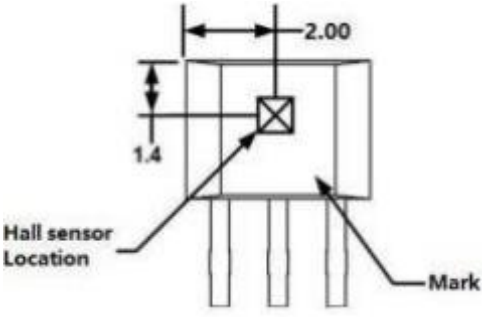
UA package



NOTES:

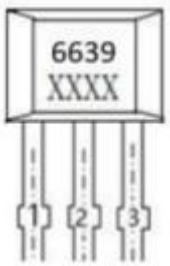
1. Controlling dimension: mm
2. Leads must be free of flash an plating voids
3. Do not bend leads within 1 mm of lead to package interface.
4. PINOUT:
   Pin 1 VCC
   Pin 2 GND
   Pin 3 Output
5. XXXX, 1st X = A/B/C/D
   2nd -4th X=Date Code

Hall Chip location

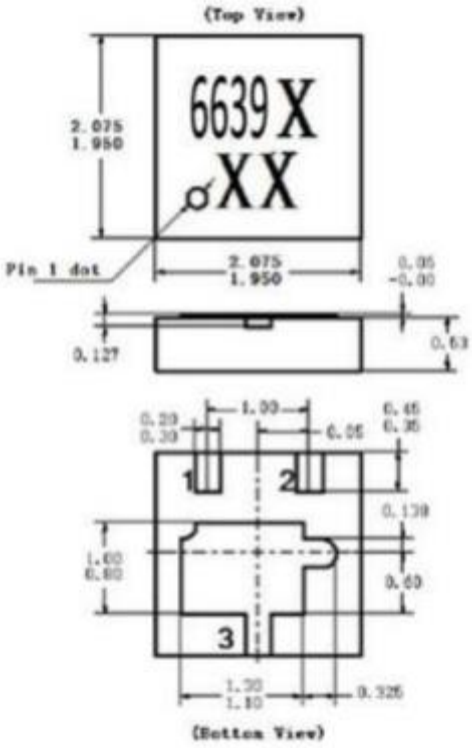


Output Pin Assignment

(Top view)



SQ Package

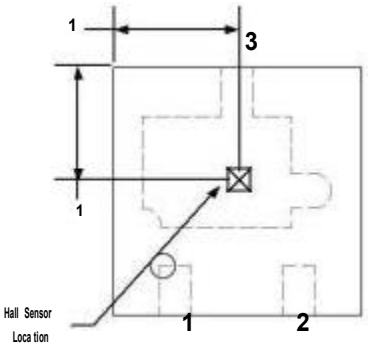


NOTES:

1. PINOUT (See Top View at left)
   Pin 1 Vcc
   Pin 2 Output
   Pin 3 GND
2. Controlling dimension: mm;
3. Chip rubbing will be 10mil maximum;
4. Chip must be in PKG. center.
5. 6639X，X=A/B/C/D
6. XX= Date code

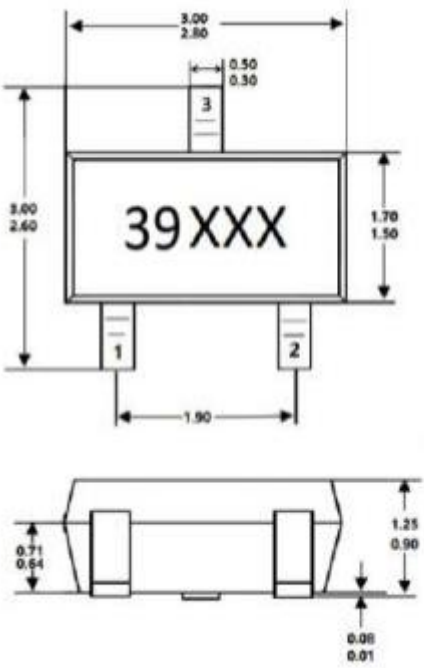
Hall Plate Chip Location

(Top view)



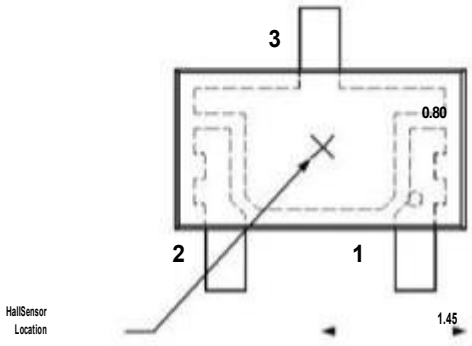
SO Package

(Top View)



Hall Plate Chip Location

(Bottom view)



NOTES:

1. PINOUT (See Top View at left :)

   Pin 1 V_{DD}

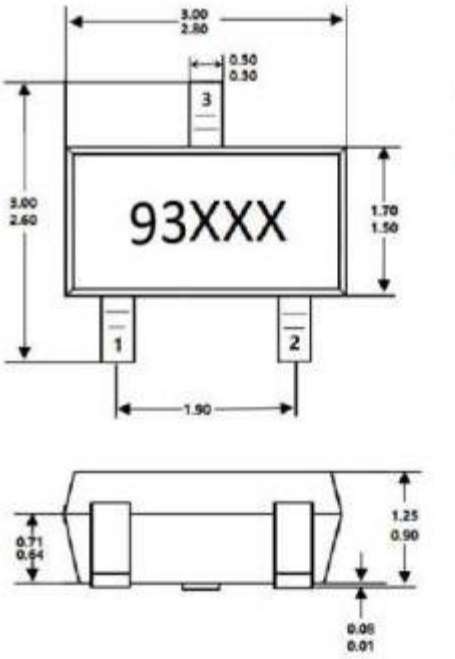
   Pin 2 Output

   Pin 3 GND

2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. Chip must be in PKG. center.
5. 39XXX , 1st X = A/B/C/D 2nd~3rd =Date Code

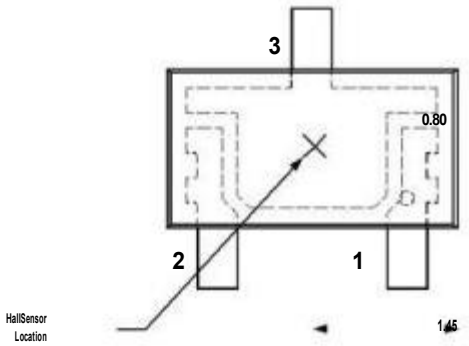
SO Package

(Top View)



Hall Plate Chip Location

(Bottom view)



NOTES:

1. PINOUT (See Top View at left :)

   Pin 1 V_{DD}

   Pin 2 Output

   Pin 3 GND

2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. Chip must be in PKG. center.
5. 93XXX , 1^{st} X = A/B/C/D 2^{nd}~3^{rd} =Date Code