

# TLE7257

LIN Transceiver

TLE7257SJ  
TLE7257LE

## Data Sheet

Rev. 1.1, 2015-08-20

## Table of Contents

|          |                                                    |           |
|----------|----------------------------------------------------|-----------|
| <b>1</b> | <b>Overview</b>                                    | <b>3</b>  |
| <b>2</b> | <b>Block Diagram</b>                               | <b>4</b>  |
| <b>3</b> | <b>Pin Configuration</b>                           | <b>5</b>  |
| 3.1      | Pin Assignment                                     | 5         |
| 3.2      | Pin Definitions and Functions                      | 5         |
| <b>4</b> | <b>Functional Description</b>                      | <b>6</b>  |
| 4.1      | Operating Modes                                    | 7         |
| 4.2      | Normal Operation Mode                              | 8         |
| 4.3      | Standby Mode                                       | 9         |
| 4.4      | Sleep Mode                                         | 10        |
| 4.5      | Bus Wake-up Event                                  | 12        |
| 4.6      | Mode Transition via EN input                       | 13        |
| 4.7      | Over-Temperature Protection                        | 14        |
| 4.8      | Undervoltage Detection                             | 15        |
| 4.9      | TxD Time-out                                       | 16        |
| 4.10     | 3.3 V and 5 V Logic Capability                     | 16        |
| 4.11     | Short Circuit                                      | 16        |
| <b>5</b> | <b>General Product Characteristics</b>             | <b>17</b> |
| 5.1      | Absolute Maximum Ratings                           | 17        |
| 5.2      | Functional Range                                   | 18        |
| 5.3      | Thermal Characteristics                            | 18        |
| <b>6</b> | <b>Electrical Characteristics</b>                  | <b>19</b> |
| 6.1      | Functional Device Characteristics                  | 19        |
| 6.2      | Diagrams                                           | 23        |
| <b>7</b> | <b>Application Information</b>                     | <b>24</b> |
| 7.1      | Application Example                                | 24        |
| 7.2      | ESD Susceptibility according to IEC61000-4-2       | 25        |
| 7.3      | Transient Robustness according to ISO 7637-2       | 25        |
| 7.4      | LIN Physical Layer Compatibility                   | 25        |
| 7.5      | TxD Fail-Safe Input                                | 25        |
| 7.6      | RxD Pull-up Resistor                               | 26        |
| 7.7      | Compatibility with other Infineon LIN Transceivers | 27        |
| <b>8</b> | <b>Package Outlines</b>                            | <b>29</b> |
| <b>9</b> | <b>Revision History</b>                            | <b>30</b> |

**TLE7257SJ**  
**TLE7257LE**

**1 Overview**
**Features**

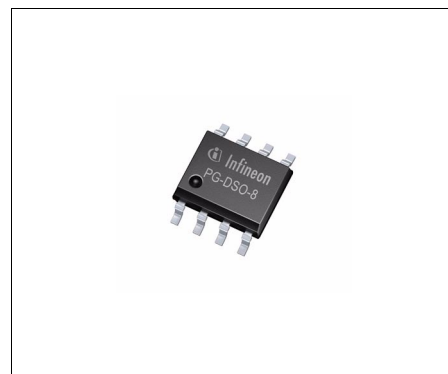
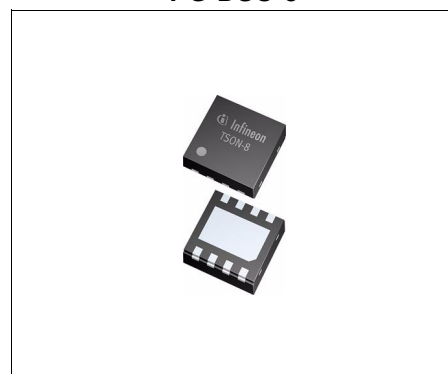
- Single-wire LIN transceiver for transmission rates up to 20 kbps
- Compliant to ISO 17987-4, LIN Specification 2.2A and SAE J2602
- Very low current consumption in Sleep mode with wake-up capability
- Very low leakage current on the BUS pin
- Digital I/O levels compatible with 3.3 V and 5 V microcontrollers
- Tx/D protected with dominant time-out function and state check after mode change to Normal Operation mode
- BUS short to  $V_{BAT}$  protection and BUS short to GND handling
- Over temperature protection and supply undervoltage detection
- Very high ESD robustness,  $\pm 10$  kV according to IEC61000-4-2
- Optimized for high electromagnetic compatibility (EMC);  
Very low emission and high immunity to interference
- Available in standard PG-DSO-8 and leadless PG-TSON-8 packages
- PG-TSON-8 package supports Automated Optical Inspection (AOI)
- Green Product (RoHS compliant)
- AEC Qualified

**Description**

The TLE7257 is a transceiver for the Local Interconnect Network (LIN) with integrated wake-up and protection features. It is designed for in-vehicle networks using data transmission rates up to 20 kbps. The TLE7257 operates as a bus driver between the protocol controller and the physical bus of the LIN network. Compliant to all LIN standards and with a wide operational supply range the TLE7257 can be used in all automotive applications.

The usage of different operation modes and the INH output allows the TLE7257 to control external components like e.g. voltage regulators. In Sleep mode the TLE7257 draws typically less than 10  $\mu$ A of quiescent current while still being able to wake-up when detecting LIN bus traffic. The very low leakage current on the BUS pin makes the TLE7257 especially suitable for partially supplied networks.

Based on the Infineon BiCMOS technology the TLE7257 provides excellent ESD robustness together with a very high electromagnetic compatibility (EMC). The TLE7257 reaches a very low level of electromagnetic emission (EME) within a broad frequency range and independent from the battery voltage. The TLE7257 is AEC qualified and tailored to withstand the harsh conditions of the automotive environment.


**PG-DSO-8**

**PG-TSON-8**

| Type      | Package   | Marking |
|-----------|-----------|---------|
| TLE7257SJ | PG-DSO-8  | 7257    |
| TLE7257LE | PG-TSON-8 | 7257    |

## 2 Block Diagram

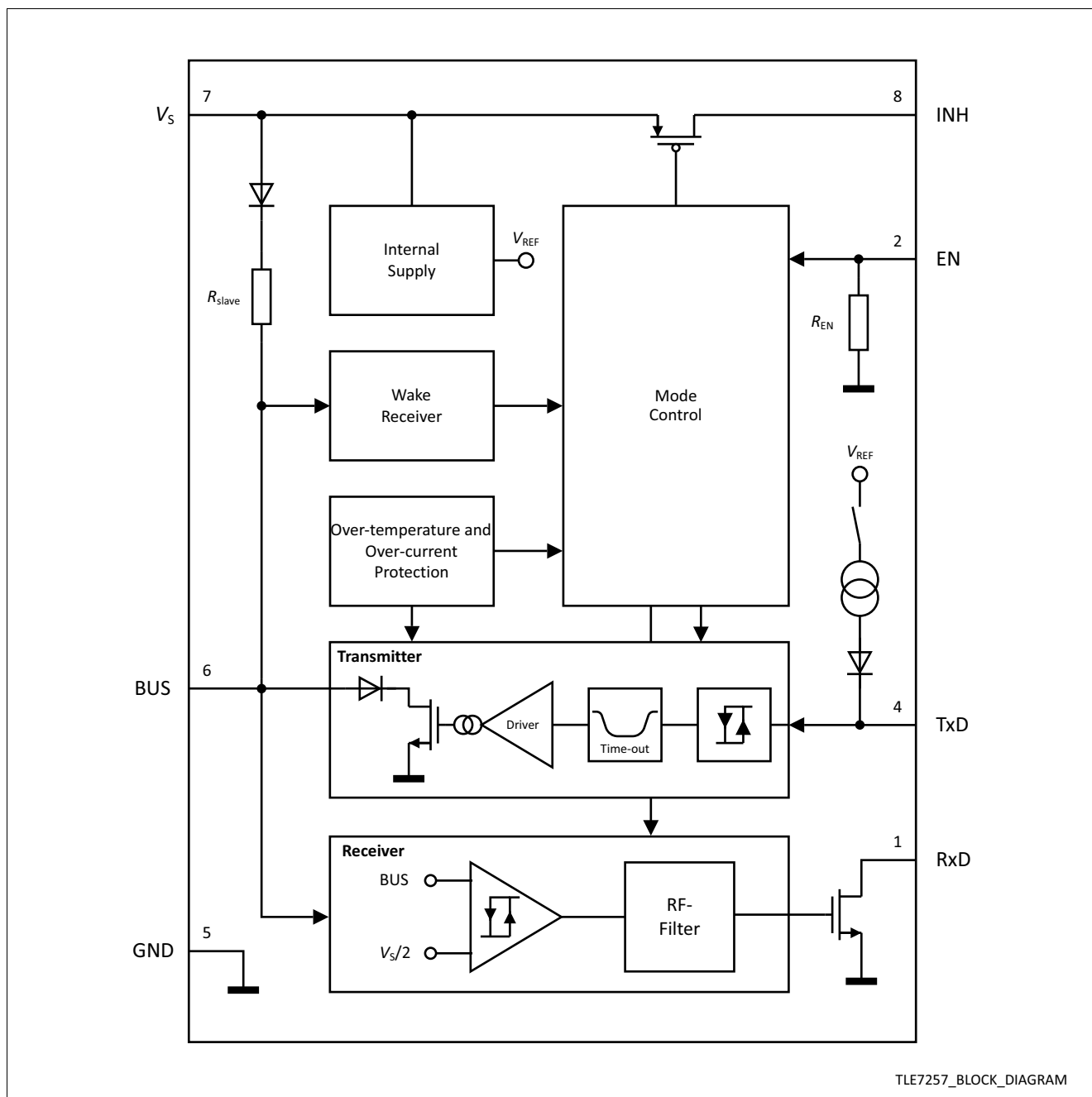


Figure 1 Block diagram

## 3 Pin Configuration

### 3.1 Pin Assignment

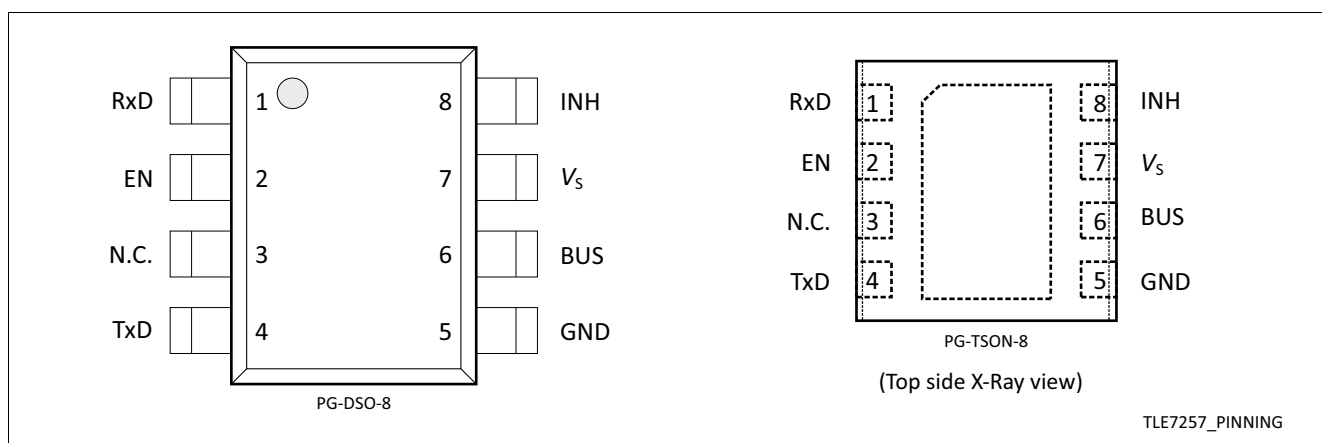


Figure 2 Pin configuration

### 3.2 Pin Definitions and Functions

| Pin               | Symbol | Function                                                                                                                                                       |
|-------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                 | RxD    | <b>Receive data output;</b><br>External pull-up necessary<br>Monitors the LIN bus signal in Normal Operation mode<br>Indicates a wake-up event in Standby mode |
| 2                 | EN     | <b>Enable input;</b><br>Integrated pull-down resistor<br>Logical "high" to select Normal Operation mode                                                        |
| 3                 | N.C.   | <b>Not Connected</b>                                                                                                                                           |
| 4                 | TxD    | <b>Transmit data input;</b><br>Integrated pull-up current source<br>Logical "low" to drive a "dominant" signal on the LIN bus                                  |
| 5                 | GND    | <b>Ground</b>                                                                                                                                                  |
| 6                 | BUS    | <b>Bus input / output;</b><br>Integrated LIN slave termination                                                                                                 |
| 7                 | $V_s$  | <b>Battery supply input;</b><br>100 nF decoupling capacitor required                                                                                           |
| 8                 | INH    | <b>Inhibit output;</b><br>Battery supply related output<br>Active in Normal Operation mode and Standby mode                                                    |
| PAD <sup>1)</sup> | –      | Connect to PCB heat sink area. Do not connect to other voltage potential than GND                                                                              |

1)Only for PG-TSON-8 package version (TLE7257LE)

## 4 Functional Description

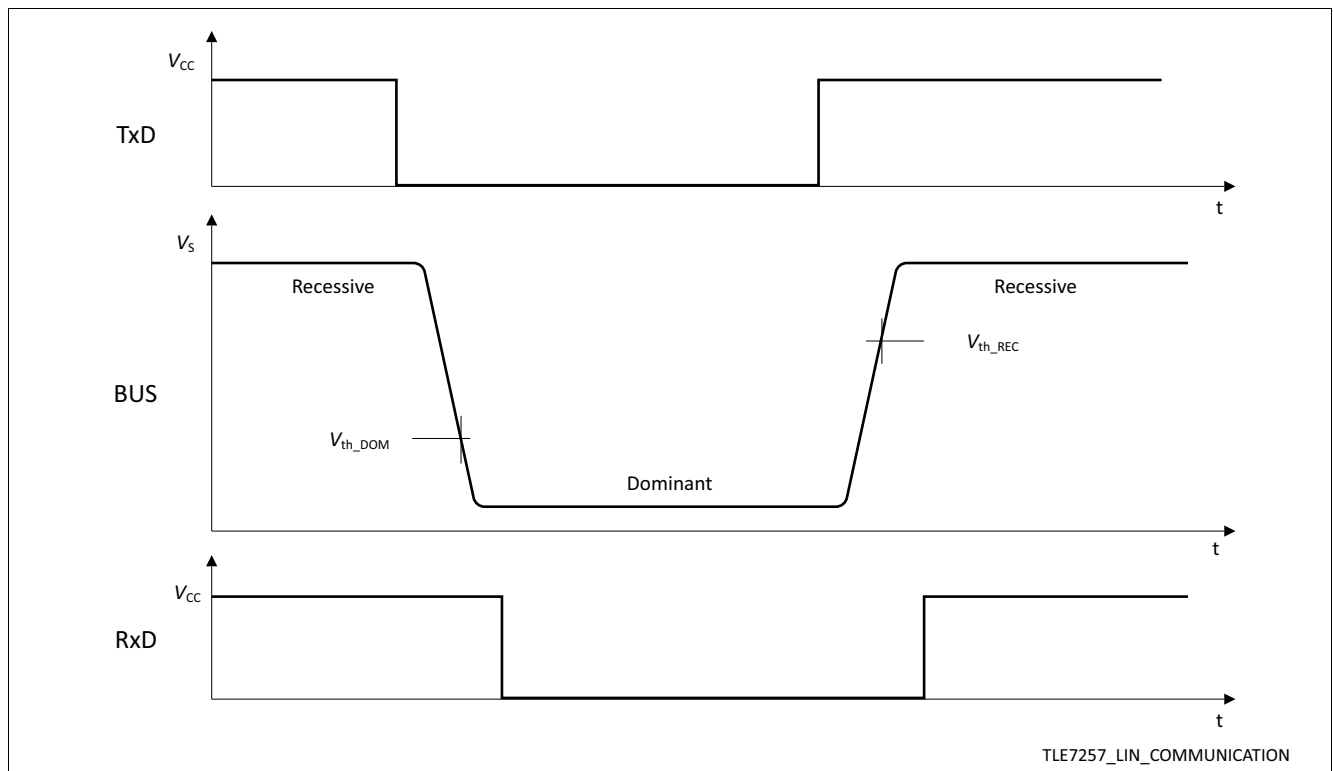
The LIN interface is a single wire, bi-directional bus, used for in-vehicle networks. The TLE7257 LIN transceiver is the interface between the microcontroller and the physical LIN Bus (see [Figure 16](#)). Data from the microcontroller is driven to the LIN bus via the TxD input of the TLE7257. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rates in order to minimize the electromagnetic emission level of the LIN network. The RxD output reads back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise from the LIN bus and to increase the electromagnetic immunity level of the transceiver.

The LIN specification defines two valid bus states (see [Figure 3](#)):

- “Dominant” state with the LIN bus voltage level near GND.
- “Recessive” state with the LIN bus voltage pulled up to the supply voltage  $V_S$  through the bus termination.

By setting the TxD input of the TLE7257 to a logical “low” signal, the transceiver generates a “dominant” level on the BUS interface pin. The receiver reads back the signal on the LIN bus and indicates the “dominant” LIN bus signal with a logical “low” level on the RxD output to the microcontroller. By setting the TxD input to logical “high”, the transceiver sets the LIN interface pin to the “recessive” level. At the same time the “recessive” level on the LIN bus is indicated by a logical “high” level on the RxD output.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE7257 for master node applications, a termination resistor of 1 k $\Omega$  and a diode must be connected between the LIN bus and the power supply  $V_S$  (see [Figure 16](#)).



**Figure 3** LIN bus signals

## 4.1 Operating Modes

The TLE7257 has 3 major operation modes (see [Figure 4](#)):

- Normal Operation mode
- Standby mode
- Sleep mode

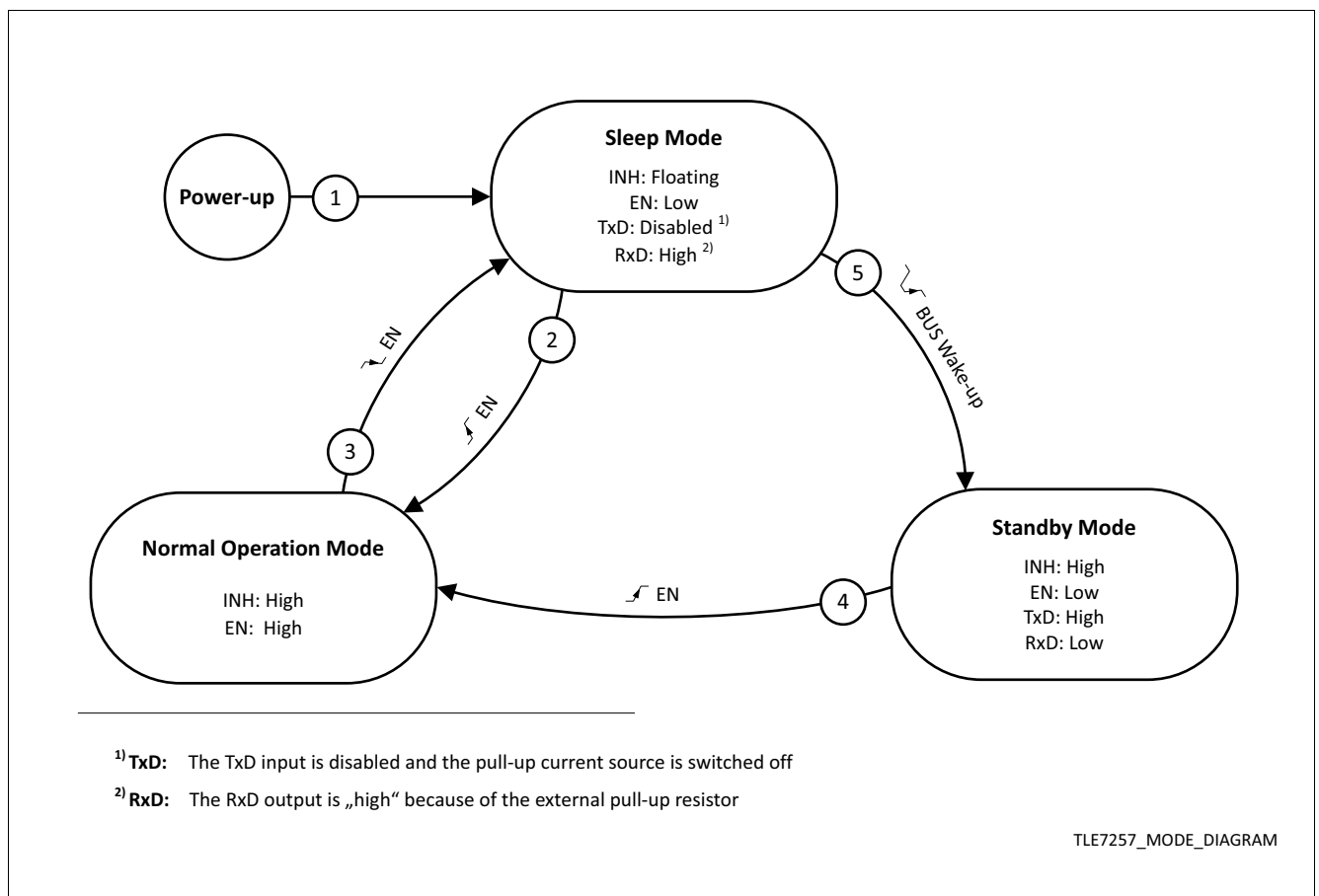
**Table 1 Operating modes**

| Mode             | EN   | INH      | TxD                   | RxD                | LIN Bus Termination | Comments                                                                |
|------------------|------|----------|-----------------------|--------------------|---------------------|-------------------------------------------------------------------------|
| Sleep            | Low  | Floating | Disable <sup>1)</sup> | High <sup>2)</sup> | 30 kΩ (typical)     | No wake-up request detected                                             |
| Standby          | Low  | High     | High <sup>3)</sup>    | Low                | 30 kΩ (typical)     | –                                                                       |
| Normal Operation | High | High     | Low<br>High           | Low<br>High        | 30 kΩ (typical)     | RxD reflects the signal on the bus<br>TxD driven by the microcontroller |

1) The TxD input is disabled in Sleep mode and the internal pull-up current source is switched off (see [Figure 1](#)).

2) A pull-up resistor to the external microcontroller supply is required.

3) In case the TxD input is open the state is internally set to logical "high" through the internal pull-up current source.



**Figure 4 Operation mode state diagram**

**Table 2**      **Operation mode transitions**

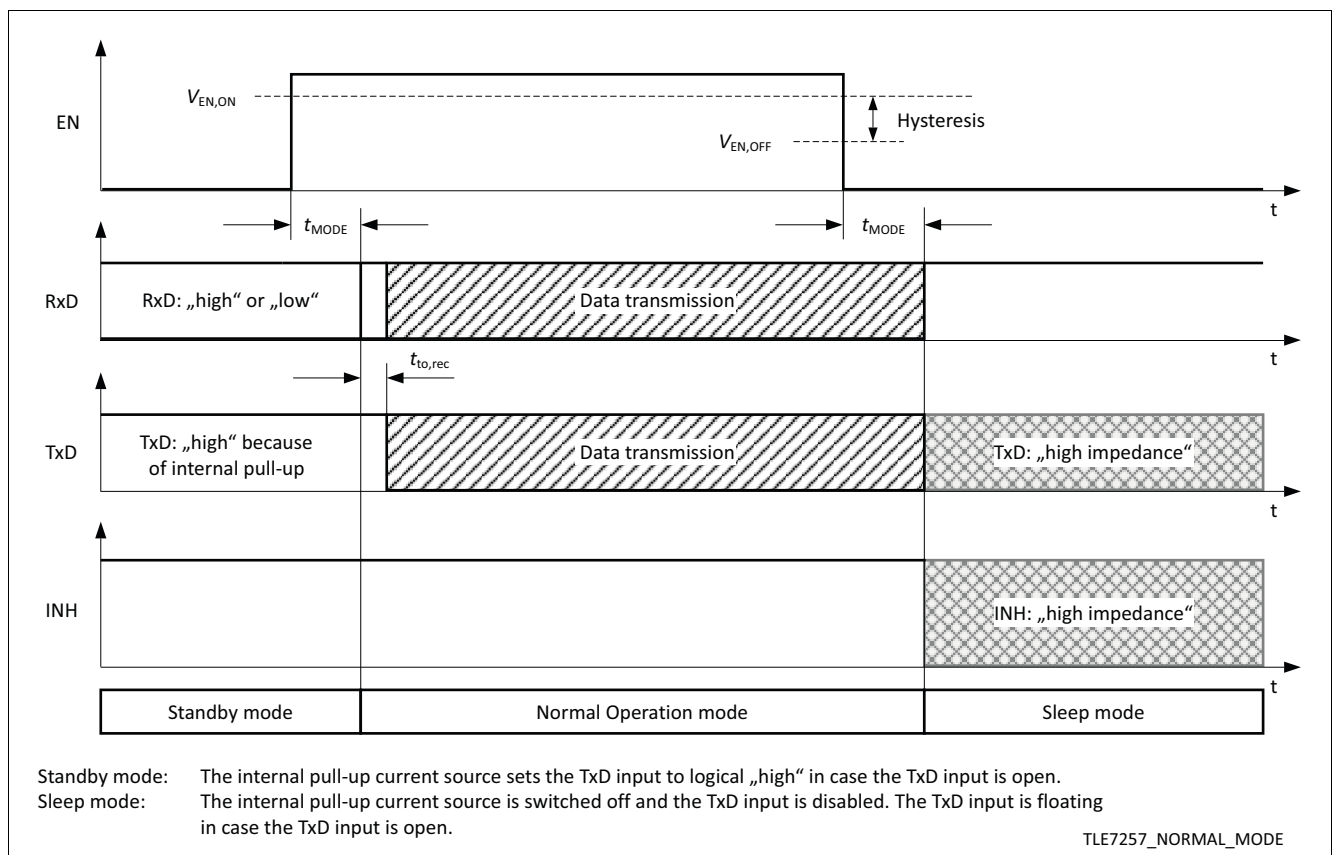
| Number | Reason for transition     | Comment                                                                     |
|--------|---------------------------|-----------------------------------------------------------------------------|
| 1      | Power-on detection        | The $V_S$ supply voltage rise above the $V_{S,UV,PON}$ power-on reset level |
| 2      | Mode change with EN input | Triggered by logical "high" level                                           |
| 3      | Mode change with EN input | Triggered by logical "low" level                                            |
| 4      | Mode change with EN input | Triggered by logical "high" level                                           |
| 5      | Bus wake-up detection     | RxD set "low" for signalling the bus wake-up event to the microcontroller   |

## 4.2 Normal Operation Mode

While operating in Normal Operation mode the LIN bus receiver and transmitter are active and support data transmission rates up to 20 kbps. Data from the microcontroller is transmitted to the LIN bus via the TxD input. Simultaneously the receiver detects the data stream on the LIN bus and forwards it to the RxD output.

Normal Operation mode can be entered from either Sleep mode (see [Figure 9](#)) or from Standby mode (see [Figure 5](#)), by setting the EN input to logical "high". From Normal Operation mode the TLE7257 can only enter Sleep mode, it is not possible to enter Standby mode directly (see [Figure 4](#)).

The transition time for mode change to Normal Operation mode  $t_{MODE}$  specifies the delay between the threshold, where the EN pin detects a "high" input signal, and the actual mode change of TLE7257 to Normal Operation mode.


**Figure 5**      **Entering Normal Operation mode from Standby mode**

While the TLE7257 is in Normal Operation mode the following functions are available:

- The transmitter is turned on; data on the TxD input are driven on the LIN bus.
- The receiver is turned on; data on the LIN bus are monitored and signaled on the RxD output.
- The BUS pin is terminated to  $V_S$  via the internal termination resistor  $R_{BUS}$  (see [Figure 1](#)).
- The TxD input is pulled up via a current source to the internal power supply of the TLE7257.
- The INH output is switched on.
- The bus wake-up comparator is turned off.
- The two-level undervoltage detection is active. In case  $V_S$  drops below the undervoltage detection level the TLE7257 blocks the transmitter and receiver. In case  $V_S$  drops below the power-on reset level  $V_{S,UV,PON}$  the TLE7257 changes the operation mode to Standby mode after recovery (see [“Undervoltage Detection” on Page 15](#)).
- The EN input is active. A “low” signal on the EN input triggers a transition to Sleep.

After a mode change to Normal Operation the TLE7257 requires a logical “high” signal for the time  $t_{to,rec}$  on the TxD input before releasing the data communication (see [Figure 5](#)). The transmitter remains deactivated as long as the signal on the TxD input remains logical “low”, preventing possible bus communication disturbance.

### 4.3 Standby Mode

The Standby mode is entered automatically after bus wake-up event.

In Standby mode no communication to the LIN bus is possible. The transmitter and the receiver are disabled.

While the TLE7257 is in Standby mode the following functions are available:

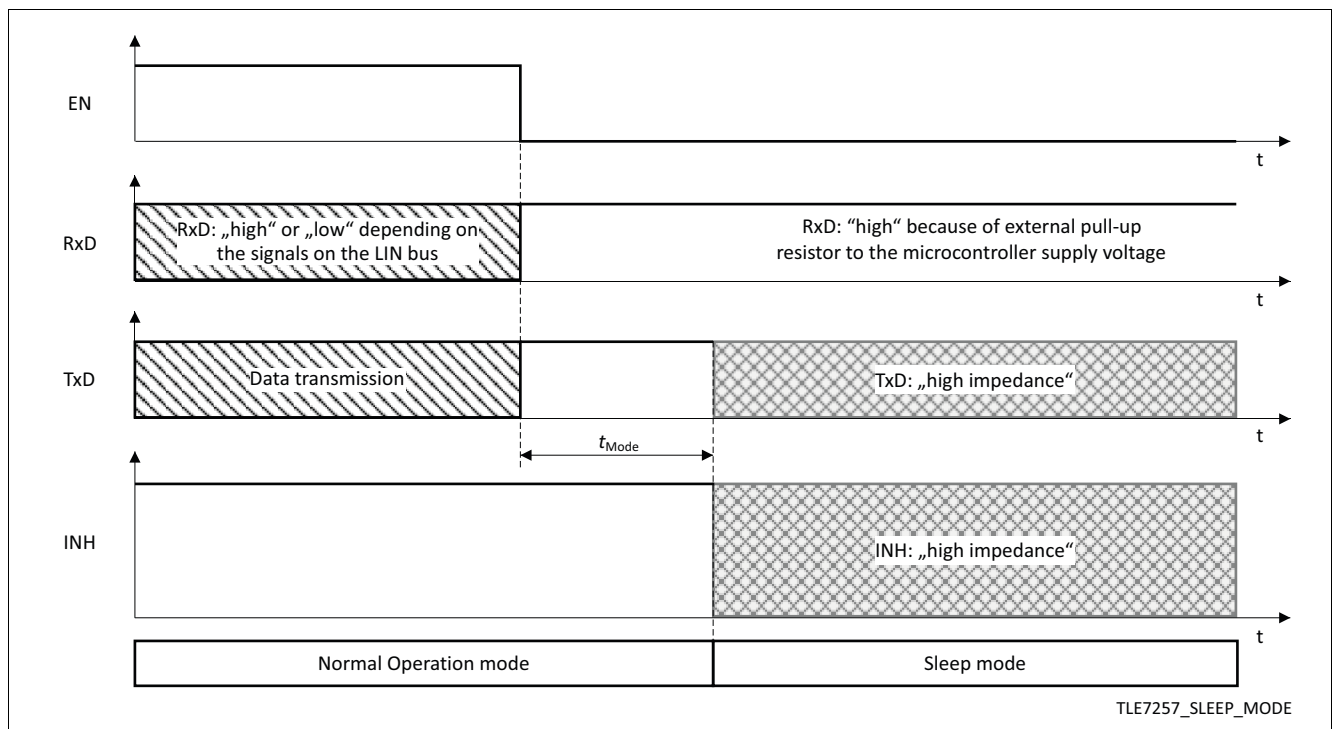
- The transmitter is turned off, the TxD input is inactive and the bus output is permanent “recessive”.
- The receiver is turned off.
- The RxD output indicates a wake-up event (see [Figure 4](#) and [Table 1](#)).
- The BUS pin is terminated to  $V_S$  via the internal termination resistor  $R_{BUS}$  (see [Figure 1](#)).
- The TxD input is pulled up with a current source to the internal power supply of the TLE7257.
- The INH output is switched on.
- In Standby mode only the power-on reset level of the undervoltage detection is active (see [“Undervoltage Detection” on Page 15](#)).
- The EN input is active. A “high” signal on the EN input triggers a transition to Normal Operation mode (see [Figure 5](#)).

#### 4.4 Sleep Mode

Sleep mode is a low power mode with quiescent current consumption reduced to a minimum while the device is still able to wake-up by a message on the LIN bus.

After a power-up event the TLE7257 enters Sleep mode by default. The EN pin has an internal pull-down resistor and the TLE7257 remains in Sleep mode until the external microcontroller applies a logical "high" signal at the EN input.

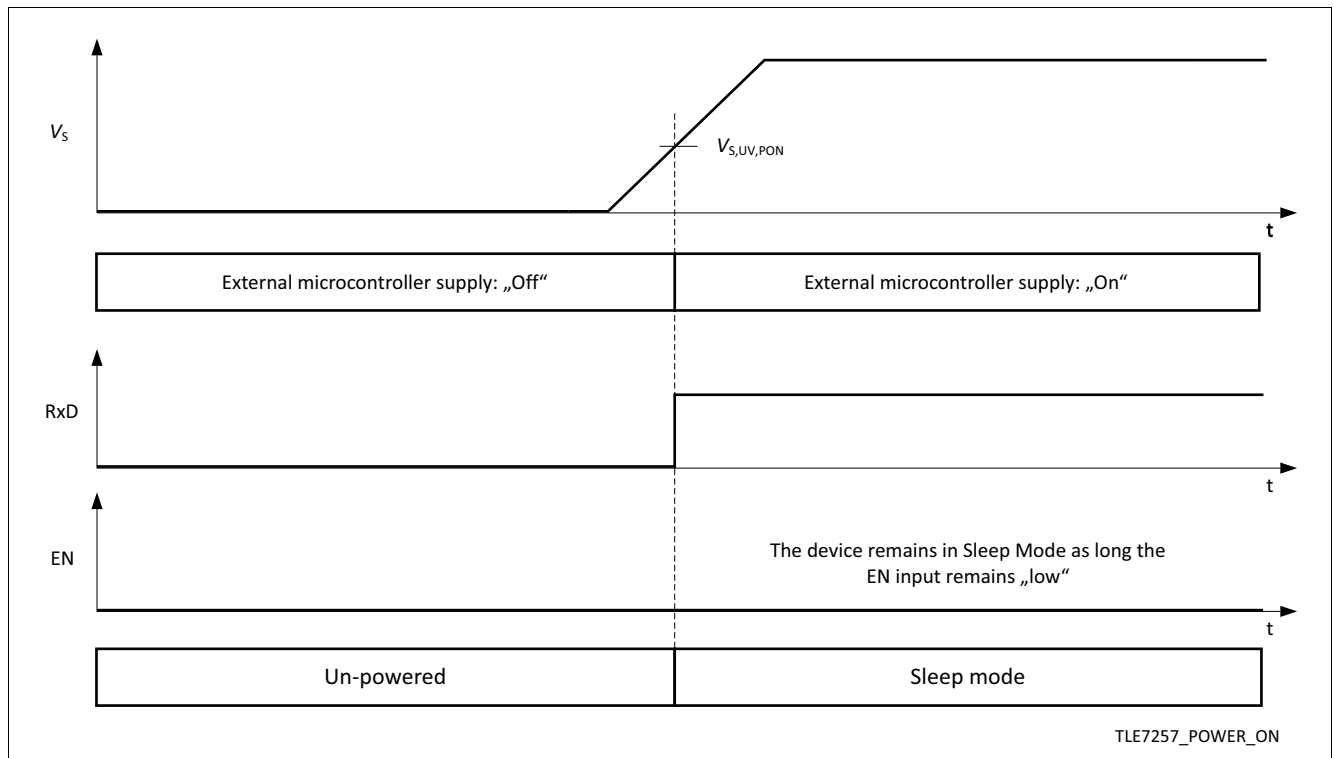
To switch the TLE7257 from Normal Operation mode to Sleep mode, the EN input has to be set to "low". Conversely a logical "high" signal on the EN input sets the device directly back to Normal Operation mode (see [Figure 4](#)). The TLE7257 can only enter Sleep mode from Normal Operation mode.



**Figure 6 Entering Sleep mode from Normal Operation mode**

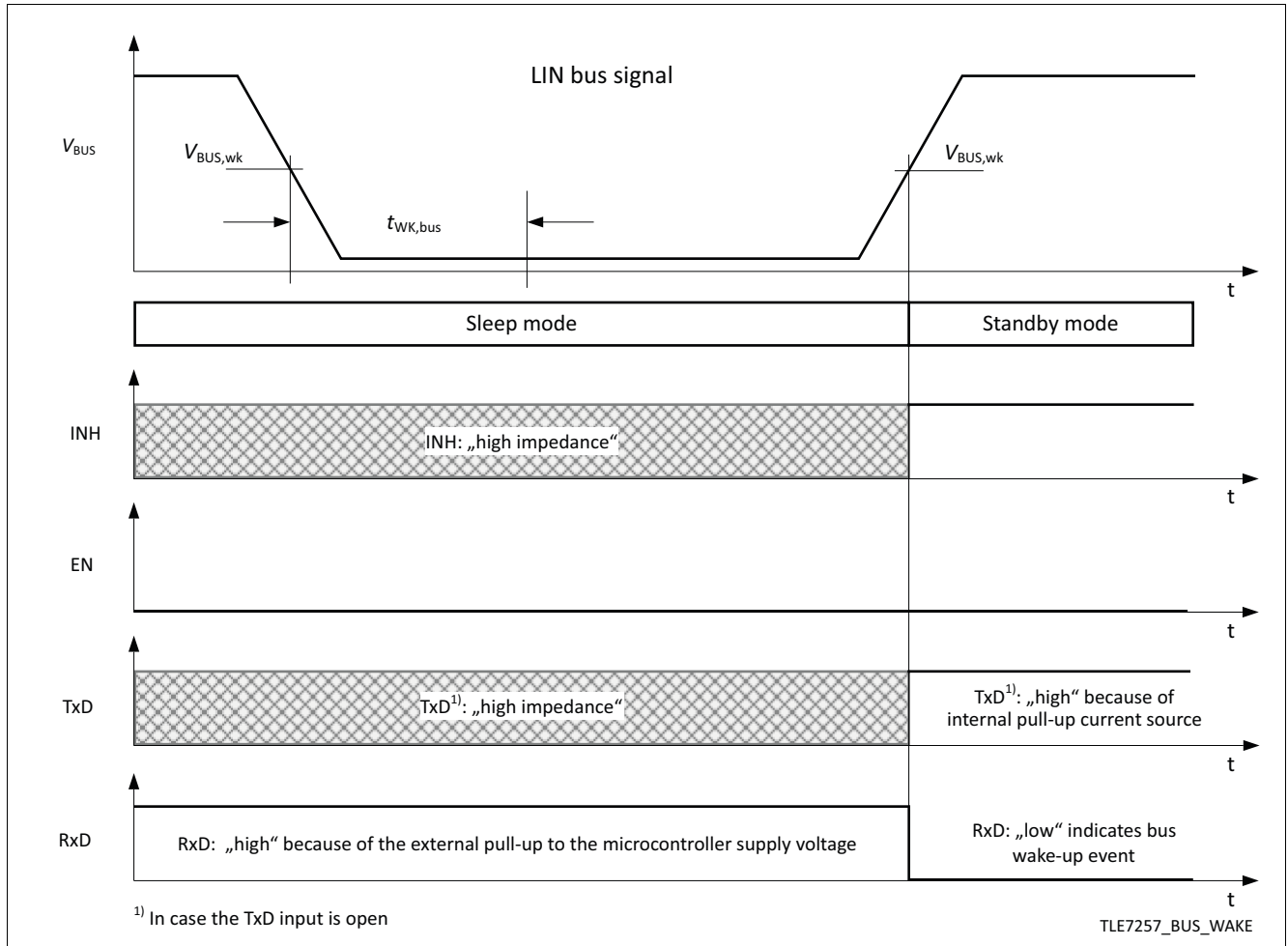
While the TLE7257 is in Sleep mode the following functions are available:

- The transmitter is turned off.
- The receiver is turned off.
- The BUS output is terminated to  $V_S$  via the internal termination resistor  $R_{BUS}$  (see [Figure 1](#)).
- The RxD output is "high" if a pull-up resistor is connected to the external microcontroller supply.
- The TxD input is disabled and the internal pull-up current source is switched off.
- The INH output is switched off and is floating.
- The bus wake-up comparator is active and will cause transition to Standby mode in case of a wake-up event.
- In Sleep mode only the power-on reset level of the undervoltage detection is active (see ["Undervoltage Detection" on Page 15](#)).
- The EN input remains active. A "high" signal on the EN input triggers a transition to Normal Operation mode.



**Figure 7** Entering Sleep mode after Power-up

## 4.5 Bus Wake-up Event

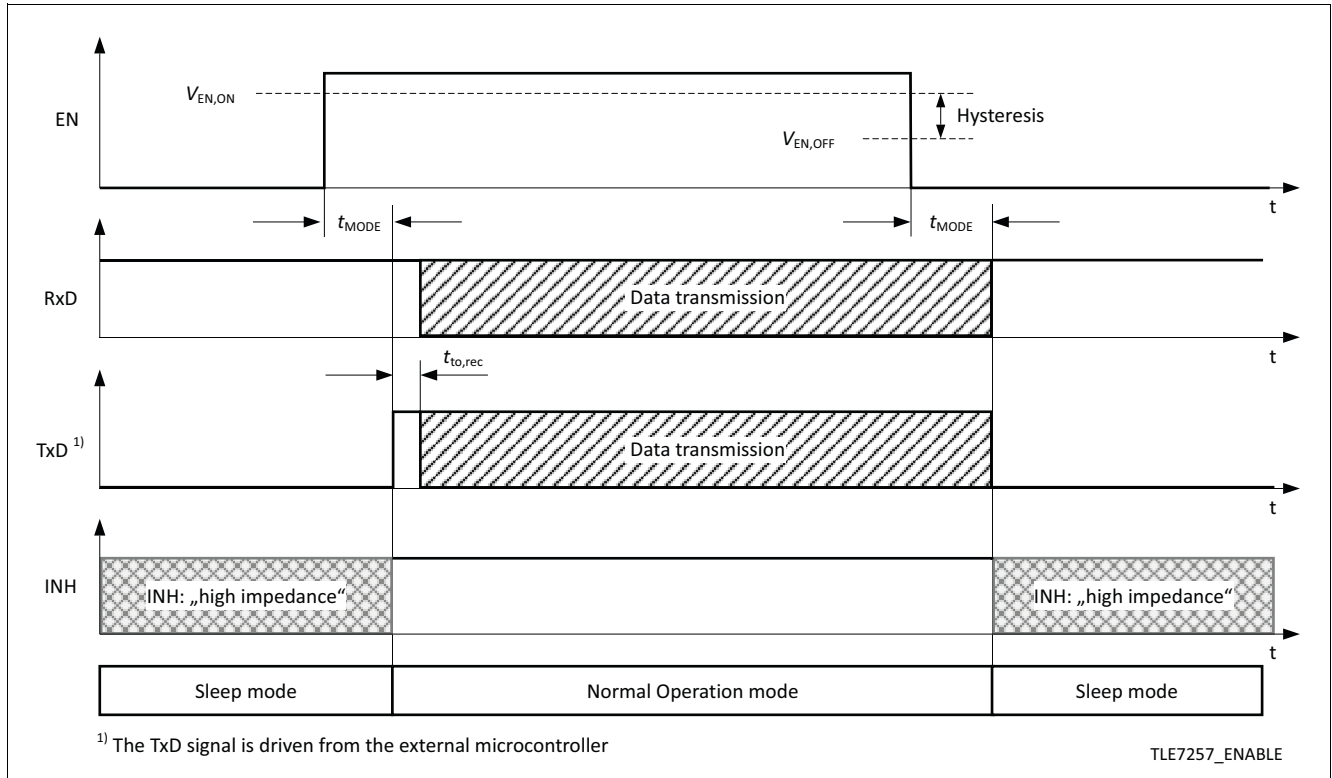


**Figure 8 Bus wake-up behavior**

A bus wake-up event, also called remote wake-up, changes the operation mode from Sleep mode to Standby mode. A falling edge on the LIN bus, followed by a "dominant" bus signal for the time  $t_{WK,bus}$  results in a bus wake-up event. The mode change to Standby mode becomes active with the following rising edge on the LIN bus. The TLE7257 remains in Sleep mode until it detects a state change on the LIN bus from "dominant" to "recessive" (see [Figure 8](#)).

In Standby mode a logical "low" signal on the RxD output indicates a bus wake-up event.

## 4.6 Mode Transition via EN input



**Figure 9 Entering Normal Operation mode from Sleep mode**

The EN input is used for operation mode control of the TLE7257. By setting the EN input logical “high” for the time  $t_{\text{MODE}}$  while being Sleep or Standby mode, a transition to Normal Operation mode will be triggered (see [Figure 9](#)). The EN input has an integrated pull-down resistor to ensure the device remains in Sleep or Standby mode even if the EN pin is left open. The EN input has an integrated hysteresis.

A signal transition from logical “high” to “low” on the EN input changes the operation mode from Normal Operation mode to Sleep mode (see [Figure 5](#)).

The TLE7257 changes the operation modes regardless of the signal on the BUS pin. In the case of a short circuit between the LIN bus and GND, resulting in a permanent “dominant” signal, the TLE7257 can be set to Sleep mode by setting the EN input to logical “low”.

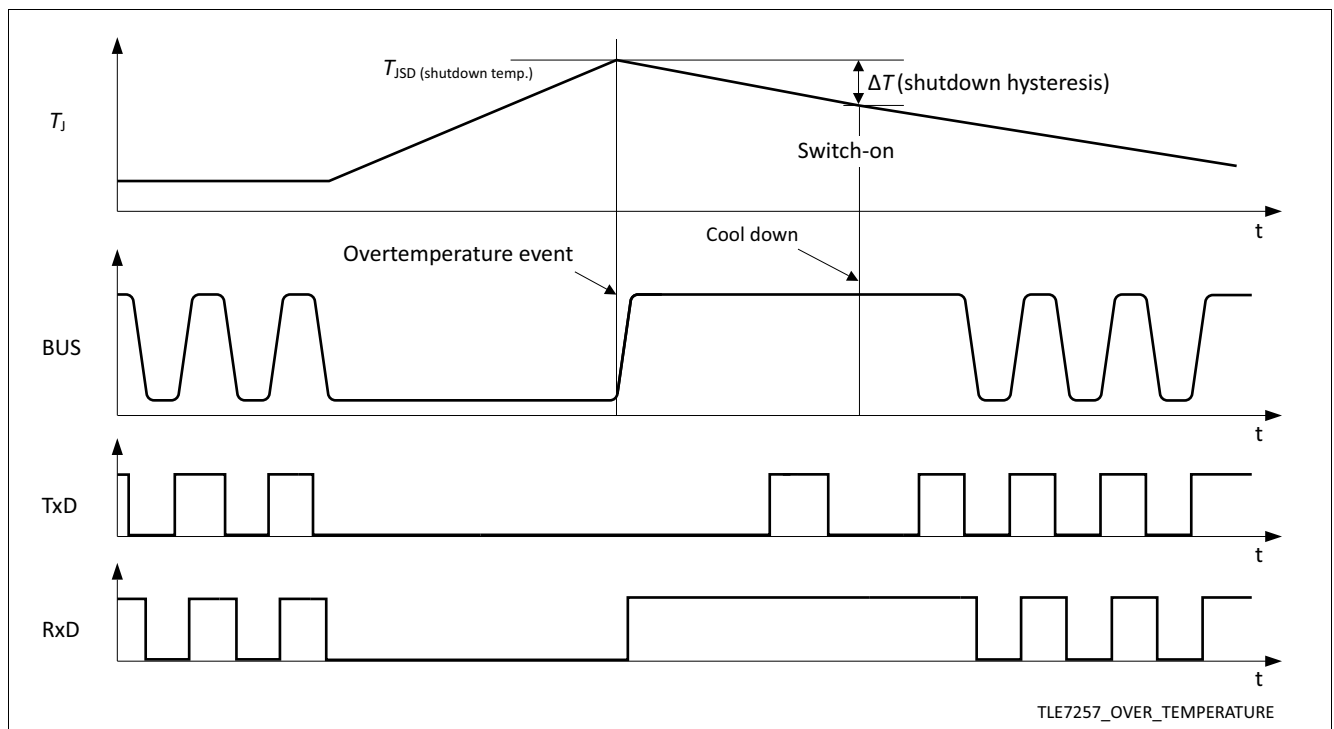
After a mode change to Normal Operation mode, a logical “high” signal for the time  $t_{\text{to,rec}}$  on the Tx D input is required to release the data communication.

## 4.7 Over-Temperature Protection

The TLE7257 has an integrated over-temperature sensor to protect the device against thermal overstress on the transmitter. In case of an over-temperature event, the transmitter will be disabled (see [Figure 10](#)). An over-temperature event will not cause any mode change and will not be directly indicated on the RxD output or the TxD input.

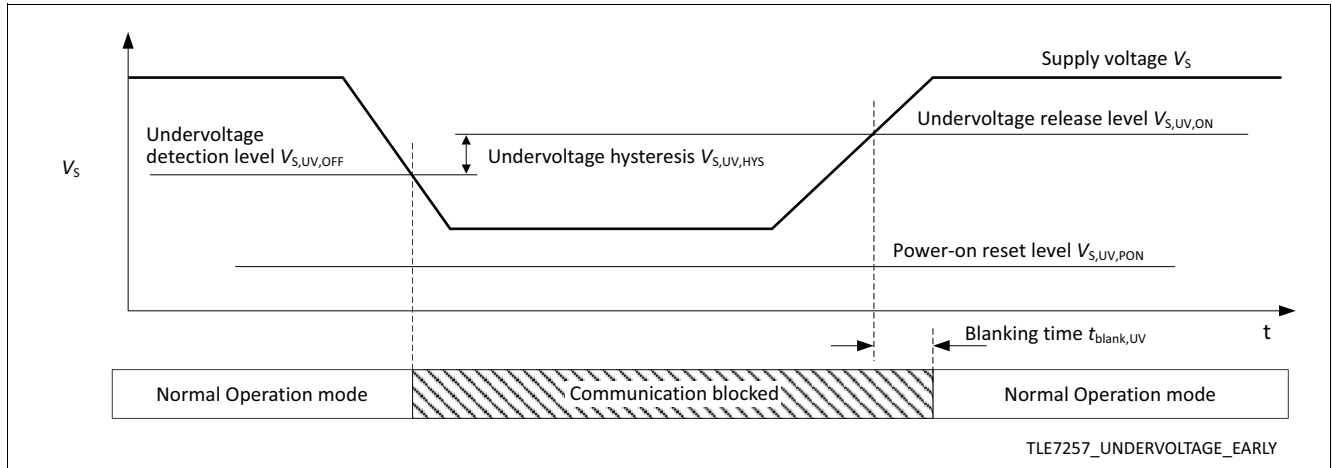
When the junction temperature falls below the thermal shut down level  $T_J < T_{JSD}$ , the transmitter will be reactivated. After an over-temperature recovery the TxD input requires a logical "high" signal before restarting data transmission.

A 10°C hysteresis avoids toggling during the temperature shut down.



**Figure 10** Over-temperature shut down

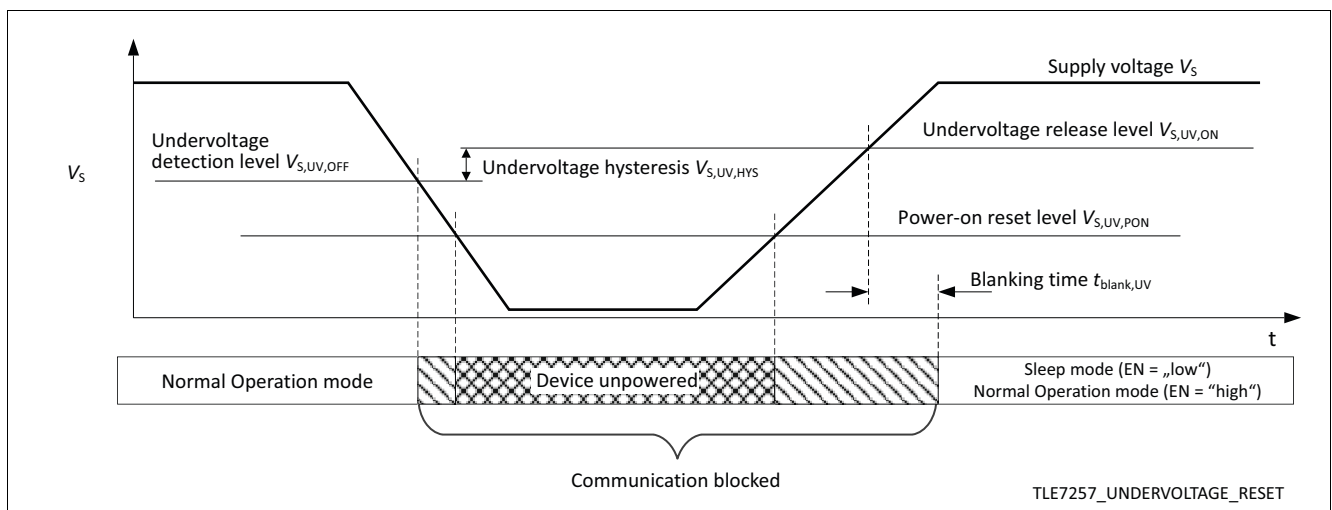
## 4.8 Undervoltage Detection



**Figure 11 Early undervoltage detection**

The TLE7257 has undervoltage detection on the  $V_S$  supply pin with two different thresholds:

- In Normal Operation mode the TLE7257 blocks the communication between the LIN bus and the microcontroller when detecting undervoltage events. However, no mode change will occur. After  $V_S$  rises above the undervoltage release level  $V_{S,UV,REL}$ , the bus communication interface will be released when the signal on the TxD input goes "high". See [Figure 11](#).
- In case the  $V_S$  power supply drops down below the power-on reset level  $V_{S,UV,PON}$  the TLE7257 blocks the communication between the LIN bus and the microcontroller, and also changes the operation mode to Sleep mode after  $V_S$  supply recovery. The power-on reset level is active in all operation modes. See [Figure 12](#).



**Figure 12 Undervoltage detection and power-on reset**

## 4.9 TxD Time-out

The TxD time-out feature protects the LIN bus against permanent blocking in case the logical signal on the TxD input is continuously “low”, caused by e.g. a malfunctioning microcontroller or a short circuit on the printed circuit board. In Normal Operation mode, a logical “low” signal on the TxD input for the time  $t_{\text{TxD}}$  disables the output stage of the transmitter (see [Figure 13](#)). The receiver will remain active and the data on the bus are still monitored on the RxD output.

The TLE7257 will release the output stage after a TxD time-out event first when detecting a logical “high” signal on the TxD input for the time  $t_{\text{to,rec}}$ .

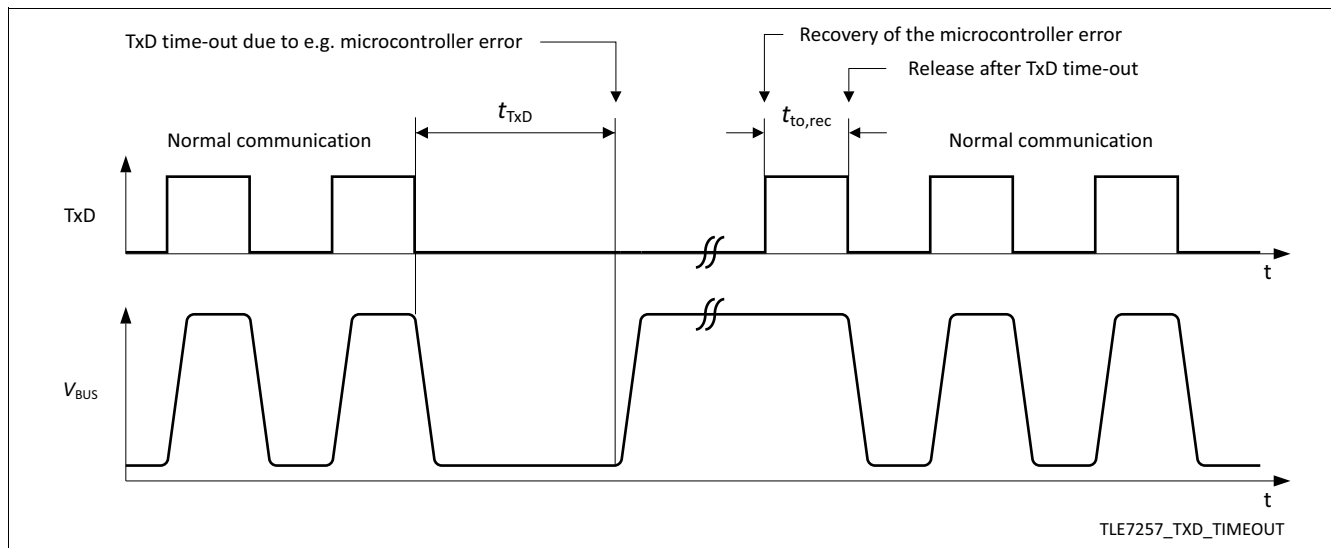


Figure 13 TxD time-out

## 4.10 3.3 V and 5 V Logic Capability

The TLE7257 can be used for 3.3 V and 5 V microcontrollers. The logic inputs and the outputs are capable to operate with both voltage levels. The RxD output needs an external pull-up resistor to the microcontroller supply to define the voltage level (see [Chapter 7.6 “RxD Pull-up Resistor” on Page 26](#) and [Figure 16](#)).

## 4.11 Short Circuit

The BUS pin of TLE7257 can withstand short circuits to either GND or to the  $V_S$  power supply. The integrated over-temperature protection may disable the transmitter in case of a permanent short circuit on the bus pin is causing the overheating.

## 5 General Product Characteristics

### 5.1 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings Voltages, Currents and Temperatures<sup>1)</sup>**

All voltages with respect to ground; positive current flowing into pin; unless otherwise specified

| Parameter                                      | Symbol      | Values |             | Unit | Note / Test Condition                              | Number |
|------------------------------------------------|-------------|--------|-------------|------|----------------------------------------------------|--------|
|                                                |             | Min.   | Max.        |      |                                                    |        |
| Voltages                                       |             |        |             |      |                                                    |        |
| Battery supply voltage                         | $V_S$       | -0.3   | 40          | V    | LIN Spec 2.2A (Par. 11)                            | 1.1.1  |
| BUS input voltage                              | $V_{BUS,G}$ | -27    | 40          | V    | –                                                  | 1.1.2  |
| Logic voltages at EN, TxD, RxD                 | $V_{logic}$ | -0.3   | 6.0         | V    | –                                                  | 1.1.3  |
| INH voltage                                    | $V_{INH}$   | -0.3   | $V_S + 0.3$ | V    | –                                                  | 1.1.4  |
| Currents                                       |             |        |             |      |                                                    |        |
| Output current at RxD                          | $I_{RxD}$   | 0      | 15          | mA   | –                                                  | 1.2.1  |
| Output current at INH                          | $I_{INH}$   | -5     | 5           | mA   | –                                                  | 1.2.2  |
| Temperatures                                   |             |        |             |      |                                                    |        |
| Junction temperature                           | $T_j$       | -40    | 150         | °C   | –                                                  | 1.3.1  |
| Storage temperature                            | $T_s$       | -55    | 150         | °C   | –                                                  | 1.3.2  |
| ESD Susceptibility                             |             |        |             |      |                                                    |        |
| Electrostatic discharge voltage at $V_S$ , BUS | $V_{ESD}$   | -10    | 10          | kV   | Human Body Model (100 pF via 1.5 kΩ) <sup>2)</sup> | 1.4.1  |
| Electrostatic discharge voltage all other pins | $V_{ESD}$   | -4     | 4           | kV   | Human Body Model (100 pF via 1.5 kΩ) <sup>2)</sup> | 1.4.2  |
| Electrostatic discharge voltage all pins       | $V_{ESD}$   | -1     | 1           | kV   | Charged Device Model <sup>3)</sup>                 | 1.4.3  |

1) Not subject to production test, specified by design

2) ESD susceptibility HBM according to ANSI / ESDA / JEDEC JS-001

3) ESD susceptibility, Charged Device Model "CDM" EIA / JESD 22-C101 or ESDA STM5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 5.2 Functional Range

**Table 4 Operating Range**

| Parameter                                   | Symbol       | Values |      | Unit | Note / Test Condition         | Number |
|---------------------------------------------|--------------|--------|------|------|-------------------------------|--------|
|                                             |              | Min.   | Max. |      |                               |        |
| Supply Voltages                             |              |        |      |      |                               |        |
| Extended supply voltage range for operation | $V_{S(ext)}$ | 18     | 40   | V    | Parameter deviations possible | 2.1.1  |
| Supply voltage range for normal operation   | $V_{S(nor)}$ | 5.5    | 18   | V    | LIN Spec 2.2A (Par. 10)       | 2.1.2  |
| Thermal Parameters                          |              |        |      |      |                               |        |
| Junction temperature                        | $T_j$        | -40    | 150  | °C   | 1)                            | 2.2.1  |

1) Not subject to production test, specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 5.3 Thermal Characteristics

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 5 Thermal Resistance<sup>1)</sup>**

| Parameter                                     | Symbol     | Values |      |      | Unit | Note / Test Condition                             | Number |
|-----------------------------------------------|------------|--------|------|------|------|---------------------------------------------------|--------|
|                                               |            | Min.   | Typ. | Max. |      |                                                   |        |
| Thermal Resistance, PG-DSO-8 Package Version  |            |        |      |      |      |                                                   |        |
| Junction ambient                              | $R_{thJA}$ | —      | 130  | —    | K/W  | 2)                                                | 3.1.1  |
| Thermal Resistance, PG-TSON-8 Package Version |            |        |      |      |      |                                                   |        |
| Junction ambient                              | $R_{thJA}$ | —      | 60   | —    | K/W  | 2)                                                | 3.2.1  |
|                                               |            | —      | 190  | —    | K/W  | 3)                                                | 3.2.2  |
|                                               |            | —      | 70   | —    | K/W  | 300 mm <sup>2</sup> heatsink on PCB <sup>3)</sup> | 3.2.3  |
| Thermal Shutdown Junction Temperature         |            |        |      |      |      |                                                   |        |
| Thermal shutdown temperature                  | $T_{JSD}$  | 150    | 175  | 200  | °C   | —                                                 | 3.3.1  |
| Thermal shutdown hysteresis                   | $\Delta T$ | —      | 10   | —    | K    | —                                                 | 3.3.2  |

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (TLE7257) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 mm Cu, 2 x 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted to the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board; The product (TLE7257) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1 inner copper layer (1 x 70 mm Cu).

## 6 Electrical Characteristics

### 6.1 Functional Device Characteristics

**Table 6 Electrical Characteristics**
 $5.5\text{ V} < V_S < 18\text{ V}$ ;  $R_L = 500\ \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ;

all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter                                                           | Symbol            | Values |      |      | Unit | Note / Test Condition                                           | Num<br>ber |
|---------------------------------------------------------------------|-------------------|--------|------|------|------|-----------------------------------------------------------------|------------|
|                                                                     |                   | Min.   | Typ. | Max. |      |                                                                 |            |
| Current Consumption                                                 |                   |        |      |      |      |                                                                 |            |
| Current consumption at $V_S$ ,<br>Recessive state                   | $I_{S,rec}$       | 0.1    | 0.6  | 2.0  | mA   | INH open, without $R_L$ ;<br>$V_{TXD}$ = “high”                 | 4.1.1      |
| Current consumption at $V_S$ ,<br>Dominate state                    | $I_{S,dom}$       | 0.1    | 1.1  | 3.0  | mA   | INH open, without $R_L$ ;<br>$V_{TXD}$ = 0 V                    | 4.1.2      |
| Current consumption at $V_S$ ,<br>Standby mode                      | $I_{S,standby}$   | 100    | 350  | 900  | μA   | Standby mode,<br>$V_{BUS}$ = $V_S$                              | 4.1.3      |
| Current consumption at $V_S$ ,<br>Sleep mode                        | $I_{S,sleep,typ}$ | 1      | 10   | 15   | μA   | Sleep mode, $T_j$ < 40 °C;<br>$V_S$ = 13.5 V; $V_{BUS}$ = $V_S$ | 4.1.4      |
| Current consumption at $V_S$ ,<br>Sleep mode                        | $I_{S,sleep}$     | 1      | 10   | 25   | μA   | Sleep mode,<br>$V_{BUS}$ = $V_S$                                | 4.1.5      |
| Current consumption at $V_S$ ,<br>Sleep mode.<br>Bus shorted to GND | $I_{S,SC\_GND}$   | 100    | –    | 700  | μA   | Sleep mode,<br>$V_S$ = 13.5 V; $V_{BUS}$ = 0 V                  | 4.1.6      |
| Undervoltage Detection                                              |                   |        |      |      |      |                                                                 |            |
| Power-on reset level on $V_S$                                       | $V_{S,UV,PON}$    | –      | –    | 4.3  | V    | Reset level for mode change                                     | 4.2.1      |
| Undervoltage threshold, $V_S$ on                                    | $V_{S,UV,ON}$     | 4.7    | 5.15 | 5.5  | V    | Rising edge                                                     | 4.2.2      |
| Undervoltage threshold, $V_S$ off                                   | $V_{S,UV,OFF}$    | 4.4    | 4.85 | 5.2  | V    | Falling edge                                                    | 4.2.3      |
| Undervoltage detection<br>hysteresis                                | $V_{S,UV,HYS}$    | –      | 300  | –    | mV   | 1)                                                              | 4.2.4      |
| Undervoltage blanking time                                          | $t_{BLANK,UV}$    | –      | 10   | –    | μs   | 1)                                                              | 4.2.5      |
| Receiver Output: RxD                                                |                   |        |      |      |      |                                                                 |            |
| “High” level leakage current                                        | $I_{RD,H,leak}$   | –      | –    | 5    | μA   | $V_{RxD}$ = 5 V; $V_{BUS}$ = $V_S$                              | 4.3.1      |
| “Low” level output current                                          | $I_{RD,L}$        | 1.3    | –    | –    | mA   | $V_{RxD}$ = 0.4 V; $V_{BUS}$ = 0 V                              | 4.3.2      |
| Transmission Input: TxD                                             |                   |        |      |      |      |                                                                 |            |
| “High” level input voltage range                                    | $V_{TD,H}$        | 2      | –    | 6.0  | V    | Recessive state                                                 | 4.4.1      |
| “Low” level input voltage range                                     | $V_{TD,L}$        | -0.3   | –    | 0.8  | V    | Dominant state                                                  | 4.4.2      |
| Input hysteresis                                                    | $V_{TD,hys}$      | –      | 200  | –    | mV   | 1)                                                              | 4.4.3      |
| Pull-up current                                                     | $I_{TD}$          | -60    | –    | -20  | μA   | $V_{TXD}$ = 0 V; Normal Operation<br>mode or Standby mode       | 4.4.4      |
| Enable Input: EN                                                    |                   |        |      |      |      |                                                                 |            |
| “High” level input voltage range                                    | $V_{EN,ON}$       | 2      | –    | 6.0  | V    | Normal Operation mode                                           | 4.5.1      |

## Electrical Characteristics

**Table 6 Electrical Characteristics (cont'd)**
 $5.5\text{ V} < V_S < 18\text{ V}$ ;  $R_L = 500\ \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ;

all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter                                              | Symbol                      | Values             |                   |                    | Unit          | Note / Test Condition                                                         | Number |
|--------------------------------------------------------|-----------------------------|--------------------|-------------------|--------------------|---------------|-------------------------------------------------------------------------------|--------|
|                                                        |                             | Min.               | Typ.              | Max.               |               |                                                                               |        |
| "Low" level input voltage range                        | $V_{\text{EN,OFF}}$         | -0.3               | –                 | 0.8                | V             | Sleep mode or Standby mode                                                    | 4.5.2  |
| Input hysteresis                                       | $V_{\text{EN,hys}}$         | –                  | 200               | –                  | mV            | <sup>1)</sup>                                                                 | 4.5.3  |
| Pull-down resistance                                   | $R_{\text{EN}}$             | 15                 | 30                | 60                 | k $\Omega$    | –                                                                             | 4.5.4  |
| <b>Inhibit Output: INH</b>                             |                             |                    |                   |                    |               |                                                                               |        |
| Inhibit voltage drop                                   | $\Delta V_{\text{INH}}$     | –                  | –                 | 1.0                | V             | $I_{\text{INH}} = -2.0\text{ mA}$                                             | 4.6.1  |
| Leakage current                                        | $I_{\text{INH,lk}}$         | -5.0               | –                 | 5.0                | $\mu\text{A}$ | Sleep mode; $V_{\text{INH}} = 0\text{ V}$                                     | 4.6.2  |
| <b>Bus Receiver: BUS</b>                               |                             |                    |                   |                    |               |                                                                               |        |
| Receiver threshold voltage, recessive to dominant edge | $V_{\text{th\_dom}}$        | $0.4 \times V_S$   | $0.44 \times V_S$ | –                  | V             | –                                                                             | 4.7.1  |
| Receiver dominant state                                | $V_{\text{BUSdom}}$         | –                  | –                 | $0.4 \times V_S$   | V             | LIN Spec 2.2A (Par. 17)                                                       | 4.7.2  |
| Receiver threshold voltage, dominant to recessive edge | $V_{\text{th\_rec}}$        | –                  | $0.56 \times V_S$ | $0.6 \times V_S$   | V             | –                                                                             | 4.7.3  |
| Receiver recessive state                               | $V_{\text{BUSrec}}$         | $0.6 \times V_S$   | –                 | –                  | V             | LIN Spec 2.2A (Par. 18)                                                       | 4.7.4  |
| Receiver center voltage                                | $V_{\text{BUS\_CNT}}$       | $0.475 \times V_S$ | $0.5 \times V_S$  | $0.525 \times V_S$ | V             | LIN Spec 2.2A (Par. 19) <sup>2)</sup>                                         | 4.7.5  |
| Receiver hysteresis                                    | $V_{\text{HYS}}$            | $0.07 \times V_S$  | $0.12 \times V_S$ | $0.175 \times V_S$ | V             | LIN Spec 2.2A (Par. 20) <sup>3)</sup>                                         | 4.7.6  |
| Wake-up threshold voltage                              | $V_{\text{BUS,wk}}$         | $0.40 \times V_S$  | $0.5 \times V_S$  | $0.6 \times V_S$   | V             | –                                                                             | 4.7.7  |
| <b>Bus Transmitter: BUS</b>                            |                             |                    |                   |                    |               |                                                                               |        |
| Bus recessive output voltage                           | $V_{\text{BUS,ro}}$         | $0.8 \times V_S$   | –                 | $V_S$              | V             | $V_{\text{TXD}} = \text{"high"};$<br>Open load                                | 4.8.1  |
| Bus short circuit current                              | $I_{\text{BUS\_LIM}}$       | 40                 | 85                | 125                | mA            | $V_{\text{BUS}} = 13.5\text{ V};$<br>LIN Spec 2.2A (Par. 12);                 | 4.8.2  |
| Leakage current                                        | $I_{\text{BUS\_NO\_GND}}$   | -1                 | -0.5              | –                  | mA            | $V_S = 0\text{ V}; V_{\text{BUS}} = -12\text{ V};$<br>LIN Spec 2.2A (Par. 15) | 4.8.3  |
| Leakage current                                        | $I_{\text{BUS\_NO\_BAT}}$   | –                  | 1                 | 5                  | $\mu\text{A}$ | $V_S = 0\text{ V}; V_{\text{BUS}} = 18\text{ V};$<br>LIN Spec 2.2A (Par. 16)  | 4.8.4  |
| Leakage current                                        | $I_{\text{BUS\_PAS\_do m}}$ | -1                 | -0.5              | –                  | mA            | $V_S = 18\text{ V}; V_{\text{BUS}} = 0\text{ V};$<br>LIN Spec 2.2A (Par. 13)  | 4.8.5  |
| Leakage current                                        | $I_{\text{BUS\_PAS\_rec}}$  | –                  | 1                 | 5                  | $\mu\text{A}$ | $V_S = 8\text{ V}; V_{\text{BUS}} = 18\text{ V};$                             | 4.8.6  |
| Forward voltage serial diode                           | $V_{\text{SerDiode}}$       | 0.4                | –                 | 1.0                | V             | $I_{\text{SerDiode}} = 75\ \mu\text{A};$<br>LIN Spec 2.2A (Par. 21)           | 4.8.7  |
| Bus pull-up resistance                                 | $R_{\text{slave}}$          | 20                 | 40                | 60                 | k $\Omega$    | LIN Spec 2.2A (Par. 26)                                                       | 4.8.8  |

## Electrical Characteristics

**Table 6 Electrical Characteristics (cont'd)**
 $5.5\text{ V} < V_S < 18\text{ V}$ ;  $R_L = 500\ \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ;

all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter                                | Symbol              | Values |      |      | Unit | Note / Test Condition                                 | Number |
|------------------------------------------|---------------------|--------|------|------|------|-------------------------------------------------------|--------|
|                                          |                     | Min.   | Typ. | Max. |      |                                                       |        |
| Bus dominant output voltage maximum load | $V_{\text{BUS,do}}$ | —      | —    | 1.4  | V    | $V_{\text{TxD}} = 0\text{ V}$ ; $R_L = 500\ \Omega$ ; | 4.8.9  |
|                                          |                     | —      | —    | 2.0  | V    | $V_S = 7\text{ V}$ ;<br>$V_S = 18\text{ V}$ ;         |        |

**Dynamic Transceiver Characteristics**

|                                                                                   |                      |       |     |       |               |                                                                                                                                                                                                                                                                                                                 |        |
|-----------------------------------------------------------------------------------|----------------------|-------|-----|-------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| Propagation delay:<br>LIN bus dominant to RxD "low"                               | $t_{\text{rx\_pdf}}$ | 1     | 3.5 | 6     | $\mu\text{s}$ | LIN Spec 2.2A (Par. 31)<br>$R_{\text{RxD}} = 2.4\text{ k}\Omega$ ; $C_{\text{RxD}} = 20\text{ pF}$                                                                                                                                                                                                              | 4.9.1  |
| LIN bus recessive to RxD "high"                                                   | $t_{\text{rx\_pdr}}$ | 1     | 3.5 | 6     | $\mu\text{s}$ |                                                                                                                                                                                                                                                                                                                 |        |
| Receiver delay symmetry                                                           | $t_{\text{rx\_sym}}$ | -2    | —   | 2     | $\mu\text{s}$ | LIN Spec 2.2A (Par. 32)<br>$t_{\text{rx\_sym}} = t_{\text{rx\_pdf}} - t_{\text{rx\_pdr}}$ ;<br>$R_{\text{RxD}} = 2.4\text{ k}\Omega$ ; $C_{\text{RxD}} = 20\text{ pF}$                                                                                                                                          | 4.9.2  |
| Dominant time for bus wake-up                                                     | $t_{\text{WK,bus}}$  | 30    | —   | 150   | $\mu\text{s}$ | —                                                                                                                                                                                                                                                                                                               | 4.9.3  |
| Delay time for mode change                                                        | $t_{\text{MODE}}$    | —     | —   | 50    | $\mu\text{s}$ | 4)                                                                                                                                                                                                                                                                                                              | 4.9.4  |
| TxD time-out                                                                      | $t_{\text{TxD}}$     | 8     | 18  | 28    | ms            | —                                                                                                                                                                                                                                                                                                               | 4.9.5  |
| TxD recessive time to release transmitter                                         | $t_{\text{to,rec}}$  | —     | —   | 10    | $\mu\text{s}$ | 1)                                                                                                                                                                                                                                                                                                              | 4.9.6  |
| Duty cycle D1<br>(for worst case at 20 kBit/s)                                    | $DI$                 | 0.396 | —   | —     |               | Duty cycle 1 <sup>5)</sup><br>$TH_{\text{Rec}}(\text{max}) = 0.744 \times V_S$ ;<br>$TH_{\text{Dom}}(\text{max}) = 0.581 \times V_S$ ;<br>$V_S = 7.0 \dots 18\text{ V}$ ; $t_{\text{bit}} = 50\ \mu\text{s}$ ;<br>$DI = t_{\text{bus\_rec}(\text{min})} / 2 \times t_{\text{bit}}$ ;<br>LIN Spec 2.2A (Par. 27) | 4.9.7  |
| Duty cycle D1<br>for $V_S$ supply 5.5 V to 7.0 V<br>(for worst case at 20 kBit/s) | $DI$                 | 0.396 | —   | —     |               | Duty cycle 1 <sup>5)</sup><br>$TH_{\text{Rec}}(\text{max}) = 0.760 \times V_S$ ;<br>$TH_{\text{Dom}}(\text{max}) = 0.593 \times V_S$ ;<br>$5.5\text{ V} < V_S < 7.0\text{ V}$ ;<br>$t_{\text{bit}} = 50\ \mu\text{s}$ ;<br>$DI = t_{\text{bus\_rec}(\text{min})} / 2 \times t_{\text{bit}}$                     | 4.9.8  |
| Duty cycle D2<br>(for worst case at 20 kBit/s)                                    | $D2$                 | —     | —   | 0.581 |               | Duty cycle 2 <sup>5)</sup><br>$TH_{\text{Rec}}(\text{min}) = 0.422 \times V_S$ ;<br>$TH_{\text{Dom}}(\text{min}) = 0.284 \times V_S$ ;<br>$V_S = 7.6 \dots 18\text{ V}$ ; $t_{\text{bit}} = 50\ \mu\text{s}$ ;<br>$D2 = t_{\text{bus\_rec}(\text{max})} / 2 \times t_{\text{bit}}$ ;<br>LIN Spec 2.2A (Par. 28) | 4.9.9  |
| Duty cycle D2<br>for $V_S$ supply 6.1 V to 7.6 V<br>(for worst case at 20 kBit/s) | $D2$                 | —     | —   | 0.581 |               | Duty cycle 2 <sup>5)</sup><br>$TH_{\text{Rec}}(\text{min}) = 0.410 \times V_S$ ;<br>$TH_{\text{Dom}}(\text{min}) = 0.275 \times V_S$ ;<br>$6.1\text{ V} < V_S < 7.6\text{ V}$ ;<br>$t_{\text{bit}} = 50\ \mu\text{s}$ ;<br>$D2 = t_{\text{bus\_rec}(\text{max})} / 2 \times t_{\text{bit}}$                     | 4.9.10 |

## Electrical Characteristics

**Table 6** Electrical Characteristics (cont'd)

 $5.5\text{ V} < V_S < 18\text{ V}$ ;  $R_L = 500\ \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ;

all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter                                                                           | Symbol | Values |      |       | Unit | Note / Test Condition                                                                                                                                                                                                                                      | Number |
|-------------------------------------------------------------------------------------|--------|--------|------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
|                                                                                     |        | Min.   | Typ. | Max.  |      |                                                                                                                                                                                                                                                            |        |
| Duty cycle D3<br>(for worst case at 10.4 kBit/s)                                    | $D3$   | 0.417  | —    | —     |      | Duty cycle 3 <sup>5)</sup><br>$TH_{Rec}(\max) = 0.778 \times V_S$ ;<br>$TH_{Dom}(\max) = 0.616 \times V_S$ ;<br>$V_S = 7.0 \dots 18\text{ V}$ ; $t_{bit} = 96\ \mu\text{s}$ ;<br>$D3 = t_{bus\_rec(\min)} / 2 \times t_{bit}$ ;<br>LIN Spec 2.2A (Par. 29) | 4.9.11 |
| Duty cycle D3<br>for $V_S$ supply 5.5 V to 7.0 V<br>(for worst case at 10.4 kBit/s) | $D3$   | 0.417  | —    | —     |      | Duty cycle 3 <sup>5)</sup><br>$TH_{Rec}(\max) = 0.797 \times V_S$ ;<br>$TH_{Dom}(\max) = 0.630 \times V_S$ ;<br>$5.5\text{ V} < V_S < 7.0\text{ V}$ ;<br>$t_{bit} = 96\ \mu\text{s}$ ;<br>$D3 = t_{bus\_rec(\min)} / 2 \times t_{bit}$                     | 4.9.12 |
| Duty cycle D4<br>(for worst case at 10.4 kBit/s)                                    | $D4$   | —      | —    | 0.590 |      | Duty cycle 4 <sup>5)</sup><br>$TH_{Rec}(\min) = 0.389 \times V_S$ ;<br>$TH_{Dom}(\min) = 0.251 \times V_S$ ;<br>$V_S = 7.6 \dots 18\text{ V}$ ; $t_{bit} = 96\ \mu\text{s}$ ;<br>$D4 = t_{bus\_rec(\max)} / 2 \times t_{bit}$ ;<br>LIN Spec 2.2A (Par. 30) | 4.9.13 |
| Duty cycle D4<br>for $V_S$ supply 6.1 V to 7.6 V<br>(for worst case at 10.4 kBit/s) | $D4$   | —      | —    | 0.590 |      | Duty cycle 4 <sup>5)</sup><br>$TH_{Rec}(\min) = 0.378 \times V_S$ ;<br>$TH_{Dom}(\min) = 0.242 \times V_S$ ;<br>$6.1\text{ V} < V_S < 7.6\text{ V}$ ;<br>$t_{bit} = 96\ \mu\text{s}$ ;<br>$D4 = t_{bus\_rec(\max)} / 2 \times t_{bit}$                     | 4.9.14 |

1) Not subject to production test, specified by design

2)  $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec}) / 2$ 

3)  $V_{HYS} = V_{th\_rec} - V_{th\_dom}$ 

4) Delay time specified for a load of 10 k $\Omega$  / 20 pF on the INH output

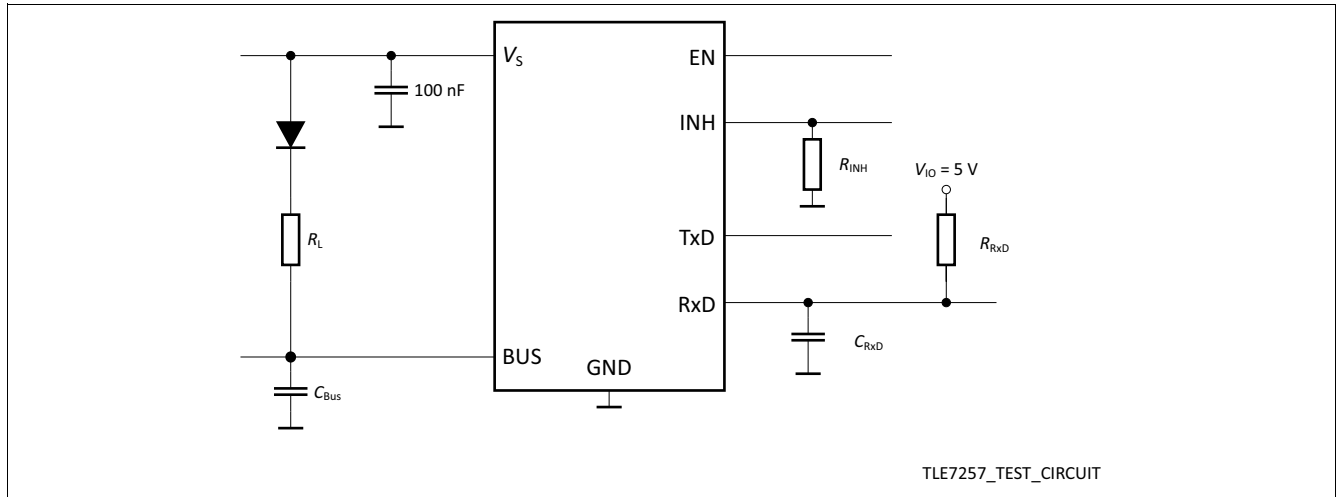
5) Bus load concerning LIN Spec 2.2A:

Load 1 = 1 nF / 1 k $\Omega$  =  $C_{BUS} / R_L$ 

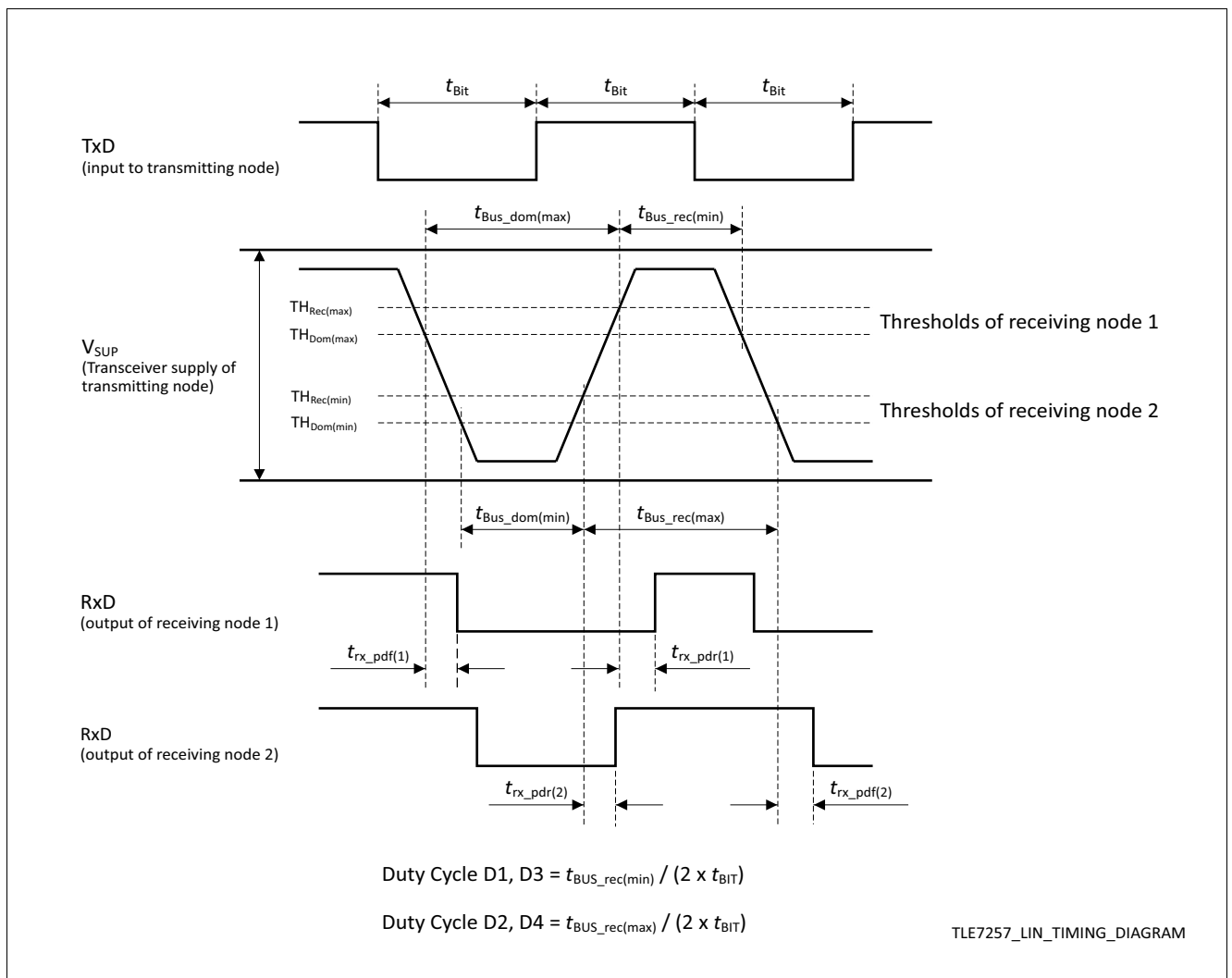
Load 2 = 6.8 nF / 660  $\Omega$  =  $C_{BUS} / R_L$ 

Load 3 = 10 nF / 500  $\Omega$  =  $C_{BUS} / R_L$

## 6.2 Diagrams



**Figure 14** Simplified test circuit

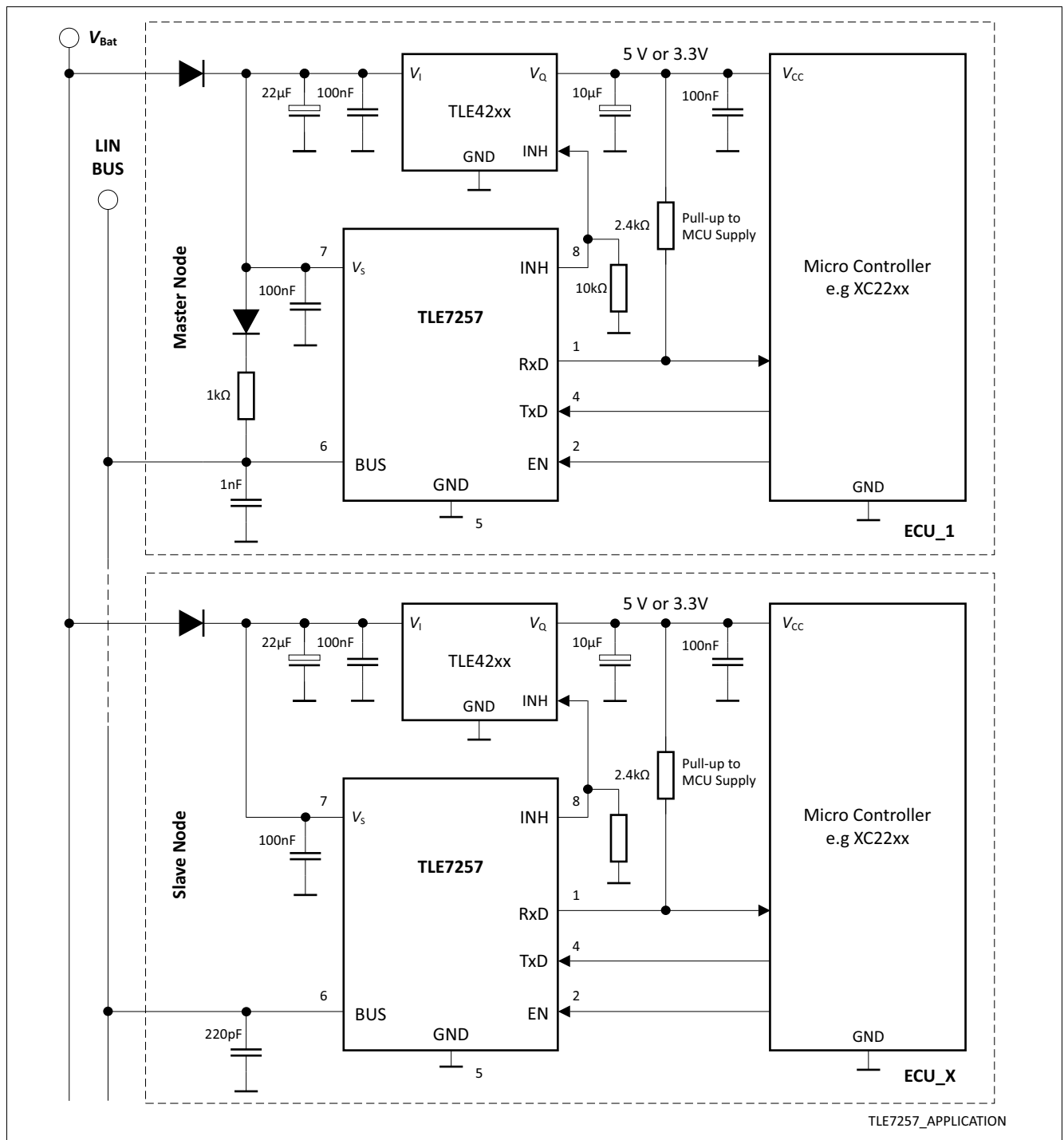


**Figure 15** Timing diagram for dynamic characteristics

## 7 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

### 7.1 Application Example



**Figure 16** Simplified application circuit

## 7.2 ESD Susceptibility according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 "Gun test" (150 pF, 330  $\Omega$ ) have been performed. The results and test conditions are available in a separate test report.

**Table 7 ESD Susceptibility according to IEC61000-4-2**

| Performed Test                                                | Result | Unit | Remarks                      |
|---------------------------------------------------------------|--------|------|------------------------------|
| Electrostatic discharge voltage at pin $V_S$ , BUS versus GND | +10    | kV   | <sup>1)</sup> Positive pulse |
| Electrostatic discharge voltage at pin $V_S$ , BUS versus GND | -10    | kV   | <sup>1)</sup> Negative pulse |

1) ESD susceptibility "ESD GUN" according IEC 61000-4-2, tested by external test house.

## 7.3 Transient Robustness according to ISO 7637-2

Test for transient robustness according to ISO 7637-2 have been performed. The results and test conditions are available in a separate test report.

**Table 8 Automotive Transient Robustness according to ISO 7637-2**

| Performed Test | Result | Unit | Remarks       |
|----------------|--------|------|---------------|
| Pulse 1        | -100   | V    | <sup>1)</sup> |
| Pulse 2        | +75    | V    | <sup>1)</sup> |
| Pulse 3a       | -150   | V    | <sup>1)</sup> |
| Pulse 3b       | +100   | V    | <sup>1)</sup> |

1) Automotive Transient Robustness according to ISO 7637-2, tested by external test house.

## 7.4 LIN Physical Layer Compatibility

The TLE7257 fulfills the Physical Layer Specification of LIN 1.2, 1.3, 2.0, 2.1, 2.2 and 2.2A.

The differences between LIN specification 1.2 and 1.3 is mainly the physical layer specification. The reason was to improve the compatibility between the nodes.

The LIN specification 2.0 is a super set of the 1.3 version. The 2.0 version offers new features. However, it is possible to use the LIN 1.3 slave node in a 2.0 node cluster, as long as the new features are not used. Vice versa it is possible to use a LIN 2.0 node in the 1.3 cluster without using the new features.

In terms of the physical layer the LIN 2.1, LIN 2.2 and LIN 2.2A Specification does not include any changes and is fully compliant to the LIN Specification 2.0.

LIN 2.2A is the latest version of the LIN specification, released in December 2010. The physical layer specification of LIN 2.2A will be included in the ISO 17987-4 without modifications.

Additionally, the TLE7257 is compliant to the SAE J2602-2 standard for usage in the US automotive market.

## 7.5 TxD Fail-Safe Input

The TxD input has an internal pull-up structure to avoid any bus disturbance in case the TxD input is open and floating. In case of an not connected TxD input, the pin is pulled to an internal voltage supply (see [Figure 1](#)) and the output to the LIN bus on the BUS pin is always "recessive". Therefore the TLE7257 can not disturb the communication on the LIN bus.

In order to optimize the quiescent current of the TLE7257 in Sleep mode, the pull-up structure inside the TxD input is disabled in Sleep mode. The logic inside the TxD input is not reacting at any signal change provide to the TxD input pin and the transmitter is turned off. In Sleep mode the TLE7257 can not disturb or block the LIN bus in any case.

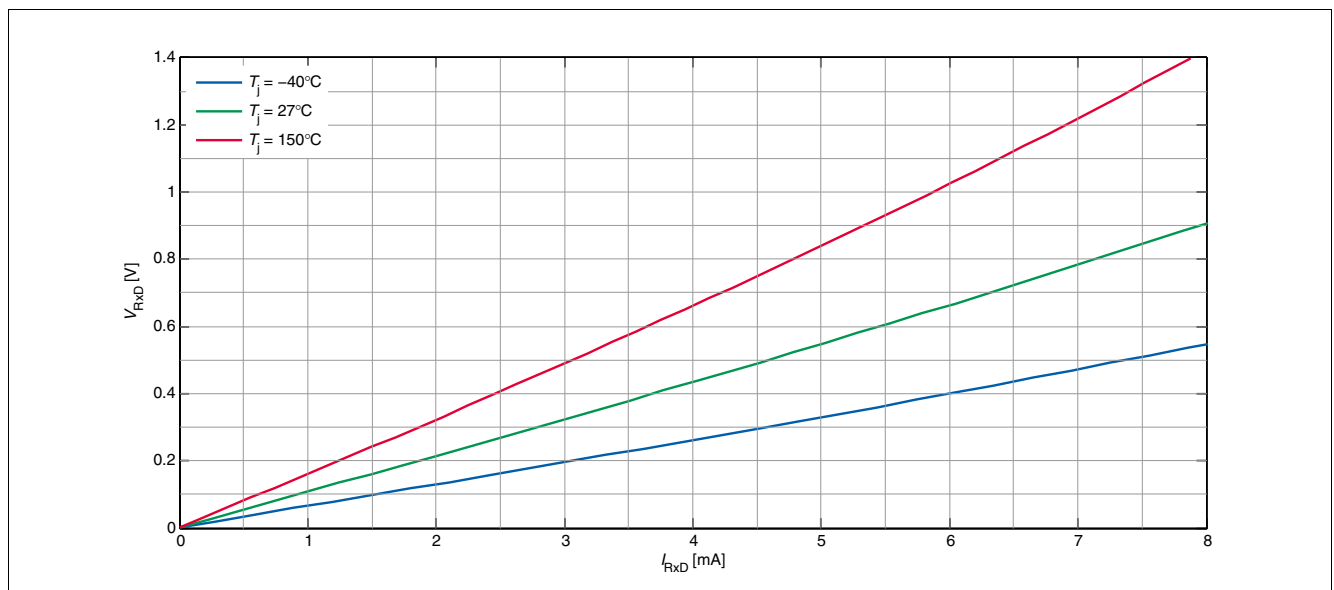
**Table 9 TxD Termination**

| Operation Mode        | Remarks                                                                                                                                                                                                                 |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Normal Operation mode | The internal pull-up structure is active, in case the TxD input is open the TxD input signal is "high" and the output on the BUS pin is "recessive"                                                                     |
| Standby mode          | The internal pull-up structure is active, in case the TxD input is open the TxD input signal is "high". In Standby mode the transmitter is turned off and therefore the output on the BUS pin always is "recessive"     |
| Sleep mode            | The internal pull-up structure is inactive, in case the TxD input is open the TxD input signal is "floating". In Sleep mode the transmitter is turned off and therefore the output on the BUS pin always is "recessive" |

## 7.6 RxD Pull-up Resistor

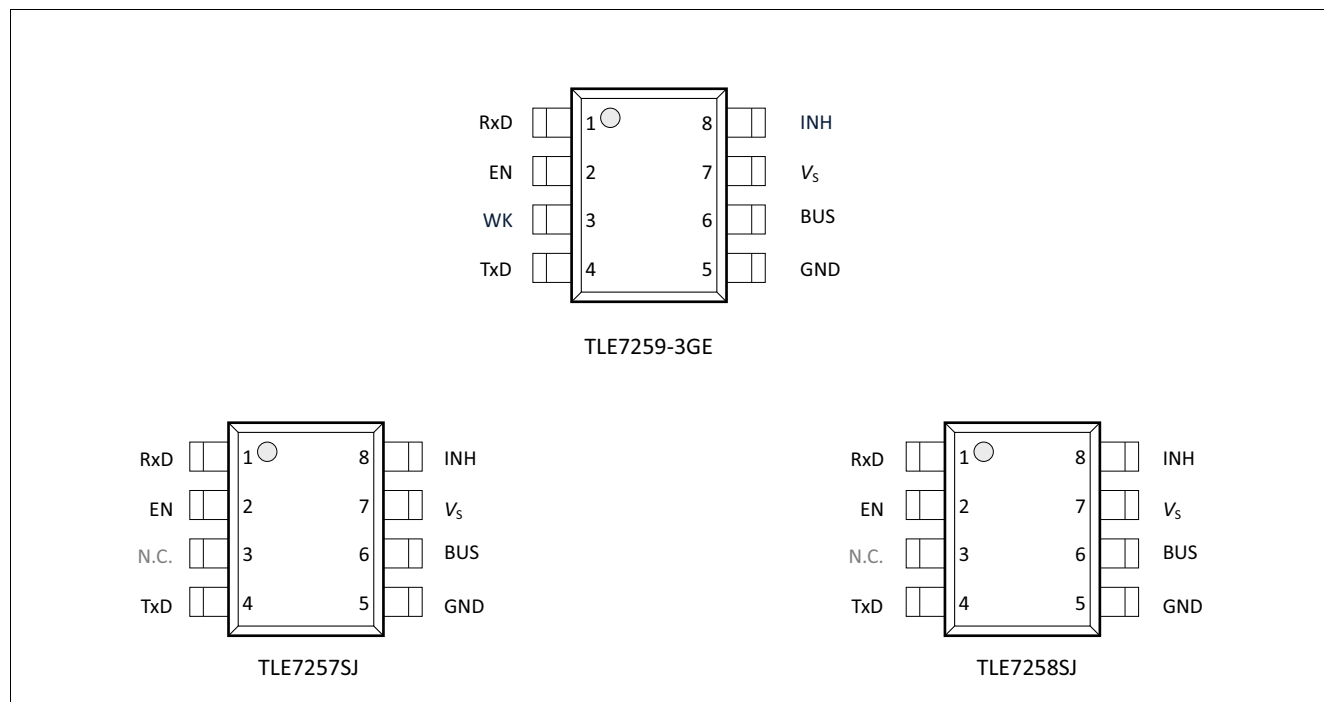
The receive data output (RxD) provides an open drain behavior for allowing the output level to be adapted to the microcontroller supply voltage. Thus 3.3 V microcontroller derivatives without 5 V tolerant ports can be used. In case the microcontroller port pin does not provide an integrated pull-up, an external pull-up resistor connected to the microcontroller's  $V_{CC}$  supply voltage is required.

The typical RxD pin current / voltage characteristic over temperature is given in [Figure 17](#). With the applications microcontroller port pins' (Rx) minimum "high"-level and maximum "low"-level input voltage the pull-up resistor can be dimensioned. For most applications a pull-up resistor  $R_{RX}$  of 2.4 k $\Omega$  is recommended.


**Figure 17 Typical RxD output sink characteristics**

## 7.7 Compatibility with other Infineon LIN Transceivers

Infineon offers a complete LIN transceiver family consisting of devices in PG-DSO-8 package (TLE7257SJ, TLE7258SJ and TLE7259-3GE) and PG-TSON-8 package (TLE7257LE, TLE7258D, TLE7258LE and TLE7259-3LE). All these devices are pin-to-pin compatible, with the only differences at the pins named N.C. (= Not Connected). The N.C. pins can be left open on the PCB in applications where these functionalities are not needed. The N.C. pins are internally not bonded, so the devices will not be affected if these pins are connected to signals on the application PCB.

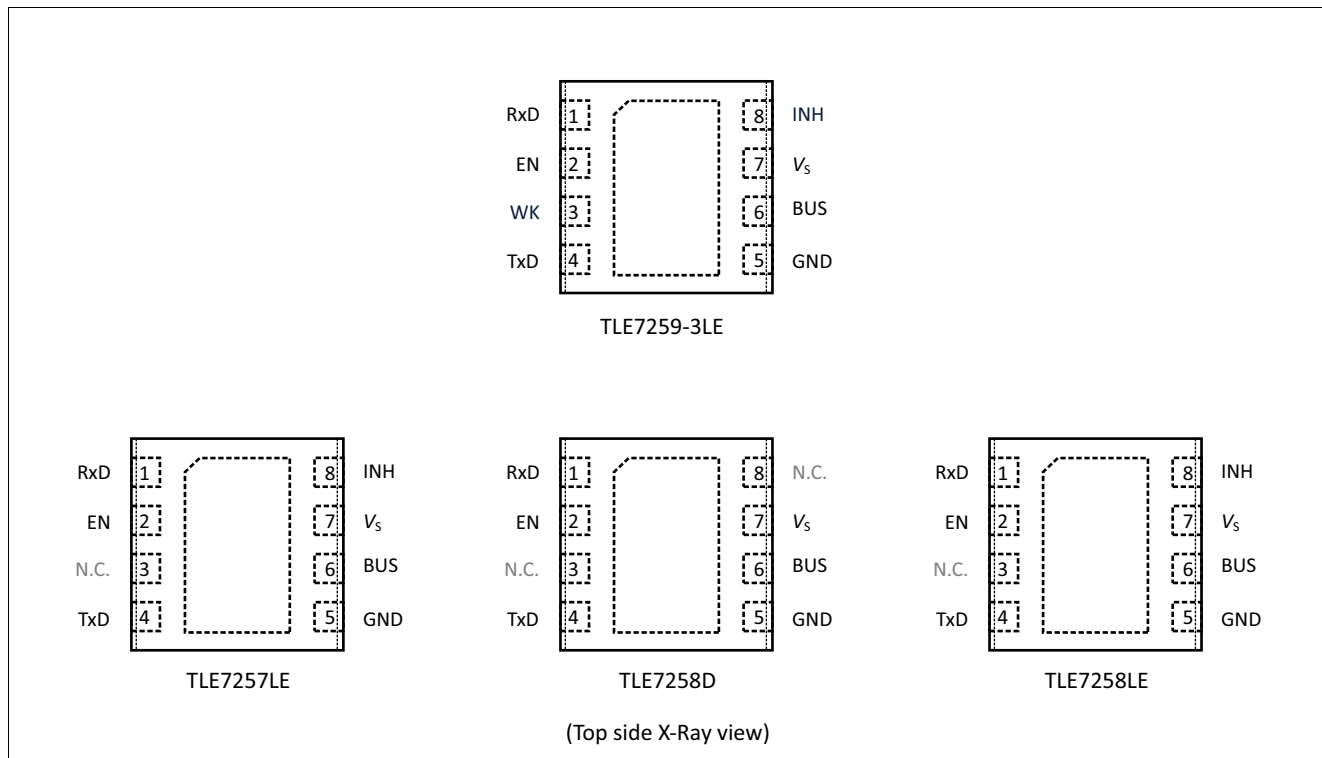


**Figure 18 Pin compatibility between TLE7257SJ, TLE7258SJ and TLE7259-3GE**

**Table 10 Functionality of LIN transceiver family, PG-DSO-8 package**

| Device                | TLE7257SJ                | TLE7258SJ               | TLE7259-3GE                        |
|-----------------------|--------------------------|-------------------------|------------------------------------|
| <b>Applications</b>   | Standard LIN Master node | Standard LIN Slave node | High End LIN All kind of nodes     |
| <b>Features</b>       |                          |                         |                                    |
| Fast Programming mode | –                        | –                       | ✓                                  |
| Local Wake input      | –                        | –                       | ✓                                  |
| Inhibit output usage  | VREG control             | VREG control            | VREG control<br>Master Termination |
| TxD Time-out          | ✓                        | ✓                       | ✓                                  |
| Power-Up mode         | Sleep mode               | Standby mode            | Standby mode                       |

The functional difference between the devices in the Infineon LIN transceiver family is summarized in [Table 10](#) and in [Table 11](#). For mode details on the functional and parametric differences, please refer to the respective part's datasheet.



**Figure 19 Pin compatibility between TLE7257LE, TLE7258LE, TLE7258D and TLE7259-3LE**

**Table 11 Functionality of LIN transceiver family, PG-TSON-8 package**

| Device                | TLE7257LE                | TLE7258LE               | TLE7258D        | TLE7259-3LE                     |
|-----------------------|--------------------------|-------------------------|-----------------|---------------------------------|
| <b>Applications</b>   | Standard LIN Master node | Standard LIN Slave node | K-Line MOST ECL | High End LIN All kind of nodes  |
| <b>Features</b>       |                          |                         |                 |                                 |
| Fast Programming mode | –                        | –                       | –               | ✓                               |
| Local Wake input      | –                        | –                       | –               | ✓                               |
| Inhibit output usage  | VREG control             | VREG control            | –               | VREG control Master Termination |
| TxD Time-out          | ✓                        | ✓                       | –               | ✓                               |
| Power-Up mode         | Sleep mode               | Standby mode            | Standby mode    | Standby mode                    |



## 9 Revision History

**Table 12** Revision History

| Revision | Data       | Changes                                                                                                                      |
|----------|------------|------------------------------------------------------------------------------------------------------------------------------|
| 1.1      | 2015-08-20 | Data Sheet updated based on Data Sheet Rev. 1.0.<br><br>Marking of SJ type updated:<br>• <a href="#">Chapter 1, Overview</a> |
| 1.0      | 2013-10-16 | Data Sheet created.                                                                                                          |

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