



650V N-ch Multi-Epi Super-Junction MOSFET

Pb Lead Free Package and Finish

General Features

- Multi-Epi Process
- Proprietary New Super-Junction Technology
- $R_{DS(ON),typ.}=0.32\Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

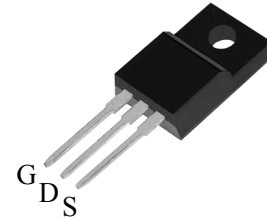
$BV_{DSS@T_{JMAX}}$	$R_{DS(ON),typ.}$	I_D
700V	0.32Ω	12A

Applications

- Adaptor
- Charger
- SMPS Standby Power

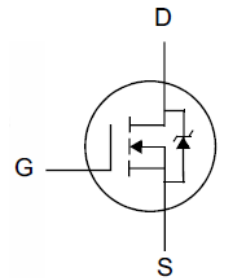
Ordering Information

Part Number	Package	Brand
SPTA65R350E	TO-220F	



TO-220F

Package No to Scale



Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Unit
		SPTA65R350E	
V_{DSS}	Drain-to-Source Voltage	650	V
V_{GSS}	Gate source voltage (static)	±20	
	Gate source voltage (dynamic) AC (f>1Hz)	±30	
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	12	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	7.2	
I_{DM}	Pulsed Drain Current at $V_{GS}=10V^{[1]}$	36	
dv/dt	Reverse diode dv/dt	15	V/ns
d_{iF}/dt	Maximum diode commutation speed	50	A/us
E_{AS}	Single Pulse Avalanche Energy ^[2]	624	mJ
P_D	Power Dissipation	31.3	W
T_J & T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Max. Value	Unit
		SPTA65R350E	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	



Electrical Characteristics

OFF Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=650V, V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

ON Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance ^[3]	--	0.32	0.35	Ω	$V_{GS}=10V, I_D=5.5A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	--	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
gfs	Forward Transconductance ^[3]	--	8.5	--	S	$V_{DS}=10V, I_D=5.0A$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	380	--	pF	$V_{GS}=0V,$ $V_{DS}=50V,$ $f=10KHz$
C_{oss}	Output Capacitance	--	40	--		
R_G	Gate resistance (Intrinsic)	--	11	--	Ω	$f = 1.0MHz$ Open Drain
Q_g	Total Gate Charge	--	11	--	nC	$V_{DD}=400V,$ $I_D=2.2A, V_{GS}=0$ to 13V
Q_{gs}	Gate-to-Source Charge	--	2.0	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	2.6	--		
$V_{plateau}$	Gate plateau voltage	--	7.1	--	V	

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	25	--	pF	$V_{DD}=400V,$ $I_D=2.2A,$ $V_{GS}=13V$ $R_g=10\Omega$
t_{rise}	Rise Time	--	30	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	40	--		
t_{fall}	Fall Time	--	30	--		

**Source-Drain Body Diode Characteristics**T_J=25°C unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I _{SD}	Continuous Source Current ^[2]	--	--	12	A	Maximum Ratings
I _{SM}	Pulsed Source Current ^[2]	--	--	36		
V _{SD}	Diode Forward Voltage	--	--	1.2	V	I _S =3.8A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	125	--	ns	V _R =400V, V _{GS} =0V I _F =2.2A, di/dt =100A/μs
Q _{rr}	Reverse Recovery Charge	--	0.625	--	uC	
I _{rrm}	PeakReverseRecoveryCurrent	--	10	--	A	

Note:

[1] Repetitive Rating: Pulse width limited by maximum junction temperature

[2] L = 10mH, VDD= 80V, Starting T_J= 25°C

[3] Pulse Test: Pulse width ≤ 380us, Duty Cycle ≤ 2%

Test Circuits and Waveforms

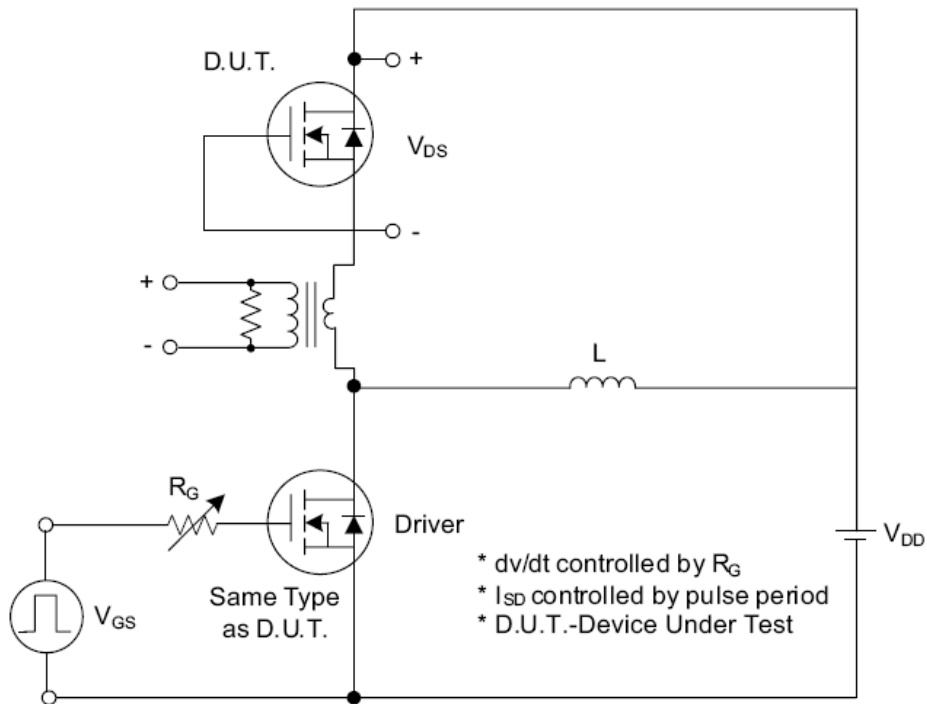


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

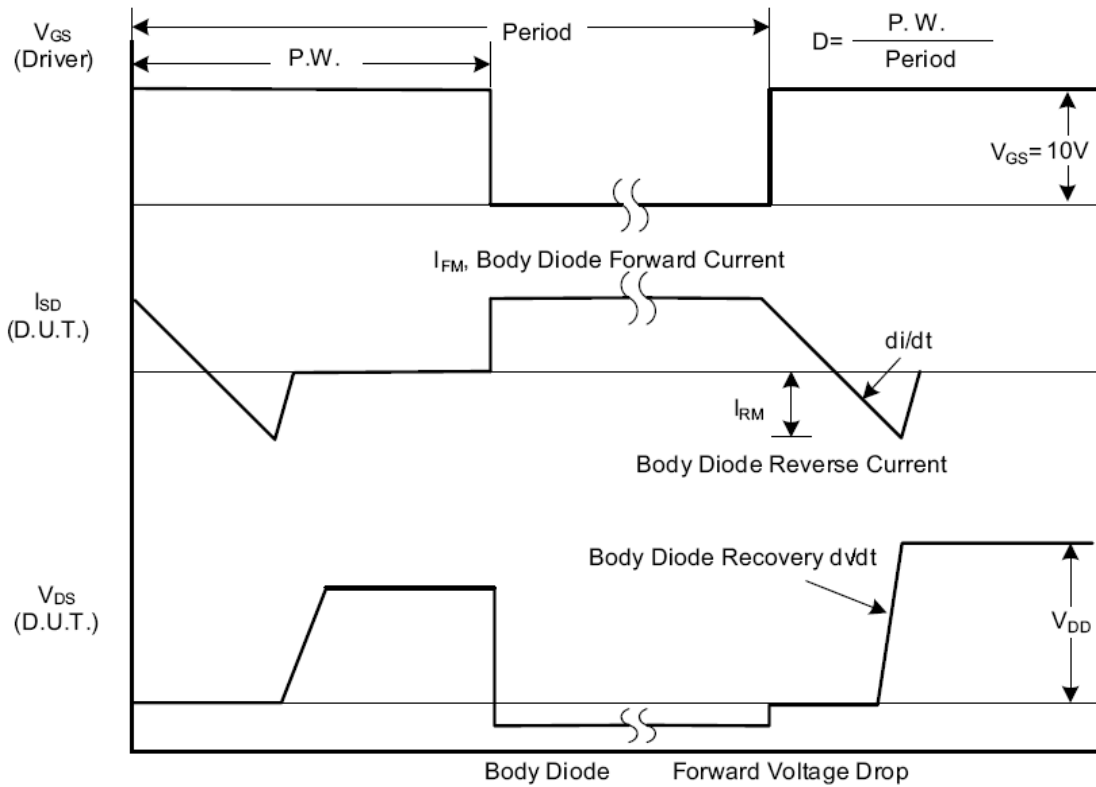


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

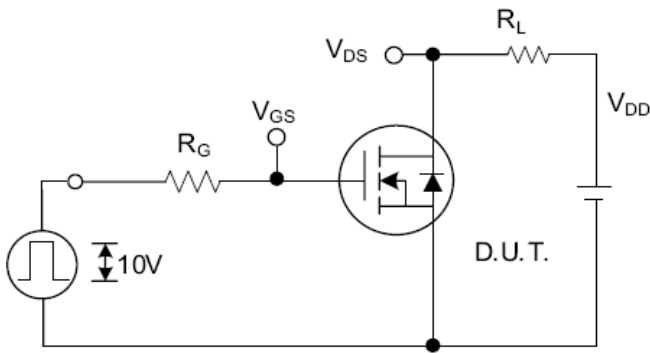
Test Circuits and Waveforms (Cont.)


Fig. 2.1 Switching Test Circuit

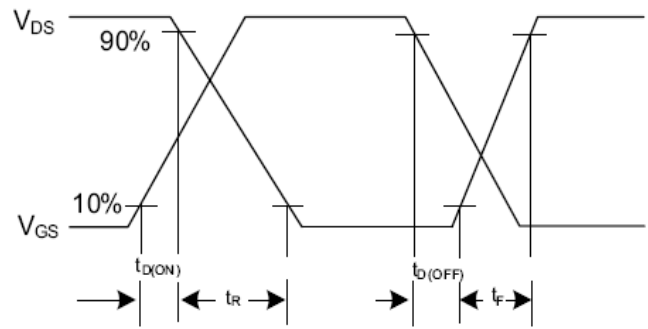


Fig. 2.2 Switching Waveforms

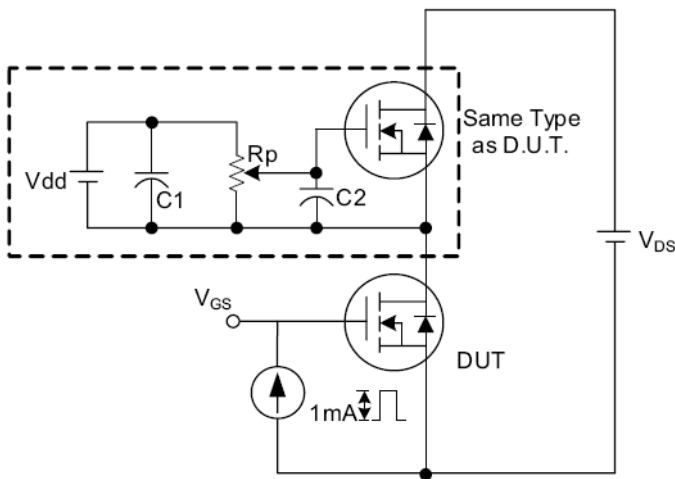


Fig. 3.1 Gate Charge Test Circuit

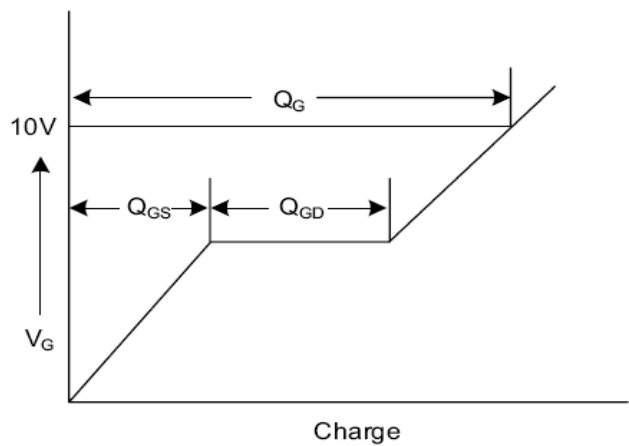


Fig. 3.2 Gate Charge Waveform

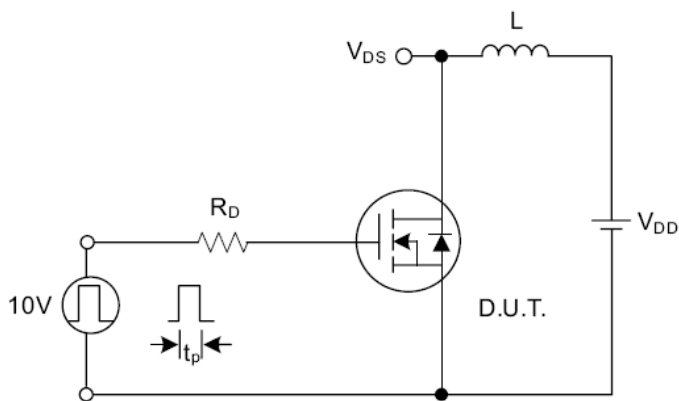


Fig. 4.1 Unclamped Inductive Switching Test Circuit

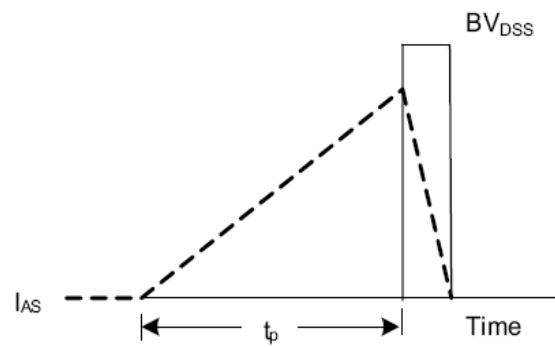


Fig. 4.2 Unclamped Inductive Switching Waveforms



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