

Non-Synchronous PWM Boost Controller



General Description

The FP5208 and FP5208B are boost topology switching regulator for wide operating voltage applications. They provide built-in gate driver pin for driving external N-MOSFET. The non-inverting input of error amplifier connects to a 0.6V precision reference voltage. They have programmable soft start time and PWM frequency set by external capacitors and resistors. FP5208B has programmable current detection and over current protection set by external resistors.

The FP5208B is available in the small footprint DFN-12L package to fit in space-saving PCB layout for application fields.

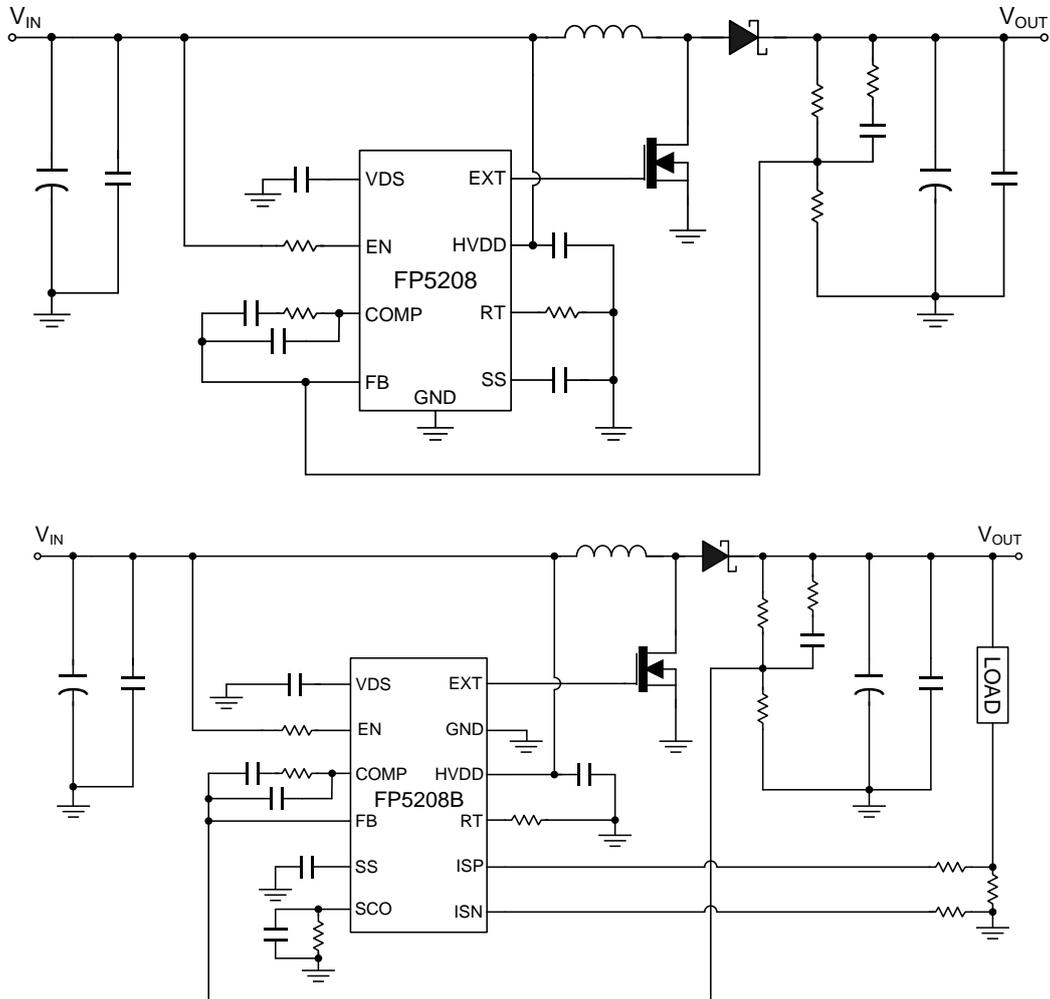
Features

- Wide Supply Voltage Operating Range: 2.5V to 24V
- Precision Feedback Reference Voltage: 0.6V ($\pm 2\%$)
- Shutdown Current: $< 1\mu\text{A}$
- Programmable PWM Frequency: 100KHz~1000KHz
- Programmable Soft Start Function (SS)
- Light Load Detection / FP5208B
- Programmable Over Current Protection (OCP) / FP5208B
- Over Temperature Protection (OTP)
- Package: SOP-8L(EP) / FP5208, DFN-12L / FP5208B

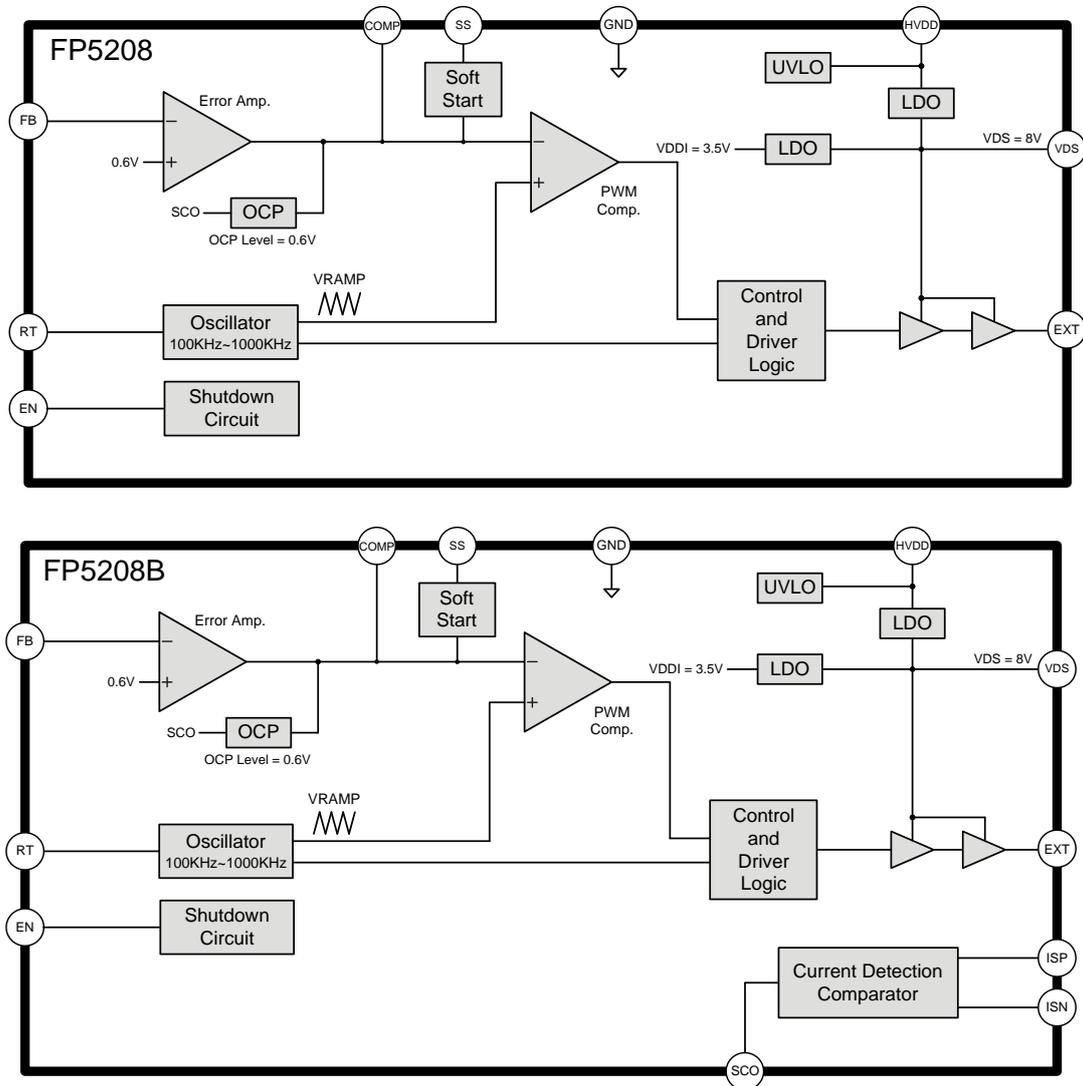
Applications

- Chargers
- LCD Displays
- Handheld Devices
- Portable Products

Typical Application Circuit



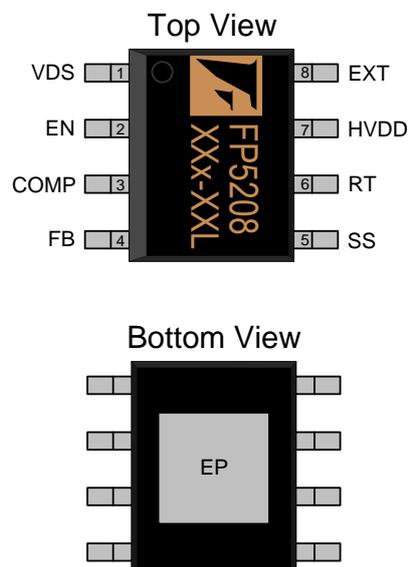
Function Block Diagram



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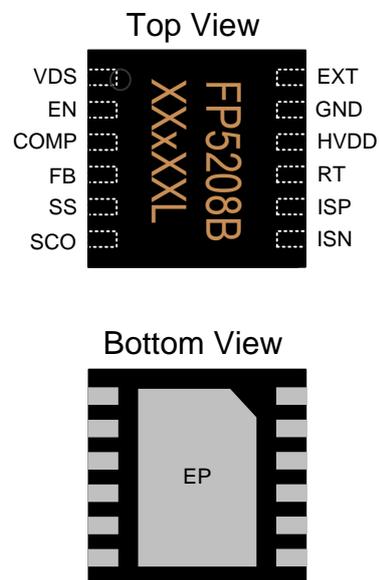
Pin Descriptions

SOP-8L (EP)



Name	No.	I / O	Description
VDS	1	P	Power Supply for Internal Control Circuits and Gate Drivers
EN	2	I	Enable Control
COMP	3	O	Compensation
FB	4	I	Error Amplifier Inverting Input
SS	5	I	Soft Start Programming
RT	6	I	Frequency Programming
HVDD	7	P	IC Power Supply
EXT	8	O	Gate Driver Output
GND	9	P	IC Ground (Exposed PAD) – Must Connect to Ground

DFN-12L

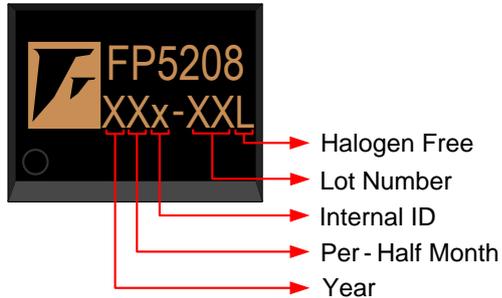


Name	No.	I / O	Description
VDS	1	P	Power Supply for Internal Control Circuits and Gate Drivers
EN	2	I	Enable Control
COMP	3	O	Compensation
FB	4	I	Error Amplifier Inverting Input
SS	5	I	Soft Start Programming
SCO	6	I	Adjustable Output Current Protection
ISN	7	I	Current Sense Comparator Inverting Input
ISP	8	I	Current Sense Comparator Non-inverting Input
RT	9	I	Frequency Programming
HVDD	10	P	IC Power Supply
GND	11	P	IC Ground
EXT	12	O	Gate Driver Output
EP	13	P	Exposed PAD – Connect to Ground

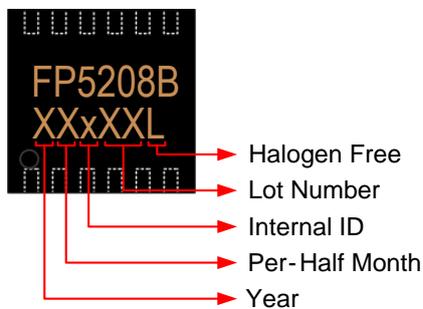
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Marking Information

SOP-8L(EP)



DFN-12L



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example → Lot : 123456 → XXx-56L

Internal ID: Internal Identification Code

Per-Half Month: Production period indicator in half month time unit

For Example : A → First Half Month of January

B → Second Half Month of January

C → First Half Month of February

D → Second Half Month of February

Year: Production year's last digit

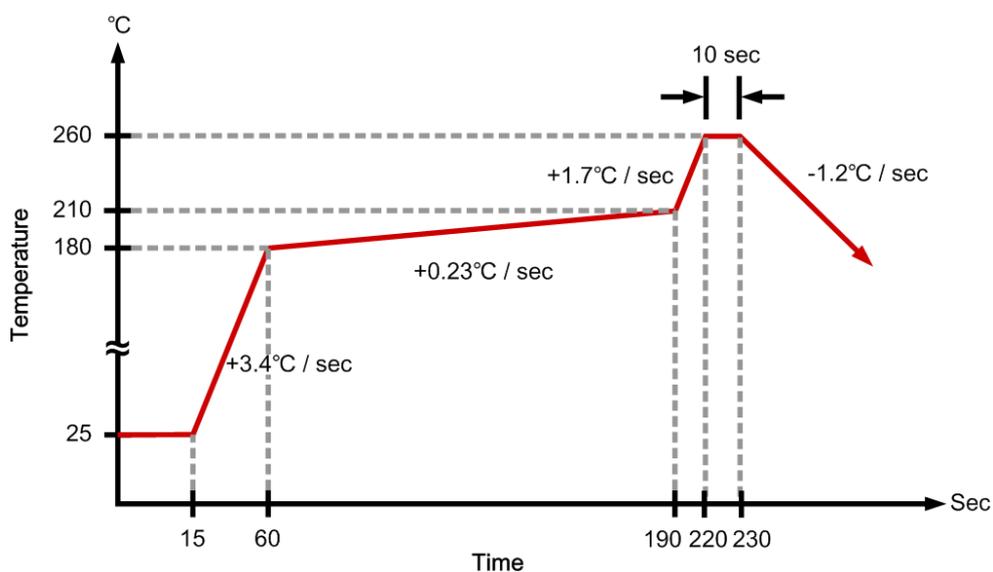
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP5208XR-G1	-25°C ~ 85°C	SOP-8L (EP)	2500EA	Tape & Reel
FP5208BdR-G1	-25°C ~ 85°C	DFN-12L	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	HVDD		0		25	V
ISP, ISN (FP5208B)			0		6	V
VDS,EXT Voltage			0		16	V
Others Pin Voltage			0		6	V
Thermal Resistance (Junction to Ambient)	θ_{JA}	SOP-8L (EP)			+60	°C / W
		DFN-12L			+60	°C / W
Thermal Resistance (Junction to Case)	θ_{JC}	SOP-8L (EP)			+10	°C / W
		DFN-12L			+10	°C / W
Junction Temperature	T_J				+150	°C
Operating Temperature	T_{OP}		-25		+85	°C
Storage Temperature	T_{ST}		-65		+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	HVDD		2.5		24	V
Operating Temperature Range	T _A	Ambient Temperature	-25		+85	°C

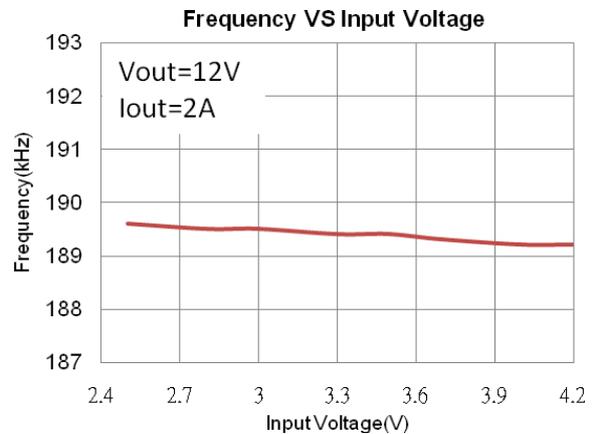
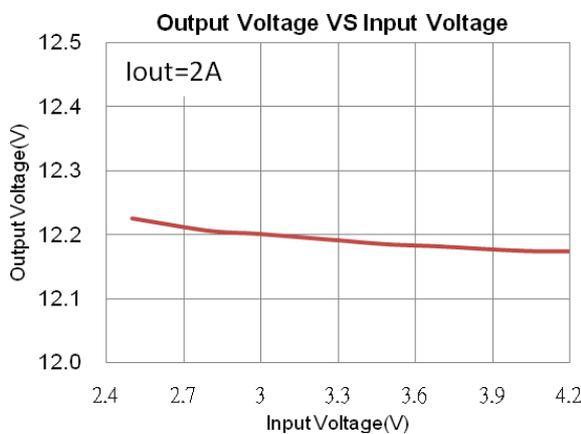
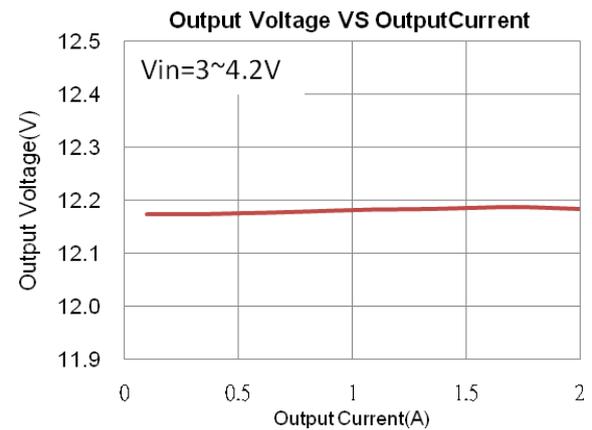
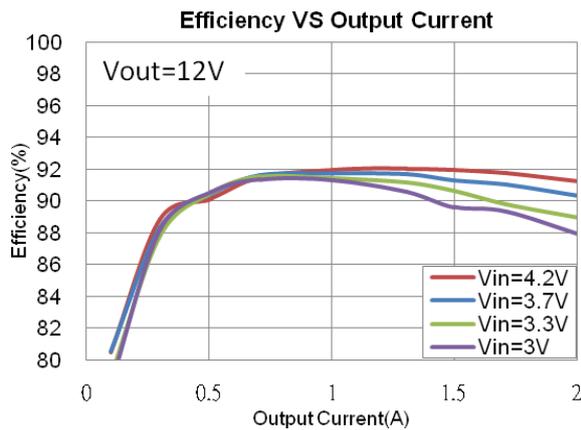
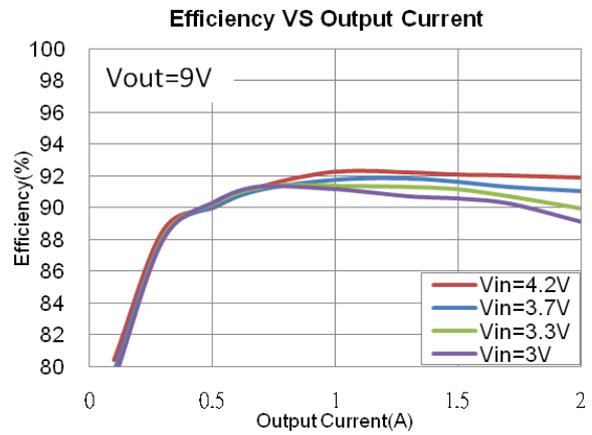
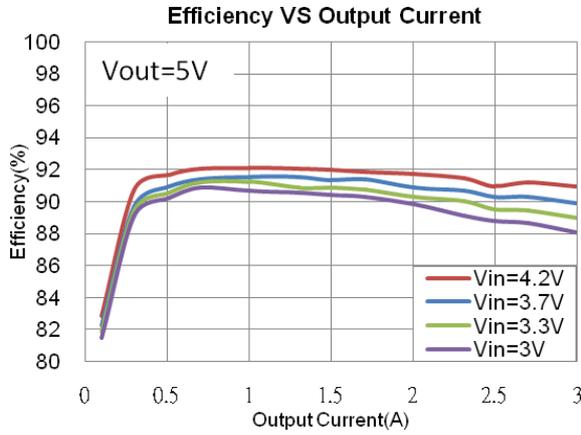
DC Electrical Characteristics (HVDD=12V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System Supply Input						
Input Supply Range	HV _{DD}		2.5		24	V
Under Voltage Lockout	V _{UVLO}			2.2		V
UVLO Hysteresis				0.1		V
Average Current	I _{CC}	FB=0.4V, Switching		1		mA
Quiescent Current	I _{CC}	FB=0.8V, No Switching		245		μA
Shutdown Current	I _{CC}	V _{EN} =GND			1	μA
Input Supply Voltage	V _{DS}	HV _{DD} =12V, I _{DS} =0A		8.5		V
Oscillator						
Operation Frequency	f _{OSC}	RT=NC	160	200	240	KHz
		RT=50KΩ	400	500	600	KHz
Maximum Duty Ratio	%	FB=0.4V		90		%
Soft Start						
Soft-Start bias Current	I _{SS}	V _{SS} =0V		1.5		μA
Reference Voltage						
Feedback Voltage	V _{FB}	HV _{DD} =12V	0.588	0.6	0.612	V
Enable Control						
Enable Voltage	V _{EN}		1.6			V
Shutdown Voltage	V _{EN}				0.7	V
External Transistor Connection current						
EXT Pull-UP Resistance	R _{EXTH}	V _{DS} =8.5V		1		Ω
EXT Pull-Down Resistance	R _{EXTL}	V _{DS} =8.5V		1		Ω
Current Sense						
SCO Voltage	V _{SCO}	ISP-ISN=1mV RG1=RG2=1KΩ, R _{SCO} =20KΩ	16	20	24	mV
		ISP-ISN=10mV RG1=RG2=1KΩ, R _{SCO} =20KΩ	190	200	210	mV
		ISP-ISN=20mV RG1=RG2=1KΩ, R _{SCO} =20KΩ	380	400	420	mV
SCO Source Current	I _{SCO}	V _{SCO} =0V			100	μA
Current Limit						
SCO Threshold Voltage	V _{SCO}		1.176	1.2	1.224	V
Thermal Shutdown						
Thermal Shutdown Threshold	T _{TS}			+150		°C

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Typical Operating Characteristics

($T_A=25^{\circ}\text{C}$, unless otherwise specified)



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Function Description

Operation

The FP5208 and FP5208B are voltage mode boost controllers. They operate with pulse width modulation (PWM). The internal resistive divider provides 0.6V reference for the error amplifier. They change to PSM mode when outputs are light load. They can increase efficiency, but PSM mode also increases output voltage ripple.

Soft Start Function

Soft start time is programmable to connect capacitor between SS pin to ground. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current during power on. The soft start bias current is 1.5μA.

Oscillator

The oscillator frequency can be set from 100KHz to 1000KHz by connecting a resistance between RT to ground. Acceptable resistance values range from 300KΩ to 20KΩ. The frequency is 200KHz when the resistance is unconnected. The relationship between the timing resistance RT and frequency is shown in Figure 1. The oscillator frequency can be calculated using formula below.

$$RT(K\Omega) = \frac{25000}{f_{OSC}(KHz)}$$

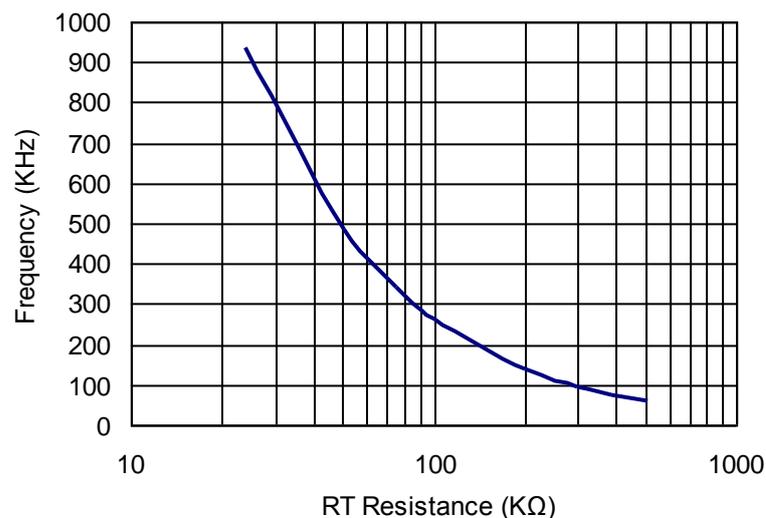


Figure 1. Frequency vs. RT Resistance

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Enable Mode / Shutdown Mode

Drive the EN pin to ground to shutdown the IC. Shutdown mode forces to turn off all internal circuitry, and reduces the HVDD supply current to 1uA (max). The EN pin rising threshold is 1.6V. Before any operation begins, the voltage at EN pin must exceed 1.6V. For automatic startup application, pull up the EN pin with 100kΩ resistance. The EN pin can't be left floating.

Current Detection and Over Current Protection

Figure 2 shows as below the FP5208B current detection and over current application circuit, the load current (I_L) flows from V_{OUT} to ground and generates a voltage difference V_S at the sense resistance (R_S). The SCO pin voltage can be calculated using formula below.

$$V_S = I_L \times R_S, \quad V_{SCO} = V_S \times \frac{R_{SCO}}{RG2}$$

The over current protection is triggered when the SCO pin voltage is higher than 1.2V, which cause output voltage decreasing. The capacitor is added from SCO pin to ground, which is a simple method to delay the converting time. When a transient voltage happens at sense resistance (R_S), the IC would change sourcing current to the SCO pin and generate a voltage change.

To set the over current trip point, follow below equation:

$$I_{OCP} = \frac{1.2V}{R_S} \times \frac{RG2}{R_{SCO}}$$

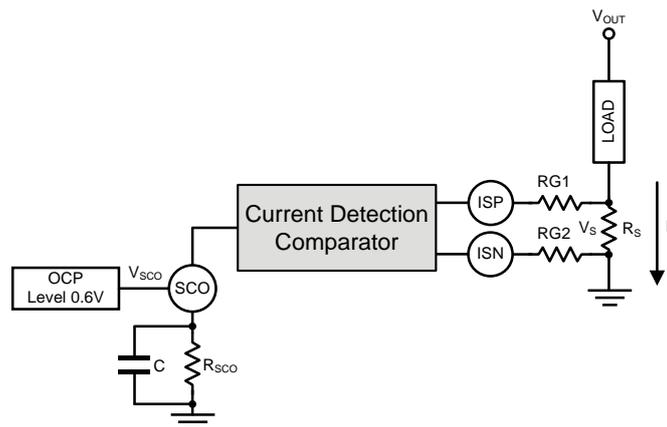


Figure 2. FP5208B Current Detection and Over Current Application Circuit

Thermal Shutdown Protection

The IC will shut down automatically when the internal junction temperature exceeds +150°C. The device can restart until the junction temperature drops below +120°C approximately.

Application Information

Inductor Selection

Inductance value is decided based on different condition. 4.7μH to 22μH inductance value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency.

Capacitor Selection

The output capacitor is required to maintain the DC voltage during switching. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

Diode Selection

Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

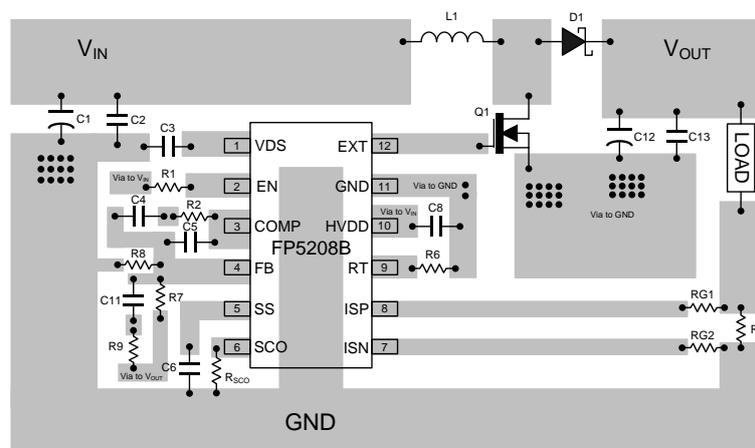
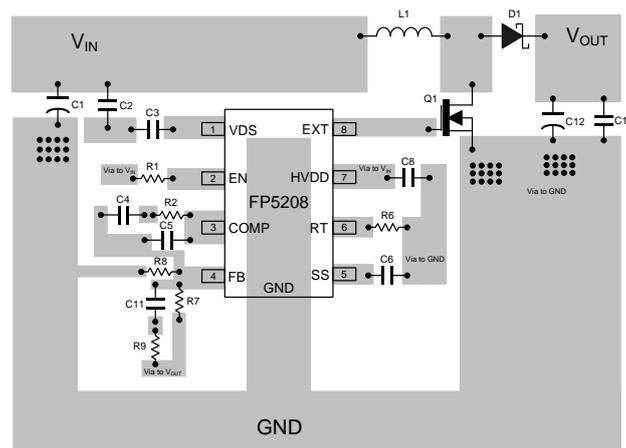
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{\text{OUT}} = 0.6V \left(1 + \frac{R7}{R8} \right)$$

Layout Considerations

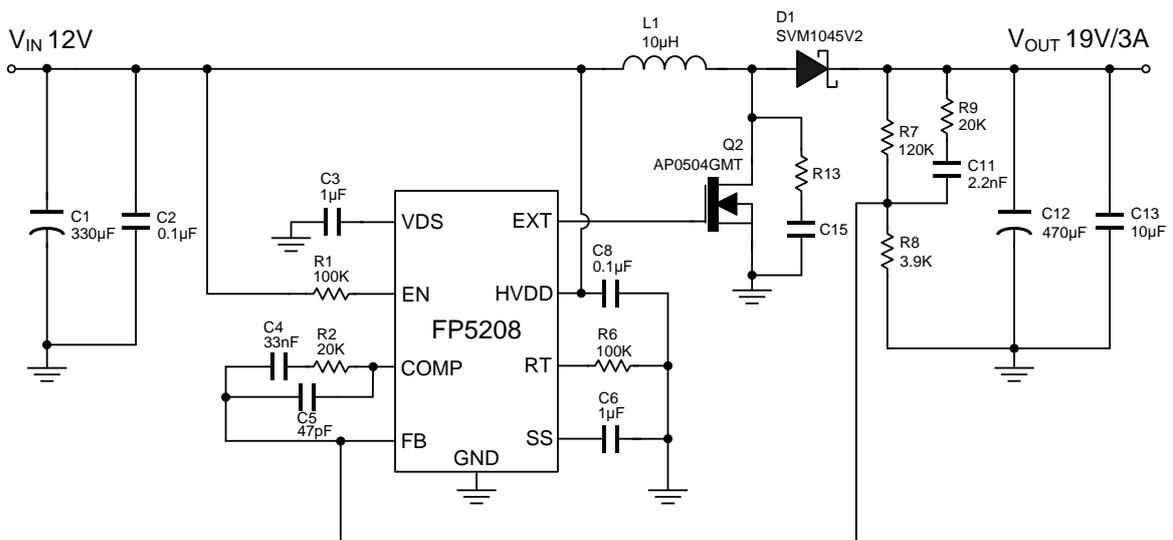
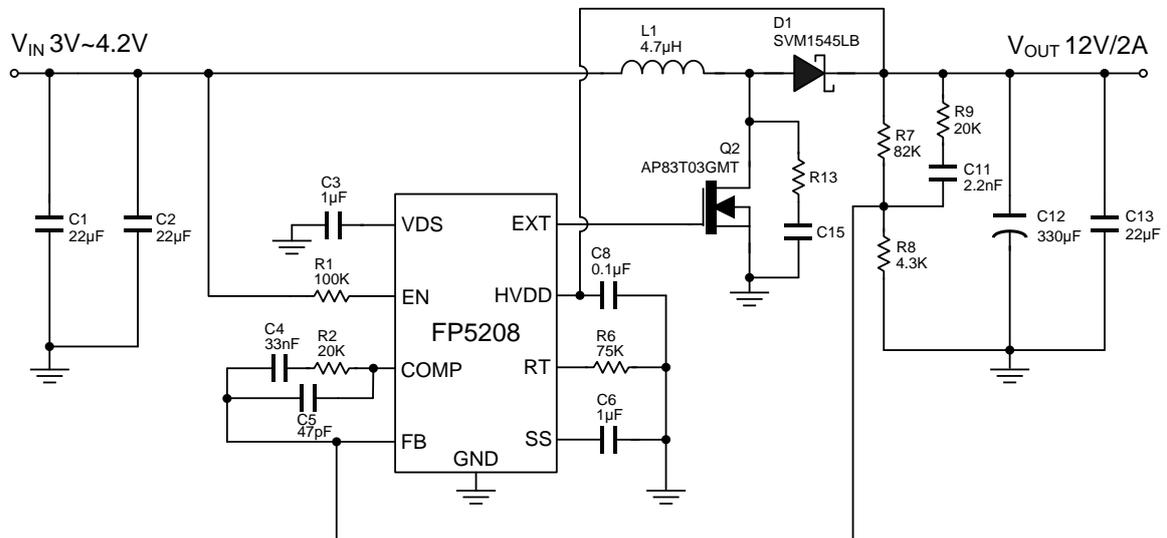
1. The power traces, consisting of the GND trace, the MOS drain trace and the V_{IN} trace should be kept short, direct and wide.
2. Layout switching node MOS drain, inductor and schottky diode connection traces wide and short to reduce EMI.
3. Place C8 nearby HVDD pin as closely as possible to maintain input voltage steady and filter noise.
4. The resistive divider R7 and R8 must be connected to FB pin directly and as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node, MOS drain.
6. The GND of the Q1, C1, C2, C12 and C13 should be connected close and together directly to a ground plane.
7. RG1 and RG2 must be connected to sense resistance (R_s) directly as closely as possible.
8. The output capacitor C12 and C13 should be connected close and together directly to the ground of Q1.



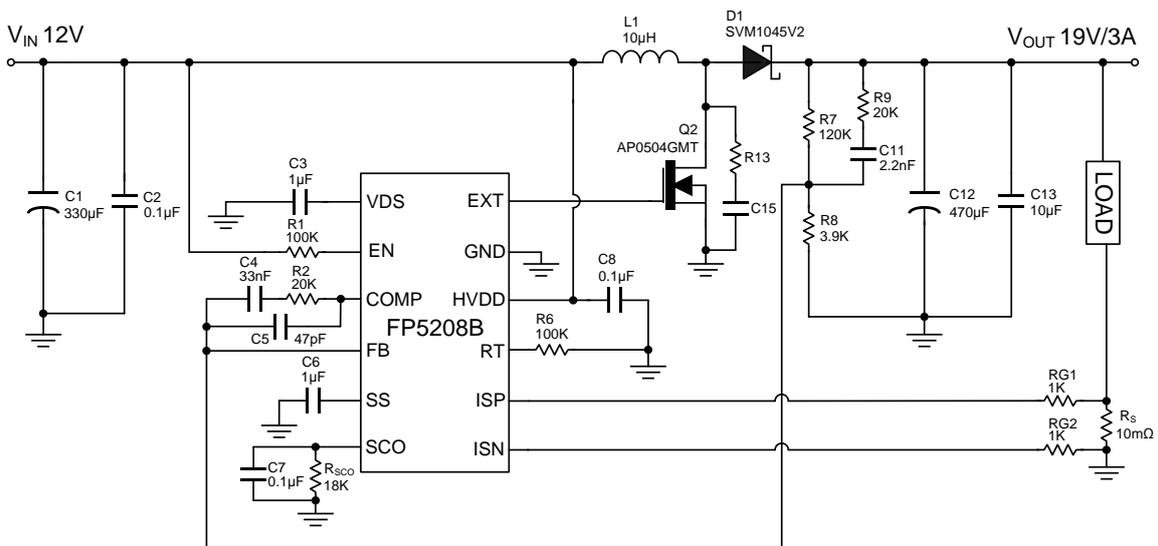
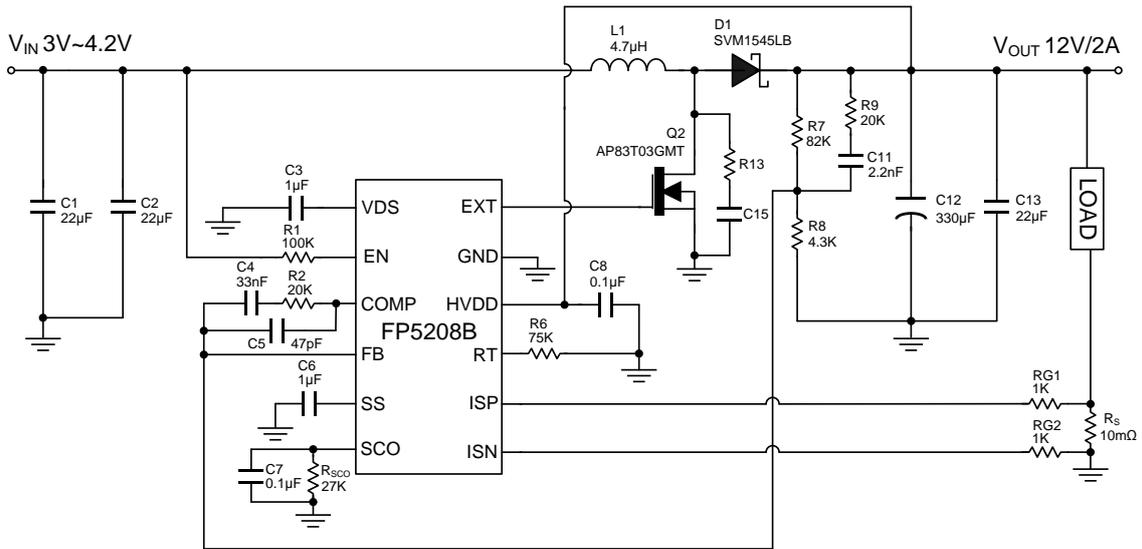
Suggested Layout

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Application Information



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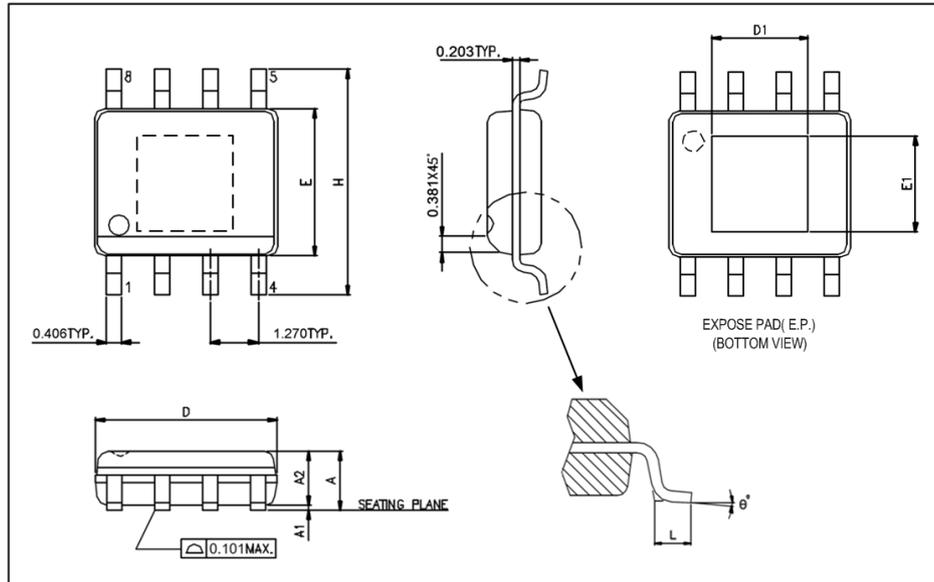

Note:

1. The X5R and X7R of ceramic capacitors are recommended to choose.
2. R13 and C15 are added for reducing EMI (Electromagnetic Interference).

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Package Outline

SOP-8L (EP)



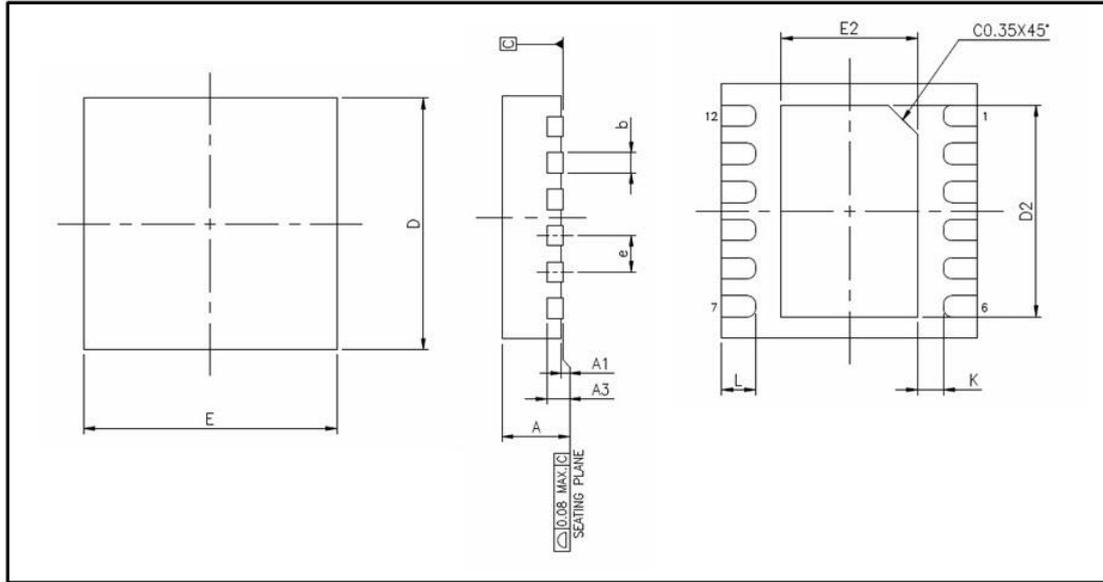
Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	1.94	2.29
D1	1.94	2.29

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E" does not include inter-lead flash or protrusions.

DFN-12L


Symbols	Min. (mm)	Max. (mm)
A	0.700	0.800
A1	0.000	0.050
A3	0.200 REF	
b	0.180	0.280
D	3.000BSC	
E	3.000BSC	
e	0.450BSC	
L	0.300	0.500
K	0.200	-

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)	LEAD FINISH		JEDEC CODE
			Pure Tin	PPF	
E2	1.500	1.650	V	X	N/A
D2	2.400	2.550			

Note:

1. All dimensions are in millimeters.
2. Dimension "b" applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

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