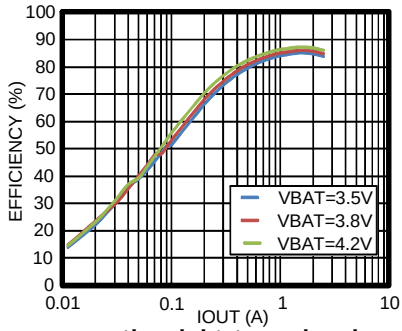
I2C Controlled 3A Single Cell USB Charger with Narrow VDC Power Path Management and USB OTG

Features

- **High Efficiency 3A Switch Mode Charge**
- **Single Input USB-compliant/Adapter Charge**
  - Input Voltage and Current Limit Supports USB 2.0 and USB 3.0
  - Input Current Limit: 100mA, 150mA, 500mA, 900mA, 1A, 1.5A, 2A and 3A
- **3.9V - 6.2V Input Operating Voltage Range**
  - Support Adapter with Input Voltage DPM Regulation
- **USB OTG with Adjustable Output 4.55V to 5.5V at 1 A or 1.5A**
  - Accurate +/- 15%
  - Hiccup Mode Overcurrent Protection
- **Narrow VDC (NVDC) Power Path Management**
  - Instant-on Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- **1.5MHz Switching Frequency for Low Profile Inductor**
- **Autonomous Battery Charging with or without Host Management**
  - Battery Charge Enable
  - Battery Charge Preconditioning
  - Charge Termination and Recharge
- **Accuracy**
  - ±0.5% Charge Voltage Regulation
  - ±7% Charge Current Regulation
  - ±7.5% Input Current Regulation
  - ±3% Output Regulation in Boost Mode



- **High Integration**
  - Power Path Management
  - Synchronous Switching MOSFETs
  - Integrated Current Sensing
  - Internal Loop Compensation
- **Safety**
  - Battery Temperature Sensing for Charging and Discharging in OTG Mode
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input System Over-Voltage Protection
  - MOSFET Over-Current Protection
- **Charge Status Outputs for LED or Host Processor**
- **Maximum Power Tracking capability by Input Voltage Regulation**
- **32μA Low Battery Leakage Current and Support Shipping Mode**
- **TQFN 4x4 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Tablet PC**
- **Smart Phone**
- **Portable Audio Speaker**
- **Portable Media Players**
- **Internet Devices**

General Description

The APW7264 is a highly-integrated switch-mode battery charge management and system power path management device for single cell Li-ion and Li-polymer battery in a wide range of tablet and other portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I²C serial interface with charging and system settings makes the device a truly flexible solution.

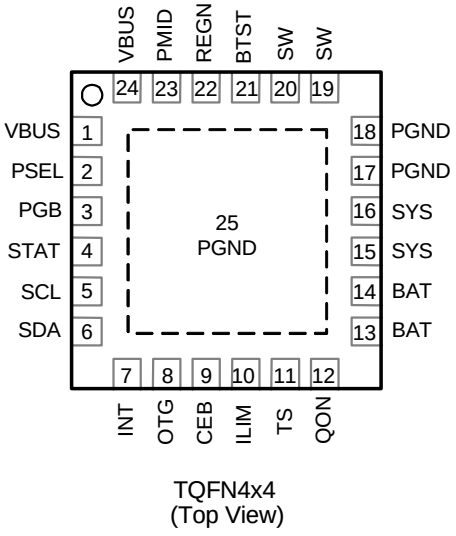
The device supports 3.9V - 6.2V USB input sources, including standard USB host port and USB charging port with 6. 4V over-voltage protection. The device supports USB 2.0 and USB 3.0 power specifications with input current and voltage regulation. To set the default input current limit, the APW7264 takes the result from the detection circuit in the system, such as USB PHY device. The device also supports USB On-the-Go operation by providing fast startup and supplying adjustable voltage 4.55 ˇV 5.5V (default 5V) on the VBUS with an accurate current limit up to 1.5A. The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system keeps operating even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, the power path management automatically reduces the charge current to zero and then starts discharges the battery until the system power requirement is met. This supplement mode operation keeps the input source from getting overloaded.

The device initiates and completes a charging cycle when host control is not available. It automatically charges the battery in three phases: pre-conditioning, constant current and constant voltage. In the end, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. Later on, when the battery voltage falls below the recharge threshold, the charger will automatically start another charging cycle. The charge device provides various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer and over-voltage/over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable).

The STAT output reports the charging status and any fault conditions. The INT immediately notifies host when fault occurs.

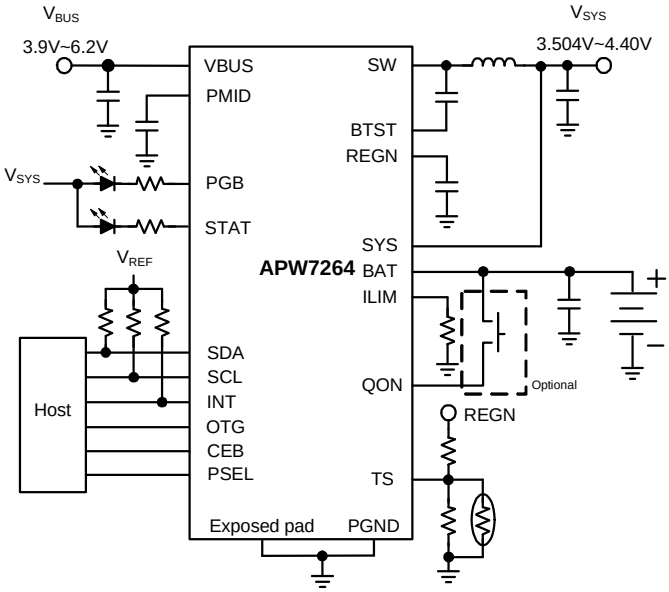
The APW7264 is available in a 24-pin, 4x4 mm² thin QFN package.

Pin Configuration



TQFN4x4
(Top View)

Simplified Application Circuit



Ordering and Marking Information

APW7264 □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QB: TQFN4x4
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW7264 QB : 

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VBUS}	VBUS to GND Voltage	-2 ~ 15	V
	PMID to GND Voltage	-0.3 ~ 15	V
	BTST, STAT, PGB to GND Voltage	-0.3 ~ 12	V
	SW to GND Voltage	-2 ~ 7	V
	BAT, SYS (converter not switching) to GND Voltage	-0.3 ~ 6	V
	SDA, SCL, INT, OTG, ILIM, REGN, TS, QON, CEB, PSEL to GND Voltage	-0.3 ~ 7	V
	BTST to SW Voltage	-0.3 ~ 7	V
	PGND to GND	-0.3 ~ 0.3	V
	INT, STAT, PGB Output Sink Current	6	mA
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	52	°C/W
θ_{JC}	Junction-to-Case Resistance	7	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN4x4 is soldered directly on the PCB

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VBUS}	VBUS to GND Voltage	3.9 ~ 6.2	V
I_{SYS}	SYS Output Current	0 ~ 3.5	A
V_{BAT}	BAT to GND Voltage	3.5 ~ 4.4	V
I_{BAT}	Fast Charging Current	~ 3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLOZ}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEP}$, and T_A= -40 to 85 °C. Typical values are at T_A = 25°C

Symbol	Parameter	Test Conditions		APW7264			Unit
				Min	Typ	Max	
QUIESCENT CURRENTS							
I_{BAT}	Battery Discharge Current (BAT, SW, SYS)	V_{VBUS}=flaoting, V_{BAT}=4.2V, leakage between BAT and VBUS (VBUS to GND Leakage)		-	-	5	µA
		High-Z mode, or no V_{VBUS}, BATFET disabled (REG07[5]=1), T_A= -40 to 85 °C		-	32	55	µA
		High-Z mode, or no V_{VBUS}, BATFET enabled REG07[5]=0, T_A= -40 to 85 °C		-	32	55	µA
I_{VBUS}	Input Supply Current (VBUS)	V_{VBUS}=5V, High-Z mode, No battery		-	32	55	µA
		$V_{VBUS}>V_{VBUS\_UVLOZ}$, $V_{VBUS}>V_{BAT}$, converter not switching			4.5	6	mA
		$V_{VBUS}>V_{VBUS\_UVLOZ}$, $V_{VBUS}>V_{BAT}$, converter switching, V_{BAT}=3.2V, I_{SYS}=0A		-	35	-	mA
		$V_{VBUS}>V_{VBUS\_UVLOZ}$, $V_{VBUS}>V_{BAT}$, converter switching, V_{BAT}=3.8V, I_{SYS}=0A		-	35	-	mA
$I_{OTGBOOST}$	Battery Discharge Current In Boot Mode	V_{BAT}=4.2V, Boost mode, I_{VBUS}=0A, converter switching		-	25	-	mA
VBUS/BAT POWER UP							
	VBUS Operating Voltage Range			3.9	-	6.2	V
V_{VBUS_UVLOZ}	VBUS For Active I²C, No Battery	V_{VBUS} rising		3.6	-	-	V
V_{SLEEP}	Sleep Mode Falling Threshold	V_{VBUS} falling, V_{VBUS}-V_{BAT}		35	80	120	mV
V_{SLEEPZ}	Sleep Mode Rising Threshold	V_{VBUS} rising, V_{VBUS}-V_{BAT}		170	250	350	mV
V_{ACOV}	VBUS Over Voltage Rising Threshold	V_{VBUS} rising		6.2	-	6.6	V
V_{ACOV_HYS}	VBUS Over Voltage Falling Hysteresis	V_{VBUS} falling		-	200	-	mV
V_{BAT_DPL}	Battery Depletion Threshold	V_{BAT} falling		-	2.4	2.6	V
$V_{BAT\_DPL\_HYS}$	Battery Depletion Rising Hysteresis	V_{BAT} rising		-	150	-	mV
POWER PATH MANAGEMENT							
V_{SYS_MAX}	Maximum DC System Voltage Output	I_{SYS}=0A, BATFET (Q4) off, V_{BAT} up to 4.35V		-	-	4.43	V
V_{SYS_MIN}	Minimum DC System Voltage Output	REG01[3:1]=101, V_{SYSMIN}=3.5V		3.5	3.65	-	V
$R_{ON(RBFET)}$	Internal Top Reverse Blocking MOSFET On-Resistance	Measured between VBUS and PMID		-	28	41	mΩ
R_{ON_HS}	Internal Top Switching MOSFET On-resistance	Measured between PMID and SW	T_A=-40°C ~85°C	-	61	82	mΩ
			T_A=-40°C~125°C	-	61	90	
R_{ON_LS}	Internal Bottom Switching MOSFET On-resistance	Measured between SW and PGND	T_A=-40°C~85°C	-	61	82	mΩ
			T_A=-40°C~125°C	-	61	90	

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLOZ}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEP}$, and T_A= -40 to 85 °C. Typical values are at T_A = 25°C

Symbol	Parameter	Test Conditions		APW7264			Unit
				Min	Typ	Max	
POWER PATH MANAGEMENT							
V_{FWD}	BATFET Forward Voltage In Supplement Mode	V_{BAT} -V_{SYS}, BAT discharge current 10mA		-	30	-	mV
V_{BATGD}	Battery Good Comparator Rising Threshold	V_{BAT} rising		-	3.55	-	V
V_{BATGD_HYS}	Battery Good Comparator falling Hysteresis	V_{BAT} falling		-	100	-	mV
BATTERY CHARGER							
$V_{BAT\_REG\_ACC}$	Charge Voltage Regulation Accuracy	V_{BAT}=4.112V and 4.208V		-0.5	-	+0.5	%
$I_{CHG\_REG\_ACC}$	Fast Charge Current Regulation Accuracy	V_{BAT}=3.8V, I_{CHG}=1024mA	T_A= 25°C	-4	-	+4	%
			T_A= -20°C ~125°C	-7	-	+7	
		V_{BAT}=3.8V, I_{CHG}=1792mA	T_A= -20°C ~125°C	-10	-	+10	
$I_{CHG\_20\%}$	Charge Current With 20% Option On	V_{BAT}=3.8V, REG02=01		-	100	-	mA
$V_{BATLOWV\_F}$	Battery LOWV Falling Threshold	Fast charge to precharge, REG04[1]=1		2.6	2.8	2.9	V
$V_{BATLOWV\_R}$	Battery LOWV Rising Threshold	Precharge to fast charge, REG04[1]=1		2.8	3.0	3.1	V
I_{PRECHG_ACC}	Precharge Current Regulation Accuracy	V_{BAT}=2.6V, I_{CHG}=128mA		-	20	-	%
I_{TERM_ACC}	Termination Current Accuracy	I_{TERM}=256mA, I_{CHG}=2048mA		-20	-	+20	%
V_{BAT_SHORT}	Battery Short Voltage	V_{BAT} falling		-	2	-	V
$V_{BAT\_SHORT\_HYS}$	Battery Short Voltage Hysteresis	V_{BAT} rising		-	200	-	mV
I_{SHORT}	Battery Short Current	V_{BAT}<2.2V		-	100	-	mA
V_{RECHG}	Recharge Threshold Below VBAT_REG	V_{BAT} falling, REG04[0]=0		-	100	-	mV
t_{RECHG}	Recharge Deglitch Time	V_{BAT} falling, REG04[0]=0		-	100	-	ms
R_{ON_BATFET}	SYS-BAT MOSFET On-resistance	T_A= 25°C		-	24	28	mΩ
		T_A= -20°C ~125°C		-	24	35	
INPUT VOLTAGE/CURRENT REGULATION							
$V_{INDPM\_REG\_ACC}$	Input Voltage Regulation Accuracy			-2	-	+2	%
I_{USB_DPM}	USB Input Current Regulation Limit	V_{BUS}=5V, current pulled from SW	USB100	85	-	100	mA
			USB150	125	-	150	mA
			USB500	440	-	500	mA
			USB900	750	-	900	mA
I_{ADPT_DPM}	Input Current Regulation Accuracy	Input current limit 1.5A, REG00[2:0]=101		1.3	-	1.5	A
I_{IN_START}	Input Current Limit During Start Up	V_{SYS}<2.2V		-	100	-	mA
	ILIM Pin Source Current	ILIM Pin Current Limit method		17	20	23	µA
BATTERY OVER-VOLTAGE PROTECTION							
V_{BATOVP}	Battery Over-Voltage Threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		-	106	-	%
V_{BATOVP_HYS}	Battery Over-Voltage Hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		-	2	-	%
THERMAL REGULATION AND THERMAL SHUTDOWN							
T_{J_REG}	Junction Temperature Regulation	REG06[1:0]=11		-	120	-	°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature increasing		-	160	-	°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis			-	30	-	°C

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLOZ}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEP}$, and T_A= -40 to 85 °C. Typical values are at T_A = 25°C

Symbol	Parameter	Test Conditions	APW7264			Unit
			Min	Typ	Max	
COLD/HOT THERMISTER COMPARATOR						
V_{LTF}	Cold Temperature Threshold	TS pin voltage rising threshold. Charger suspends charge. As percentage to V_{REGN}	73	73.5	74	%
V_{LTF_HYS}	Cold Temperature Hysteresis	TS pin voltage falling. As percentage to V_{REGN}	-	0.4	-	%
V_{HTF}	Hot Temperature Threshold	TS pin voltage rising threshold. As percentage to V_{REGN}	46.6	47.2	48.8	%
V_{TCO}	Cut-off Temperature Threshold	TS pin voltage falling. As percentage to V_{REGN}	44.2	44.7	45.2	%
V_{BCOLD0}	Cold Temperature Threshold 0	TS pin voltage rising, As persentage to V_{REGN} REG02[1]=0 (Approx. -10°C w/103AT)	75	76	77	%
V_{BCOLD0_HYS}	Cold Temperature Threshold 0 Hysteresis	TS pin voltage falling, As persentage to V_{REGN} REG02[1]=0 (Approx. 1°C w/103AT)	-	1	-	%
V_{BCOLD1}	Cold Temperature Threshold 1	TS pin voltage rising, As persentage to V_{REGN} REG02[1]=1 (Approx. -20°C w/103AT)	77.5	78.5	79.5	%
V_{BCOLD1_HYS}	Cold Temperature Threshold 1 Hysteresis	TS pin voltage falling, As persentage to V_{REGN} REG02[1]=0 (Approx. 1°C w/103AT)	-	1	-	%
V_{BHOT0}	Hot Temperature Threshold 0	TS pin voltage falling, As persentage to V_{REGN} REG06[3:2]=01 (Approx. 55°C w/103AT)	35.5	36	36.5	%
V_{BHOT0_HYS}	Hot Temperature Threshold 0 Hysteresis	TS pin voltage rising, As persentage to V_{REGN} REG06[3:2]=01 (Approx. 3°C w/103AT)	-	3	-	%
V_{BHOT1}	Hot Temperature Threshold 1	TS pin voltage falling, As persentage to V_{REGN} REG06[3:2]=00 (Approx. 60°C w/103AT)	32.5	33	33.5	%
V_{BHOT1_HYS}	Hot Temperature Threshold 1 Hysteresis	TS pin voltage rising, As persentage to V_{REGN} REG06[3:2]=00 (Approx. 3°C w/103AT)	-	3	-	%
V_{BHOT2}	Hot Temperature Threshold 2	TS pin voltage falling, As persentage to V_{REGN} REG06[3:2]=10 (Approx. 65°C w/103AT)	29.5	30	30.5	%
V_{BHOT2_HYS}	Hot Temperature Threshold 2 Hysteresis	TS pin voltage rising, As persentage to V_{REGN} REG06[3:2]=10 (Approx. 3°C w/103AT)	-	3	-	%
CHARGE OVER-CURRENT COMPARATOR						
I_{HSFET_OCP}	HSFET Over-Current Threshold		5.3	7	-	A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{LSFET_ZC}	Low Side MOSFET Zero Crossing Threshold	From sync mode to non-sync mode	-	100	-	mA
PWM OPERATION						
f_{SW}	PWM Switching Frequency		1.3	1.5	1.7	MHz
D_{MAX}	Maximum PWM Duty Cycle		-	97	-	%

Electrical Characteristics (Cont.)

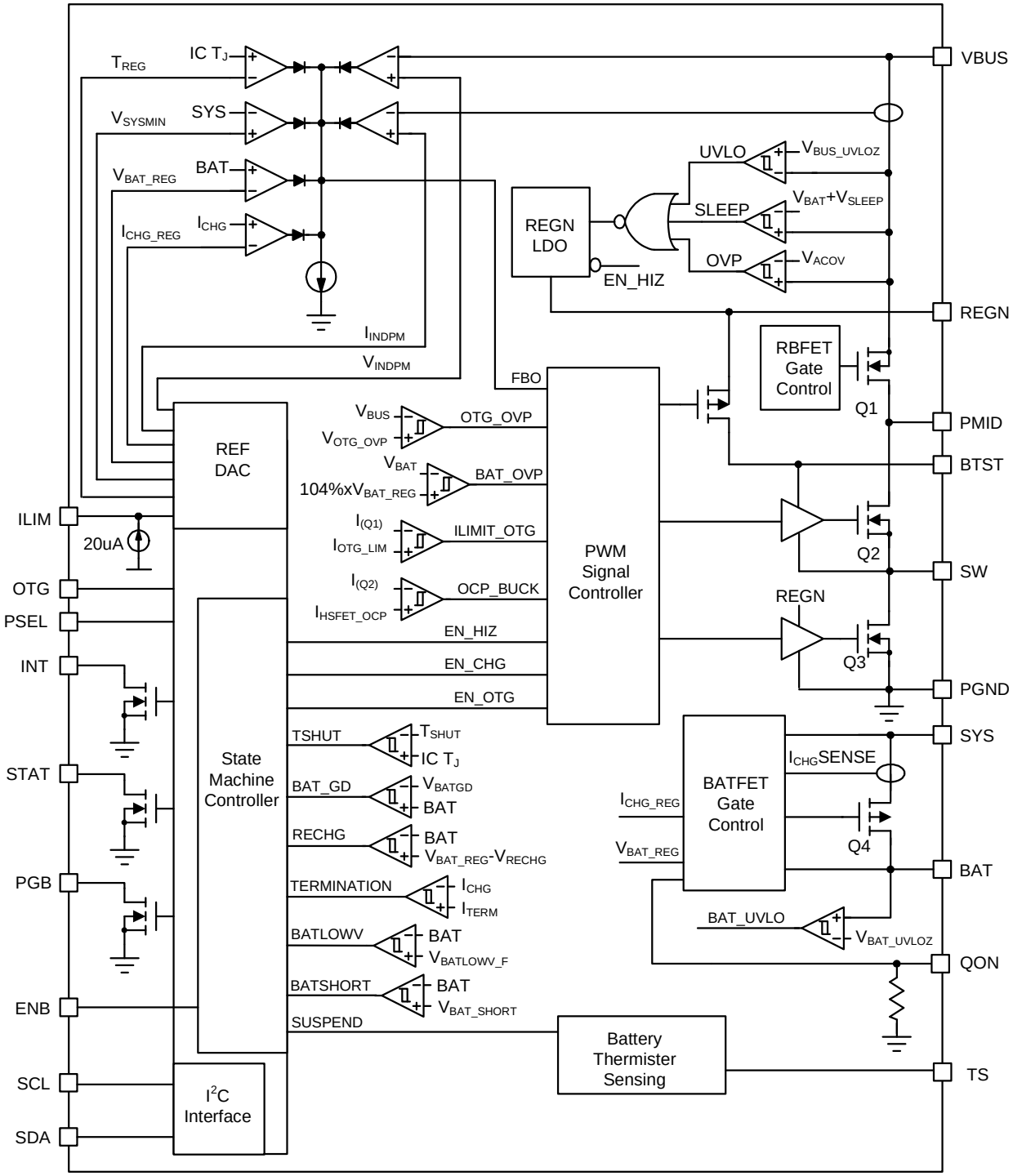
Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLOZ}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEP}$, and T_A= -40 to 85 °C. Typical values are at T_A = 25°C

Symbol	Parameter	Test Conditions	APW7264			Unit
			Min	Typ	Max	
BOOST MODE OPERATION						
V_{OTG_REG}	OTG Output Voltage	I_{VBUS}=0A, REG06[7:4]=0111(4.998V)	-	5	-	V
$V_{OTG\_REG\_ACC}$	OTG Output Voltage Accuracy	I_{VBUS}=0A, REG06[7:4]=0111(4.998V)	-3	-	+3	%
V_{INOTG_BAT}	Battery Voltage Into OTG mode	VBAT Rising, IOTG=0A, REG04[1]=1	-	-	3.1	V
V_{OUTOTG_BAT}	Battery Voltage Exit OTG mode	VBAT Falling, IOTG=0A, REG04[1]=1	2.9	-	-	V
I_{OTG}	OTG Mode Output Current	REG01[0]=0	1	-	-	A
		REG01[0]=1	1.5	-	-	
V_{OTG_OVP}	OTG Over-Voltage Threshold	Rising threshold	-	6	-	V
V_{BATMAX}	Maximum Battery Voltage for Boost Mode	V_{BAT} Rising Edge During Boost Mode	-	4.9	-	V
V_{BATMAX_HYS}	Maximum Battery Voltage Hysteresis for Boost Mode	V_{BAT} Falling From Above V_{BATMAX}	-	200	-	mV
I_{OTG_LIM}	Low Side MOSFET Cycle-by-cycle Current Limit		-	5	-	A
I_{OTG_ZC}	High Side MOSFET Zero Crossing Threshold	High side FET current falling	-	100	-	mA
I_{RBFET_LIM}	RBFET Current Limit Threshold	REG01[0]=1	1.5	1.7	1.9	A
		REG01[0]=0	1	1.15	1.3	
$T_{OTG\_OCP\_OFF}$	OTG OCP Off Time	OTG mode over-current protection off cycle time	-	32	-	ms
$T_{OTG\_OCP\_ON}$	OTG OCP On Time	OTG mode over-current protection on cycle time	-	2	-	ms
REGN LDO						
V_{REGN}	REGN LDO Output Voltage	V_{VBUS}=5V, I_{REGN}=0mA	4.8	5	5.5	V
		V_{VBUS}=5V, I_{REGN}=20mA	4.4	4.8	-	V
I_{REGN}	REGN LDO Output Current	V_{VBUS}=5V, V_{REGN}=3.8V	30	-	-	mA
LOGIC I/O PIN CHARACTERISTICS (OTG, CEB, STAT, QON, PSEL, PGB)						
V_{IL}	Input Low Voltage		-	-	0.4	V
V_{IH}	Input High Voltage		1.3	-	-	V
V_{O_LOW}	Output Low Saturation Voltage	Sink current=5mA, Include STAT/PGB Pins	-	-	0.4	V
I_{BIAS}	High Level Leakage Current (OTG, CEB, STAT, PSEL, PGB)	Pull up rail 1.8V	-	-	1	µA
I_{BIAS}	High Level Leakage Current (QON)	Pull up rail 3.6V	-	-	8	µA
I²C INTERFACE (SDA, SCL, INT)						
V_{IH}	Input High Threshold Level	VPULL-UP=1.8V, SDA and SCL	1.3	-	-	V
V_{IL}	Input Low Threshold Level	VPULL-UP=1.8V, SDA and SCL	-	-	0.4	V
V_{O_LOW}	Output Low Threshold Level	Sink current=5mA	-	-	0.4	V
I_{BIAS}	High Level Leakage Current	VPULL-UP=1.8V, SDA and SCL	-	-	1	µA
f_{SCL}	SCL Clock Frequency		-	-	400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
T_{QON}	QON Pulsed width	QON Pin High to Turn On BATFET	2	-	-	ms
t_{WDT}	Watchdog Timer	REG05[5:4]=11	-	160	-	sec

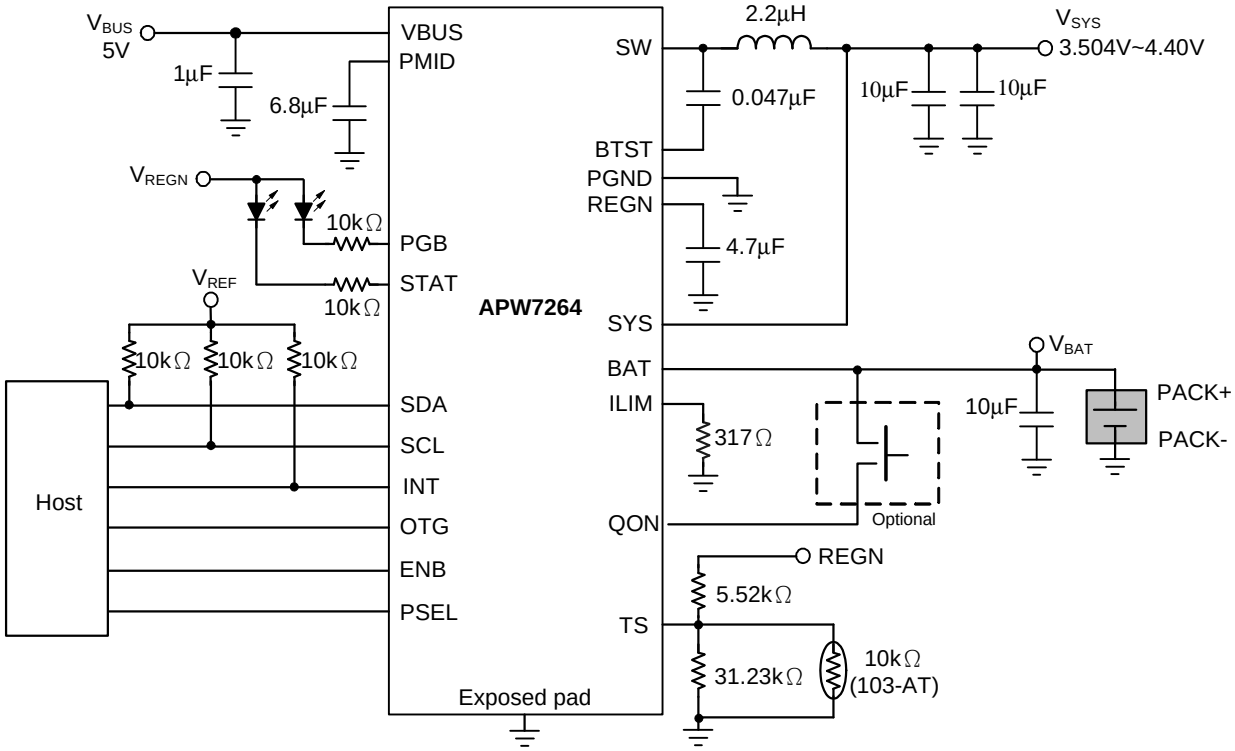
Pin Description

PIN		FUNCTION
NO.	NAME	
1,24	VBUS	Charger input voltage. Place a 1µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
2	PSEL	Power source selection input. Low indicates an adapter source and High indicates a USB host source.
3	PGB	Open drain active low power good indicator. Connect to the pull up rail via 10kΩ resistor. Low indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold.
4	STAT	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via a 10kΩ resistor. Low indicates charge in progress. High indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks at 1Hz.
5	SCL	I^2C interface clock.
6	SDA	I^2C interface data.
7	INT	Open interrupt output. Connect the INT to the pull up rail via 10kΩ resistor. The INT pin sends active low, 256µs pulse to host to report charger device status and fault.
8	OTG	USB current limit selection pin during buck mode, and OTG mode enabled control pin. In buck mode with USB host (PSEL=High), when OTG=High, IIN limit=500mA and when OTG=Low, IIN limit=100mA. The OTG mode is activated when the REG01[5:4]="10" or "11" and OTG pin is high.
9	CEB	Active low charge enable pin. Battery charging is enabled when REG01[6:5]="01" and CEB pin=low. CEB pin must be pulled high or low.
10	ILIM	Input Current Limit Setting Pin. Connect a resistor (R_{ILIM}) from this pin to the GND. This resistor, an internal 20µA current source (I_{ILIM}) set the maximum input current limit.The actual input current limit is the lower on set by ILIM and by I^2C REG00[2:0].
11	TS	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. Recommend 103AT-2 thermistor.
12	QON	BATFET enable control in shipping mode. A logic low to high transition on this pin with minimum 2ms high level turns on BATFET to exit shipping mode.
13	BAT	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10µF closely to the BAT pin.
14		
15	SYS	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage.
16		
17	PGND	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the N-channel low side MOSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
18		
19	SW	Junction point of the Internal high-side MOSFET Source, output filter inductor and internal the low-side MOSFET Drain. Connect the 47nF bootstrap capacitor from SW to BTST.
20		
21	BTST	Supply Input for the Internal high-side gate driver and an internal level-shift circuit. Connect to an external ceramic capacitor 47nF from SW to BTST to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
22	REGN	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7µF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
23	PMID	Converter Input Voltage. Connect at least 6.8µF ceramic capacitor from PMID to PGND and place it as close as possible to IC.
-	Exposed Pad	Exposed pad beneath the IC for heat dissipation and also the IC analog ground. Always solder thermal pad to the board, and have vias on the thermal pad plane to PGND and ground plane for high-current power converter.

Block Diagram



Typical Application Circuit



Function Description

The APW7264 is an I²C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery.

The APW7264 is a switch-mode battery charger with fixed 1.5MHz switching frequency, which drives two integrated N-channel power MOSFETs. The step-down DC/DC converter is ideally suited for portable electronic devices. In addition, the APW7264 can supply 5V to USB On-The-Go (OTG) peripherals through I²C programmable.

The APW7264 has three operation states in substance:

1.Charge State - charges a single-cell Li-ion or Li-polymer battery with an integrated synchronous rectification buck regulator.

2.Boost State - supply 5V power to USB-OTG with an integrated synchronous rectification boost regulator using battery terminal as input.

3.High-Impedance State - Both the charging and OTG circuits are off. This state consumes low quiescent current from VBUS or the battery.

Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. The battery depletion comparator, sleep comparator and BATFET driver are active when VBUS or VBAT rises above UVLOZ. I²C interface is actived and all the registers are reset to default value.

Power Up from Battery without DC Source

If only battery is present and the VBAT voltage is above depletion threshold (V_{BAT_DEPL}), it turns the BATFET on to connect battery to system. The REGN LDO stays off to minimize the quiescent current and maximize the battery run time.

BATFET Turn Off

The host can through I²C REG07[5] force the BATFET to tunn off . When the battery condition becomes abnormal during charging, the user can use this bit to independently turn off the BATFET. When the BATFET is off, there is no path to charge or discharge the battery.

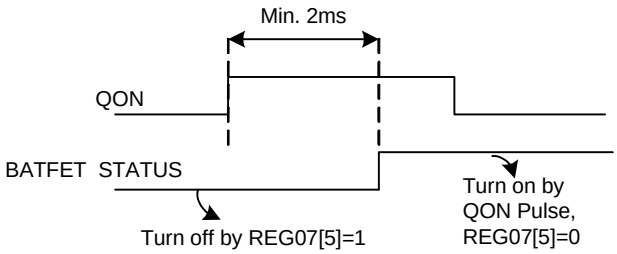
When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode. In general, no the battery attached condition is not recommended.

Shipping Mode

When end equipment is assembled, the system is connected to battery through BATFET. There will be a small leakage current to discharge the battery even when the system is powered off. In order to extend the battery life during shipping and storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage.

In order to keep BATFET off during shipping mode, the host has to turn off BATFET (REG07[5]=1) and disable the watchdog timer (REG05[5:4]=00) at the same time. Once the BATFET is disabled, one of the following events can turn on BATFET and clear REG07[5] (BATFET_DISABLE) bit.

1. Plug in adapter
2. Write REG07[5] = 0
3. Watchdog timer expiration
4. Register reset (REG01[7] = 1)
5. A logic low to high transition on QON pin



Turn on BATFET by QON Low to high Pulse

Power Up from DC Source

When the DC source plugs in, the APW7264 checks the input source voltage to turn on REGN LDO and all the bias circuits. It also cateches the input current limit setting value before starts the buck converter.

Function Description (Cont.)

REGN LDO

The APW7264 internal bias circuits as well as the HSFET and LSFET gate drive are supplied by REGN LDO. The REGN LDO also provides bias rail to TS external resistors and the pull-up rail of STAT and PGB can be connected to REGN as well.

The REGN is enabled when all the conditions are valid.
1. VBUS above UVLOZ
2. VBUS above battery + VSLEEPZ in buck mode or VBUS below battery + VSLEEPZ in boost mode

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. In HIZ state, the device draws less than 50μA from VBUS. The system powered up by battery when the device is in HIZ.

Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 3A. After the PGB is low or REG08[2] goes high, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode. The APW7264 sets input current limit through PSEL/OTG and ILIM pins. After the input current limit detection is done, the host can write to REG00[2:0] to change the input current limit.

PSEL/OTG Pins Set Input Current Limit

The APW7264 has PSEL and OTG pin instead of D+/D-. It directly takes the USB PHY device output to decide whether the input is USB host or charging port.

PSEL	OTG	Input Current Limit	REG08[7:6]
HIGH	LOW	100mA	01
HIGH	HIGH	500mA	01
LOW	X	3A	10

Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

When the system rail is below 2V, the input current limit is forced to 100mA. After the system rises above 2.2V, the charger device sets the input current limit value by the lower value between register and ILIM pin setting. As a battery charger, the APW7264 deploys a 1.5MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light-load efficiency, the device provides PFM control at light load condition. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

Boost Mode Operation from Battery

The APW7264 supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 1A output requirement. The maximum output current is 1.5A. The following conditions are valid to enable the boost operation.
1. VBAT above BATLOWV threshold ($V_{BATLOWV}$ set by REG04[1])
2. VBUS less than VBAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4]=10)
4. After 40ms delay from boost mode enable

In boost mode, APW7264 employs a 1.5MHz step-up switching regulator. To improve ligh load efficiency, the device operates on PFM operation at light load.

During boost mode, the status register REG08[7:6] is set to 11, the VBUS output is 5V. The output current selected via I^2C (REG01[0]) can reach up to 1A or 1.5A. Any fault during boost operation sets the fault register REG09[6] to 1 and an INT is asserted.

Function Description (Cont.)

Power Path Management

The APW7264 accommodates a wide range of input sources from wall adapter, USB, to car battery. The system (SYS) is provided by the automatic power path selection from input source (VBUS), battery (BAT), or both.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is programmed by REG01[3:1]. The system is regulated above the minimum system voltage (default 3.5V) even with a fully depleted battery.

The BATFET operates in linear mode, and the system is 150mV above the minimum system voltage setting when the battery is below minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging, termination are disabled and the battery voltage is above minimum system volatge setting, the system is regulated at 150mV above the battery voltage until V_{SYS} reaches to the programmed battery charging target. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

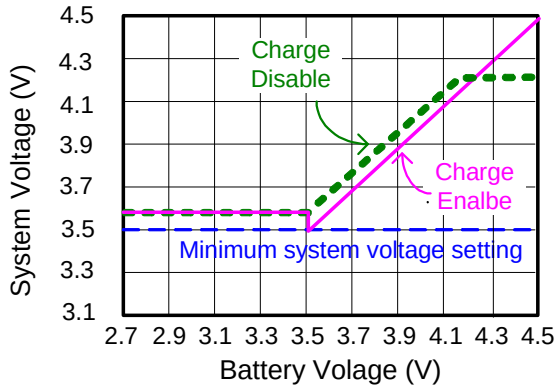


Figure 1. System Voltage vs. Battery Volage

Dynamic Power Management

The total input current is a function of the system supply current and the battery charging current. When the summation of system power and charge power exceeds the maximum VBUS input power, the device will reduce input current by using Dynamic Power Management (DPM).

When input current exceeds the programmed input current limit (REG00[2:0]) or the VBUS falls below the programmed input voltage limit (REG00[6:3]), the device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the battery starts discharging so that the system is provided from both the input source and battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

The Figure 2. as below shows the DPM response and supplement mode.

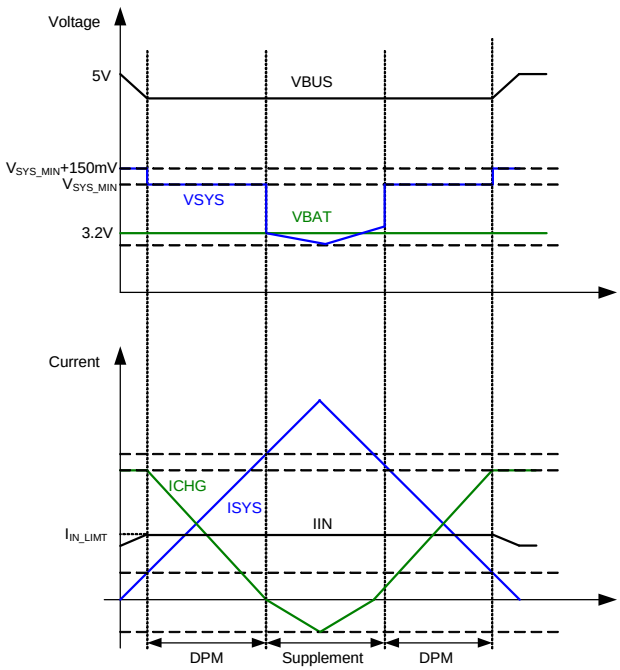


Figure 2. DPM Response

Function Description (Cont.)

Supplement Mode

When the system voltage falls below the battery voltage, the device fully turns on the BATFET. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

Battery Charging Management

The APW7264 charges 1-cell Li-Ion battery with up to 2.5A charge current for high capacity tablet battery. The 24mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), the APW7264 can complete a charging cycle without host involvement.

When the following conditions are valid, a new charge cycle will start.

- Converter starts
- Battery charging is enabled by I²C register bit (REG01[5:4]) = 01 and CEB is low
- No safety timer fault
- No thermistor fault on TS
- BATFET is not forced to turn off (REG07[5])

When the charging current is below programmed termination threshold and battery voltage is above recharge threshold, the charger device automatically terminates the charging cycle. When a full battery voltage is discharged below recharge threshold (REG04[0]), the APW7264 automatically starts another charging cycle. The STAT output indicates the charging status. STAT is low, the device is in charging state; STAT is high, the device is in charging complete or charge disable; STAT is blinking, the device indicates the charging fault. The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host. The host can always control the charging operation by writing to the registers through I²C.

Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and determines the applied current.

VBAT	Charging current	Register default setting	Reg08[5:4]
<2V	100mA	-	01
2~3V	Reg03[7:4]	128mA	01
>3V	Reg02[7:2]	2048mA	10

The actual charging current will be less than the programmed value if the charger device is in DPM state or thermal regulation during charging. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

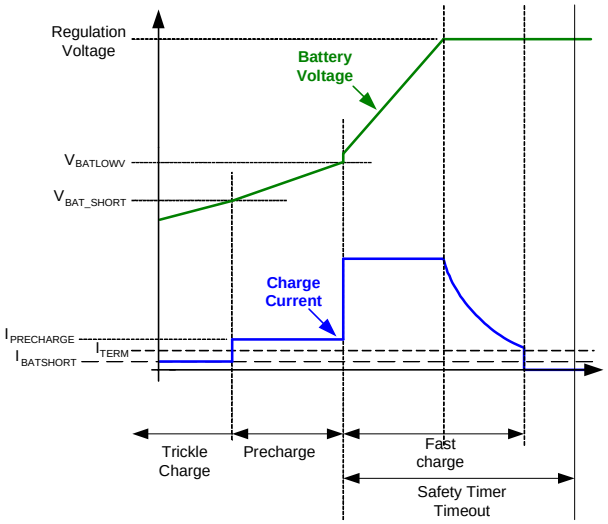


Figure 3. Battery Chaging Profile

Thermistor Qualification

The high capacity battery usually has two or more single cells in parallel. The APW7264 provides TS pins to monitor the thermistor (NTC) in each cell independently.

Function Description (Cont.)

Cold/Hot Temperature Window

By measuring the voltage between the TS pin and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider to continuously monitor battery temperature. The device compares this voltage against its internal thresholds to determine if charging is allowed. When the V_{TS} rises above the V_{LTF} threshold or falls below the V_{TCO} threshold, the charging is suspended until the battery temperature is back to the NTC Fault Hysteresis range, V_{LTF_HYS} and V_{HTF}.

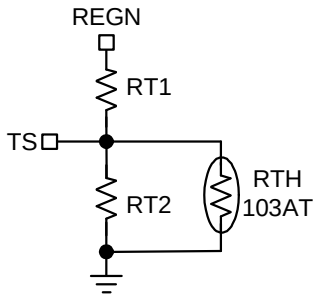


Figure 4. TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. When charging is suspended, the fault status will be indicated on STAT pin.

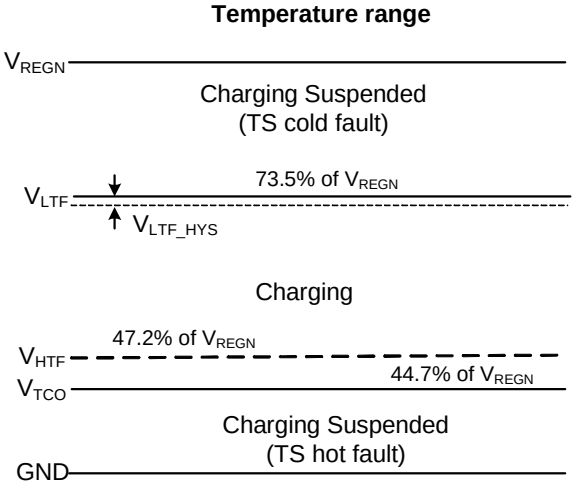


Figure5. TS pin thermistor sense thresholds in Charge Mode

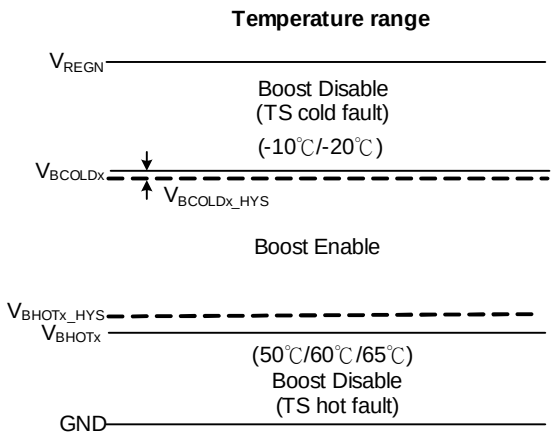


Figure6. TS pin thermistor sense thresholds in OTG Mode

For the charge mode case, assuming a 103AT NTC thermistor is used on the battery pack Figure 4, the value RT1 and RT2 can be determined by using the following equation:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1\right)}$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,

RTHCOLD = 27.28 kΩ

RTHHOT = 4.911 kΩ

RT1 = 5.52 kΩ

RT2 = 31.23 kΩ

Function Description (Cont.)

Charging Termination

The APW7264 terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below programmed termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to supply the system. When the device is into supplement mode, the device can turn on BATFET to supply the system. When termination occurs, the status register REG08[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in DPM or thermal regulation. Termination also can be disabled by writing 0 to REG05[7].

Termination when REG02[0] = 1

When REG02[0] is "1" to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through CEB pin or REG01[5:4].

Charging Safety Timer

The APW7264 has safety timer to prevent extended charging cycle due to abnormal battery conditions.
In default mode, the device keeps charging the battery with 8-hour fast charging safety timer (default value). At the end of the 8 hours, the EN_HIZ (REG00[7]) is set 1 to stops the buck converter operation and the system load is supplied by the battery. The EN_HIZ bit can be cleared to restart the buck converter.
In host mode, the device keeps charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the REG05[2:1] bits (default = 8 hours). At the end of safety timer, the EN_HIZ (REG00[7]) is cleared to signal the buck converter continues to operation to supply system load.
The safety timer is 1 hour when the battery is below BATLOWV threshold. The user can program fast charge safety timer through I^2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I^2C (REG05[3]).

The following actions restart the safety timer:

- At the beginning of a new charging cycle
- Toggle the CEB pin High to Low to High (charge enable)
- Write REG01[5:4]= 00 and to 01 (charge enable)
- Write REG05[3]= 0 and to 1 (safety timer enable)
- Write REG01[7] to 1 (software reset)

During input voltage/current regulation or thermal regulation, or when FORCE_20PCT (REG02[0]) bit is set with $V_{BAT} > V_{SYS\_MIN}$, the safety timer counts at half clock rate. For example, if the charger is in input voltage regulation (VINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

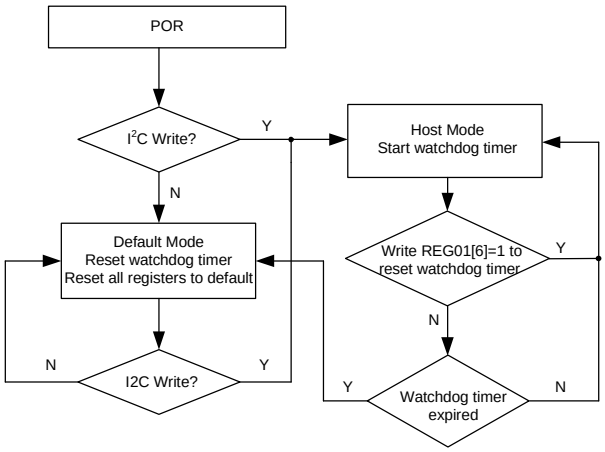
USB Timer when Charging from USB100mA Source

When the device is in default mode from USB100mA source, the charging time is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

Host Mode and Default Mode

The APW7264 can operate in default mode without host management. In default mode, APW7264 can be used as an autonomous charger without host or with host in sleep mode. When the charger is in default mode, REG09[7] is High. When the charger is in host mode, REG09[7] is Low.
After power-on-reset, the device starts in watchdog timer expiration state, or default mode. And all the registers are in the default settings.
All the device parameters can be programmed by the host. Writing any command to APW7264 transitions the device from default mode to host mode. The host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4]=11 to keep the device in host mode.

Function Description (Cont.)



Default/Host Mode Flow Chart

Status Outputs (PG, STAT, and INT)

Power Good Indicator (PG)

In APW7264 PGB goes Low to indicate a good input source when:

1. VBUS above UVLO
2. VBUS above battery (not in sleep mode)
3. VBUS below ACOV threshold

Charging Status Indicator (STAT)

The APW7264 indicates charging state on STAT pin. The STAT pin can drive LED as the application circuit shows.

Charging State	STAT
Charging in progress	Low
Charging complete	High
Sleep mode, charge disable	High
Charge suspend (input over-voltage, TS fault, timer fault, BAT over-voltage)	Blinking

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate INT pulse.

- USB/adapter source identified (through PSEL with OTG pin)
- Good input source detected
  - Not in sleep mode
  - Not in VBUS OV
- Input removed or VBUS OV
- Charge Complete
- FAULT event in REG09

When a fault occurs, the device sends out INT 256µs low pulse width and latches the first fault state in REG09 until the host reads the fault register. Before the host reads REG09, the charger device would not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. The host has to read REG09 two times consecutively to read the current fault status. The first reads fault register status from the last INT and the second reads the current fault register status.

Charge/Buck Mode Protections

Input Current Limit on ILIM

For safe operation, theAPW7264 has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

V_{ILIM}=20uA x R_{ILIM}

I_{ILIM}= V_{ILIM} x 2

For example, if R_{ILIM} = 50 kΩ, we can get V_{ILIM}=1V and then the I_{ILIM}=2A.

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and ILIM has a 50kΩ resistor to ground for 2A, the input current limit is 2A.

When I_{ILIM} pin is flaoting, the input current limit is programmed by the resigister 00[2:0]. When the V_{ILIM} voltage is below 250mV (typ), the device ignores the I_{ILIM} pin setting and the input current limit is programmed by the resigister 00[2:0] at the same time.

Function Description (Cont.)

Thermal Regulation and Thermal Shutdown

The APW7264 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the programmed thermal regulation threshold (REG06[1:0]), the device starts to decrease the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

The device also has thermal shutdown protection to turn off the converter. When the device triggers the thermal shutdown threshold, the fault register REG09[5:4] is 10 and an INT is asserted to the host.

Input Over-Voltage (ACOV)

If VBUS voltage exceeds 6.2V to trigger the input over-voltage threshold (ACOV), the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

System Over-Voltage Protection (SYSOVP)

The APW7264 always monitors the voltage at SYS terminal. When system over-voltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

Voltage and Current Monitoring in Boost Mode

The APW7264 closely monitors the VBUS voltage, as well as HSFET and LSFET current to ensure safe boost mode operation.

VBUS Over-Voltage Protection

The boost mode regulated output is 5V. During boost mode, the VBUS voltage will rise above regulation target when an adapter plugs in. Once the VBUS voltage exceeds 6V, the device stops switching and the device exits boost mode. The OTG Enable bit REG01[5] is cleared to 0 simultaneously. The fault register REG09[6] is set high to indicate fault in boost operation. An INT is asserted to the host.

VBUS Over-Current Protection

When the VBUS terminal load is bigger than the register BOOST_LIM setting value, the device will operate in hiccup mode for protection. While in hiccup mode cycle, the device turns off RBFET for $t_{OTG\_OCP\_OFF}$ (32ms typical) and turns on RBFET for $t_{OTG\_OCP\_ON}$ (2ms typical) to attempt to restart. If the over-current condition is removed, the RBFET is continuous turned on and the VBUS OTG output will operate normally. When over-current condition still exists, the device will repeat the hiccup cycle until over-current condition is removed. When over-current condition is detected, the fault register bit OTG_FAULT (REG09[6]) is set high to indicate fault in boost operation. An INT is asserted to the host.

Battery Protection

Battery Over-Current Protection (BATOVP)

When the battery voltage is at 4% above the battery regulation voltage, the APW7264 immediately disables charge opreration. The fault register REG09[3] goes high and an INT is asserted to the host.

Charging During Battery Short Protection

If the battery voltage falls below 2V, the charge current is reduced to 100mA for battery safety.

Application Information

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Below are Layout consideration checklist, recommended layout Schematic diagram and demoboard layout for your reference:

- Keep the switching nodes (BTST and SW) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The large layout plane between the drain of the MOSFETs (VBUS, PMID and SW nodes) can get better heat sinking.
- The high-current charge paths into VBUS, PMID and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- Place all decoupling capacitors close to their respective IC pins and close to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors.
- In order to better anti-interference ability, the middle layer of the board covered with GND is recommended.

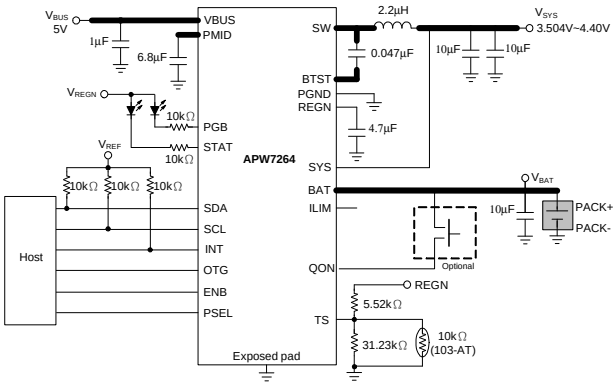


Figure 5. Layout Circuit Abridged General View

Minimum Footprint

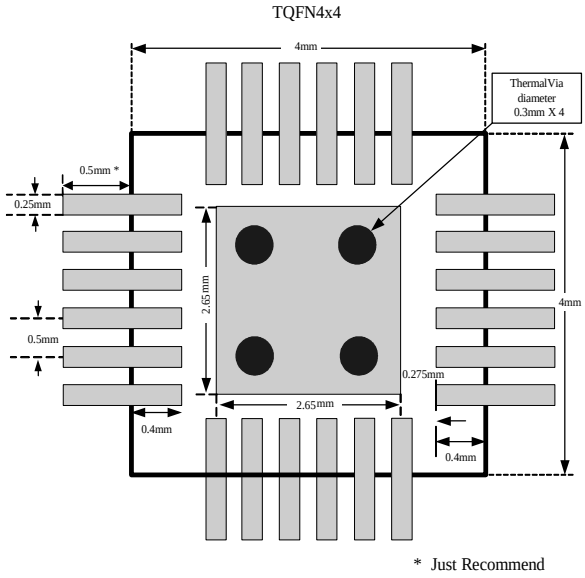
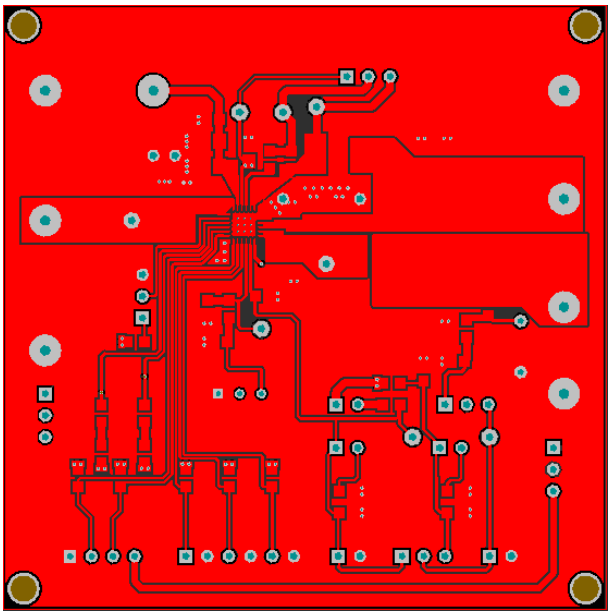


Figure 6. Recommended Minimum Footprint

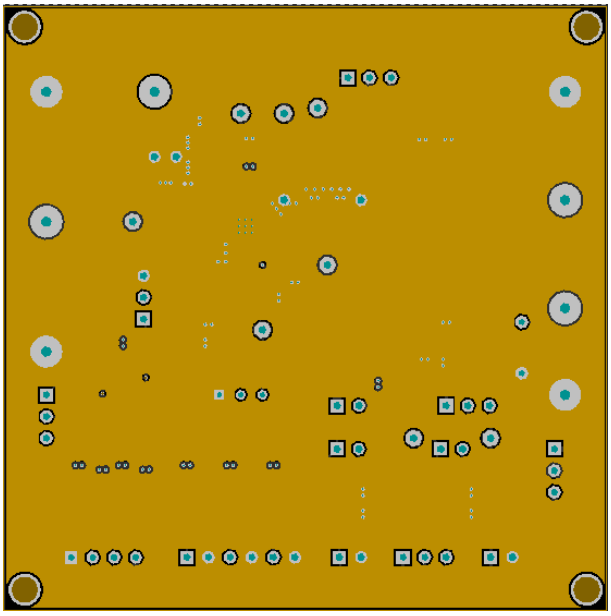
Application Information (Cont.)

Evalution Board

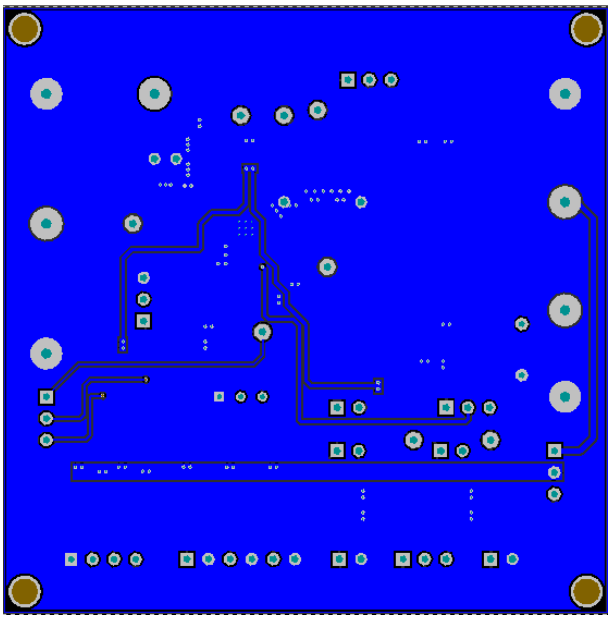
TOP LAYER



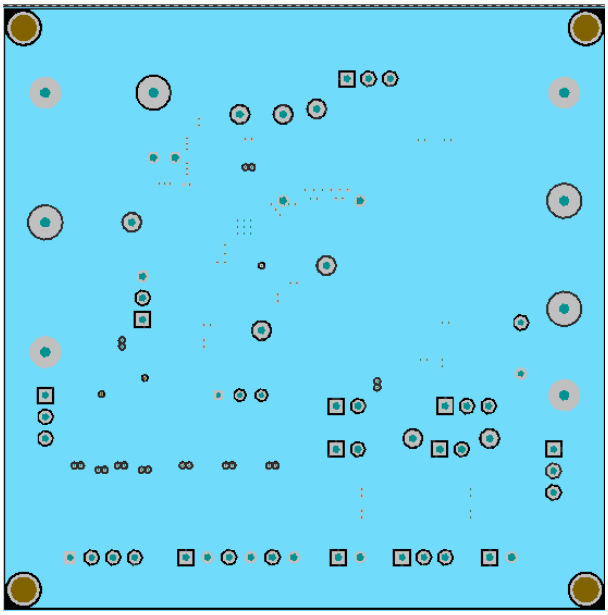
MIDLAYER1



BOTTOM LAYER



MIDLAYER2



I²C Programming

I²C SERIAL CONTROL INTERFACE

The APW7264 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz), fast mode (400-kHz) and the high-speed mode (up to 3.4Mbps in wire mode) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum), the fast I²C bus operation (400 kHz maximum) and the high-speed mode (up to 3.4Mbps in wire mode). The DAP performs all I²C operations without I2C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 7. The master generates the 7-bit slave address and the R/$\overline{W}$ bit - a “zero” indicates a transmission (WRITE), a “one” indicates a request for data (READ) to open communication with another device and then waits for an acknowledge condition. The APW7264 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

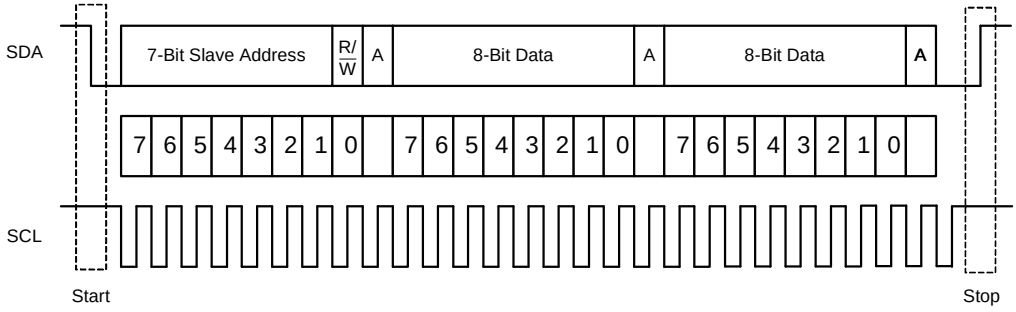


Figure 7. Typical I²C sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 7.

Pin A_SEL defines the I2C device address. The device 7-bit address is defined as "1101011" (6BH) for APW7264.

I²C Programming (Cont.)

Single-Byte Transfer

The serial control interface supports single-byte R/$\overline{W}$ operations for sub-addresses 0x00 to 0xFF.
Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7264 also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7264. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 8, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit determines the direction of the data transfer. For a write data transfer, the R/$\overline{W}$ bit will be a 0. After receiving the correct I²C device address and the R/$\overline{W}$ bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7264 internal memory address being accessed. After receiving the address byte, the APW7264 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7264 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

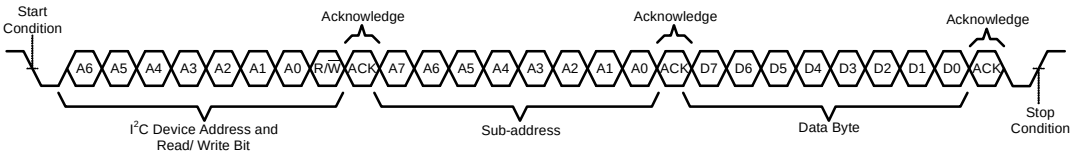


Figure 8. Single-Byte Write Transfer

I²C Programming (Cont.)

Single-Byte Read

As shown in Figure 9, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/$\overline{W}$ bit becomes a 0. After receiving the APW7264 address and the R/$\overline{W}$ bit, APW7264 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7264 address and the R/$\overline{W}$ bit again. This time the R/$\overline{W}$ bit becomes a 1, indicating a read transfer. After receiving the address and the R/W bit, the APW7264 again responds with an acknowledge bit. Next, the APW7264 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

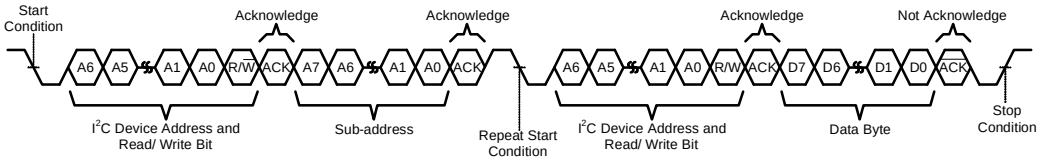


Figure 9. Single-Byte Read Transfer

Register Map

Register Address	Register Name	Read/Write/Read Only State	Default Value
00h	Input Source Control Registor	R/W	3xh
01h	Power-On Configuration Input Source Control Register	R/W	1Bh
02h	Charge Current Control Register	R/W	60h
03h	Pre-charge/Termination Current Control Register	R/W	11h
04h	Charge Volage Control Register	R/W	B2h
05h	Charge Termination/Timer Control Register	R/W	9Ch
06h	Thermal Regulation Control Register	R/W	73h
07h	Miscellanea Operation Control Register	R/W	4Bh
08h	System Status Register	R	-
09h	Fault Register	R	-
0Ah	Vender/Part/Revision And Charging Temperature Profile Selection Register	R/W	38h

I²C Programming (Cont.)

REG00 Input Source Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	EN_HIZ	VINDPM[3:0]				IINLIM[2:0]		
Read/Write	R/W	R/W				R/W		
Power On Default	0	0	1	1	0			

Bit Name	Bit Definition
EN_HIZ	High-Z mode Enable/Disable Control: **0: Disable**. 1: Enable.
VINDPM[3:0]	Input Voltage Limit Setting: 0000: 3.88V 0100: 4.20V 1000: 4.52V 1100: 4.84V 0001: 3.96V 0101: 4.28V 1001: 4.60V 1101: 4.92V 0010: 4.04V **0110: 4.36V** 1010: 4.68V 1110: 5.00V 0011: 4.12V 0111: 4.44V 1011: 4.76V 1111: 5.08V
IINLIM_MIN[2:0]	The IINLIM[2:0] value is power-on strapped by both the statuses of PSEL and OTG. Please note that the actual input current limit is the lower one between IINLIM[2:0] and ILIM pin setting. Default mode: IINLIM[2:0]=000 when PSEL=high, OTG=low IINLIM[2:0]=010 when PSEL=high, OTG=high IINLIM[2:0]=111 when PSEL=low, OTG=don't care Input Current Limit Setting: 000: 100mA 011: 900mA 110: 2A 001: 150mA 100: 1.2A 111: 3A 010: 500mA 101: 1.5A

I²C Programming (Cont.)

REG01 Power-On Configuration Input Source Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	REG_RST	WDT_RST	OTG_CONFIG	CHG_CONFIG	SYS_MIN[2:0]			BOOST_LIM
Read/Write	R/W	R/W	R/W	R/W	R/W			R/W
Power On Default	0	0	0	1	1	0	1	1

Bit Name	Bit Definition
REG_RST	Reset Register Value Control: **0: Keep current register setting** 1: Reset all registers' value to default.
WDT_RST	Watch Dog Timer Reset Control: **0: Normal** 1: Reset Watch Dog Timer Back to 0 after timer reset
OTG_CONFIG	OTG Configuration: **0: OTG disabled** 1: OTG enabled Note: OTG_CONFIG would over-ride Charge Enable Function in CHG_CONFIG
CHG_CONFIG	Charger Configuration: 0: Charger disabled **1: Charge battery**
VSYS_MIN[2:0]	Minimum System Voltage Limit: 000: 3.0V 010: 3.2V 100: 3.4V 110: 3.6V 001: 3.1V 011: 3.3V **101: 3.5V** 111: 3.7V
BOOST_LIM	Boost Mode Current Limit: 0: 1A **1: 1.5A**

I²C Programming (Cont.)

REG02 Charge Current Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	ICHG[5:0]						BCOLD	FORCE_20PCT
Read/Write	R/W						R/W	R/W
Power On Default	0	1	1	0	0	0	0	0

Bit Name	Bit Definition					
ICHG[5:0]	Charge current setting:					
	000000: 512mA	001010: 1152mA	010100: 1792mA	011110: 2432mA	100111: 3008mA	101000~111111 :ICHG higher than 3008mA is not supported
	000001: 576mA	001011: 1216mA	010101: 1856mA	011111: 2496mA		
	000010: 640mA	001100: 1280mA	010110: 1920mA	100000: 2560mA		
	000011: 704mA	001101: 1344mA	010111: 1984mA	100001: 2624mA		
	000100: 768mA	001110: 1408mA	**011000: 2048mA**	100010: 2688mA		
	000101: 832mA	001111: 1472mA	011001: 2112mA	100011: 2752mA		
	000110: 896mA	010000: 1536mA	011010: 2176mA	100100: 2816mA		
	000111: 960mA	010001: 1600mA	011011: 2240mA	100101: 2880mA		
	001000: 1024mA	010010: 1664mA	011100: 2304mA	100110: 2944mA		
BCOLD	Set Boost Mode temperature monitor threshold voltage to disable boost mode: **0 – Vbcold0 (Typ. 76% of REGN or -10°C w/ 103AT thermistor)** 1 – Vbcold1 (Typ. 79% of REGN or -20°C w/ 103AT thermistor)					
FORCE _20PCT	Shrink ICHG to 20% of I_{CHG} as REG03[5:0] programmed **0: I_{CHG} follows REG02[7:2] setting** 1: I_{CHG} is equal to 20% of REG02[7:2] setting					

I²C Programming (Cont.)

REG03 Pre-charge/Termination Current Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IPRECHG[3:0]				Reserved	ITERM[2:0]		
Read/Write	R/W				R/W	R/W		
Power On Default	0	0	0	1	0	0	0	1

Bit Name	Bit Definition
IPRECHG[3:0]	Pre-charge current limit setting 0000: 128mA 0100: 512mA 1000: 1152mA 1100: 1664mA **0001: 128mA** 0101: 768mA 1001: 1280mA 1101: 1792mA 0010: 256mA 0110: 896mA 1010: 1480mA 1110: 1920mA 0011: 384mA 0111: 1024mA 1011: 1536mA 1111: 2048mA
Reserved	No used.
ITERM[2:0]	Termination current limit: seting 000: 128mA 100: 640mA **001: 256mA** 101: 768mA 010: 384mA 110: 896mA 011: 512mA 111: 1024mA

I²C Programming (Cont.)

REG04 Charge Voltage Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VREG[5:0]						BATLOWV	VRECHG
Read/Write	R/W						R/W	RW
Power On Default	1	0	1	1	0	0	1	0

Bit Name	Bit Definition
VREG[5:0]	Charge voltage setting: 000000: 3.504V / 001010: 3.664V / 010100: 3.824V / 011110: 3.984V / 101000: 4.144V / 110010: 4.304V 000001: 3.520V / 3.680V / 010101: 3.840V / 011111: 4.000V / 101001: 4.160V / 110011: 4.320V 000010: 3.536V / 001100: 3.696V / 010110: 3.856V / 100000: 4.016V / 101010: 4.176V / 110100: 4.336V 000011: 3.552V / 001101: 3.712V / 010111: 3.872V / 100001: 4.032V / 101011: 4.192V / 110101: 4.352V 000100: 3.568V / 001110: 3.728V / 011000: 3.888V / 100010: 4.048V / **101100: 4.208V** / 110110: 4.368V 000101: 3.584V / 001111: 3.744V / 011001: 3.904V / 100011: 4.064V / 101101: 4.224V / 110111: 4.384V 000110: 3.600V / 010000: 3.760V / 011010: 3.920V / 100100: 4.080V / 101110: 4.240V / 111000: 4.400V 000111: 3.616V / 010001: 3.776V / 011011: 3.936V / 100101: 4.096V / 101111: 4.256V 001000: 3.632V / 010010: 3.792V / 011100: 3.952V / 100110: 4.112V / 110000: 4.272V 001001: 3.648V / 010011: 3.808V / 011101: 3.968V / 100111: 4.128V / 110001: 4.288V
BATLOWV	Battery pre-charge to fast charge threshold: 0: 2.8V **1: 3.0V**
VRECHG	Battery recharge threshold (below battery regulation voltage V_{REG}) **0: 100mV** 1: 300mV

I²C Programming (Cont.)

REG05 Charge Termination/Timer Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	EN_TERM	Reserved	WD_TIMER[1:0]		EN_TIMER	CHG_TIMER[1:0]		Reserved
Read/Write	R/W	R/W	R/W		R/W	R/W		RW
Power On Default	1	0	0	1	1	1	0	0

Bit Name	Bit Definition
EN_TERM	Charging termination enable control 0: Disable Charging Termination **1: Enable Charging Termination**
Reserved	Not used, Must Write "0"
WD_TIMER[1:0]	Watch dog timer setting 00: disable WD timer **01: 40 seconds** 10: 80 seconds 11: 160 seconds
EN_TIMER	Charging Safety Timer enable control 0: disable Charging Safety Timer **1: enable Charging Safety Timer**
CHG_TIMER[1:0]	Fast Charge Timer setting (see Charging Safety Timer for details) 00: 5 hours 01: 8 hours **10: 12 hours** 11: 20 hours
Reserved	Not used, Must Write "0"

REG06 Boost Voltage/Thermal Regulation Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	BOOSTV[3:0]				BHOT[1:0]		TREG[1:0]	
Read/Write	R/W				R/W		RW	
Power On Default	0	1	1	1	0	0	1	1

Bit Name	Bit Definition
BOOSTV[3:0]	OTG boost voltage setting: 0000: 4.55V / 0100: 4.806V / 1000: 5.062V / 1100: 5.318V 0001: 4.614V / 0101: 4.87V / 1001: 5.126V / 1101: 5.382V 0010: 4.678V / 0110: 4.934V / 1010: 5.19V / 1110: 5.446V 0011: 4.742V / **0111: 4.998V** / 1011: 5.254V / 1111: 5.51V
BHOT[1:0]	Set Boost Mode temperature monitor threshold voltage to disable boost mode voltage to disable boost mode: **00 – Vbhot1 (33% of REGN or 55°C w/ 103AT thermistor)** 01 – Vbhot0 (36% of REGN or 60°C w/ 103AT thermistor) 10 – Vbhot2 (30% of REGN or 65°C w/ 103AT thermistor) 11 – Disable boost mode thermal protection. Note: For BHOT[1:0]=11, boost mode operates without temperature monitor and the NTC_FAULT is generated based on Vbhot1 threshold.
TREG[1:0]	Thermal regulation threshold: 00: 60℃ 01: 80℃ 10: 100℃ **11: 120℃**

I²C Programming (Cont.)

REG07 Miscellanea Operation Control Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	TMR2X_EN	BATFET_EN	Reserved			INT_MASK[1:0]	
Read/Write	R/W	R/W, Write clear	R/W, Write clear	R/W			R/W	
Power On Default	0	1	0	0	1	0	1	1

Bit Name	Bit Definition
Reserved	Not used.
TMR2X_EN	0: The Safety Timer is not slowed by 2X during DPM or thermal regulation. **1: The Safety Timer is slowed by 2X during DPM or thermal regulation.**
BATFET_EN	BATFET Q4 turn on/off control **0: Allow Q4 turn on**. 1: Turn off Q4.
Reserved[4:2]	Not used.
INT_MASK[1:0]	Interupt Mask control: 00: No INT during CHRG_FAULT and BAT_FAULT. 01: INT only on BAT_FAULT. 10: INT only on CHRG_FAULT. **11: INT on BAT_FAULT and CHRG_FAULT.**

REG08 System Status Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VBUS_STAT[1:0]		CHRG_STAT[1:0]		DPM_STAT	PG_STAT	THERM_STAT	VSYS_STAT
Read/Write	R	R	R	R	R	R	R	R
Power On Default								

Bit Name	Bit Definition
VBUS_STAT[1:0]	VBUS status 00: Unknow (no input, or DPDM detection incomplete) 01:USB host 10: Adapter port 11: OTG
CHRG_STAT[1:0]	Charging status 00: not charging 01: Pre-charge 10: Fast charging 11: Charge termination done
DPM_STAT	DPM status: 0: not DPM 1: VINDPM or IINDPM
PG_STAT	Power good status: 0: Not power good 1: Power good
THERM_STAT	Thermal regulation status: 0: Normal 1: In thermal regulation
VSYS_STAT	VSYS status: 0: Not in VSYSMIN regulation (V_{BAT}>V_{SYSMIN}) 1: In VSYSMIN regulation (V_{BAT}<V_{SYSMIN})

I²C Programming (Cont.)

REG09 New Fault Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	WD_FAULT	BOOST_FAULT	CHRG_FAULT[1:0]		BAT_FAULT	Reserved	NTC_FAULT[2:0]	
Read/Write	R	R	R	R	R	R	R	R
Power On Default								

Bit Name	Bit Definition
WD_FAULT	Watchdog timer timeout report: 0: Normal 1: Watchdog timer expiration
BOOST_FAULT	Boost converter fault event report: 0: Normal 1: VBUS overloaded (OCP) or VBUS OVP in boost mode
CHRG_FAULT[1:0]	Charger fault event report: 00: Normal 01: Input fault (VBUS OVP or V_{BAT}<V_{VBUS}<3.8V) 10: Thermal shutdown 11: Charge safety timer expiration
BAT_FAULT	Battery fault event report: 0: Normal 1: Battery OVP (V_{BAT}>104%*V_{BAT_REG})
Reserved	No used
NTC_FAULT[1]	0-Normal 1–Cold Note: Cold temperature threshold is different based on device operates in buck or boost mode
NTC_FAULT[0]	0-Normal 1–Hot Note: Hot temperature threshold is different based on device operates in buck or boost mode

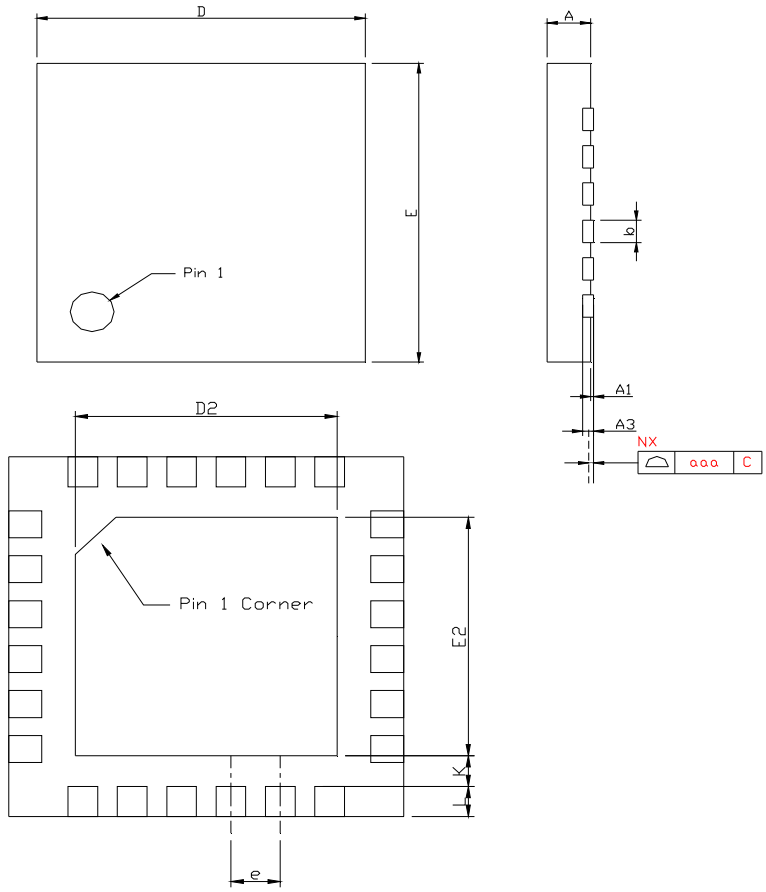
REG0A Vender/Part/Revision And Charging Temperature Profile Selection Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PN[7:5]			Reserved[4:3]		Revision_ID[2:0]		
Read/Write	R					R	R	R
Power On Default	0	0	1	1	1	0	0	0

Bit Name	Bit Definition
PN[7:5]	Device part number
Reserved[4:3]	No used
Revision_ID[2:0]	Device revision ID

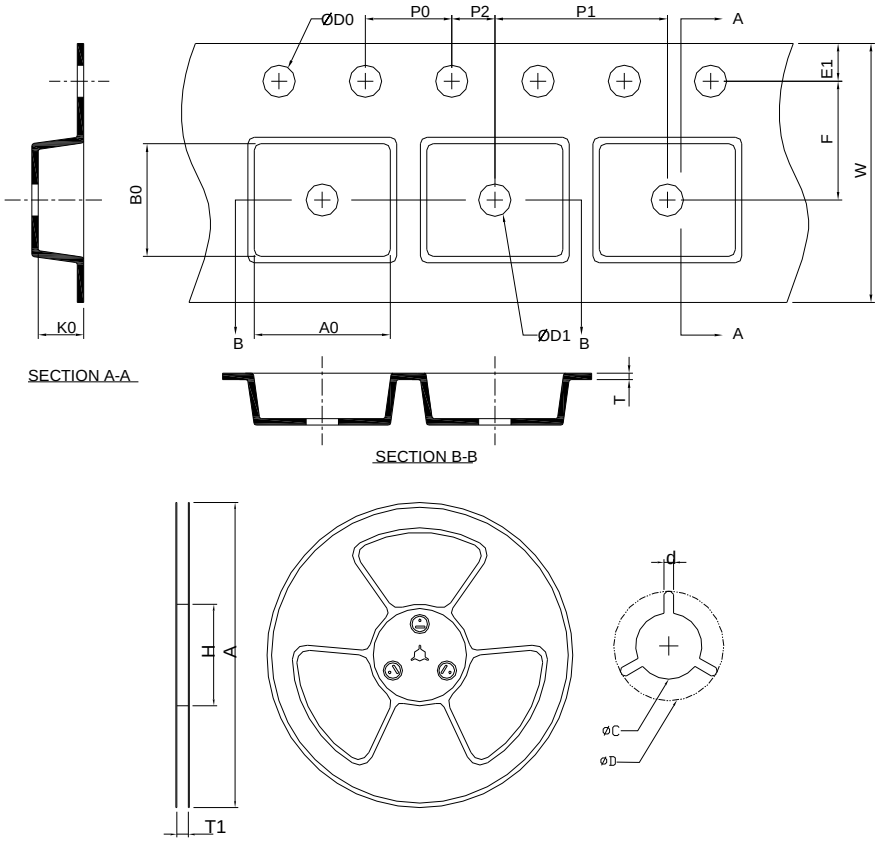
Package Information

TQFN4x4



SYMBOL	TQFN4x4			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.60	2.80	0.102	0.110
E	3.90	4.10	0.154	0.161
E2	2.60	2.80	0.102	0.110
e	0.50 BSC		0.020 BSC	
L	0.25	0.35	0.010	0.014
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

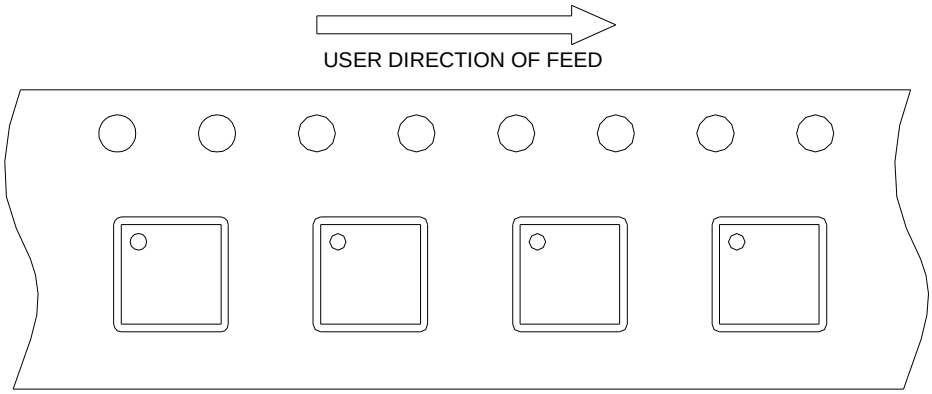
(mm)

Devices Per Unit

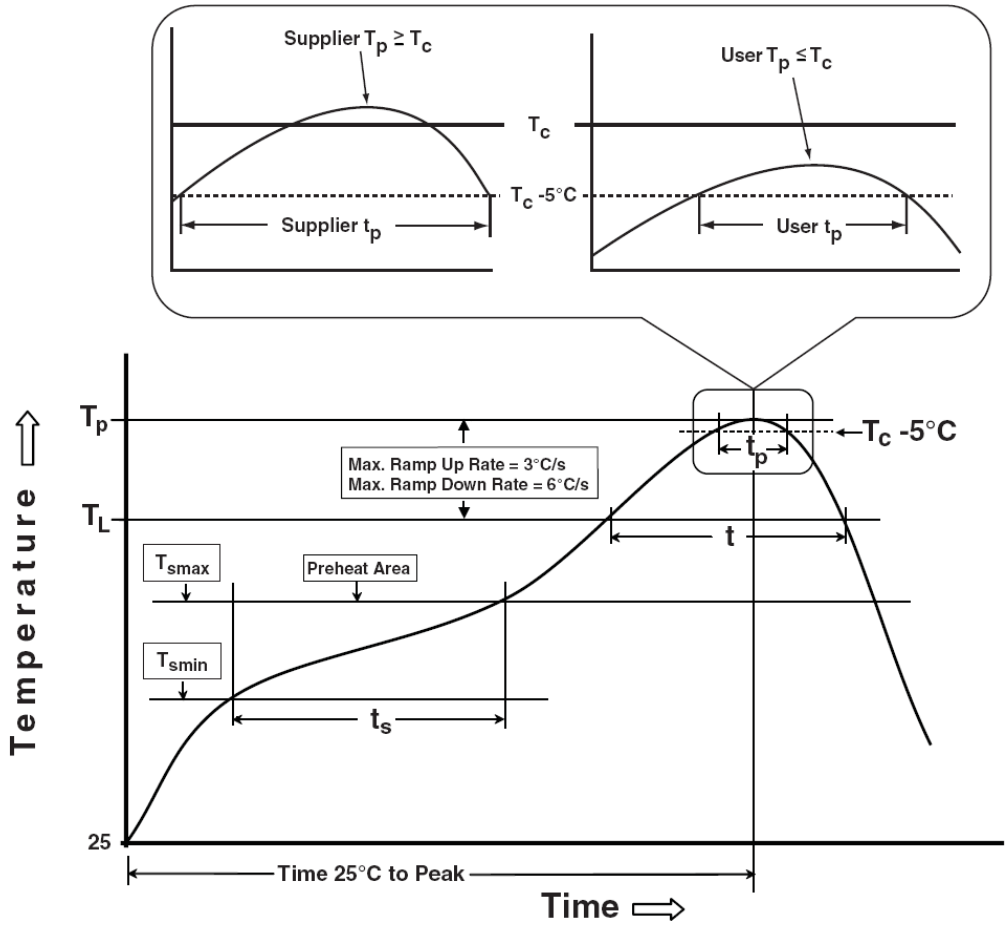
Package Type	Unit	Quantity
TQFN4x4	Tape & Reel	3000

Taping Direction Information

TQFN4x4



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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