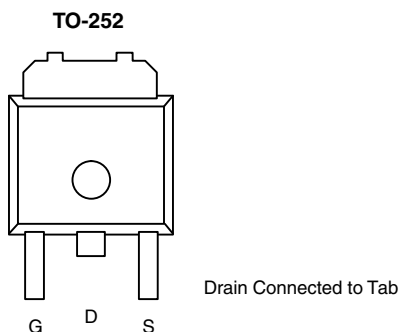


N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
60	0.073 at V _{GS} = 10 V	18.2	19.8
	0.085 at V _{GS} = 4.5 V	13.2	



FEATURES

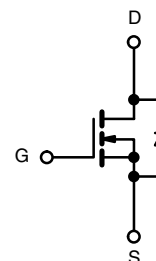
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC Converters
- DC/AC Inverters
- Motor Drives



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current	I _D	T _C = 25 °C	16.9	A
		T _C = 70 °C	13.6	
Pulsed Drain Current (t = 300 μs)	I _{DM}	25		
Avalanche Current	I _{AS}	15		
Single Avalanche Energy ^a	E _{AS}	L = 0.1 mH	11.25	mJ
Maximum Power Dissipation ^a	P _D	T _C = 25 °C	41.7 ^b	W
		T _A = 25 °C ^c	2.1	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	60	°C/W
Junction-to-Case (Drain)	R _{thJC}	3	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Base on T_C = 25 °C.

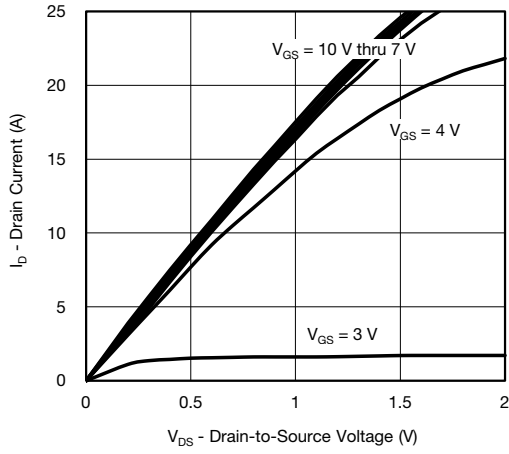
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 6.6 A		0.073		Ω
		V _{GS} = 4.5 V, I _D = 6 A		0.083		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 6.6 A		25		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		860		pF
Output Capacitance	C _{oss}			85		
Reverse Transfer Capacitance	C _{rss}			40		
Total Gate Charge ^c	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 6.6 A		19.8	30	nC
Gate-Source Charge ^c	Q _{gs}			3.6		
Gate-Drain Charge ^c	Q _{gd}			4.1		
Gate Resistance	R _g	f = 1 MHz	0.4	2	4	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 9.6 Ω I _D ≅ 5.2 A, V _{GEN} = 10 V, R _g = 1 Ω		8	16	ns
Rise Time ^c	t _r			11	20	
Turn-Off Delay Time ^c	t _{d(off)}			18	27	
Fall Time ^c	t _f			5	10	
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 9.6 Ω I _D ≅ 5.2 A, V _{GEN} = 4.5 V, R _g = 1 Ω		38	57	
Rise Time ^c	t _r			58	87	
Turn-Off Delay Time ^c	t _{d(off)}			18	27	
Fall Time ^c	t _f			8	16	
Drain-Source Body Diode Ratings and Characteristics^b T_C = 25 °C						
Continuous Current	I _S				16.9	A
Pulsed Current	I _{SM}				25	
Forward Voltage ^a	V _{SD}	I _F = 5.2 A, V _{GS} = 0 V		0.8	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 5.2 A, di/dt = 100 A/μs		34	51	ns
Peak Reverse Recovery Current	I _{RM(REC)}			3	5	A
Reverse Recovery Charge	Q _{rr}				50	75

Notes:

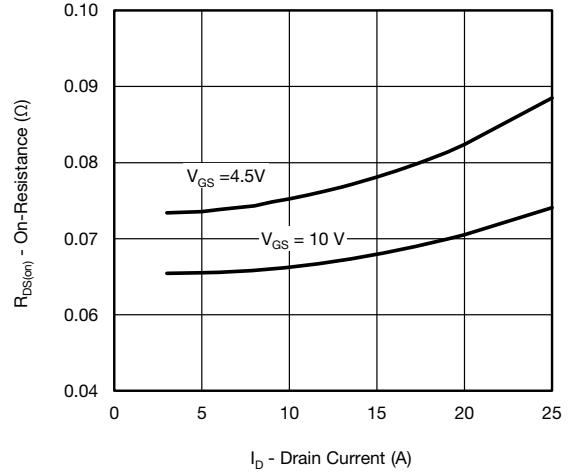
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

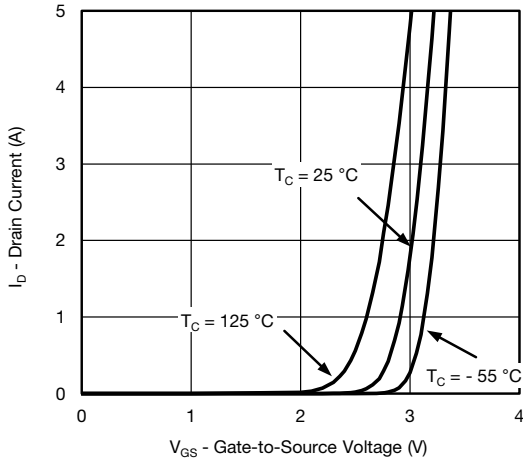
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



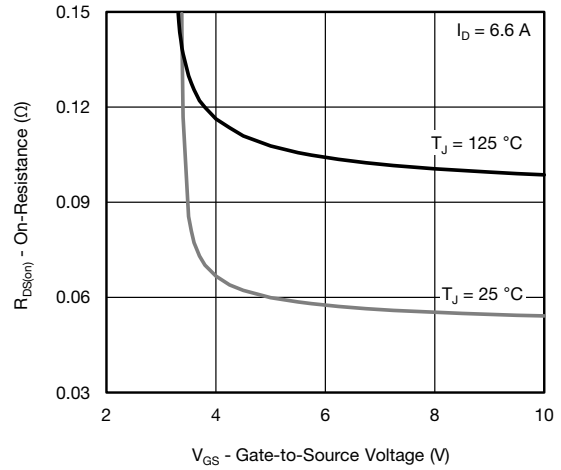
Output Characteristics



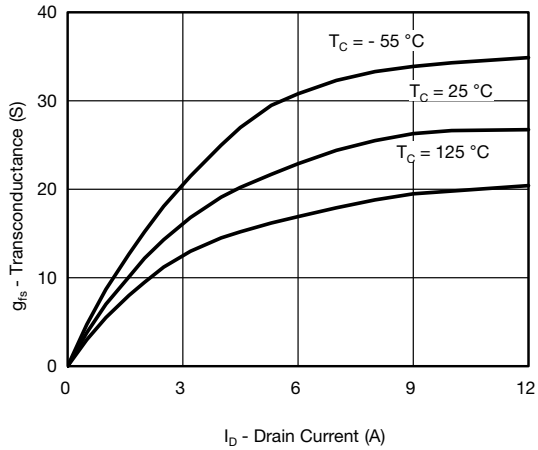
On-Resistance vs. Drain Current



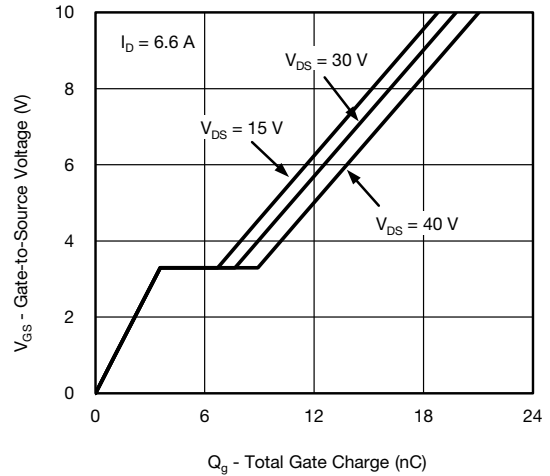
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

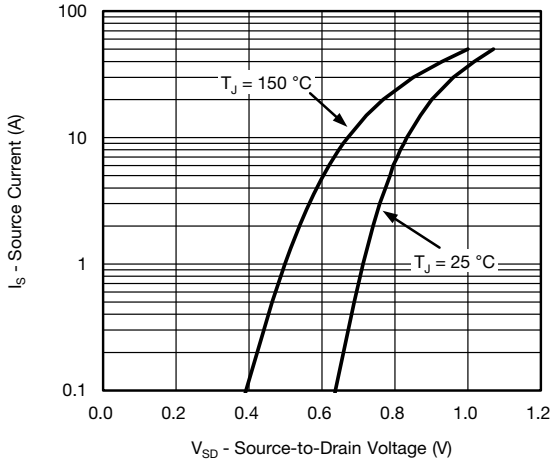


Transconductance

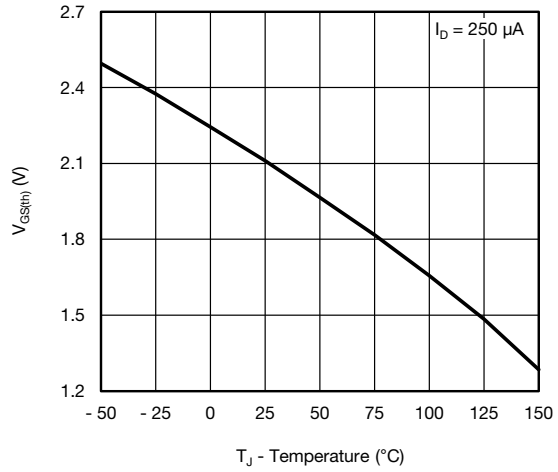


Gate Charge

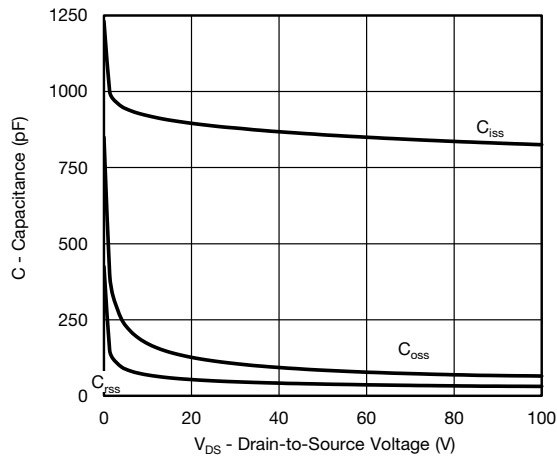
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



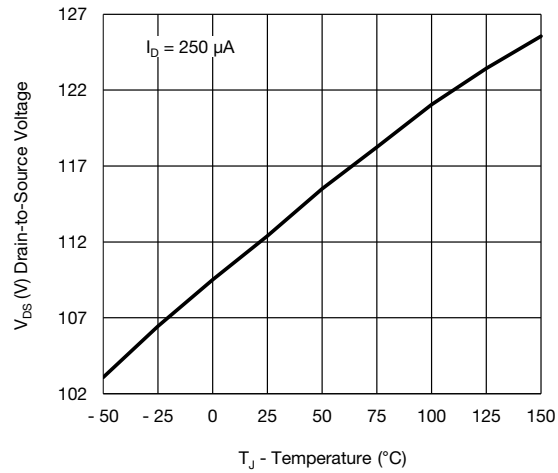
Source-Drain Diode Forward Voltage



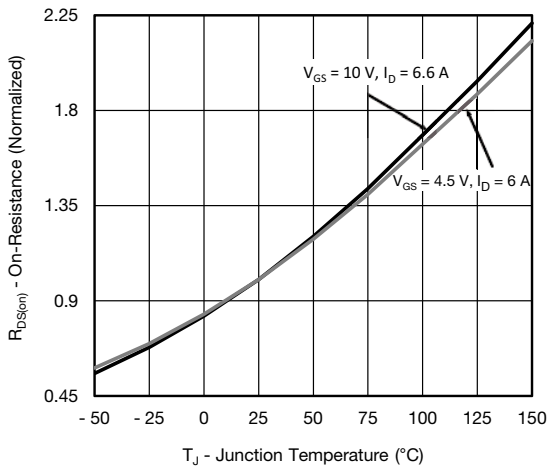
Threshold Voltage



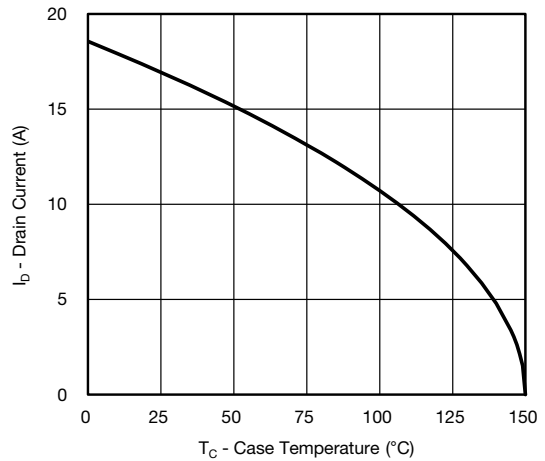
Capacitance



Drain Source Breakdown vs. Junction Temperature

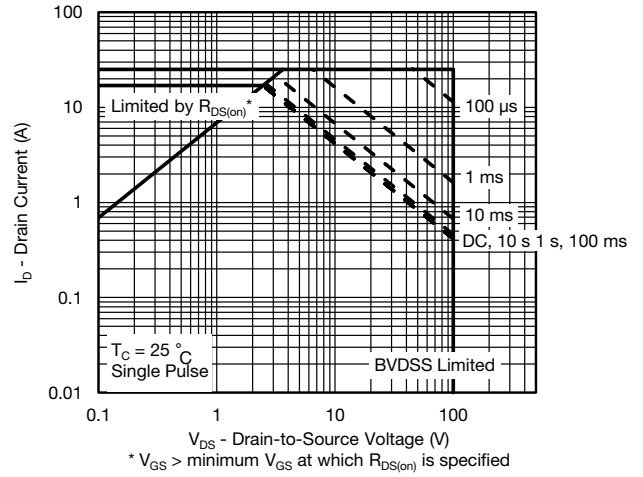
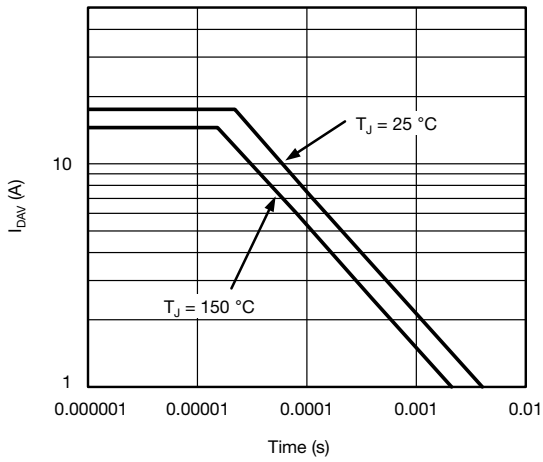


On-Resistance vs. Junction Temperature



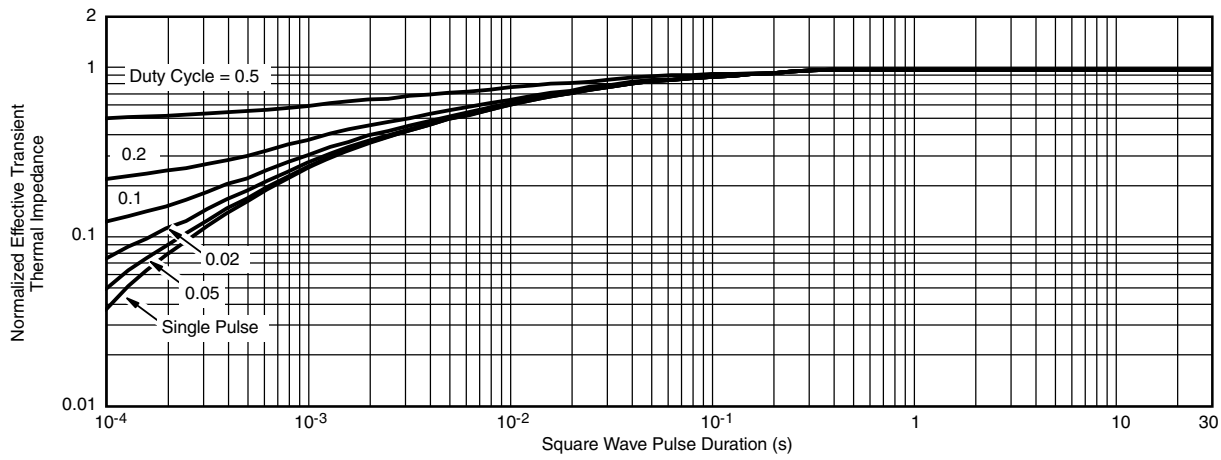
Current Derating

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



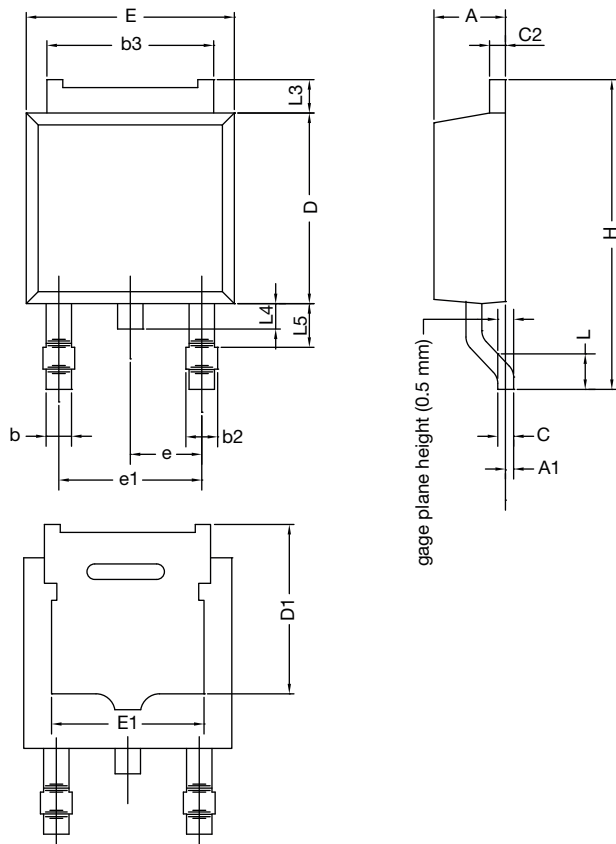
Single Pulse Avalanche Current Capability vs. Time

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-252AA Case Outline

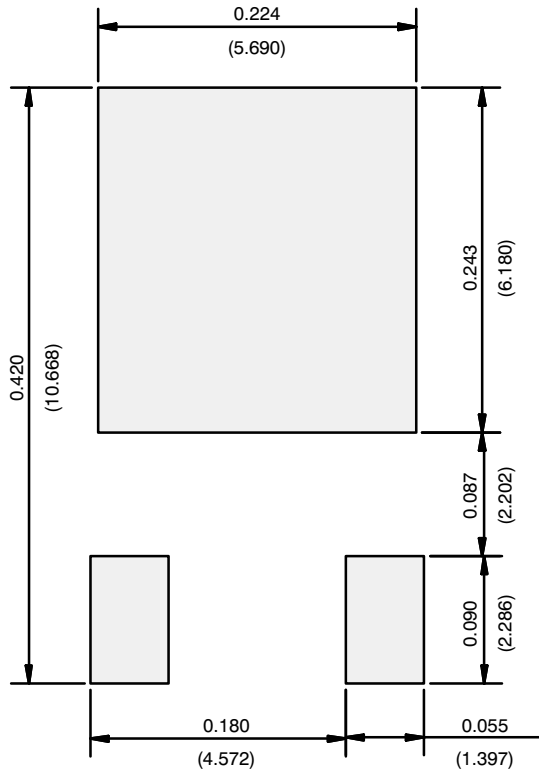


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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