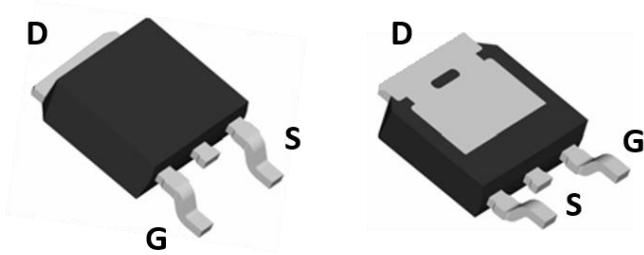
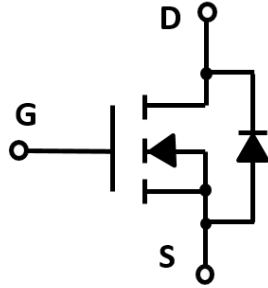


## N-Channel Enhancement Mode Field Effect Transistor



**TO-252**



### Product Summary

- $V_{DS}$  20V
- $I_D$  30A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <8.0 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) <9.0 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=1.8V$ ) <14 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	20	V
Gate-source Voltage		$V_{GS}$	$\pm 10$	V
Drain Current	$T_C=25^\circ\text{C}$	$I_D$	30	A
	$T_C=100^\circ\text{C}$		21	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	125	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	30	W
	$T_C=100^\circ\text{C}$		15	W
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	100	mJ
Thermal Resistance Junction-to-Case <sup>C</sup>		$R_{\theta JC}$	5	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+175	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD30N02A	F2	YJD30N02A	2500	2500	25000	13" reel



# YJD30N02A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A		5.6	8.0	mΩ
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> =7A		7.1	9.0	
		V <sub>GS</sub> = 1.8V, I <sub>D</sub> =3A		10	14	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =15A, V <sub>GS</sub> =0V		0.9	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				30	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHZ		1700		pF
Output Capacitance	C <sub>oss</sub>			305		
Reverse Transfer Capacitance	C <sub>rss</sub>			145		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =10V, I <sub>D</sub> =15A		29		nC
Gate-Source Charge	Q <sub>gs</sub>			6		
Gate-Drain Charge	Q <sub>gd</sub>			7		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>r</sub> =15A, di/dt=100A/us		23		
Reverse Recovery Time	t <sub>rr</sub>			39		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =4.5V, V <sub>DD</sub> =10V, I <sub>D</sub> =10A, R <sub>L</sub> =1Ω R <sub>GEN</sub> =3Ω		7		ns
Turn-on Rise Time	t <sub>r</sub>			35		
Turn-off Delay Time	t <sub>D(off)</sub>			30		
Turn-off fall Time	t <sub>f</sub>			6		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=20V, V<sub>G</sub>=10V, L=0.5mH, R<sub>g</sub>=25 Ω

C. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

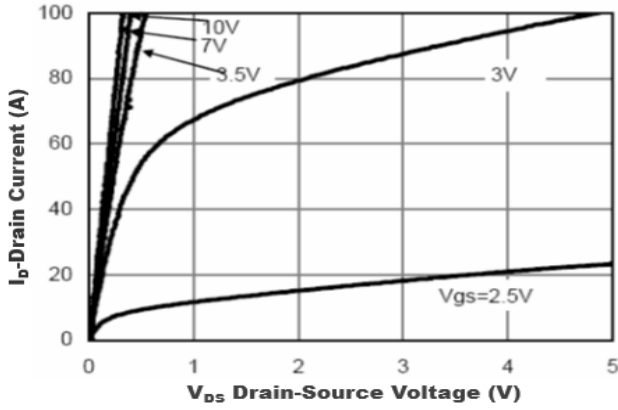


Figure1. Output Characteristics

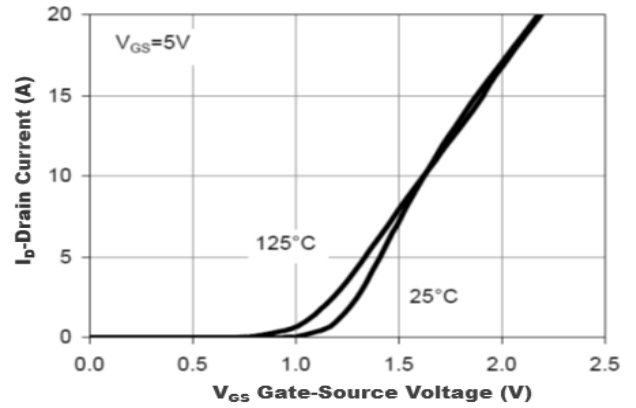


Figure2. Transfer Characteristics

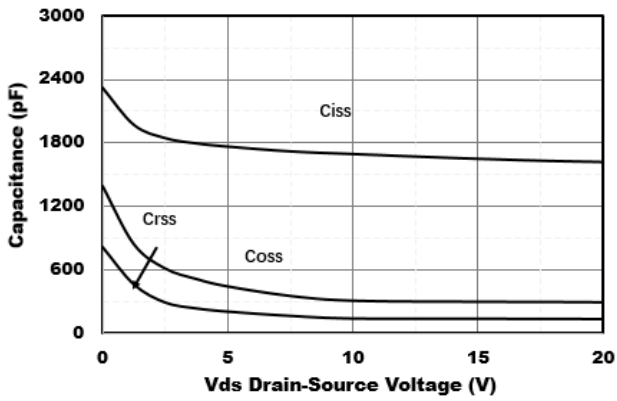


Figure3. Capacitance Characteristics

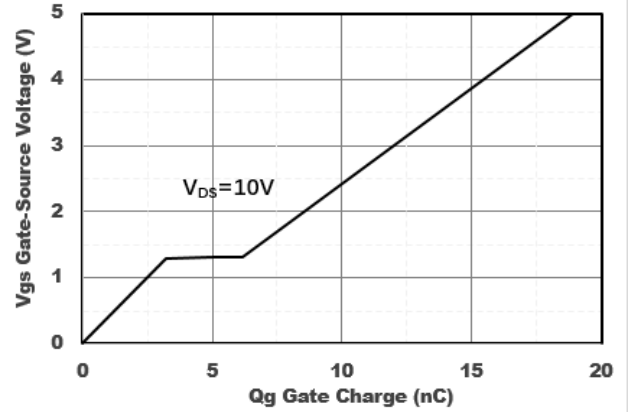


Figure4. Gate Charge

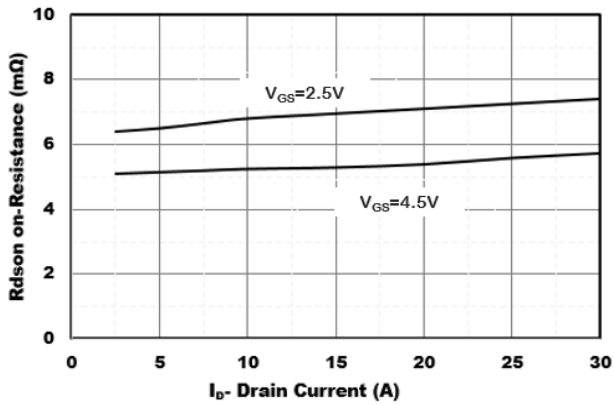


Figure5. Drain-Source on Resistance

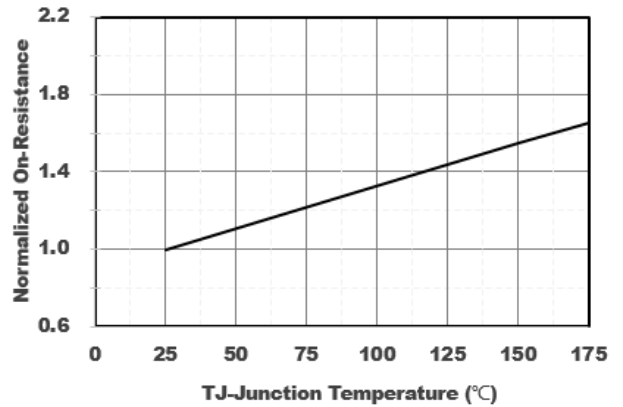


Figure6. Drain-Source on Resistance



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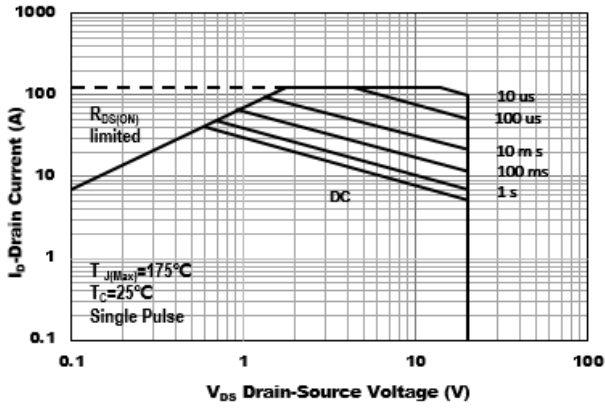


Figure7. Safe Operation Area

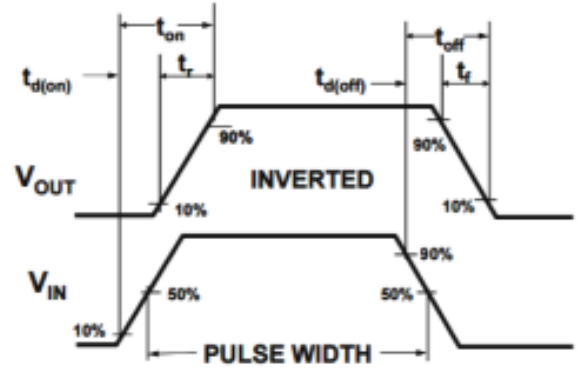
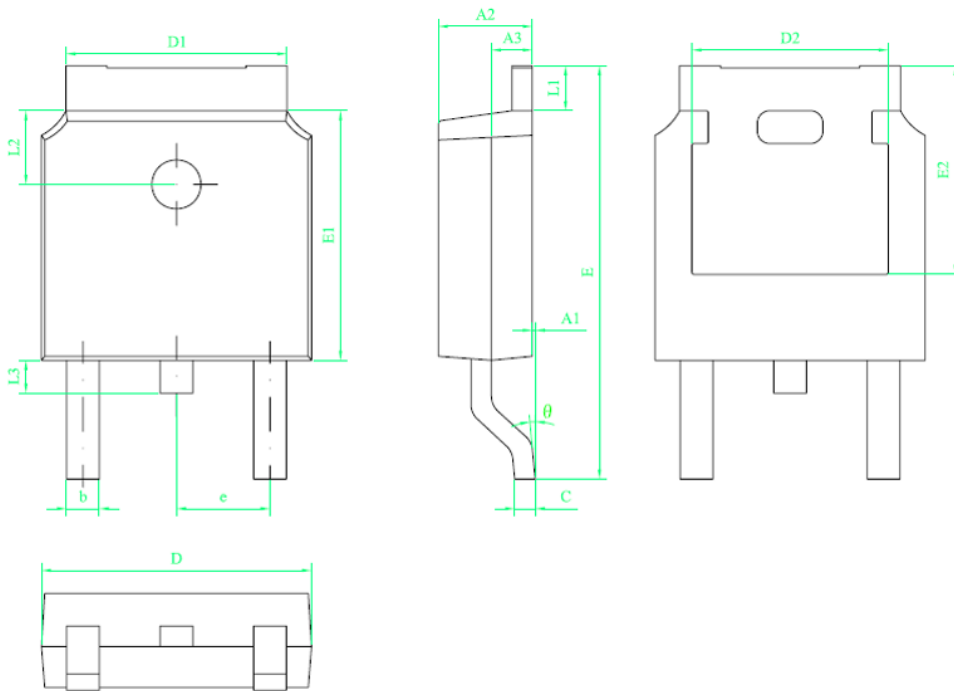


Figure8. Switching wave



# YJD30N02A

## ■ TO-252 Package information



符号	尺寸		
	min	nom	max
A1	0	---	0.10
A2	2.20	2.30	2.40
A3	0.90	1.00	1.10
b	0.75	---	0.85
c	0.50	---	0.60
D	6.50	6.60	6.70
D1	5.30	5.40	5.50
D2	4.70	4.80	4.90
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.20	5.30	5.40
e	2.20	2.286	2.40
L1	0.90	---	1.25
L2	1.70	1.80	1.90
L3	0.60	0.80	1.00
θ	0°	---	8°

### 技术要求:

1. 树脂体不应有崩裂、缺损等缺陷;
2. 树脂上下部X、Y方向偏差不得超过0.20;
3. 胶体两端留胶总和宽度不超过0.50;
4. 所有单位为mm;



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