# N-Channel 500V (D-S) Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 500 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.80 |
| $Q_g$ (Max.) (nC) | 81 | |
| $Q_{gs}$ (nC) | 20 | |
| $Q_{gd}$ (nC) | 36 | |
| Configuration | Single | |

## FEATURES

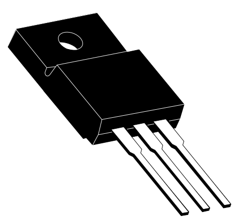
- Lower Gate Charge $Q_g$ Results in Simpler Drive Reqirements
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* Available

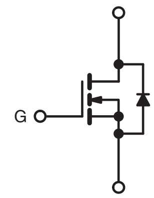
## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supplies
- High Speed Power Switching

TO-220 FULLPAK




Top View




N-Channel MOSFET

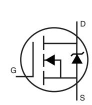
| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | | $V_{DS}$ | 500 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 13 | A |
| | | $T_C$ = 100 °C | | 8.1 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 50 | |
| Linear Derating Factor | | | | 2.0 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 560 | mJ |
| Avalanche Current[a] | | | $I_{AR}$ | 13 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 25 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 250 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 9.2 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |
| Mounting Torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J$ = 25 °C, L = 5.7 mH, $R_g$ = 25 Ω, $I_{AS}$ =14 A, dV/dt = 7.6 V/ns (see fig. 12a).
c. $I_{SD} \le$ 14 A, dI/dt $\le$ 250 A/μs, $V_{DD} \le V_{DS}$, $T_J \le$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | °C/W |
| Case-to-Sink, Flat, Greasd Surface | $R_{thCS}$ | 0.50 | - | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.50 | |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 500 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.55 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | - | - | 25 | µA |
| | | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 8.4 A[b] | - | - | 0.80 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 8.4 A | 8.1 | - | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | - | 1910 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 290 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 11 | - | |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 1.0 V, f = 1.0 MHz | - | 2730 | - | |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 400 V, f = 1.0 MHz | - | 82 | - | |
| Effective Output Capacitance | $C_{oss}$ eff. | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 400 V[c] | - | 160 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V, $I_D$ = 14 A, $V_{DS}$ = 400 V, see fig. 6 and 13[b] | - | - | 81 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | - | 20 | |
| Gate-Drain Charge | $Q_{gd}$ | | - | - | 36 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 250 V, $I_D$ = 14 A, $R_g$ = 7.5 Ω, see fig. 10[b] | - | 15 | - | ns |
| Rise Time | $t_r$ | | - | 39 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 39 | - | |
| Fall Time | $t_f$ | | - | 31 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 13 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | - | - | 56 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 14 A, $V_{GS}$ = 0 V[b] | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 14 A, $T_J$ = 125 °C, dI/dt = 100 A/µs[b] | - | 370 | 550 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 4.4 | 6.5 | µC |
| Body Diode Reverse Recovery Current | $I_{RRM}$ | | - | 21 | 31 | A |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DS}$.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

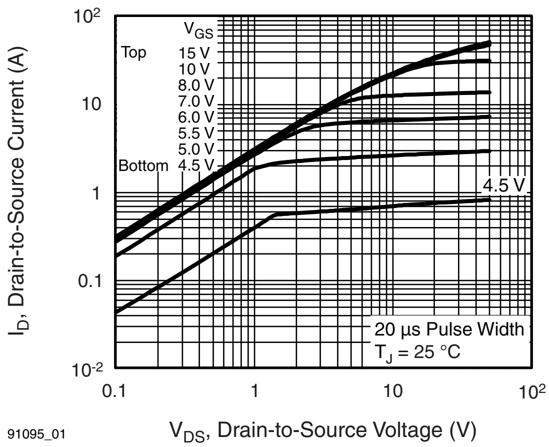



**Fig. 1 - Typical Output Characteristics**

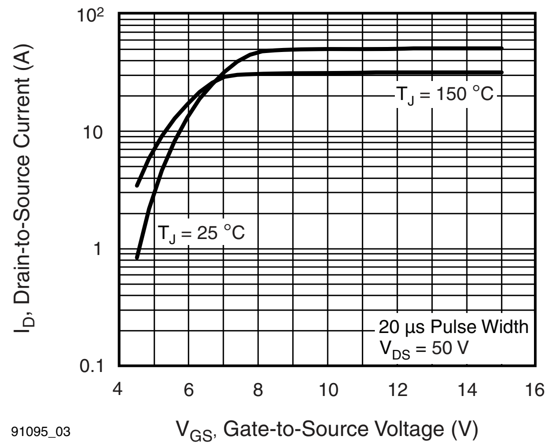



**Fig. 3 - Typical Transfer Characteristics**

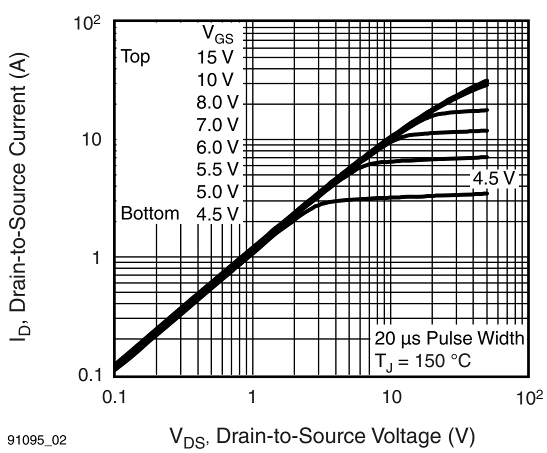



**Fig. 2 - Typical Output Characteristics**

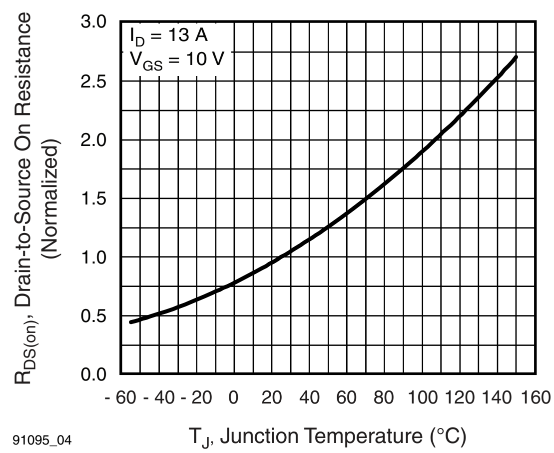



**Fig. 4 - Normalized On-Resistance vs. Temperature**

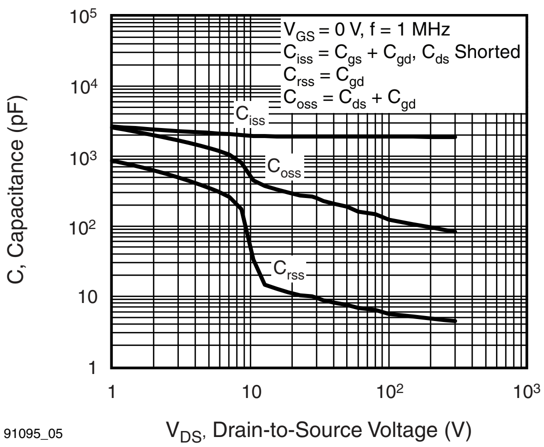



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

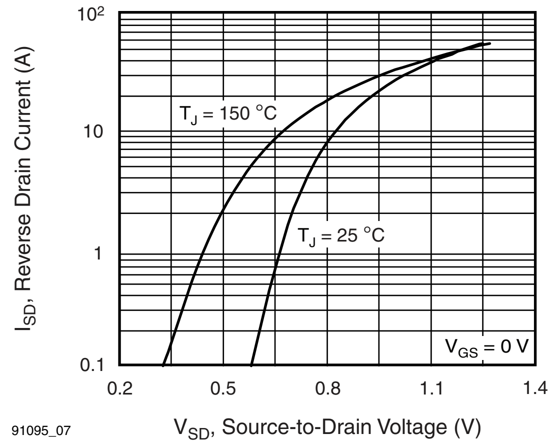



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

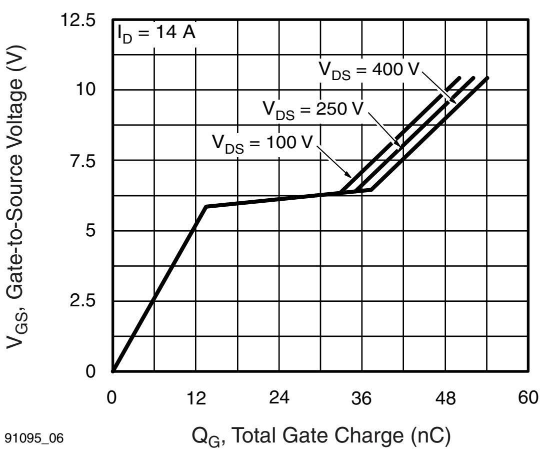



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

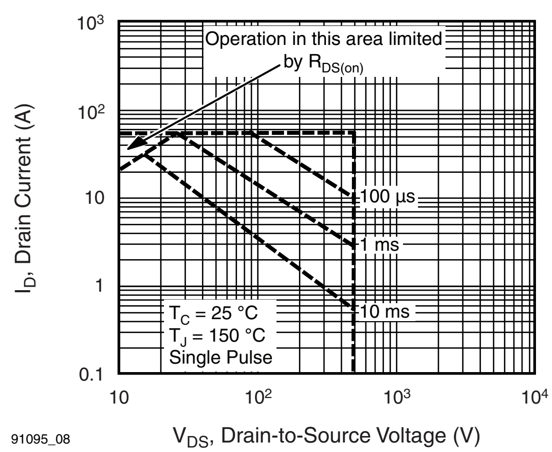



**Fig. 8 - Maximum Safe Operating Area**

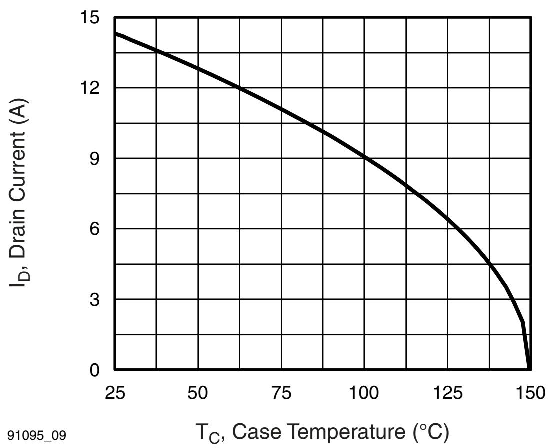



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

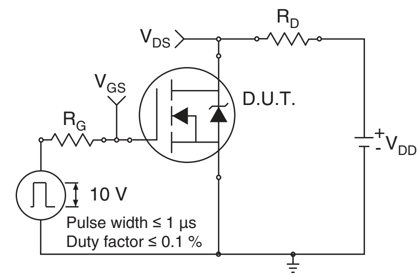



**Fig. 10a - Switching Time Test Circuit**

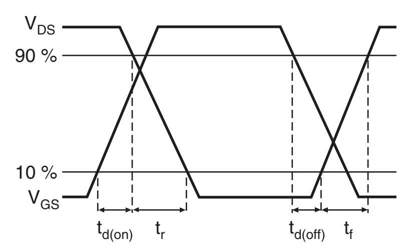



**Fig. 10b - Switching Time Waveforms**

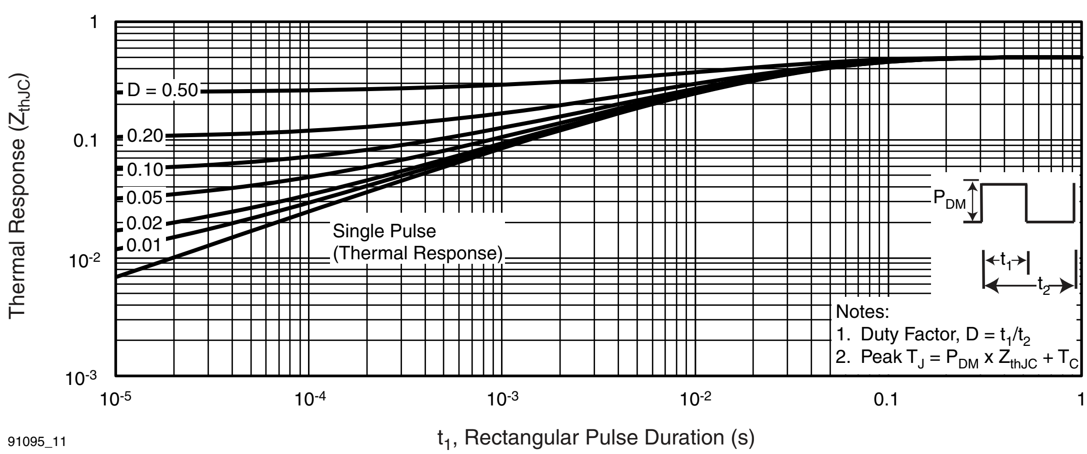



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

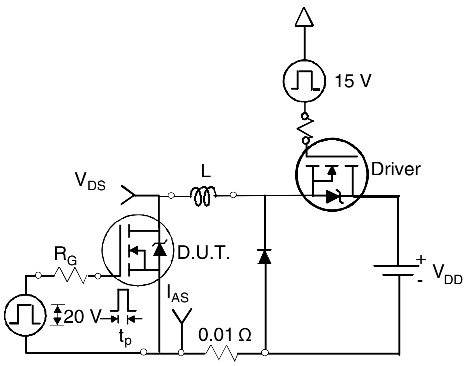



**Fig. 12a - Unclamped Inductive Test Circuit**

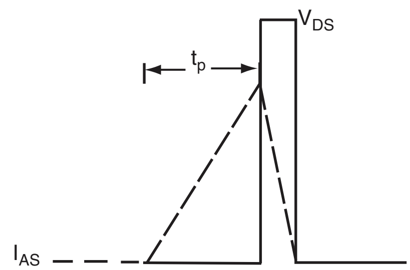



**Fig. 12b - Unclamped Inductive Waveforms**

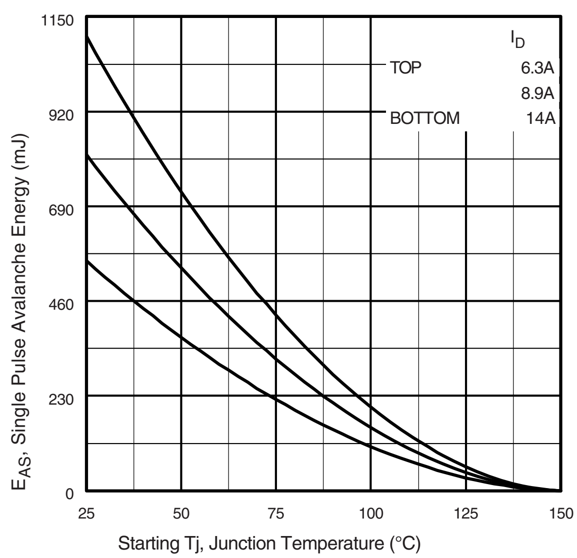



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

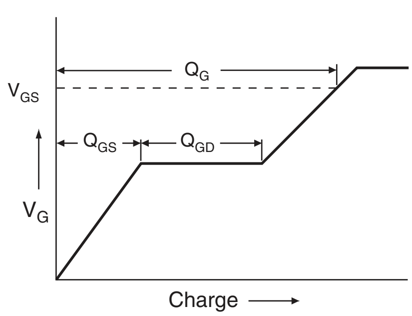



**Fig. 13a - Basic Gate Charge Waveform**

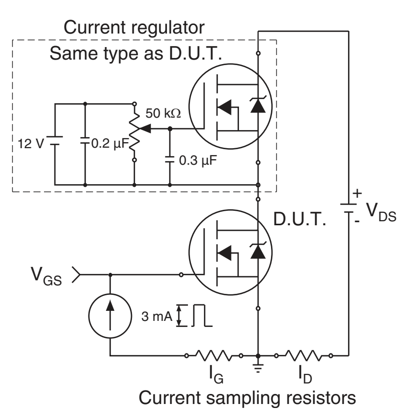
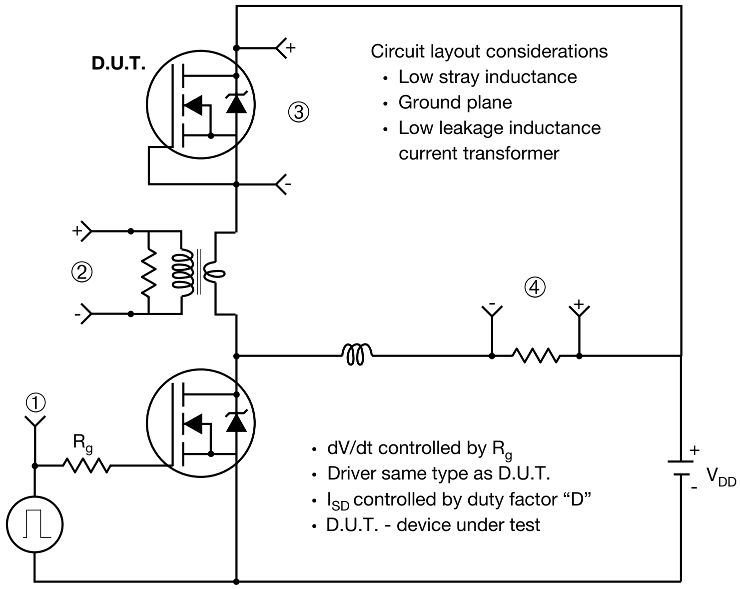
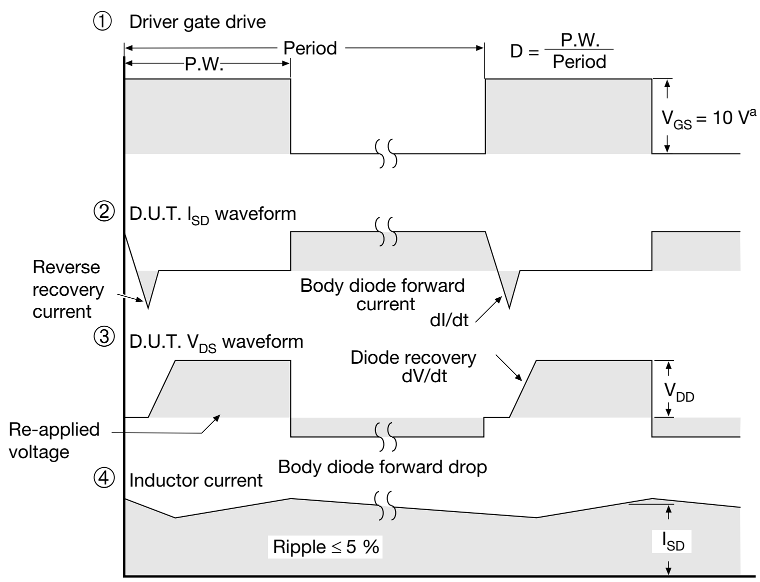



**Fig. 13b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**



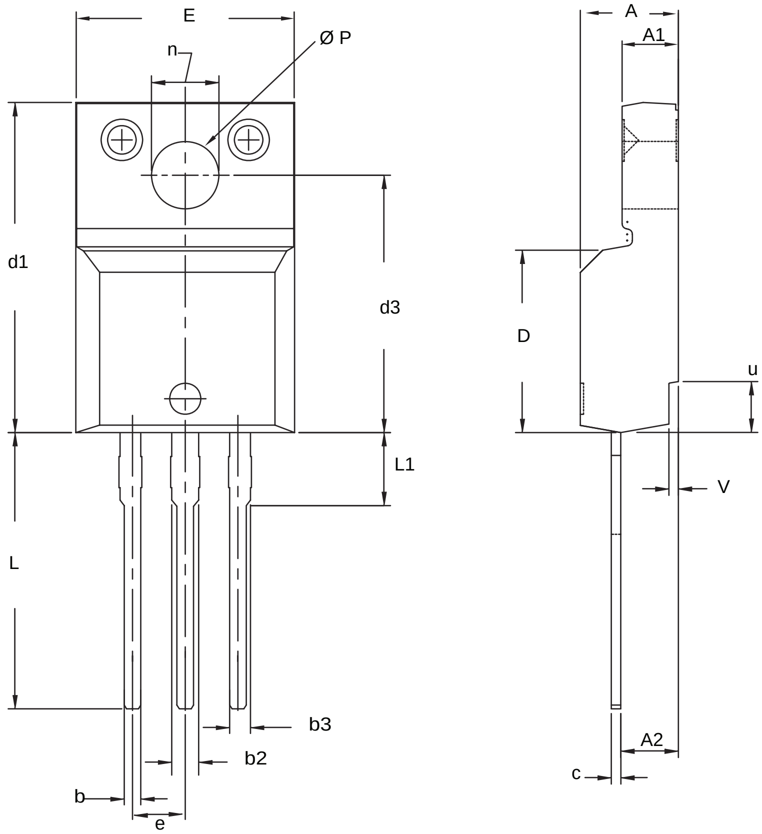




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

**TO-220 FULLPAK (HIGH VOLTAGE)**




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| v | 0.400 | 0.500 | 0.016 | 0.020 |
| ECN: X09-0126-Rev. B, 26-Oct-09<br>DWG: 5972 | | | | |

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk}$ > 1.33.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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