# 56-Output Serial-to-Parallel LED Driver / 52 GPIO Control Unit

## Features

- Supports serial-to-parallel dual LED driver and GPIO controller
- Serial-to-parallel LED Driver
  - Support one serial input with 56 parallel LEDs or triple serial input with 16 parallel LEDs for each serial input.
  - Support 4~16mA adjustable current source driving without current-limiting resistor
  - Support LED off mode for power saving function
  - Provides cascade ability to provide more LED driver outputs.
  - Support 1.8V to 3.3V logic level at the serial input stage
  - Single 3.3V supply voltage for core and LED driver
- General Purpose Input Output (GPIO)
  - Can be accessed by 2 wire serial interface
  - Provide 52 General Purpose inputs or outputs
  - Provide adjustable Input stable interval for input de-bouncing function
  - Provides up to 4 device ID
  - Provides interrupt for input change
  - Provides interrupt mask for each input
  - System clock input up to 25MHz
- 0.35 um process
- 68 pin QFN with E-pad 8x8mm package
- Single 3.3V power source

## General Description

The IP403 is a dual-functional controller chip, the serial-to-parallel LED driver and GPIO controller. The serial-to-parallel LED driver can replace up to 7 74LV164 glue logic chips.

The GPIO controller is similar to the commonly used 8255 I/O controller. Furthermore IP403 provides the programmable input stable timer, allowing the designer to set the input de-bounce time. IP403 also provides the flexibility for the designer to program the interrupt source of individual input change.

When set to LED driver mode, IP403 can directly drive 56 LEDs or 48 LEDs, depending on either single serial input or triple serial input. If set to single serial input mode, all LED driver pins are linked internally with the internal shift registers. If set to triple serial input mode, each serial input corresponds to 16 LED driver pins, meaning that 48 LEDs driver pins in total. In GPIO mode provide 52 GPIO.

## Application

- Serial-to-parallel LED Driver
  - High port count switch LED driver
  - Bi-color or mono-color LED driver
  - Static (non-scan method) 7 digit 7-segment LED driver
  - LED matrix driver
- General Purpose Input Output(GPIO)
  - Factory/Office security system
  - Keyboard scanning
  - LED display board control
  - Ethernet I/O

**Table of Contents**

## Revision History

| Revision Number | Revision |
|---|---|
| R01 | First Release |
| R02 | 1. Add application diagrams of LED driver mode.<br>2. Revise the feature and application |
| R03 | 1. Modify the pin description of Mode[2:0]<br>2. Modify the description of Serial-to-parallel LED mode |
| R04 | 1. Add AC/DC characteristics paramter<br>2. Modify the pin number for correct pin 10~12 description – page 6,7<br>3. Modify the pin number for correct pin 48 M_CLK description – page 7<br>4. Modify the LED driver output pin and Last_Stage_out1,2 number for correct pin 38~31,29~12,10~1,68~61,59~52 and 35,36 description – page 6, |

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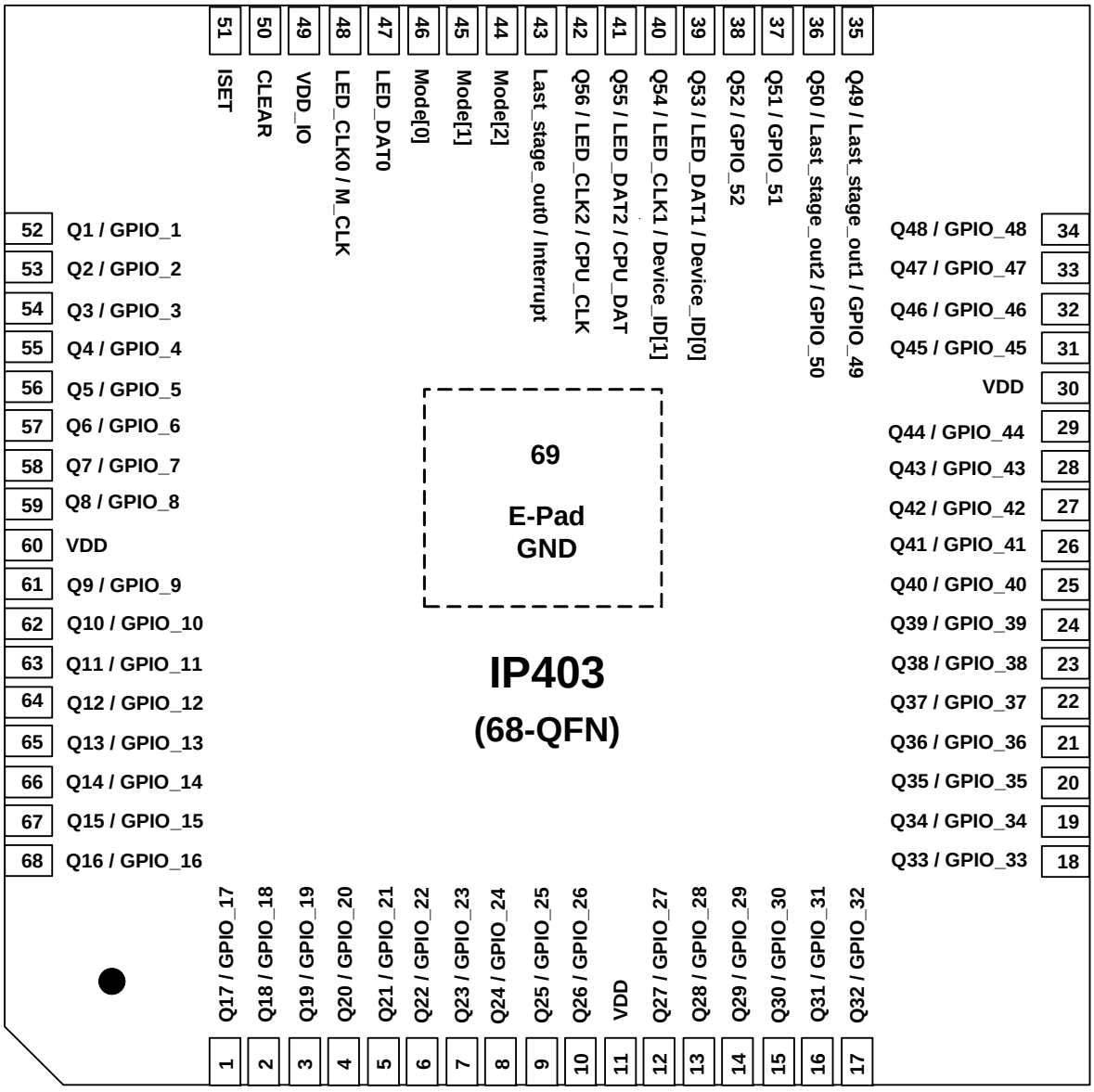
## 1 PIN Diagram (68QFN top view)



## 2 Pin Descriptions

Abbreviation

| Abbreviation | Description |
|---|---|
| P | Power and Ground |
| I | Input |
| LI | The input is latched at the end of reset and used as a default value |
| O | Output |
| I/O | Schmitt trigger input/ Output |
| OD | Open drain output |
| IPH | Schmitt trigger input with 60K ohm internal pull high |
| IPL | Schmitt trigger input with 60K ohm internal pull low |

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th></th></tr>
<tr><td colspan="4">System Configuration</td></tr>
<tr><td>44,45,46</td><td>MODE[2..0]</td><td>IPH</td><td>These pins are used to configure the operating mode.
<table>
<tr><th>MODE [2:0]</th><th>Mode</th><th>Description</th></tr>
<tr><td>000</td><td>TEST mode</td><td>Reserved for test.</td></tr>
<tr><td>001</td><td>GPIO mode</td><td>General Purpose Input Output mode</td></tr>
<tr><td>010</td><td>56-bit LED shift left</td><td>56-bit serial-to-parallel LED mode. The LED state will be shifted from Q1 to Q56.</td></tr>
<tr><td>100</td><td>56-bit LED shift right</td><td>56-bit serial-to-parallel LED mode. The LED state will be shifted from Q56 to Q1.</td></tr>
<tr><td>110</td><td>Turns off all LEDs in 56-bit LED mode</td><td>Turns LED off</td></tr>
<tr><td>111</td><td>Turns all LEDs off in triple 16-bit LED mode.</td><td>Turns LED off</td></tr>
<tr><td>011</td><td>Triple 16-bit LED shift left</td><td>Triple 16 bits serial-to-parallel LED mode. The LED state will be shifted from Q1 to Q16, from Q17 to Q32 and from Q33 to Q48.</td></tr>
<tr><td>101</td><td>Triple 16-bit LED shift right</td><td>Triple 16 bits serial-to-parallel LED mode. The LED state will be shifted from Q16 to Q1, from Q32 to Q17 and from Q48 to Q33.</td></tr>
</table></td></tr>
<tr><td>50</td><td>CLEAR</td><td>I</td><td>Low active input.<br>This pin is used to reset the internal register to the default state and should be set to “low” state for at least 0.1 ms.</td></tr>
</table>

**Pin description** (**continued**)
LED mode

| Pin no. | Label | Type | |
|---|---|---|---|
| **Serial-to-Parallel LED Driver** | | | |
| 38~31<br>29~12<br>10~1<br>68~61<br>59~52 | Q52~Q1 | O | The LED driver output, The current flowing on the LED can be adjusted by setting a resistor on ISET(see Pin 51). |
| 47<br>48 | LED_DAT0;<br>LED_CLK0 | I | LED_DAT0 is the data input pin of the serial-to-parallel shift register.<br><br>When set to 56-bit LED mode, IP403 utilizes these pins as the clock source and data source to shift all registers.<br><br>When set to triple 16-bit LED mode, IP403 utilizes these pins as the clock source and data source for these shift registers corresponding to Q[16:1].<br><br>The signal level of these pins should comply with the operating voltage of VDD_IO. |
| 39<br>40<br>41<br>42 | LED_DAT1/Q53;<br>LED_CLK1/Q 54<br>LED_DAT2/Q 55;<br>LED_CLK2/Q 56; | I/O | There are 2 modes implemented on these pins.<br><br>**Triple 16-bit LED mode:**<br>When set to this mode, IP403 functions as 3 separate serial-to-parallel shift registers. LED_CLK0 and LED_DAT0 correspond to the first 16-bit shift register, named as Q[16:1]. LED_CLK1 and LED_DAT1 correspond to the second 16-bit shift register, named as Q[32:17]. LED_CLK2 and LED_DAT2 correspond to the third 16-bit shift register, named as Q[48:33].<br><br>**56-bit LED mode:**<br>When set to this mode, theses pins function as a 56-bit serial-to-parallel LED driver. |
| 35<br><br>36<br><br>43 | Last_Stage_out1 /Q49;<br>Last_Stage_out2 /Q50;<br>Last_Stage_out0 | O | The output comes from the last stage of the serial-to-parallel shift register. The designer can use this pin to cascade to the next LED_DAT input.<br>In triple 16-bit mode, the Q49 and Q50 function as the last stage of the third and second serial-to-parallel shift register respectively. |
| 51 | ISET | I | In serial-to-parallel LED mode, the LED current is determined by setting a proper resistor on this pin. Leave this pin unconnected in GPIO mode.<br><br>The relationship between the resistor and the current is as following.<br>6.2K:16mA<br>8.2K:12mA<br>12.4K:8mA<br>24.8K:4mA |

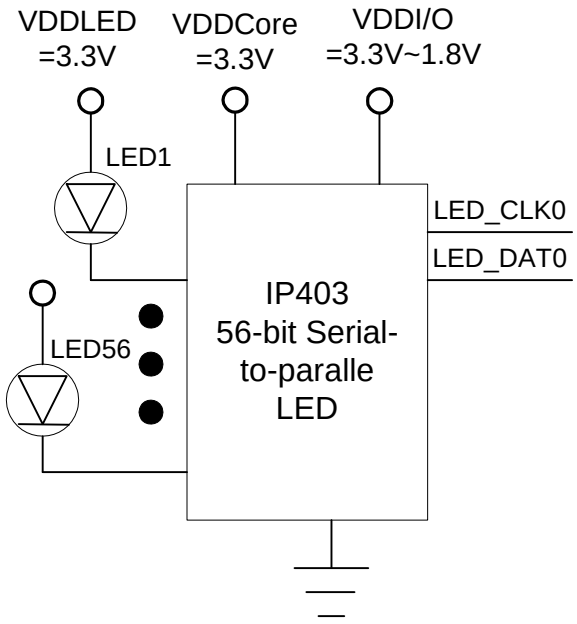
| Pin no. | Label | Type | |
|---|---|---|---|
| **GPIO Mode** | | | |
| 38~31<br>29~12<br>10~1<br>68~61<br>59~52 | GPIO52~GPIO1 | I/O | There pins can be configured as input or output by setting register 00h~03h. These pins are set to input state by reset default. |
| 39<br>40 | Device_ID[0]<br>Device_ID[1] | I | In GPIO mode, each IP403 should be set to a unique device ID. With this ID, the CPU can identify which device is under control. |
| 48 | M_CLK | I/O | Main clock input pin in GPIO mode.<br>The maximum input clock frequency is 25Mhz. |
| 41 | CPU_DAT | I/O | If IP403 is set to GPIO mode, this pin function as the data pin of the serial management interface. The CPU can read/write the internal register through this interface. |
| 42 | CPU_CLK | I | CPU access clock input in GPIO mode. In conjunction with CPU_DAT, this pin function as the serial management interface. The maximum clock rate is 1/2 system clock. |
| 43 | Interrupt | O | In GPIO mode, this pin indicates the input state change.<br>The interrupt pin is self-cleared after all of Reg 12~15h registers are read. |
| **System Power Supply** | | | |
| 11,30,60 | VDD | PWR | 3.3V supply voltage of core. |
| 69(E-Pad) | VSS | PWR | The exposed pad is the ground of this chip. |
| 49 | VDD_IO | PWR | 3.3V~1.8V supply voltage for LED_CLK[2:0]; LED_DAT[2:0] input stage. |

# 3 Functional Description

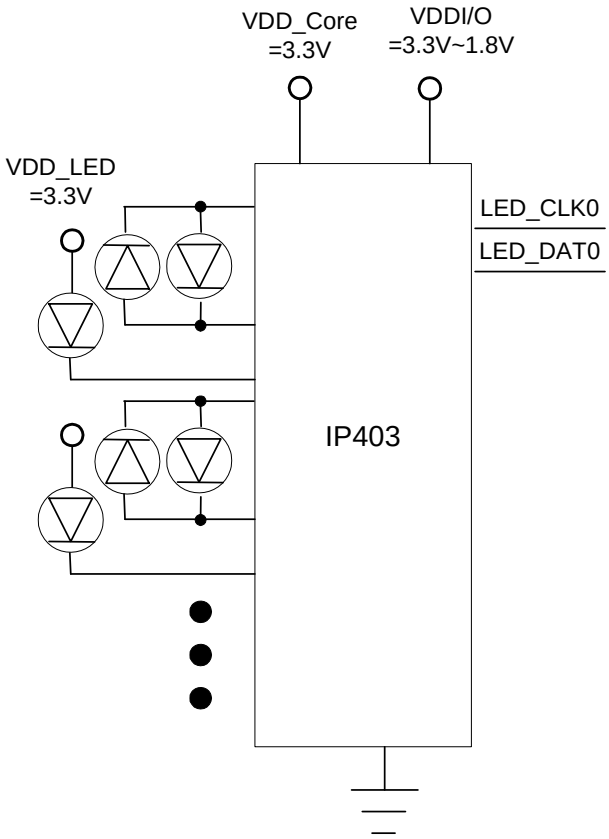
## 3.1 Serial-to-Parallel LED Mode

### 3.1.1 56-bit Serial-to-Parallel LED

LED_CLK0 is used as the global clock input of 56-bit shift registers and LED_DAT0 is the data input. IP403 sequentially shifts LED status at the rising edge of LED_CLK0. There are 2 modes for 56-bit serial-to-parallel LED mode, shift to left and shift to right.

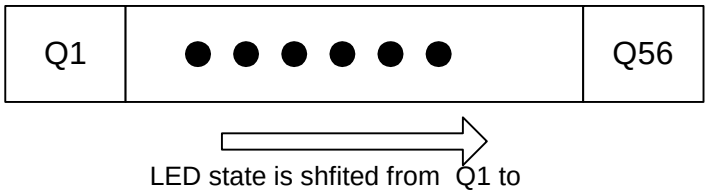



56-Bit Mono-color LED



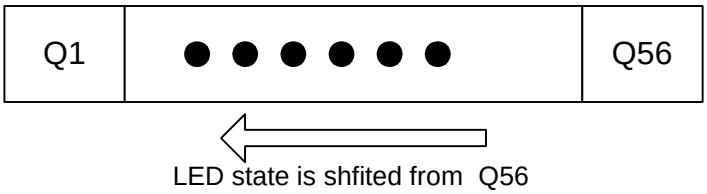

56-Bit Bi-color LED + Mono-color LED

- If mode[2:0] pins are set to “010”, the last bit present on LED_DAT0 will be stored on Q1.




LED state is shfited from Q1 to Q56.
The last bit present on LED_DAT0 will be stored a Q1

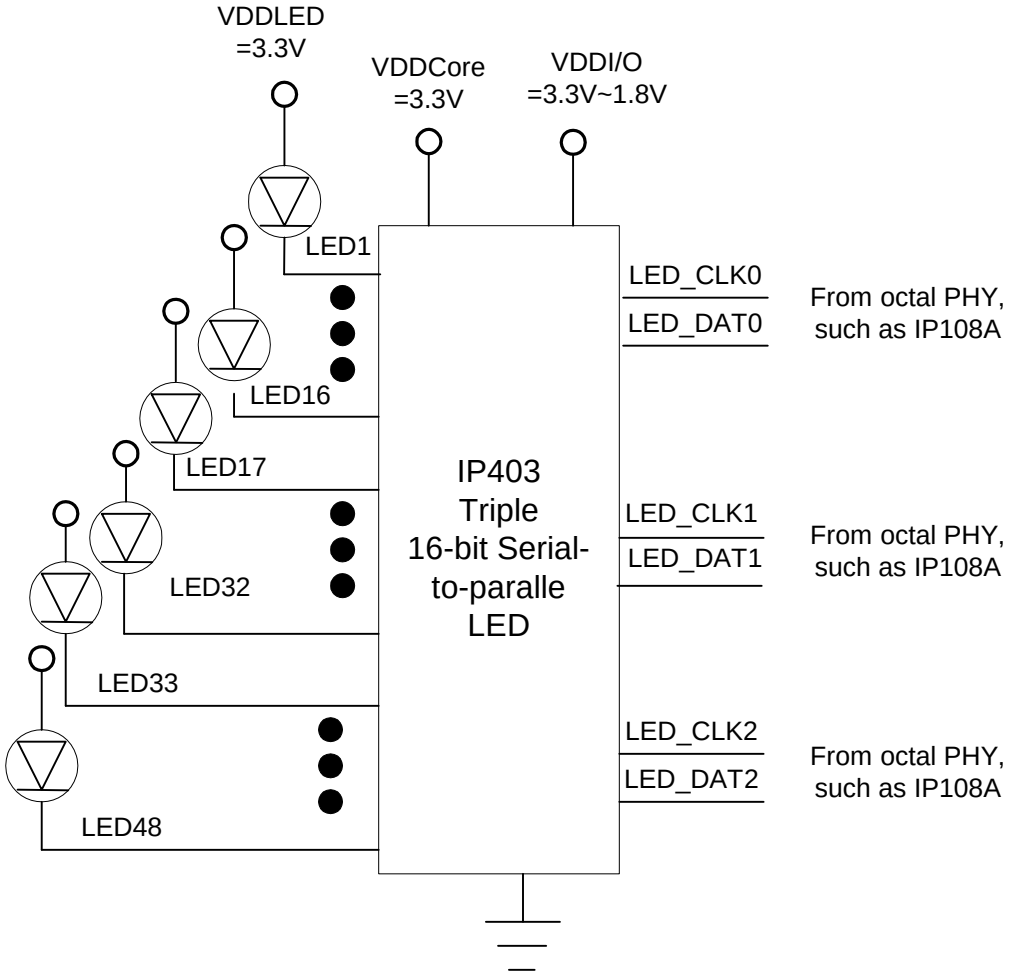
- If mode[2:0] pins are set to “100”, the last bit present on LED_DAT0 will be stored on Q56.

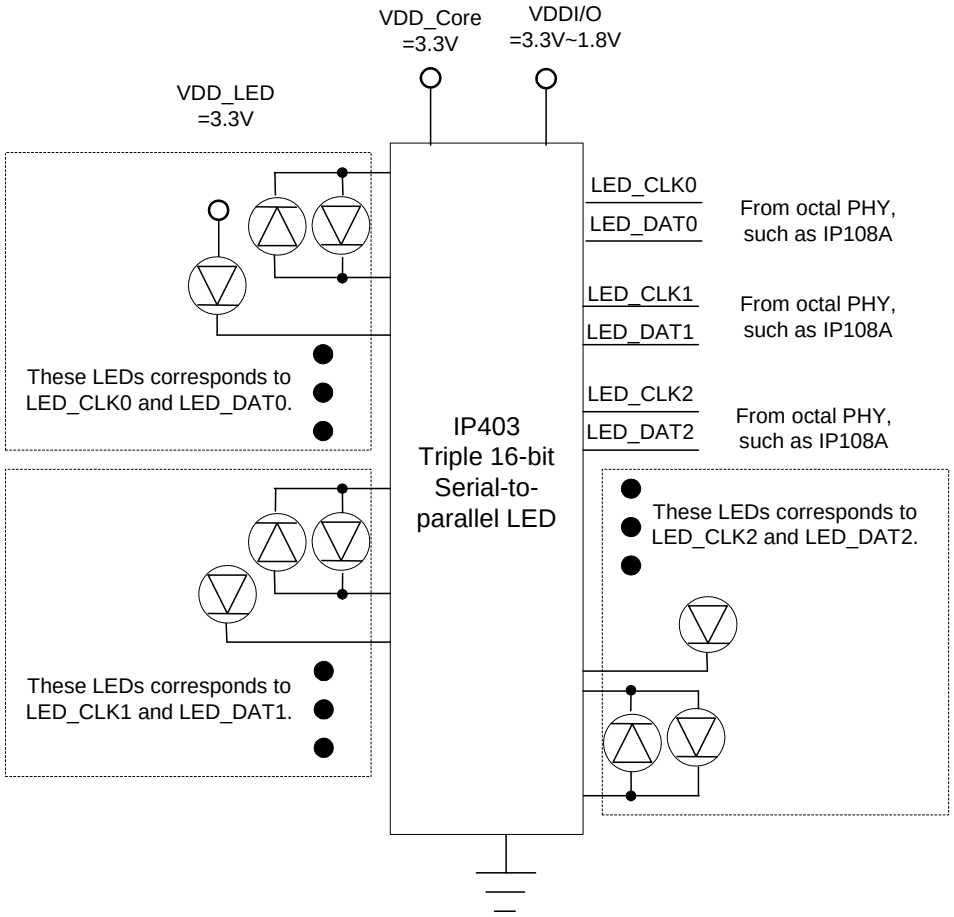



LED state is shfited from Q56 to Q1.
The last bit present on LED_DAT0 will be stored a Q56

### 3.1.2 Triple 16-bit Serial-to-Parallel LED

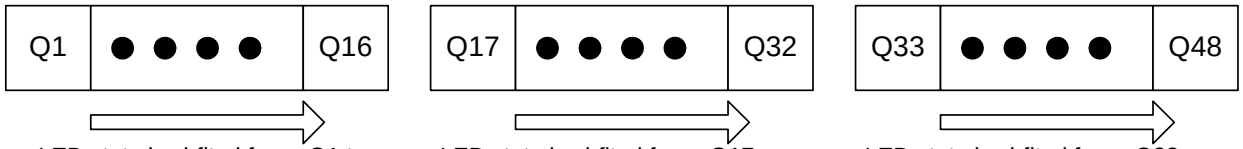
If Mode[2:0] pins are set to triple 16-bit shift register, Q1~ Q48 are divided as triple serial-to-parallel LED output. LED_CLK0, LED_DAT0 corresponds to Q1~ Q16 LED driver pins. Similarly LED_CLK1, LED_DAT1, LED_CLK2 and LED_DATA2 correspond to Q17~ Q32 and Q33~Q48 respectively.






Triple 16-bit : Bi-color LED + Mono-color LED

- If Mode[2:0] = “011”, the last incoming bits present on LED_DAT0, LED_DAT1 and LED_DAT2 are stored at Q1, Q17 and Q33 respectively.

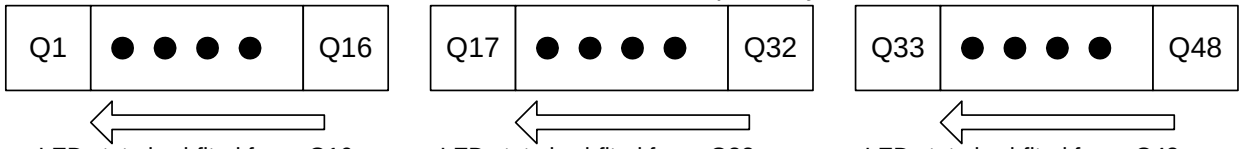



LED state is shfited from Q1 to Q16.
The last bit present on LED_DAT0 will be stored a Q1

LED state is shfited from Q17 to Q32.
The last bit present on LED_DAT1 will be stored a Q17

LED state is shfited from Q33 to Q48.
The last bit present on LED_DAT1 will be stored a Q33

- If Mode[2:0] = “101”, the last incoming bit present on LED_DAT0, LED_DAT1 and LED_DAT2 are stored at Q16, Q32 and Q48 respectively.




LED state is shfited from Q16 to Q1.
The last bit present on LED_DAT0 will be stored a Q16

LED state is shfited from Q32 to Q17.
The last bit present on LED_DAT1 will be stored a Q32

LED state is shfited from Q48 to Q33
The last bit present on LED_DAT2 will be stored a Q48

### 3.1.3 LED Off

For most application, the Ethernet switch is mounted on the chassis and is invisible to the network administrator. In this case, it may be necessary to turn LED off to save the power consumption. IP403 can perform this function by setting Mode[2:0] pins to “111’ while using triple 16-bit LED mode or setting to “110” while using 56-bit LED mode.

## 3.2 GPIO Mode

If Mode[2:0] pins are set to “001”, IP403 will function as a 52-bit General Purpose Input/Output(GPIO) controller. This function is much like the commonly used I/O controller 8255. In addition to the input/output attribute, IP403 also supports the following functions for various applications.

### 3.2.1 Programmable Input De-bounce Time

In some applications, it may be desired to filter the input bounce until the input state is stable. IP403 provides a programmable timer to filter the bounce. The de-bounce time can be calculated by the following formula.

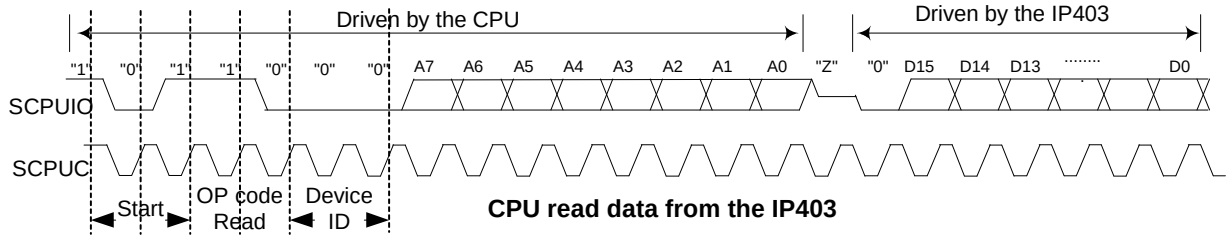
### 3.2.2 Interrupt

The interrupt is activated upon the state change of the selected input. Each input can be programmed to generate an interrupt as long as the corresponding interrupt is not masked. Setting Reg0x10 to Reg0x13[3:0] to “0” will activate the interrupt of the corresponding input.

### 3.2.3 Serial Control Interface

If set to GPIO mode, IP403 can be configured through serial control bus which comprises CPU_CLK and CPU_DAT. Like the access cycle of the serial management interface, the serial control interface comprises the device ID, the read/write command, the address and the data. The access cycle is depicted as below.

By setting IP403 to the value, ranging from “0” to “3”, the CPU can configure up to 4 IP403 in total.



## 4 Register Description

Abbreviation description

| Abbreviation | Description |
|---|---|
| SC | Self-Clear |
| LH | Latched High |
| LL | Latched Low |
| RO | Read Only |
| R/W | Read and Write |
| NA | Not Affected |
| RC | All bits are cleared to “0” after read |

**Note:**
The register address listed in the following table is in “hex-decimal” number.

| Reg Addr. | Registor Description | R/W | Default value |
|---|---|---|---|
| GPIO control register | | | |
| 00H | **REG_0**<br>GPIO[52:49] input/output setting<br>bit [3:0] : 1 : set to output<br>0 : set to input (default) | R/W | 4'h-0 |
| 01H | **REG_1**<br>GPIO[16:1] input/output setting<br>bit [15:0] : 1 : set to output<br>0 : set to input (default) | R/W | 16'h0000 |
| 02H | **REG_2**<br>GPIO[32:17] input/output setting<br>bit [15:0] : 1 : set to output<br>0 : set to input (default) | R/W | 16'h0000 |
| 03H | **REG_3**<br>GPIO[48:33] input/output setting<br>bit [15:0] : 1 : set to output<br>0 : set to input (default) | R/W | 16'h0000 |
| 04H | **REG_4**<br>GPIO[16:1] output state. The output state of these pins are valid only if the corresponding bit of REG_1 is set to output.<br>bit [15:0] : 1 : output high<br>0 : output low (default) | R/W | 16'h0000 |
| 05H | **REG_5**<br>GPIO[32:17] output state. The output state of these pins are valid only if the corresponding bit of REG_2 is set to output.<br>bit [15:0] : 1 : output high<br>0 : output low (default) | R/W | 16'h0000 |
| 06H | **REG_6**<br>GPIO[48:33] output state. The output state of these pins are valid only if the corresponding bit of REG_3 is set to output.<br>bit [15:0] : 1 : output high<br>0 : output low (default) | R/W | 16'h0000 |
| 07H | **REG_7**<br>GPIO[52:49] output state. The output state of these pins are valid only if the corresponding bit of REG_0 is set to output. | R/W | 16'h6020 |

| Reg Addr. | Registor Description | R/W | Default value |
|---|---|---|---|
| | bit [3:0] : 1 : output high<br>0 : output low<br><br>GPIO input stable time<br>bit [8:4] : 5-bit counter for the input stable time<br>(a) No effect on this counter if this register is set to 0 or 1.<br>(b) setting a value between 2 to 127 will filter the input bounce noise of the GPIO input. The de-bounce time can be calculated by the following formula.<br>**(N-1) * P**, where N is the value of bit[8:4] and P is bit[14:12]<br>the input latch clock selection.<br>bit [10:9] : input counting way<br>00,11 : both positive edge and negative edge<br>01 : only positive edge<br>10 : only negative edge<br>bit [11] : reserved<br>bit [14:12]: input latch clock selection(P)<br>000 : 1T(Time slot)<br>001 : 5T<br>010 : 25T<br>011 : 500T<br>100 : 2500T<br>101 : 50000T<br>110 : 250000T(default)<br>111 : 5000000T<br>Ex. The system clock input is 25MHz (1T=40ns)<br>If bit[14:12] equals to 3'b101 and bit[8:4] equals to 5'd101,<br>the input stable time is 50000x40nsx100 = 200ms.<br>bit [15] : clear input changing counter<br>1 : clear<br>0 : no action | | |
| 08H | **REG_8**<br>GPIO[16:1]: Latched input<br>bit [15:0] : 1 : Input high 0 : Input low(default) | RO | 16'h0000 |
| 09H | **REG_9**<br>GPIO[32:17]: Latched input<br>bit [15:0] : 1 : Input high 0 : Input low(default) | RO | 16'h0000 |
| 0AH | **REG_10**<br>GPIO[48:33]: Latched input<br>bit [15:0] : 1 : Input high 0 : Input low(default) | RO | 16'h0000 |
| 0BH | **REG_11**<br>GPIO[52:49]: Latched input<br>bit [15:0] : 1 : Input high 0 : Input low(default)<br>bit [15:4] : 12-bit input level change counter | RO | 16'h0000 |
| 0CH | **REG_12** (RC)<br>INTERRUPT[15:0] for GPIO[16:1].<br>bit [15:0] : 1 : Input change occurred<br>0 : No change | RC | 16'h0000 |
| 0DH | **REG_13** (RC)<br>INTERRUPT[15:0] for GPIO[32:17].<br>The function of this register is the same as REG 0CH. | RC | 16'h0000 |

| Reg Addr. | Registor Description | R/W | Default value |
|---|---|---|---|
| 0EH | **REG_14** (RC)<br>INTERRUPT[15:0] for GPIO[48:33]<br>The function of this register is the same as REG 0CH. | RC | 16'h0000 |
| 0FH | **REG_15** (RC)<br>INTERRUPT[15:0] for GPIO[51:48]<br>bit [3:0] : The function of this field is the same as REG 0CH.<br><br>**GPIO Status**(RO):<br>bit [4] : The Input level change counter overflows<br>bit [5] : All GPIO are outputs<br>bit [6] : All GPIO are inputs | RC/RO | 7'h0000 |
| 10H | **REG_16**<br>Input interrupt mask for GPIO[16:1].<br>This register is valid only if GPIO is set to input.<br><br>bit [15:0] :<br>1 : The interrupt of the corresponding input change is masked.<br>0 : interrupt enabled. | R/W | 16'h0000 |
| 11H | **REG_17**<br>Input interrupt mask for GPIO[32:17].<br>This register is valid only if GPIO is set to input.<br><br>bit [15:0] :<br>1 : The interrupt of the corresponding input change is masked.<br>0 : interrupt enabled. | R/W | 16'h0000 |
| 12H | **REG_18**<br>Input interrupt mask for GPIO[48:33].<br>This register is valid only if GPIO is set to input.<br><br>bit [15:0] :<br>1 : The interrupt of the corresponding input change is masked.<br>0 : interrupt enabled. | R/W | 16'h0000 |
| 13H | **REG_19**<br>Input interrupt mask for GPIO[52:49]<br>(work when GPIO is set as input)<br>bit [3:0] :<br>1 : The interrupt of the corresponding input change is masked.<br>0 : interrupt enabled. | R/W | 4'h0 |

# 5 Electrical Characteristics

## 5.1 Absolute Maximum Ratings

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

| | |
|---|---|
| Supply Voltage | –0.3V to 4.0V |
| Input Voltage | –0.3V to 5.0V |
| Storage Temperature | –65°C to 150°C |
| IC Junction Temperature | 125°C |
| Ambient Operating Temperature (Ta) | 0°C to 70°C |

## 5.2 DC Characteristics

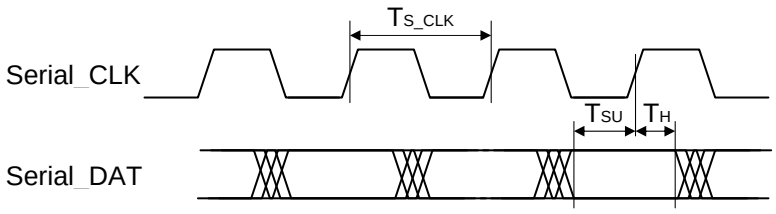
| Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| DVDD | Digital core supply voltage | 2.97 | 3.3 | 3.63 | V |
| VDDO | I/O pad supply voltage 1.8/3.3V(Selectable) | 1.62 | 1.8 | 1.98 | |
| | | 2.97 | 3.3 | 3.63 | |

## 5.3 I/O Characteristics

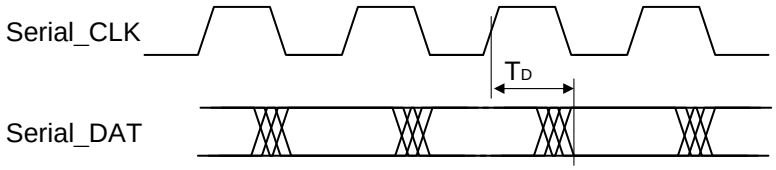
| Symbol | Specific Name | VDDO | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Threshold Voltage | 1.8V | 0.8 | - | V |
| | | 3.3V | 1.2 | - | |
| $V_{IL}$ | Input Low threshold Voltage | 1.8V | - | 0.5 | |
| | | 3.3V | - | 0.8 | |
| $V_{OH}$ | Output High Voltage | 1.8V | 1.8 | - | |
| | | 3.3V | 3.3 | - | |
| $V_{OL}$ | Output Low Voltage | 1.8V | - | 0 | |
| | | 3.3V | - | 0 | |
| $V_{RST}$ | RESETB Threshold Voltage | 1.8V | 0.8 | - | |
| | | 3.3V | 1.2 | - | |

## 6 AC Characteristics

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{M\_CLK}$ | Main clock Frequency | - | - | 25 | Mhz |
| $T_{M\_CLK}$ | Main clock cycle time | 40 | - | - | ns |
| $T_{S\_CLK}$ | Serial clock cycle time | 80 | - | - | ns |
| $T_{SU}$ | Serial_DAT setup time | 10 | - | - | ns |
| $T_H$ | Serial_DAT hold Time | 10 | - | - | ns |
| $T_D$ | Serial _CLK to CPU_DAT output delay | - | - | 20 | ns |




**Serial_DAT Input**




**Serial_DAT Output**

### 6.1 Thermal Resistor

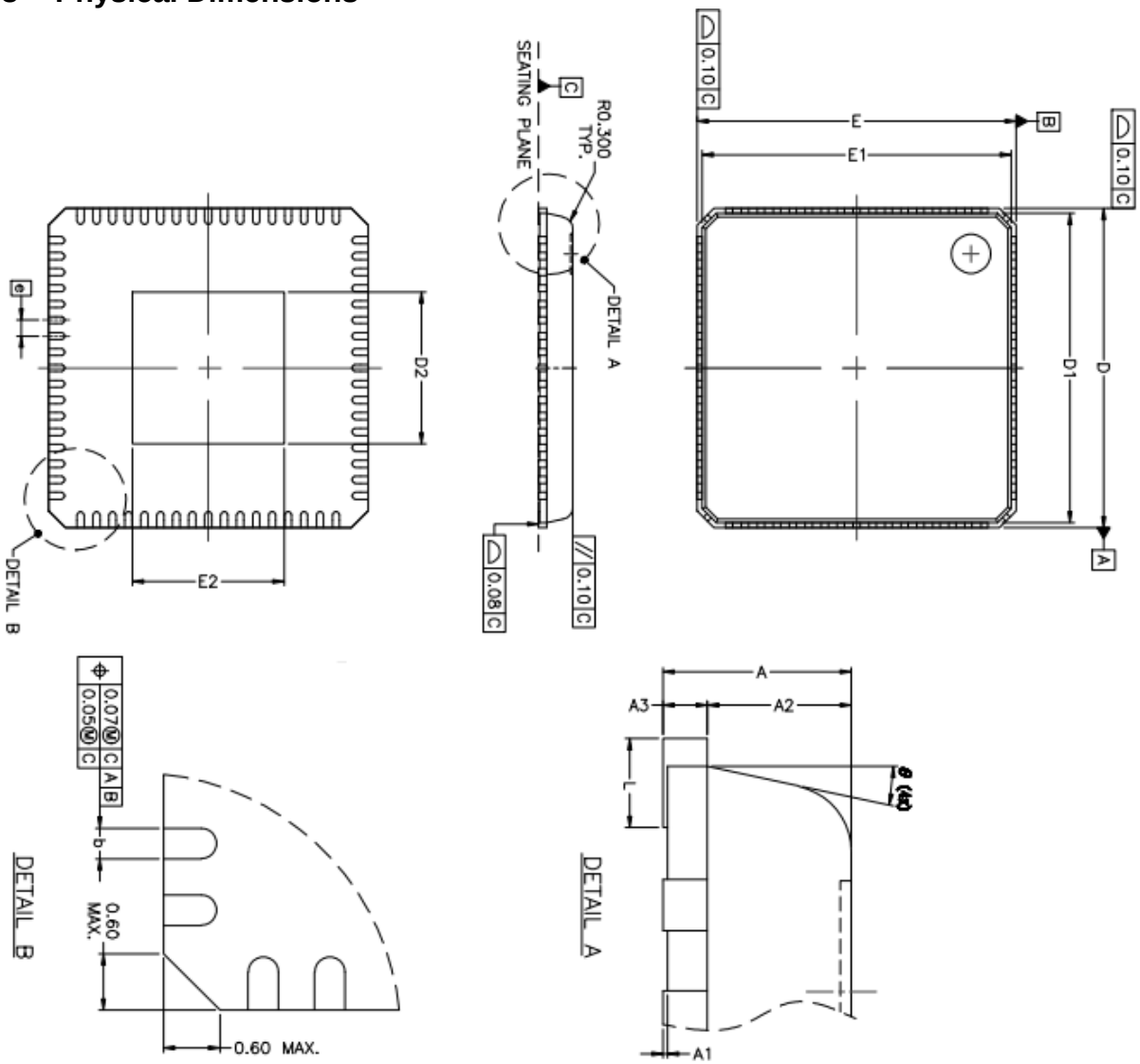
| $\theta_{JA}$ | $\theta_{JC}$ | $\varphi_{JC}$ | Conditions | Units |
|---|---|---|---|---|
| 89.8 | 22.3 | 12.9 | 2 Layer PCB | °C/W |
| 33.8 | 18.0 | 4.6 | 4 Layer PCB | °C/W |

* PCB size : base on JEDEC standard specifications 3”x 4.5”.

## 7 Order Information

| Part No. | Package | Notice |
|---|---|---|
| IP403 LF | 68-QFN | Lead free |

## 8 Physical Dimensions




| Symbol | Dimemsion(MM) | | | Dimemsion(Mil) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.8 | 0.85 | 1.0 | 31 | 33 | 39 |
| A1 | 0 | 0.02 | 0.05 | 0 | 1 | 2 |
| A2 | -- | 0.65 | 1.0 | -- | 26 | 39 |
| A3 | -- | 0.2 | -- | -- | 8 | -- |
| b | 0.15 | 0.2 | 0.25 | 6 | 8 | 10 |
| D | 8.0 BSC | | | 315 BSC | | |
| D1 | 7.75 BSC | | | 305 BSC | | |
| D2 | 3.65 | 3.8 | 3.95 | 144 | 150 | 156 |
| E | 8.0 BSC | | | 315 BSC | | |
| E1 | 7.75 BSC | | | 305 BSC | | |
| E2 | 3.65 | 3.8 | 3.95 | 144 | 150 | 156 |
| e | 0.4 BSC | | | 16 BSC | | |
| L | 0.3 | 0.4 | 0.5 | 12 | 14 | 16 |
| θ | 0° | -- | 14° | 0° | -- | 14° |

**Note:**

1. Refer to JEDEC STD: MO 220.
2. Dimension “b” applies to metallized terminal and is measured between 0.15 mm and 0.3 mm from the thermal tip. The terminal has optional radius on the other end of the terminal, the dimension B should not be measured in that radius area.