IP1001C Gigabit Ethernet Combo PHY

(TP/Fiber Auto Selection, Packet Counters & RGMII_PW down to 1.8V)

Features

- Built-in a 10BASE-Te/100BASE-TX/1000BASE-T TP port
- Built-in a 100BASE-FX/1000BASE-X Fiber port
- Supports TP and Fiber auto selection
- Supports 100BASE-FX and 1000BASE-X auto detection
- Supports IEEE 1588 stamp(two steps)
  - 32 stamps for RX/TX
  - 8 event trigger stamps support
  - PPS output support
- TTL level Fiber MAU for SD detection
- Auto-negotiation, auto MDI/MDIX and auto polarity correction
- Supports IEEE802.3az (EEE) and Smart EEE
- Auto Power Saving for link down port
- Built-in high efficiency switching regulator (3.3V->1.08V)
- Supports RGMII/MII
- Supports 3.3V/2.5V/1.8V signaling for RGMII/MII
- Supports TX_CLK and RX_CLK delay option
- Supports Loopback mode for diagnostics
- Supports RX counter and CRC counter
- Jumbo frame size up to 16KB at 10/100/1000 Mbps
- On chip termination resistors for the differential pairs
- Supports Interrupt function
- Supports 4 Fixed LED modes
- Supports 25MHz external crystal or OSC
- 85 nm process
- Package -68 Pin QFN

General Description

IP1001C consists of the physical layer device for 1000BASE-T, 100BASE-TX, and 10BASE-Te and Serdes for 1000BASE-X, 100BASE-FX applications. IP1001C also offers RGMII/MII for different types of 10/100/1000 Mbps Media Access Controller (MAC) interface.

IP1001C supports TP and Fiber auto setection, 100BASE-FX and 1000BASE-X auto detection, TTL level signal for SD detection, and Green Power. For power saving option, IP1001C supports 3 types of power saving modes: IEEE802.3az (EEE), Smart EEE, APS (auto power saving). IP1001C also provides IEEE 1588 stamp function for precision time application. In addition, IP1001C have a built-in high efficiency switching regulator, this feature minimizes the power dissipation from the power conversion, simplifies the power plane and reduces the system cost.

IP1001C also supports 3.3V/2.5V/1.8V, and TXCLK and RXCLK delay option for RGMII, This feature allows IP1001C to adapt to different chips seamlessly and get the EMI lower when needed...

IP1001C supports useful tools to assist user in designing, tools included the loopback mode, RX counter, and CRC counter .., etc.

Table Of Contents

List of Figures

List of Tables

Revision History

Revision #	Date	Change Description
IP1001C-DS-R00.01	2018.08.20	Initial
IP1001C-DS-R00.02	2018.09.19	Correct the pin names' typo of pins 11,14 and 15.

Disclaimer

This document probably contains the inaccurate data or typographic error. In order to keep this document correct, IC Plus reserves the right to change or improve the content of this document.

1. Features List

Features	IP1001C
Process	85nm
Package	68 QFN (8*8mm2)
10/100/1000Base-TP	Y
100/1000Base-FX	Y
RGMII/MII	Y
Power Consumption (W)	0.81
RGMII Voltage	3.3v/2.5v/1.8v
Built In Regulator	Switching
Auto MDI/MDI-X	Y
MDC/MDIO	Y
APS(Auto PW Down)	Y
802.3az	Y
Smart AZ	Y
IEEE 1588	PTP
RGMII DDR Timing support	Y
TX/RX Phase Delay setting	Y
Jumbo Frame@ 1 Gbps	16K Bytes
PHY Address (Default)	0
PHY Address (Pin Setting)	0~7
PHY Address (Register Setting)	0~31
RGMII Pin Sequence reorder	Y

2. Pin Diagram

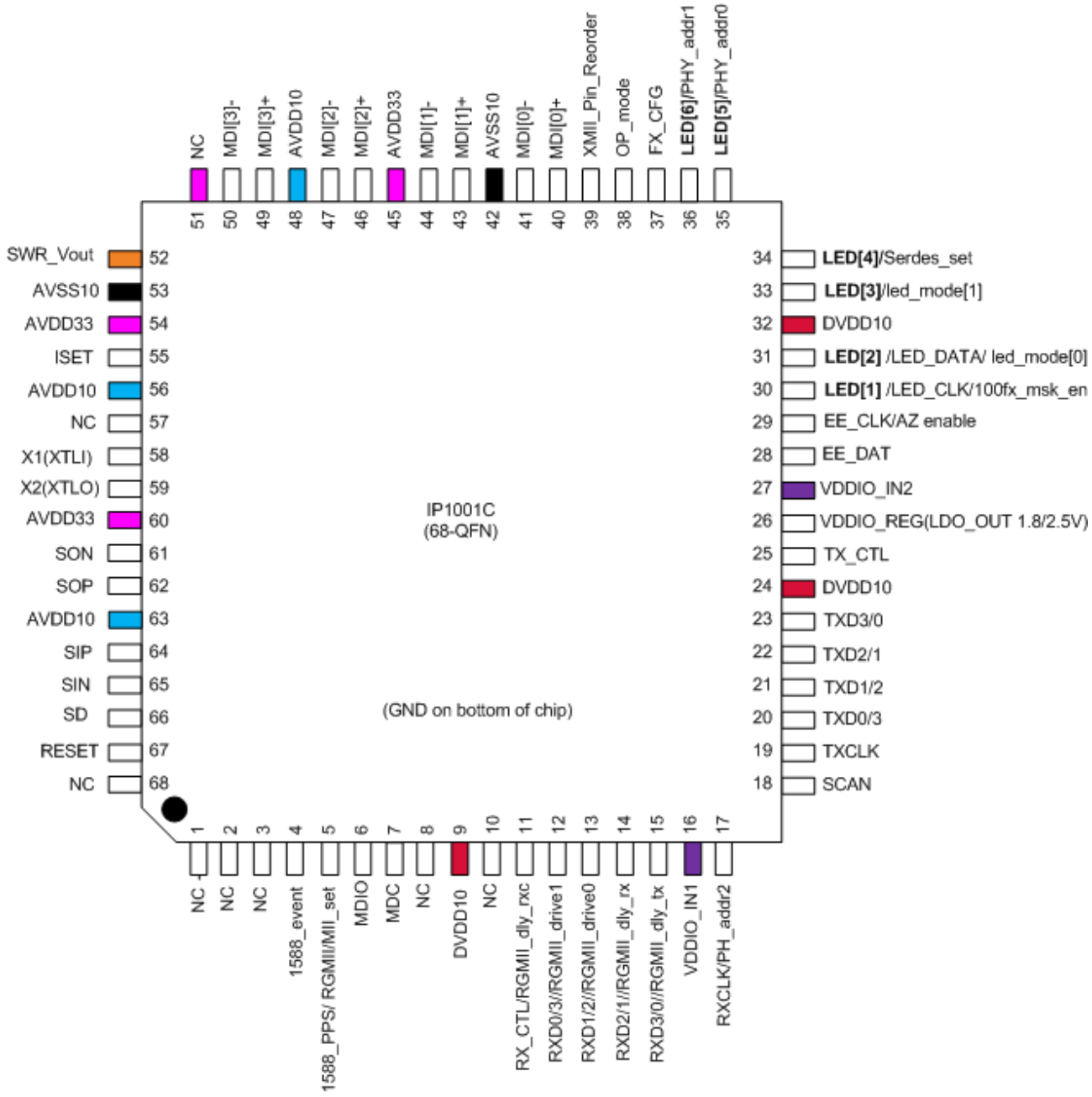


Figure 1 IP1001C 68 Pin Diagram

3. Pin description

<table>
<tr><th>Pin No.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">PHY interface(Auto-MDI/MDIX, HP-License)</td></tr>
<tr><td>50,47,44,41</td><td>MDI[3:0]-</td><td>I/O</td><td>Transmit/Receive output/input differential negative signal</td></tr>
<tr><td>49,46,43,40</td><td>MDI[3:0]+</td><td>I/O</td><td>Transmit/Receive output/input differential positive signal</td></tr>
<tr><td>65</td><td>SIN</td><td>I</td><td>Receive input differential negative signal</td></tr>
<tr><td>64</td><td>SIP</td><td>I</td><td>Receive input differential positive signal</td></tr>
<tr><td>61</td><td>SON</td><td>O</td><td>Transmit output differential negative signal</td></tr>
<tr><td>62</td><td>SOP</td><td>O</td><td>Transmit output differential positive signal</td></tr>
<tr><td colspan="4">RGMII/MII</td></tr>
<tr><td>20,21,22,23</td><td>TXD[0:3]</td><td>I</td><td>RGMII / MII transmit data.</td></tr>
<tr><td>25</td><td>TXCTL</td><td>I</td><td>RGMII transmit control.
It is sampled at both the rising edge and falling edge of TXC.
The TX_CTL indicates a TX_EN at the rising edge of TXC. TX_ER is derived from the logical operation of latched “TX_EN” and the value at the falling edge of TXC.
In MII mode, TXCTLis regarded as TX_EN</td></tr>
<tr><td>19</td><td>TXCLK</td><td>I/O</td><td>RGMII transmit clock.
<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>Gigabit</td><td>125MHz input.
IP1001C utilizes this clock to sample TXD [3:0] and TX_CTL at both the rising edge and falling edge of TXC.</td></tr>
<tr><td>100Mbps</td><td>25MHz input.
IP1001C utilizes this clock to sample TXD [3:0] and TX_CTL at both the rising edge and falling edge.</td></tr>
<tr><td>10Mbps</td><td>2.5MHz input.
IP1001C utilizes this clock to sample TXD [3:0] and TX_CTL at both the rising edge and falling edge.</td></tr>
</table>
In MII mode, TXCLK is 25Mhz and is driven by PHY</td></tr>
<tr><td>12,13,14,15</td><td>RXD[0:3]</td><td>O</td><td>RGMII /MII Sends Data.
Sends out RXD [3:0] and RX_CTL at both the rising edge and falling edge of RXCLK.</td></tr>
</table>

<table>
<tr><td>11</td><td>RXCTL</td><td>O</td><td>RGMII receive control
<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>Gigabit</td><td>RX_CTL indicates RX_DV at the rising edge of RXC. The RX_ER is derived from the logical operation of latched RX_DV and the value at the falling edge of RX_CLK.</td></tr>
</table>
In MII mode, RXCTL is regarded as RX_DV.</td></tr>
<tr><td>17</td><td>RXCLK</td><td>O</td><td>RGMII receive clock.
<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>Gigabit</td><td>125MHz output.
IP1001C sends out RXD[3:0] and RX_CTL at both the rising edge and falling edge of RX_CLK.</td></tr>
<tr><td>100Mbps</td><td>25MHz output.
IP1001C sends out RXD[3:0] and RX_CTL at both the rising edge and falling edge of RX_CLK.</td></tr>
<tr><td>10Mbps</td><td>2.5MHz output.
IP1001C sends out RXD[3:0] and RX_CTL at both the rising edge and falling edge of RX_CLK.</td></tr>
</table>
In MII mode, RXCLK is 25Mhz and is driven by PHY</td></tr>
</table>

Pin description (continue)

Pin No.	Label	Type	Description
EEPROM			
29	EE_CLK	O	Serial EEPROM clock output
28	EE_DAT	I/O	Serial EEPROM data
Serial LED			
30	LED_CLK	O	Serial LED CLK
31	LED_DAT	I/O	Serial LED data
Direct LED			
36,35,34,33,31,30	DIRECT_LED	O	Direct LED status drive output Direct LED 6~1 for IP1001C
SMI			
7	MDC	I	Serial management Clock It's recommended that add a 30pf capacitor to ground for noise filtering.
6	MDIO	I/O	Serial management I/O Data It's recommendation that add a 1.5K pull up resistor connecting to VDDIO_IN1(pin16) and a 30pf capacitor connecting to ground.
Miscellaneous			
58,59	X1,X2	I/O	Crystal input/output
67	RESET	I	System reset (low active) Should be kept at "low" for at least 10 microseconds. The input voltage should be not higher than 3.3V
18	SCAN	I	Scan input
52	SWR_Vout	O	SWR out 1.08V, Switching regulator voltage out
66	SD	I	Fiber signal detection, low active
55	ISET	I	Band gap , must be connect 6.19K resister to GND
38	OP_mode	I	The pin must be pulled down by 4.7K resistor for normal mode.
4	1588_EVENT	I	1588 Event Event trigger source input.
5	1588_PPS	O	1588 PPS Pulse per second reference output or clock/trigger output
68,57,51,10,8,3,2,1	NC		Not connect

Pin description (continue)

Pin No. IP1001C	Label	Type	Description
Power On setting. The state of these pins will be latched upon reset.			
5	RGMII/MII_set	IL, PU	RGMII/MII_set 0: MII 1: RGMII (Default) The pin is used to select interface for GMAC.
11	RGMII_dly_rxc	IL, PD	RGMII_dly_rxc 0: 1/4 clock period delay (Default) 1: No delay The pin is used to set precise RXCLK 2ns delay for RGMII I/F@ 1G speed. DDR is double data rate to generate clock and select edge to create precise 2ns delay@1G speed.
12,13	RGMII_Dirve[1:0]	IL, PD	RGMII_Drive[1:0] 00:4mA (Default) 01:8mA 10:18mA 11: 28mA The pins are used to adjust diving current ability for RGMII I/F.
14	RGMII_dly_rx	IL, PD	RGMII_dly_rx 0: No Delay (Default) 1: delay+1ns. The pin is used to adjust RX delay timing for RGMII I/F.
15	RGMII_dly_tx	IL, PD	RGMII_dly_tx 0:No Delay (Default) 1:delay+1ns. The pin is used to adjust TX delay timing for RGMII I/F.
29	AZ enable	IL, PU	AZ enable 0: enable 1: disable (Default) The pin is used to set that IP1001C will enter store and forward mode in AZ enable of PHY mode
30	100FX_msk_en	IL, PU	100FX_msk_en 0: disable 1: enable(Default) The pin is used to mask 100-FX
33,31	LED_mode[1:0]	IL, PU	LED direct mode selection 00: direct LED mode3 01: direct LED mode2 10: direct LED mode1 11: direct LED mode0 (Default) The pins are used to select 4 kinds of fixed LED modes.

34	Serdes_set	IL, PU	Serdes_ set 0: reserved 1: Serdes (Default) The pin is used to set Serdes
37	FX_CFG	IL, PU	FX_CFG Serdes is set: 0: 1000-X. 1: Auto (100-FX/1000-X) (Default) The pin is used to select serdes auto detection speed or fixed 1000-X. The FX_CFG setting is based on Serdes pin setting.
38	OP_mode	IL, PU	OP_mode 0: Normal mode ,the pin must be pull down. 1:Test mode. The pin is used to set to normal mode.
17,36,35	PHY_addr[2:0]	IL, PD IL, PU IL, PU	PHY address 011b': PHY address is 0 (Default) Others: Refer to Table 3 PHY address of IP1001C is 0~7 by setting these pins. By setting the related registers is 0~31.
39	XMII_Pin_Reorder	IL, PU	XMII_Pin_Reorder 0: xMII TXD/RXD pin bit3~0 1:xMII TXD/RXD pin reorder from bit 3~0 to 0~3 (Default). The pin is used to reorder TX/RX path for RGMII/MIII I/F

Pin description (continue)

Pin No.	Label	Type	Description
Power pin			
60,54,45	AVDD33	P	3.3V analog VDD power
63,56,48	AVDD10	P	1.08V analog VDD power
32,24,9	DVDD10	P	1.08V digital VDD power
26	VDDIO_REG	P	(LDO_out 2.5V/1.8V) for RGMII/MII/RMII/rMII I/O power
16	VDDIO_IN1	P	3.3V/2.5V/1.8V I/O power for CPU I/F,SMI I/F usage The related pins are 4,5,6,7,11~15, 17~23.
27	VDDIO_IN2	P	3.3V/2.5V I/O power for LED6~1 and EEPROM usage .The related pins are 29,30,31,33~39.
53, 42	AVSS10	P	Analog GND

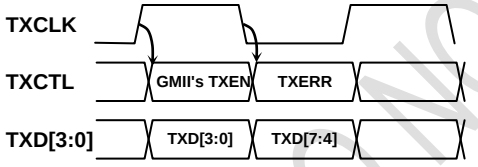
4. Functional Description

4.1 Interface

4.1.1 RGMII/MII

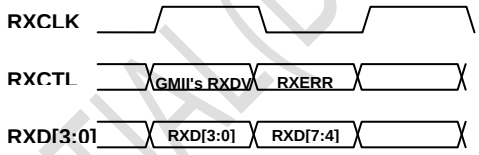
A MAC sends out data TXD[3:0] and control signal TXCTL at the rising and falling edge of TXCLK. Two GMII like signals TXEN and TXER are embedded in the TXCTL. GMII like information TXD[7:0] is embedded in the TXD[3:0]. By recognizing the decoded TXEN, TXD[7:0] and TXER, a PHY can capture the correct data stream.

A PHY sends out data RXD[3:0] and control signal RXCTL at the rising and falling edge of RXCLK. Two GMII like signals RXDV and RXER are embedded in the RXCTL. GMII like information RXD[7:0] is embedded in the RXD[3:0]. By recognizing the decoded RXDV, RXD[7:0] and RXER, IP1001C can capture the correct data stream. IP1001C samples the correct data at the rising edge of RXCLK.
At MII interface, RX_data is output,RXCTL is regards RXDV.TX_data is input,TXCTL is regards TXEN, TXCLK and RXCLK is 25Mhz and driven by PHY.



TXERR = GMII's TXEN (XOR) GMII's TXER

RGMII TX waveform



RXERR = GMII's RXDV (XOR) GMII's RXER

RGMII RX waveform

Figure 2 Waveform of RGMII Diagram

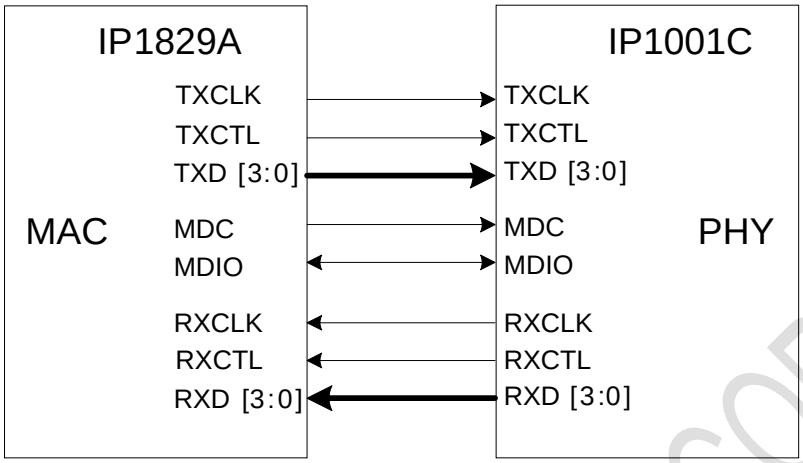


Figure 3 RGMII Application Diagram

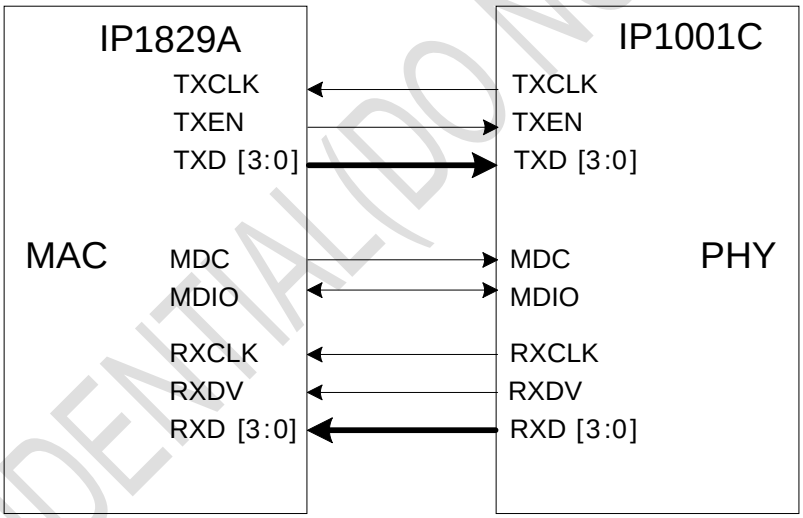


Figure 4 MII Application Diagram

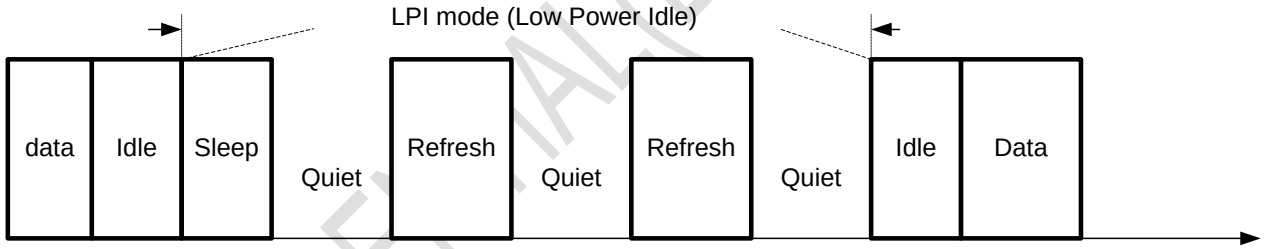
4.2 Green Power

IP1001C supports 3 types of power saving modes: IEEE802.3az Energy Efficient Ethernet, Smart EEE, APS (Auto Power Saving)

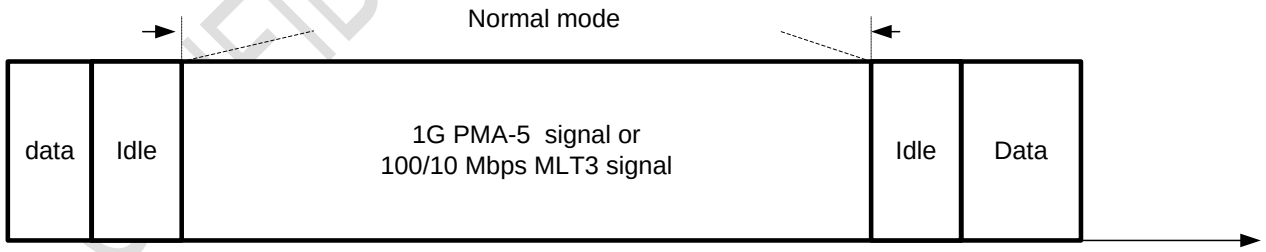
4.2.1 IEEE802.3az EEE

IP1001C supports Low Power Idle (LPI) mode in UTP port, which complies with IEEE802.3az EEE. Running this function, both of IP1001C and its link partner declare the EEE capability in auto-negotiation phase. If both ends are matched in EEE capability, IP1001C will enter Low Power Idle mode and stop sending signals onto the cable, when it receives the EEE command from the MAC device.
A MAC device must have the capability of handling the EEE commands if it wants to activate the LPI Mode of a PHY via the RGMII. The higher layer takes care of memorizing the link partner's wakeup time and waking up the link partner before sending data.
The EEE module works well at LPI (Low Power Idle) mode when
1. Link at full-duplex and
2. Auto-negotiation is enabled in both local and remote PHYs and
3. 1000/100Mbps and
4. EEE ability is supported in both local & remote PHYs and.
5. EEE_EN (MMD register 7.60[2:1]) is enabled for EEE function via default value.

IP1001C not only supports EEE ability in 100Mbps but also supports 10BASE-Te in 10Mbps, whose transmission amplitude is smaller than 10BASE-T but it still can operate well over 100 meters on Category 5 or better types of cable.
This function is default on and it can be enabled or disabled by programming register MMD Reg7.60 [2:1].



Refresh: Duration PHY sends Refresh symbols for timing recovery and synchronization.



4.2.2 Smart AZ

IP1001C provides Smart AZ function to conduct EEE function even if it is conjunction with a legacy Ethernet MAC device, which does not provide any command regarding EEE.
This function is default off and it can be enabled or disabled by programming register Page48 Reg21 [15].

4.2.3 APS (Auto Power Saving)

IP1001C will automatically enter this mode if link is down for more than 2 sec. In this mode, IP1001C will shutdown unnecessary functions and sends out normal link pulses in a period around 64 ms, much longer than that specified in IEEE 802.3, rather than fast link pluses to save power. When IP1001C receives any signal on MDI, it resumes to normal operation.
This function is default on and it can be enabled or disabled by programming register Page0 Reg16 [7].

4.3 MDI Auto-Crossover and Polarity Correction

IP1001C implements auto-crossover function, which allows the user to ignore the pin position of TX pair and Rx pair. If IP1001C is connected to a device that does not implement auto MDI/MDIX crossover, IP1001C will make the necessary adjustment prior to performing auto-negotiation. If IP1001C interoperates with a device that implements auto MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

The auto MDI/MDIX function is turned on automatically after hardware reset and the designers can disable it by programming register. The following table shows the pin mapping relationship in both the MDI and MDIX mode.

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-Te	1000BASE-T	100BASE-TX	10BASE-Te
MDI[0] +/-	BI_DA+/-	TX+/-	TX+/-	BI_DB+/-	RX+/-	RX+/-
MDI[1] +/-	BI_DB+/-	RX+/-	RX+/-	BI_DA+/-	TX+/-	TX+/-
MDI[2] +/-	BI_DC+/-	Unused	Unused	BI_DD+/-	Unused	Unused
MDI[3] +/-	BI_DD+/-	Unused	Unused	BI_DC+/-	Unused	Unused

IP1001C also performs polarity correction without any manual setting. It corrects polarity error on the receive pairs in 1000BASE-T, and 10BASE-Te modes automatically.

In 1000BASE-T mode, polarity correction is based on the sequence of idle symbols. In 10BASE-Te mode, polarity correction is based on the detection the polarity of valid normal link pulse and idle pulse. In 100BASE-TX mode, the polarity does not matter.

4.4 The link priority of the combo port

The IP1001C supported an auto-switching function to manage its Combo port.
And the managed rule is the link priority of the fiber is higher than the TP port.

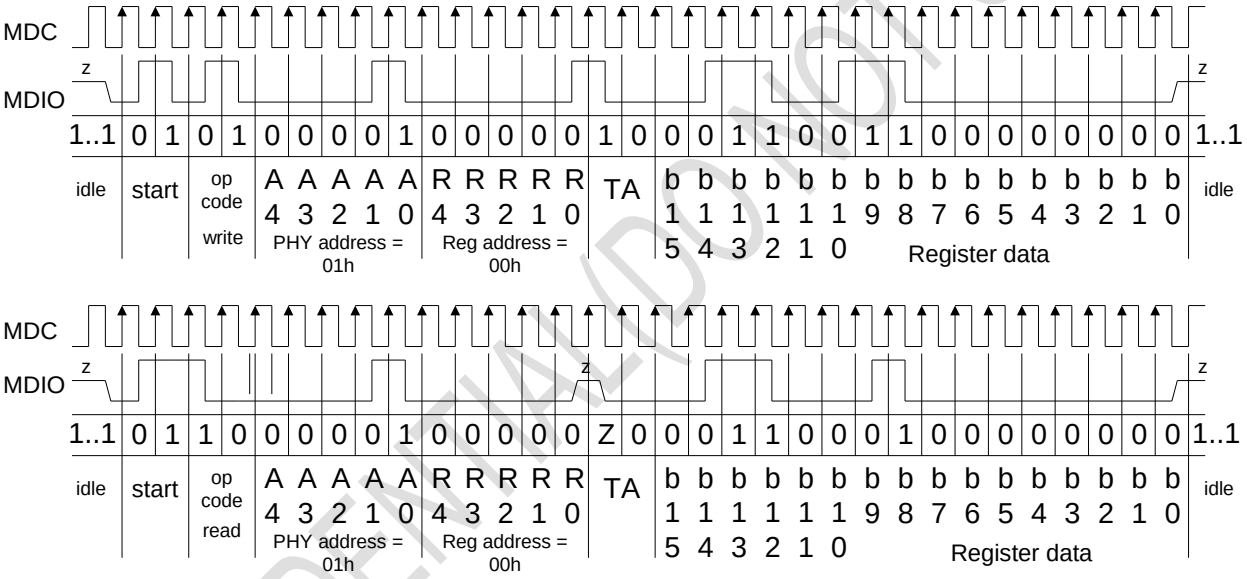
Table 1 Link sequence of the Combo port

Plugging	If condition was	Link Result
Fiber	TP Non-plugged	Fiber
Fiber	TP Plugged	Fiber
TP	Fiber Non-plugged	TP
TP	Fiber Plugged	Fiber

4.5 Serial Management Interface (SMI)

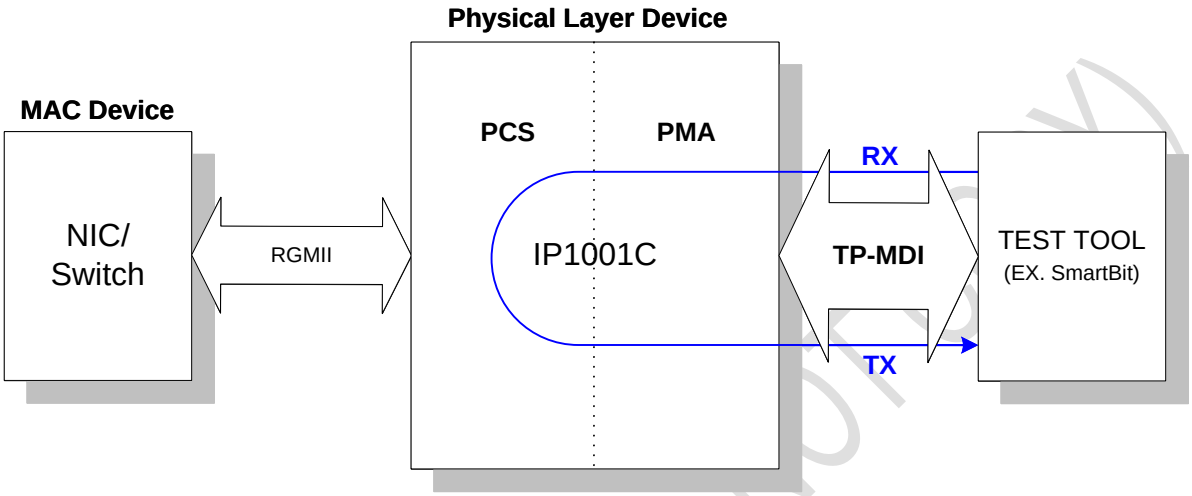
The serial management interface consists of two pins, MDC and MDIO, providing the capability to access to the registers of IP1001C. MDC is a clock input and runs at a maximum rate of 2.5 MHz. MDIO is a bi-directional data pin that runs synchronously to MDC. The MDIO pin requires a 5.1-kΩ pull up resistor for correct state transition. To access to register in IP1001C, MDC should be at least one more cycle than MDIO. This means that a complete command consists of 32 bits MDIO data and at least 33 MDC clocks, as the timing sequence depicted below.

Frame format	<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>

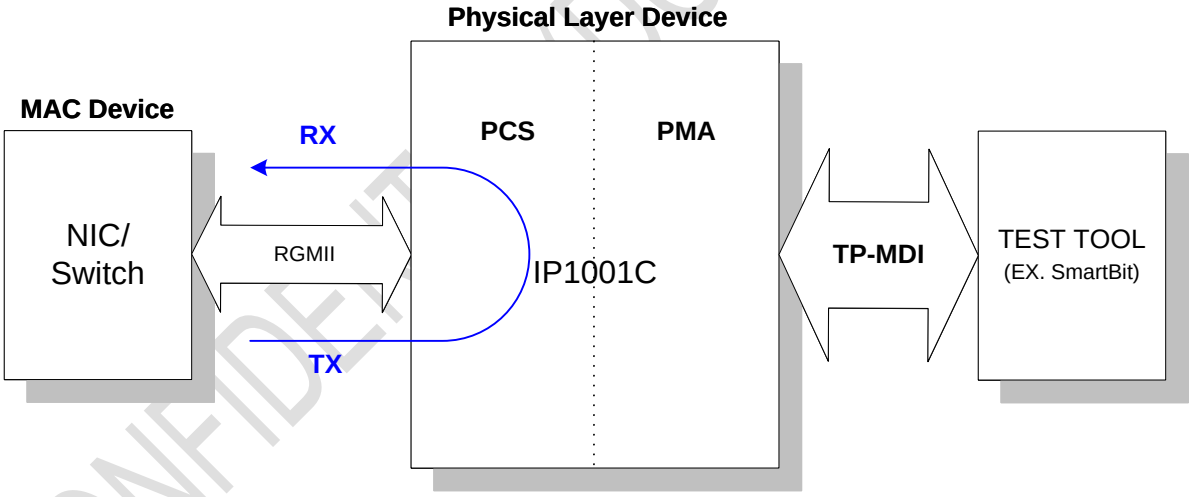


4.6 Loopback Mode

1) PMA Loopback (Page 2 Reg 18 [8] =1).



2) PCS Loopback (Page 0 Reg0 [14] =1).



4.7 Power Input

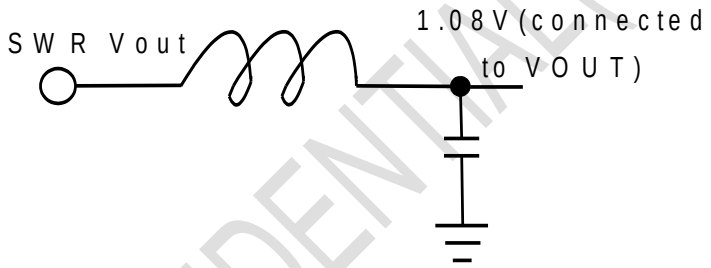
IP1001C requires 3 levels of power sources for normal operation. These 3 levels of power provide 5 kinds of circuit as described in the table.

Power source	Related circuit
AVDD33	3.3V used for analog circuit.
AVDD10	1.08V used for analog circuit.
DVDD10	1.08V used for digital circuit.
DVDD_IO	Wide range power source used for RGMII /MII I/O interface.

The typical power inputs for AVDD33 and DVDD10/AVDD10 are 3.3V and 1.08V respectively; while the power input of DVDD_IO may range from 3.3V to 1.8V, if the RGMII I/O supply voltage of MAC side is the same as DVDD_IO.

For AVDD33 and DVDD10/AVDD10 power inputs, it is recommended to place a ferrite bead to separate both power sources, even they are at the same power level. These ferrite beads can avoid the noise coupling between the digital/analog power paths to increase the system stability.

IP1001C includes a high efficiency switching regulator to convert 3.3V to 1.08V. Either the built-in switching regulator or the external 1.08 voltage power can be used as supply source, depending on the designer's choice.



4.8 LED & PHY Address configuration

4.8.1 LED configuration

The bit stream is output sequentially through LED_DAT and LED_CLK and its sequence starts from LED bit 6~1 for serial LED mode. In the other word, bit 1 LED status is present on the latest LED bit, as shown in the table. To store the serial LED stream, a serial-to-parallel shift register should be used. IP1001C also supports direct LED mode to directly drive LED without ultra glued logic for low cost need.

IP1001C supports 4 kinds of fixed LED usage for specific LED application at direct LED mode, please refer to the following table.

Table 2 Fixed LED specific application for direct LED mode

Fixed LED mode	1	2	3	4	5	6
0	L/A-TP	G-L-TP (speed)	FDX/COL-TP	L/A-FX	Reserved	Reserved
1	L-TP	ACT-TP	FDX/COL_TP	L-FX	/ACT-FX	FDX/COL-FX
2	G-L-TP (speed)	10/100-L-TP (speed)	ACT-TP	G-L-FX (speed)	100-L-FX (speed)	ACT-FX
3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

4.8.2 PHY Address configuration

IP1001C only responds to a command through SMI with correct PHY address. Before accessing the register of IP1001C, initial PHY address should be configured to 0~7 with pin PHY_addr0, PHY_addr1, PHY_addr2 in advance. The value on PHY_addr pins is latched at the end of power on reset. In addition to responding to a command with PHY address the same as that of IP1001C,

Table 3 PHY Address Configuration

Pin Name			Initial PHY Address
PHY_addr2	PHY_addr1	PHY_addr0	
L	H	H	0(default)
L	H	L	1
L	L	H	2
L	L	L	3
H	H	H	4
H	H	L	5
H	L	H	6
H	L	L	7

4.9 IEEE 1588 Precision Timing Protocol (PTP)

IP1001C implements the precision timing protocol (including IEEE1588/IEEE802.1as) function. For the PTP application, IP1001C uses the PTP dedicated hardware to capture the timestamp of PTP frame and store them into internal buffer; the software processes the various protocol message and co-work with PTP dedicated hardware.

To synchronous the master clock, IP1001C offers the adjustable real time clock (RTC), which could increases, decreases the clock frequency and set the specific time-value into RTC. If the PTP packet is detected, the PTP dedicated hardware will capture the time-value of SFD position for PTP or event signal. After the PTP synchronization process, the CPU uses the ingress/egress time-stamp to obtain the compensation parameter. Then, the CPU will pass the relating compensation value into PTP dedicated hardware. After the long duration, the PTP dedicated RTC is synchronous with the remote master clock.

P1001C supports 32 depth timestamp FIFO(16 for ingress, 16 for egress) to record PTP time-stamp. When all time stamps are occupied, user also set overwrite bit enable to over write time stamps cyclically. Another, IP1001C also supports 8 time stamps for incoming event trigger signal.

For the monitor system application, IP1001C support three different output synchronous signals. These output signals are pulse-per second, the programming clock duration signal and trigger-out signal. Further, please refer to PTP application note in detail.

5. Register Description

Abbreviation description

Abbreviation	Description
SC	Self-Clear.
LH	Latched High.
LL	Latched Low.
RO	Read Only.
R/W	Read and Write.
NA	Not Affected.
HW Reset	Reset by RESET# (RESET) pin.
SW Reset	Reset by register 0 bit 15.

5.1 GPHY register description

5.1.1 Control Register (Page0 Reg0)

Bit	Name	Description	Type	HW Reset	SW Reset
[5:0]	Reserved		RO	Always 0	
6	Speed Selection (MSB)	Bit 6 / Bit 13: 0 0 = 10Mb/s; 0 1 = 100Mb/s; 1 0 = 1000Mb/s; 1 1 = Reserved	R/W	1	NA
7	Collision Test	1: Enable COL signal test. 0: Disable COL signal test.	R/W	0	0
8	Duplex Mode	1: Full duplex. 0: Half duplex.	R/W	1	NA
9	Restart Auto-NEG	1: Restart Auto-Negotiation Process. 0: Normal operation.	R/W SC	0	0 (SC)
10	Isolate	1:Isolate PHY from RGMII electrically, But MDC/MDIO is still active. 0: Normal operation	R/W	0	0
11	Power Down	Link is down; only Management Interface and logical active. 1: Power down. 0: Normal operation.	R/W	0	0
12	Auto-Negotiation Enable	1: Enable Auto-Negotiation Process. 0: Disable Auto-Negotiation Process.	R/W	1	NA
13	Speed Selection (LSB)	Please refer to bit 6 for detail information.	R/W	0	NA
14	Loopback	1: Enable PCS loopback mode. 0: Disable PCS loopback mode.	R/W	0	0
15	Software Reset	1: PHY software reset. 0: Normal operation.	R/W SC	0	0 (SC)

5.1.2 Status Register (Page0 Reg1)

Bit	Name	Description	Type	HW Reset	SW Reset
0	Extended Capability	1: Support extended register capabilities. 0: Support basic register set capabilities only.	RO	1	1
1	Jabber Detect	1: Jabber condition detected. 0: No jabber condition detected.	RO LH	0	0
2	Link Status	1: Link is up. 0: Link is down.	RO LL	0	0
3	Auto-Negotiation Ability	1: PHY is able to perform Auto-Negotiation. 0: PHY is not able to perform Auto-Negotiation...	RO	1	1
4	Remote Fault	1: Remote fault condition detected 0: No remote fault condition detected.	RO LH	0	0
5	Auto-Negotiation Complete	1: Auto-Negotiation process completed. 0: Auto-Negotiation process not completed.	RO	0	0
6	MF Preamble Suppression	1: PHY accepts management frames with preamble suppressed. 0: PHY does not accept management frames with preamble suppressed.	RO	Reserved 1	
7	Reserved	Ignore when read	RO	Reserved 0	
8	Extended Status	1: There is extended status information in Register 15 0: No extended status information in Register 15	RO	Reserved 1	
9	100BASE-T2 Half Duplex	1: PHY able to perform half duplex 100BASE-T2 0: PHY not able to perform half duplex 100BASE-T2	RO	Reserved 0	
10	100BASE-T2 Full Duplex	1: PHY able to perform full duplex 100BASE-T2 0: PHY not able to perform full duplex 100BASE-T2	RO	Reserved 0	
11	10Mb/s Half Duplex	1: PHY able to operate at 10 Mb/s in half duplex mode 0: PHY not able to operate at 10 Mb/s in half duplex mode.	RO	1	1
12	10 Mb/s Full Duplex	1: PHY able to operate at 10Mb/s in full duplex mode 0: PHY not able to operate at 10Mb/s in full duplex mode.	RO	1	1
13	100BASE-TX Half Duplex	1: PHY able to perform half duplex 100BASE-TX. 0: PHY not able to perform half duplex 100BASE-TX.	RO	1	1
14	100BASE-TX Full Duplex	1: PHY able to perform full duplex 100BASE-TX. 0: PHY not able to perform full duplex 100BASE-TX.	RO	1	1
15	100BASE-T4	1: PHY able to perform 100BASE-T4. 0: PHY not able to perform 100BASE-T4.	RO	Reserved 0	

5.1.3 Identifier Register (Page0 Reg2)

Bit	Name	Description	Type	HW Reset	SW Reset
[15:0]	Organizationally Unique Identifier Bit [3:18]	0000_0010_0100_0011 Note: IC Plus's OUI is 0x0090C3	RO	Always 0x0243	

5.1.4 Identifier Register (Page0 Reg3)

Bit	Name	Description	Type	HW Reset	SW Reset
[3:0]	Revision Number		RO	Change with IC revision	
[9:4]	Manufacturer's Model Number	000010	RO	Always 000010	
[15:10]	Organizationally Unique Identifier Bit [19:24]	000011	RO	Always 000011	

5.1.5 Advertisement Register (Page0 Reg4)

Bit	Name	Description	Type	HW Reset	SW Reset
[4:0]	Selector Filed	5'b00001, supports IEEE 802.3.	RO	00001	00001
5	10BASE-T Half Duplex	1 = 10Base-T full duplex is supported 0 = 10Base-T full duplex not supported	R/W	1	1
6	10BASE-T Full Duplex	1 = 10Base-T half duplex is supported 0 = 10Base-T half duplex not supported	R/W	1	1
7	100BASE-TX Half Duplex	1 = 100Base-TX half duplex is supported 0 = 100Base-TX half duplex not supported	R/W	1	1
8	100BASE-TX Full Duplex	1 = 100Base-TX full duplex is supported 0 = 100Base-TX full duplex not supported	R/W	1	1
9	100BASE-T4	1 = 100Base-T4 is supported 0 = 100Base-T4 not supported	RO	Reserved 0	
10	PAUSE	1 = flow control is supported 0 = flow control is not supported	R/W	1	1
11	Asymmetric Pause	1 = Asymmetric flow control is supported 0 = Asymmetric flow control is not supported	R/W	0	0
12	Reserved	Ignore when read	R/W	0	0
13	Remote Fault	1 = Advertise remote fault detection capability 0 = Not advertise remote fault detection capability	R/W	0	0
14	Reserved	Ignore when read	RO	Reserved 0	
15	Next Page	1 = Next pages are supported 0 = Next pages are not supported	R/W	0	0

5.1.6 Link Partner's Ability Register (Page0 Reg5)

Bit	Name	Description	Type	HW Reset	SW Reset
[4:0]	Selector Field		RO	0	0
5	10BASE-T Half Duplex	1 = 10Base-T is supported by link partner 0 = 10Base-T not supported by link partner	RO	0	0
6	10BASE-T Full Duplex	1 = 10Base-T full duplex is supported by link partner 0 = 10Base-T full duplex not supported by link partner	RO	0	0
7	100BASE-TX Half Duplex	1 = 100Base-TX is supported by link partner 0 = 100Base-TX not supported by link partner	RO	0	0
8	100BASE-TX Full Duplex	1 = 100Base-TX full duplex is supported by link partner 0 = 100Base-TX full duplex not supported by link partner	RO	0	0
9	100BASE-T4	1 = 100Base-T4 is supported by link partner 0 = 100Base-T4 not supported by link partner	RO	0	0
10	PAUSE	1 = Flow control is supported by Link partner 0 = Flow control is not supported by Link partner	RO	0	0
11	Asymmetric Pause	1 = Asymmetric flow control is supported by Link partner 0 = Asymmetric flow control is NOT supported by Link partner	RO	0	0
12	Reserved	Ignore when read	RO	Reserved 0	
13	Remote Fault	1 = Link partner is indicating a remote fault 0 = Link partner does not indicate a remote fault. It is Received Code Word Bit 13	RO	0	0
14	Acknowledge	1 = Link partner acknowledges reception of local node's capability 0 = No acknowledgement It is Received Code Word Bit 14.	RO	0	0
15	Next Page	1 = Next pages are supported by link partner 0 = Next pages are not supported by link partner. It is Received Code Word Bit 15.	RO	0	0

5.1.7 Auto-Negotiation Expansion Register (Page0 Reg6)

Bit	Name	Description	Type	HW Reset	SW Reset
0	Link Partner Auto-Negotiation Able	1: Link partner supports Auto-Negotiation 0: Link partner does not support Auto-Negotiation	RO	0	0
1	Page Received	1: A new page has been received 0: A new page has not been received	RO LH	0	0
2	Local Next Page Able	1: Local device supports Next Page 0: Local device does not support Next Page	RO	1	0
3	Link Partner Next Page Able	1: Link Partner supports Next Page 0: Link Partner does not support Next Page	RO	0	0
4	Parallel Detection Fault	1: A fault has been detected via Parallel Detection function	RO	0	0

		0: A fault has not been detected via Parallel Detection function			
[15:5]	Reserved	Ignore when read	RO	Reserve 0	

5.1.8 Auto-Negotiation Next Page Transmit Register (Page0 Reg7)

Bit	Name	Description	Type	HW Reset	SW Reset
[10:0]	Message/Unformatted Field	Transmit Code Word Bit 10:0	R/W	1	1
11	Toggle	Transmit Code Word Bit 11	RO	0	0
12	Acknowledge 2	Transmit Code Word Bit 12	R/W	0	0
13	Message Page	Transmit Code Word Bit 13	R/W	1	1
14	Reserved	Transmit Code Word Bit 14	RO	Reserved 0	
15	Next Page	Transmit Code Word Bit 15	R/W	0	0

5.1.9 Auto-Negotiation Link Partner Next Page Register (Page0 Reg8)

Bit	Name	Description	Type	HW Reset	SW Reset
[10:0]	Message/Unformatted Field	Received Code Word Bit 10:0	RO	0	0
11	Toggle	Received Code Word Bit 11	RO	0	0
12	Acknowledge 2	Received Code Word Bit 12	RO	0	0
13	Message Page	Received Code Word Bit 13	RO	0	0
14	Acknowledge	Received Code Word Bit 14	RO	0	0
15	Next Page	Received Code Word Bit 15	RO	0	0

5.1.10 1000BASE-T Control Register (Page0 Reg9)

Bit	Name	Description	Type	HW Reset	SW Reset
[7:0]	Reserved	Ignore when read	R/W	Reserved to 0x00	
8	1000BASE-T Half Duplex	1: Advertise 1000BASE-T half duplex capable 0: Not advertise	R/W	1	0
9	1000BASE-T Full Duplex	1: Advertise 1000BASE-T full duplex capable 0: Not advertise	R/W	1	0
10	Port Type	1: Prefer multi-port device (MASTER) 0: Prefer single-port device (SLAVE)	R/W	1	0
11	Configuration Value	1: Manual configure as MASTER 0: Manual configure as SLAVE It is valid only if bit 9.12 is set to 1.	R/W	0	0
12	Manual Configuration Enable	1: Manual Configuration Enabled 0: Manual Configuration Disabled	R/W	0	0
[15:13]	Test mode	1000BASE_T test mode defined in IEEE802.3 clause 40.6.9 [15:13] Mode 000 Normal Mode 001 Test Mode 1 –Transmit waveform test	R/W	000	000

		010	Test Mode 2 –Transmit Jitter test in MASTER mode			
		011	Test Mode 3 –Transmit Jitter test in SLAVE mode			
		100	Test Mode 4 –Transmit distortion test			
		Others	Reserved			

5.1.11 1000BASE-T Status Register (Page0 Reg10)

Bit	Name	Description	Type	HW Reset	SW Reset
[7:0]	Idle Error Count	Idle Error Count	RO	0x00	0x00
8	Reserved	Ignore when read	RO	Reserved to 0	
9	Reserved	Ignore when read	RO	Reserved to 0	
10	Link Partner's 1000BASE-T Half Duplex Capability	1: Link Partner is capable of 1000BASE-T half duplex 0: Link Partner is not capable of 1000BASE-T half duplex	RO	0	0
11	Link Partner's 1000BASE-T Full Duplex Capability	1: Link Partner is capable of 1000BASE-T full duplex 0: Link Partner is not capable of 1000BASE-T full duplex	RO	0	0
12	Remote Receiver Status	1: Remote Receiver OK 0: Remote Receiver Not OK	RO	0	0
13	Local Receiver Status	1: Local Receiver OK 0: Local Receiver Not OK	RO	0	0
14	MASTER/SLAVE Configuration Resolution	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	RO	0	0
15	MASTER/SLAVE Configuration Fault	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	RO SC	0	0

5.1.12 Extended Status Register (Page0 Reg15)

Bit	Name	Description	Type	HW Reset	SW Reset
[11:0]	Reserved	Ignore when read	RO	0x000	0x000
12	1000BASE-T Half Duplex	1: Be able to perform half duplex 1000BASE-T 0: Not able to perform half duplex 1000BASE-T	RO	1	1
13	1000BASE-T Full Duplex	1: Be able to perform full duplex 1000BASE-T 0: Not able to perform full duplex 1000BASE-T	RO	1	1
14	1000BASE-X Half Duplex	1: Be able to perform half duplex 1000BASE-X 0: Not able to perform half duplex 1000BASE-X	RO	0	0
15	1000BASE-X Full Duplex	1: Be able to perform full duplex 1000BASE-X 0: Not able to perform full duplex 1000BASE-X	RO	0	0

5.1.13 Specific Control & Status Register 0 (Page0 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
0	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	Pin setting	NA
1	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	Pin setting	NA
[3:2]	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	N/A	N/A
3	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	N/A	N/A
4	MDIX	1: Force MDI when auto-MDIX is disabled 0: Force MDIX when auto-MDIX is disabled	R/W	0	0
5	EN_AUTOMDIX	1: Enable auto-MDIX 0: Disable auto-MDIX	R/W	1	1
6	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	N/A	N/A
7	APS_MODE	1: Enable APS 0: Disable APS	R/W	1	1
[10:8]	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	N/A	N/A
11	LBAS®	1: Enable LBAS® capability 0: Disable LBAS® capability *Reference Down_Speed_Select_Enable P2R16[11]	R/W	1	1
[15:12]	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.14 Link Status Register (Page0 Reg17)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Type</th><th>HW Reset</th><th>SW Reset</th></tr>
<tr><td>[9:0]</td><td>Reserved</td><td>Ignore when read</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>10</td><td>APS TX Sleep</td><td>1: TX sleep
0: TX wake up</td><td>RO</td><td>N/A</td><td>N/A</td></tr>
<tr><td rowspan="6">11</td><td rowspan="6">MDI/MDIX</td><td colspan="7">0: MDI 1: MDIX</td><td rowspan="6">RO</td><td rowspan="6">N/A</td><td rowspan="6">N/A</td></tr>
<tr><td></td><td colspan="3">MDI</td><td colspan="3">MDIX</td></tr>
<tr><td></td><td>1G</td><td>100M</td><td>10M</td><td>1G</td><td>100M</td><td>10M</td></tr>
<tr><td>MDI 0</td><td>A</td><td>TX</td><td>TX</td><td>B</td><td>RX</td><td>RX</td></tr>
<tr><td>MDI 1</td><td>B</td><td>RX</td><td>RX</td><td>A</td><td>TX</td><td>TX</td></tr>
<tr><td>MDI 2</td><td>C</td><td>---</td><td>---</td><td>D</td><td>--</td><td>--</td></tr>
<tr><td>MDI 3</td><td>D</td><td>---</td><td>---</td><td>C</td><td>--</td><td>--</td></tr>
<tr><td>12</td><td>Link_Duplex</td><td>1: Link at full duplex
0: Link at half duplex
It is valid only if bit 15 is 1.</td><td>RO</td><td>N/A</td><td>N/A</td></tr>
<tr><td>[14:13]</td><td>Link_Speed[1:0]</td><td>2’b00: link at 10Base-Te
2’b01: link at 100Base-TX
2’b10: link at 1000Base-T
2’b11: Reserved
It is valid only if bit 15 is 1</td><td>RO</td><td>N/A</td><td>N/A</td></tr>
<tr><td>15</td><td>Link_Status</td><td>1: link up
0: link down</td><td>RO</td><td>N/A</td><td>N/A</td></tr>
</table>

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.15 INT# Interrupt Control Register 0 (Page0 Reg18)

Bit	Name	Description	Type	HW Reset	SW Reset
[3:0]	Reserved	1=Enable interrupt (INT#) 0=Disable interrupt(INT#)		N/A	N/A
4	INT#_Polarity_Change_En			0	0
5	INT#_Crossover_Change_En			0	0
6	INT#_Duplex_Change_En			0	0
7	Reserved			0	0
8	INT#_False_Carrier_En			1	1
9	INT#_Symbol_Error_En			1	1
10	INT#_Link_Change_En			1	1
11	INT#_Nway_Complete_En			1	1
12	INT#_Page_Received_En			1	1
[14:13]	Reserved			N/A	N/A
15	INT#_Autoneg_Error_En			1	1

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.16 PME# Interrupt Control Register 0 (Page1 Reg18)

Bit	Name	Description	Type	HW Reset	SW Reset
0	PME#_WOL_Arp_Pkt_Det	Must be set WOL_EN enable P512R16 [10] =1 first.	R/W	0	0
1	PME#_WOL_Mymac_Addr_Det			0	0
2	PME#_WOL_Magic_Pkt_Det			0	0
3	PME#_LPI_Mode_Off	1=Enable interrupt (PME#) 0=Disable interrupt (PME#)		0	0
4	PME#_LPI_Mode_On			0	0
[15:5]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.17 INT# Interrupt Status Register 0 (Page0 Reg19)

Bit	Name	Description	Type	HW Reset	SW Reset
[3:0]	Reserved	Read for event status	RO LH	0	0
4	INT#_Polarity_Change			0	0
5	INT#_Crossover_Change			0	0
6	INT#_Duplex_Change			0	0
7	Reserved			0	0
8	INT#_False_Carrier			0	0
9	INT#_Symbol_Error			0	0
10	INT#_Link_Change			0	0
11	INT#_Nway_Complete			0	0
12	INT#_Page_Received			0	0
[14:13]	Reserved			0	0
15	INT#_Autoneg_Error			0	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.18 PME# Interrupt Status Register 1 (Page1 Reg19)

Bit	Name	Description	Type	HW Reset	SW Reset
0	PME#_Arp_Pkt_Det	Read for event status	RO LH SC	0	0
1	PME#_Mymac_Addr_Det			0	0
2	PME#_Magic_Pkt_Det			0	0
3	PME#_LPI_Mode_Off			0	0
4	PME#_LPI_Mode_On			0	0
[15:5]	Reserved	Ignore when read	N/A	N/A	N/A

5.1.19 RX to TX Loopback (Page2 Reg18)

Bit	Name	Description	Type	HW Reset	SW Reset
[7:0]	Reserved	Ignore when read	N/A	N/A	N/A
8	PMA_RX2TX_LPBK	1: Enable PMA Rx to Tx loopback mode, TXD = RXD 0:Normal mode	R/W	0	0
[15:9]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.20 Specific Control & Status Register 1 (Page2 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
[1:0]	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	0x2	1
[3:2]	Reserved	Do not change these bits when need to perform a write activity to other bits of this register	R/W	0x2	1
[10:4]	Reserved	Internal test used	R/W	NA	NA
11	Down Speed 10M Enable	When P0 R16 [11] Enable LBAS® capability is enabled, this bit is used to select down speed. 1: Select 1G -> 100M->10M speed(Default) Down to 100Mbps when 1000Mbps link fails, If 100Mbps still cannot link up, will down the speed to 10Mbps automatically. 0: Select 1G -> 100M speed Down to 100Mbps when 1000Mbps link fails. If 100Mbps still cannot link up, will be unlink	R/W	1	1
[15:12]	Reserved	Internal test used	R/W	NA	NA

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.21 RX counter Control Register (Page5 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
0	RX_CNT_EN	1=Enable RX counter 0=Disable RX counter	R/W	0	NA
[11:1]	Reserved	Ignore when read	R/W	NA	NA
[13:12]	RXERR_CNTDONE_SEL	Select the RX error count done value. 2'b00: 1 2'b01: 255 2'b10: 1026 2'b11: 65535 The interrupt(RXERR_INT_SEL) is triggered that must met the counter of RXERR_CNTDONE_SEL	R/W	0x3	NA
14	RXERR_CNT_REPEAT	1=RX error count rolls over to zero when count down. 0=RX error count keep the value when count down. This bit is set to 0 when RXERR_INT_EN = 1	R/W	1	NA
15	RXERR_CNT_RDCLR_EN	1=RX error count read clear enable 0=RX error count read clear disable	R/W	0	NA

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.22 RX CRC Error Count Register (Page1 Reg17)

Bit	Name	Description	Type	HW Reset	SW Reset
[15: 0]	CRC_ERR_CNT	RX CRC error count	RO	0	NA

5.1.23 RX Packet Count Register (Page2 Reg17)

Bit	Name	Description	Type	HW Reset	SW Reset
[15: 0]	PKT_STS_CNT	RX packet count (include CRC good and error packet)	RO	0	NA

5.1.24 RX Symbol Error Count Register (Page3 Reg17)

Bit	Name	Description	Type	HW Reset	SW Reset
[15: 0]	SYMB_ERR_CNT	RX symbol error count Each symbol error of idle will add the counter by 1. Several symbol errors of one data frame will add the counter by 1	RO	0	NA

5.1.25 Page Select Register (Reg20)

Bit	Name	Description	Type	HW Reset	SW Reset
[9:0]	PAGE_SEL	To select extension page	R/W	0	0
[15:10]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.26 Smart AZ Control Register (Page48 Reg21)

Bit	Name	Description	Type	HW Reset	SW Reset
[14:0]	Reserved	Do not change these bits when need to perform a write activity to other bits of this register.	R/W	N/A	N/A
15	SAZ_EN	Smart AZ Function Enable 1: Enable Smart AZ Function(default) 0: Disable Smart AZ Function	R/W	1	1

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.27 System Spec Control Register 0 (Page512 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
0	COMA_EN	1: Set IP1001C to COMA mode 0: Set IP1001C to normal mode"	R/W	0	0
1	XTAL_RESET_EN	1: Enable crystall reset function 0: Disable crystall reset function Crystall reset function can also be enabled via EFUSE setting."	R/W	0	0
2	BYPASS_mg_model_cfg	1: Bypass mg_model_cfg from switch 0: mg_model_cfg is used"	R/W	0	0
[9:3]	Reserved	Ignore when read	N/A	N/A	N/A
10	INTB_en	1: Enable pin "INTB" function	R/W	1	1
11	WOL_En	Wake on LAN enable 1: Enable WOL event detection 0: Disable WOL event detection	R/W	0	0
12					
13	PMEB_type	0: Open drain and active low. 1: Output type and active high.	R/W	0	0
14	INTB_type	0: Open drain and active low. 1: Output type and active high.	R/W	0	0
15	PMEB_EN	1: Enable pin "PMEB" function	R/W	1	1

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.28 System Spec Control Register 1 (Page512 Reg19)

Bit	Name	Description	Type	HW Reset	SW Reset
[4:0]	Reserved	Ignore when read	N/A	N/A	N/A
5	PHY_AD_ALL_EN	PHY_AD_SET=0 and PHY_AD_ALL_EN=1, IP1001C reply PHY address 0~31.	R/W	0	Retain
[9:6]	Reserved	Ignore when read	N/A	N/A	N/A
8	PAGE_TWICE_EN	"1=Write page register twice when switch page. 0=Write page register once when switch page."	R/W	0	
[13:9]	Reserved	Ignore when read	N/A	N/A	N/A
14	FORCE SAZ CLK ON	1=Force smart AZ clock turn on. 0=Turn off smart AZ clock when function is disabled.	R/W	0	
15	ALL_REPLY_0	1=Reply PHY address zero SMI command no matter what PHY_AD is set. 0=Reply unitary PHY address SMI command based on PHY_AD setting.	R/W	0	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.29 IO Spec Control Register 0 (Page517 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
[15:0]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.30 IO Spec Control Register 1 (Page518 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
[15:0]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.31 IO Spec Control Register 2 (Page519 Reg16)

Bit	Name	Description	Type	HW Reset	SW Reset
[15:0]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.32 MMD Control Register (Page0 Reg13)

Bit	Name	Description	Type	HW Reset	SW Reset
[4:0]	DEVAD	Device Address	R/W	0	0
[13:5]	Reserved	Reserved Write as 0, ignore on read	RO	0	0
[15:14]	Function	00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	R/W	0	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.33 MMD Data Register (Page0 Reg14)

Bit	Name	Description	Type	HW Reset	SW Reset
[15:0]	Address Data	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	R/W	0	0

Example 1, Read 0.3.20 (Read Data from MMD register 3.20 of PHY address 0):

1. Write 0.13 = 0x0003 //MMD DEVAD 3
2. Write 0.14 = 0x0014 //MMD Address 20
3. Write 0.13 = 0x4003 //MMD Data command for MMD DEVAD 3
4. Read 0.14 //Read MMD Data from 0.3.20

Example 2, Write 1.7.60 = 0x3210 (Write 0x3210 Data to MMD register 7.60 of PHY address 1):

1. Write 1.13 = 0x0007 //MMD DEVAD 7
2. Write 1.14 = 0x003C //MMD Address 60
3. Write 1.13 = 0x4007 //MMD Data command for MMD DEVAD 7
4. Write 1.14 = 0x3210 //Write MMD Data 0x3210 to 1.7.60

5.1.34 EEE PCS Control Register (MMD Reg3.0)

Bit	Name	Description	Type	HW Reset	SW Reset
[9:0]	Reserved	Ignore when read	RO	0	N/A
10	Clock stop enable	1 for RGMII RX clock is stopped during LPI mode 0 for RGMII RX clock isn't stopped during LPI mode	R/W	1	N/A
[15:11]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.35 EEE PCS Status Register (MMD Reg3.1)

Bit	Name	Description	Type	HW Reset	SW Reset
[5:0]	Reserved	Ignore when read	N/A	N/A	N/A
6	Clock stop capable	1 for TX MAC may stop the clock during LPI 0 for clock not stoppable	RO	1'	N/A
7	Reserved	Ignore when read	N/A	N/A	N/A
8	RX LPI indication	1 for RX PCS is currently receiving LPI 0 for PCS is not currently receiving LPI	RO	0	N/A
9	TX LPI indication	1 for TX PCS is currently receiving LPI 0 for PCS is not currently received LPI	RO	0	N/A
10	RX LPI received	1 for RX PCS has received LPI 0 for LPI not received	RO/LH	0	N/A
11	TX LPI received	1 for TX PCS has received LPI 0 for LPI not received	RO/LH	0	N/A
[15:12]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.36 EEE Capability Register (MMD Reg3.20)

Bit	Name	Description	Type	HW Reset	SW Reset
0	Reserved	Ignore when read	N/A	N/A	N/A
1	100BASE-TX EEE	1 for EEE is supported for 100BASE-TX 0 for EEE is not supported for 100BASE-TX	RO	1'	N/A
2	1000BASE-T EEE	1 for EEE is supported for 1000BASE-T 0 for EEE is not supported for 1000BASE-T	RO	1	N/A
3	10GBASE-T EEE	1 for EEE is supported for 10GBASE-T 0 for EEE is not supported for 10GBASE-T	RO	0	N/A
4	1000BASE-KX EEE	1 for EEE is supported for 1000BASE-KX 0 for EEE is not supported for 1000BASE-KX	RO	0	N/A
5	10GBASE-KX4 EEE	1 for EEE is supported for 10GBASE-KX4 0 for EEE is not supported for 10GBASE-KX4	RO	0	N/A
6	10GBASE-KR EEE	1 for EEE is supported for 10GBASE-KR 0 for EEE is not supported for 10GBASE-KR	RO	0	N/A
[15:7]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.37 EEE Wake Error Counter Register (MMD Reg3.22)

Bit	Name	Description	Type	HW Reset	SW Reset
[15:0]	Wake_err_count	EEE wake error counter	RO RC	0	0

5.1.38 EEE Advertisement Register (MMD Reg7.60)

Bit	Name	Description	Type	HW Reset	SW Reset
0	Reserved	Ignore when read	N/A	N/A	N/A
1	100BASE-TX EEE	1:for advertise that the 100BASE-TX has EEE capability 0:for Do not advertise that the 100BASE-TX has EEE capability	R/W	0	N/A
2	1000BASE-T EEE	1:for advertise that the 1000BASE-T has EEE capability 0:for Do not advertise that the 1000BASE-T has EEE capability	R/W	0	N/A
3	10GBASE-T EEE	1:for advertise that the 10GBASE-TX has EEE capability 0:for Do not advertise that the 10GBASE-T has EEE capability	RO	0	N/A
4	1000BASE-KX EEE	1:for advertise that the 1000BASE-KX has EEE capability 0:for Do not advertise that the 1000BASE-KX has EEE capability	RO	0	N/A
5	10GBASE-KX4 EEE	1:for advertise that the 10GBASE-KX4 has EEE capability 0:for Do not advertise that the 10GBASE-KX4 has EEE capability	RO	0	N/A
6	10GBASE-KR EEE	1:for advertise that the 10GBASE-KR has EEE capability 0:for Do not advertise that the 10GBASE-KR has EEE capability	RO	0	N/A
[15:7]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.1.39 EEE Link Partner Ability Register (MMD Reg7.61)

Bit	Name	Description	Type	HW Reset	SW Reset
0	Reserved	Ignore when read	N/A	N/A	N/A
1	LP_100BASE-TX EEE	1:for link partner is advertising EEE capability for 100BASE-TX 0:for link partner is not advertising EEE capability for 100BASE-TX	RO	0	0
2	LP_1000BASE-T EEE	1:for link partner is advertising EEE capability for 1000BASE-T 0:for link partner is not advertising EEE capability for 1000BASE-T	RO	0	0
3	LP_10GBASE-T EEE	1:for link partner is advertising EEE capability for 10GBASE-T 0:for link partner is not advertising EEE capability for 10GBASE-T	RO	0	0
4	LP_1000BASE-KX EEE	1:for link partner is advertising EEE capability for 1000BASE-KX 0:for link partner is not advertising EEE capability for 1000BASE-KX	RO	0	0
5	LP_10GBASE-KX4 EEE	1:for link partner is advertising EEE capability for 10GBASE-KX4 0:for link partner is not advertising EEE capability for 10GBASE-KX4	RO	0	0
6	LP_10GBASE-KR EEE	1:for link partner is advertising EEE capability for 10GBASE-KR 0:for link partner is not advertising EEE capability for 10GBASE-KR	RO	0	0
[15:7]	Reserved	Ignore when read	N/A	N/A	N/A

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5.2 Fiber register description

5.2.1 FX PHY 1000BASE-X Control Register(Page 0 Reg 0)

Bit	Name	Description	Type	HW Reset	SW Reset
15	Software Reset		R/W SC	0	0
14	Loopback		R/W	0	0
13	Speed LSB	see the description of P0 R0.6	Desc	Desc	Desc
12	AN Enable	1000BASE-X auto negotiation enable When P0 R0.6=0 and P0 R0.13=1, this bit is read as 0 and unable to write.	Desc	Desc	Desc
11	Power Down		R/W	0	0
10	Isolate		R/W	0	0
9	Restart AN		R/W SC	0	0
8	Duplex	Fiber duplex mode selection Duplex 1 : Full duplex 0 : Half duplex When link up, this bit reflect operating duplex mode.	R/W	Desc	Desc
7	Collision Test		R/W	0	0
6	Speed MSB	Fiber port speed selection Speed [1:0] P0 R0.6 P0 R0.13 0 1 : 100BASE-FX 1 0 : 1000BASE-X other :Invalid When link up, these bits reflect operating speed mode. Set Speed[1:0] to 2'b01 will disable fiber speed auto detection function and force to 100BASE-FX mode.	Desc	Desc	Desc
5	Unidirection		R/W	0	0
4~0			RO	0x00	0x00

5.2.2 FX PHY Status Register (Page 0 Reg 1)

Bit	Name	Description	Type	HW Reset	SW Reset
15	100BASE-T4		RO	0	0
14	100BASE-X Full	Read as 1 when P0 R0.6=0 and P0 R0.13=1 Read as 0 when P0 R0.6=1 and P0 R0.13=0	RO	Desc	Desc
13	100BASE-X Half	Read as 1 when P0 R0.6=0 and P0 R0.13=1 Read as 0 when P0 R0.6=1 and P0 R0.13=0	RO	Desc	Desc
12	10BASE-T Full		RO	0	0
11	10BASE-T Half		RO	0	0
10	100BASE-T2 Full		RO	0	0
9	100BASE-T2 Half		RO	0	0
8	Extended Status	Read as 1 when P0 R0.6=1 and P0 R0.13=0 Read as 0 when P0 R0.6=0 and P0 R0.13=1	RO	Desc	Desc
7	Unidirection Ability		RO	1	1
6	MF Preamble Suppression		RO	1	1
5	AN Complete		RO	0	0
4	Remote Fault		RO LH	0	0
3	AN Ability	Read as 1 when P0 R0.6=1 and P0 R0.13=0 Read as 0 when P0 R0.6=0 and P0 R0.13=1	RO	Desc	Desc
2	Link Status		RO LL	0	0
1	Jabber Detect		RO	0	0
0	Extended Capability		RO	1	1

5.2.3 FX PHY Identifier Register (Page 0 Reg 2)

Bit	Name	Description	Type	HW Reset	SW Reset
15~0	OUI[3:18]	ICPlus's OUI is 0x0090C3	RO	0x0243	0x0243

5.2.4 FX PHY Identifier Register (Page 0 Reg 3)

Bit	Name	Description	Type	HW Reset	SW Reset
15~10	OUI[19:24]		RO	0x03	0x03
9~4	Model Number		RO	0x05	0x05
3~0	Revision Number		RO	0x0	0x0

5.2.5 FX PHY 1000BASE-X AN Advertisement Register (Page 0 Reg 4)

Bit	Name	Description	Type	HW Reset	SW Reset
15	Next Page		R/W	0	0
14			RO	0	0
13~12	Remote Fault		R/W	0x0	0x0
11~9			RO	0x0	0x0
8	ASM_DIR		R/W	1	1
7	Pause		R/W	1	1
6	Half Duplex	In IP1001C (media converter mode) this bit is read as 0 and unable to write.	Desc	Desc	Desc
5	Full Duplex	In IP1001C (media converter mode) this bit is read as 1 and unable to write. When P256 R4.6 set to 0 this bit is read as 1 and unable to clear	Desc	Desc	Desc
4~0			RO	0x00	0x00

5.2.6 FX PHY1000BASE-X AN Link PartnerAbility Base PageRegister(Page0Reg 5)

Bit	Name	Description	Type	HW Reset	SW Reset
15	Next Page		RO	0	0
14	ACK		RO	0	0
13~12	Remote Fault		RO	0x0	0x0
11~9			RO	0x0	0x0
8	ASM_DIR		RO	0	0
7	Pause		RO	0	0
6	Half Duplex		RO	0	0
5	Full Duplex		RO	0	0
4~0			RO	0x00	0x00

5.2.7 FX PHY 1000BASE-X AN Expansion Register (Page 0 Reg 6)

Bit	Name	Description	Type	HW Reset	SW Reset
15~4			RO	0x000	0x000
3	LP NP Able		RO	0	0
2	Local NP Able		RO	1	1
1	Page Received		RO/LH	0	0
0	LP AN Able		RO	0	Retain

5.2.8 FX PHY 1000BASE-X AN Next Page Transmit Register (Page 0 Reg 7)

Bit	Name	Description	Type	HW Reset	SW Reset
15	Next Page		R/W	0	0
14			RO	0	0
13	Message Page		R/W	1	1
12	ACK2		R/W	0	0
11	Toggle		RO	0	Retain
10~0	Message/ Unformatted Field		R/W	0x001	0x001

5.2.9 FX PHY 1000BASE-X Link Partner Ability Next Page Register (Page 0 Reg 8)

Bit	Name	Description	Type	HW Reset	SW Reset
15	Next Page		RO	0	0
14	ACK		RO	0	0
13	Message Page		RO	0	0
12	ACK2		RO	0	0
11	Toggle		RO	0	0
10~0	Message/ Unformatted Field		RO	0x000	0x000

5.2.10 FX PHY 1000BASE-X Extended Status Register (Page 0 Reg 15)

Bit	Name	Description	Type	HW Reset	SW Reset
15	1000BASE-X Full	Read as 1 when P256 R0.6=1 and P256 R0.13=0 Read as 0 when P256 R0.6=0 and P256 R0.13=1	RO	Desc	Desc
14	1000BASE-X Half	Read as 1 when P256 R0.6=1 and P256 R0.13=0 Read as 0 when P256 R0.6=0 and P256 R0.13=1	RO	Desc	Desc
13	1000BASE-T Full		RO	0	0
12	1000BASE-T Half		RO	0	0
11~0			RO	0x000	0x000

5.2.11 FX PHY Spec Control Register 2 (Page 2 Reg 16)

Bit	Name	Description	Type	HW Reset	SW Reset
15	FX_SPEED _AUTO_DET	1=Enable fiber speed auto detection 0=Disable fiber speed auto detection When set P0 R0.6=0 and P0 R0.13=1, this bit is read as 0 and unable to write.	Desc	Desc	Desc
14	FX_SPEED _MODE	1=100BASE-FX is selected when fiber speed auto detection is disabled 0=1000BASE-X is selected when fiber speed auto detection is disabled When set P0 R0.6=0 and P0 R0.13=1, this bit is read as 1 and unable to write.	Desc	Desc	Desc
13	FX100_SDON_ DIS	1=Disable SdOn link in 100BASE-FX 0=Enable SdOn link in 100BASE-FX	R/W	0	Retain
12	FX100_LOCKO N _DIS	1=Disable LockOn link in 100BASE-FX 0=Enable LockOn link in 100BASE-FX	R/W	0	Retain
11	RL_ERR_RND _TMR_SEL	RL_ERR_RND_TMR_DONE 1=6.4ms~12ms 0=0~5.6ms	R/W	0	Retain
10~9			RO	0	
8	FX100_SPEED _UP	1=100BASE-FX speed up mode 0=100BASE-FX normal mode	R/W	0	Retain
7	FX100_FORCE _LINK	1=Force 100BASE-FX link up	R/W	0	Retain
6	100FX _REPEATER	1=Set 100BASE-FX to repeat mode	R/W	1	Retain
5	FX100_FEF _DIS	1=Disable 100BASE-FX FEF 0=Enable 100base-FX FEF	R/W	0	Retain
4	FX100_BYPAS S_4B5B	1=Bypass 100BASE-FX 4B/5B	R/W	0	Retain
3	FX100_BYPAS S_DSP_RST	1=Bypass 100BASE-FX DSP reset	R/W	0	Retain
2	FX100_ODD_ PREAM_COMP	1=Compensate odd preamble in 100BASE-FX RX	R/W	1	Retain
1~0			RO	0	Retain

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	.....	-0.1V to 3.63V
Input Voltage	.....	-0.1V to 3.63V
Output Voltage	.....	-0.1V to 3.63V
Storage Temperature	.....	-65°C to 150°C
Ambient Operating Temperature (Ta)		0°C to 70°C
IC Junction Temperature (Tj)		0°C to 125°C

6.2 AC Characteristics

6.2.1 Reset, Clock and Power Source

Table 4 Reset, Clock and Power Source Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{clk_lead}	X1 clock valid period before reset released.	10	-	-	ms
T_{rst}	Reset period.	10	-	-	ms
T_{diff}	Time difference between AVDD33 and AVDD10/DVDD10			TBD	ms
T_{pwr_lead}	All power source ready before reset released.	11			ms

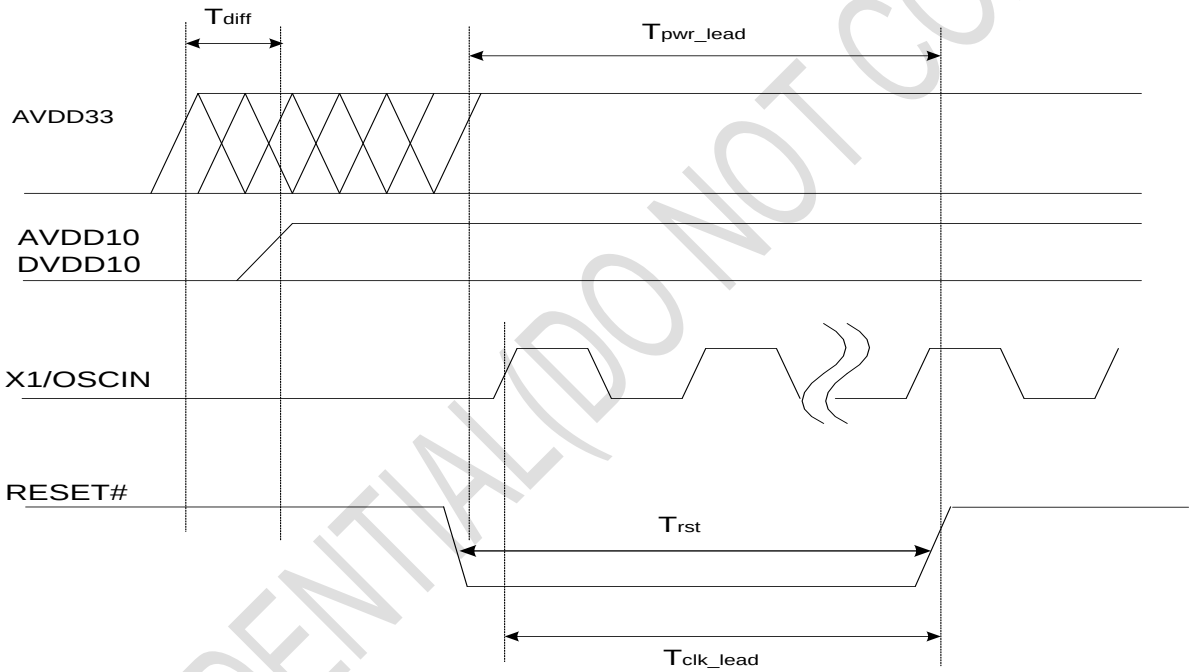


Figure 5 Reset, Clock and Power Source Timing Requirements

6.2.2 RGMII Timing

a. Transmit Timing Requirements

Table 5 RGMII Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TX_CLK}	Period of transmit clock in Giga mode.	-	8	-	ns
T_{TX_CLK}	Period of transmit clock in 100M mode.	-	40	-	ns
T_{TX_CLK}	Period of transmit clock in 10M mode.	-	400	-	ns
T_{s0}	TXEN, TXD to TXC setup time.	1.0	2.0		ns
T_{h1}	TXEN, TXD to TXC hold time.	1.0	2.0		ns

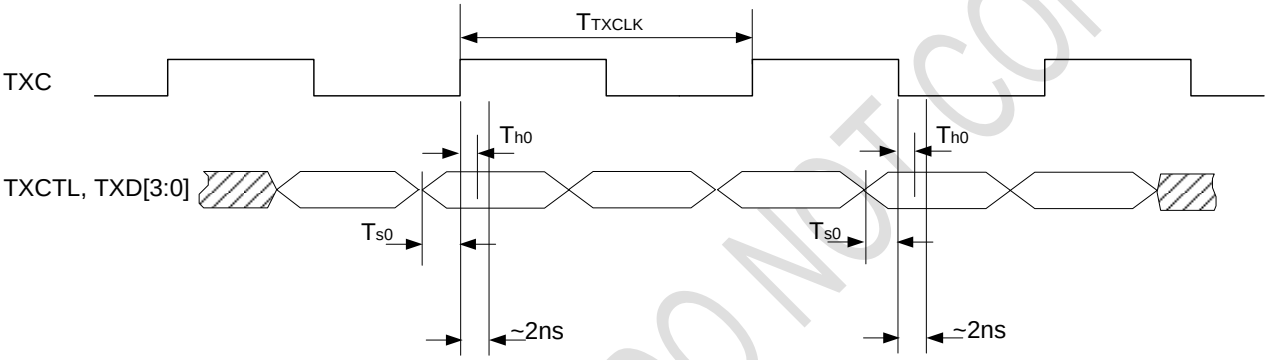


Figure 6 RGMII Transmit Timing Requirements

b. Receive Timing

Table 6 RGMII Receive Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk3}	Period of receive clock in Giga mode.	-	8	-	ns
T_{Rclk3}	Period of receive clock in 100M mode.	-	40	-	ns
T_{Rclk3}	Period of receive clock in10M mode.	-	400	-	ns
T_{d3}	RXC edge to RXCTL, RXD. (RXPHASE_SEL=0, no clock delay added.)	-0.5	0	0.5	ns
	RXC edge to RXCTL, RXD. (RXPHASE_SEL=1, clock delay added.)	1.5	2	2.5	ns

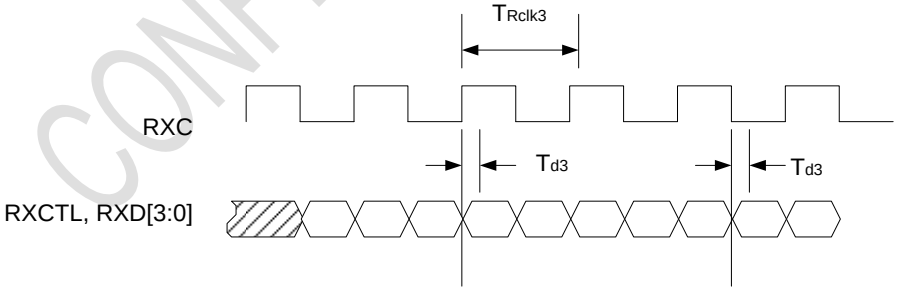


Figure 7 RGMII Receive Timing Specifications

6.2.3 MII TimingTransmit

Table 7 MII Transmit Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{sTxClk}	TXEN, TXD to MII_TXCLK setup time	10	-	-	ns
T_{htxClk}	TXEN, TXD to MII_TXCLK hold time	5	-	-	ns

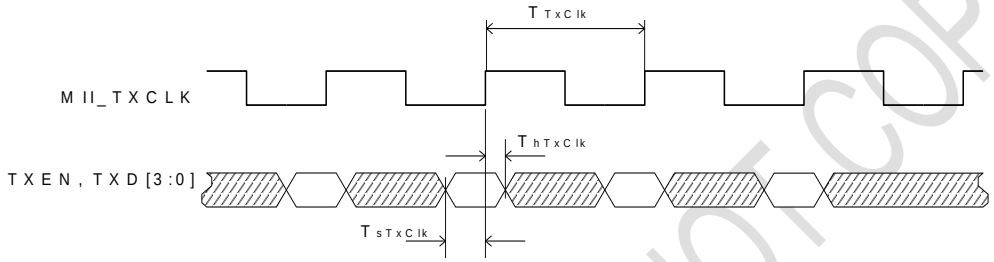
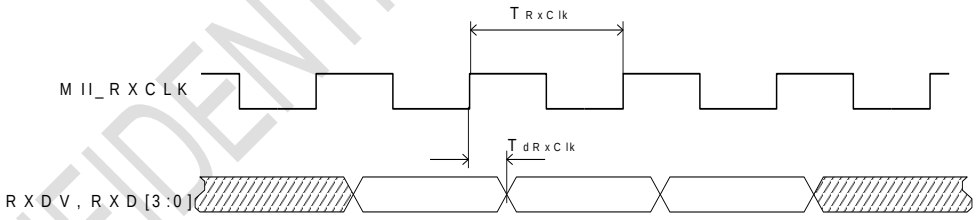


Table 8 MII Receive Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{dRxClk}	MII_RXCLK rising edge to RXDV, RXD	5	-	22	ns



6.2.4 EEPROM Timing

Table 9 RX data cycle Specifications

EEPROM Timing Rx Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	EEDAT to EECLK setup time	20	-	-	ns
T_{hSCL}	EEDAT to EECLK hold time	20	-	-	ns

Read Data Cycle

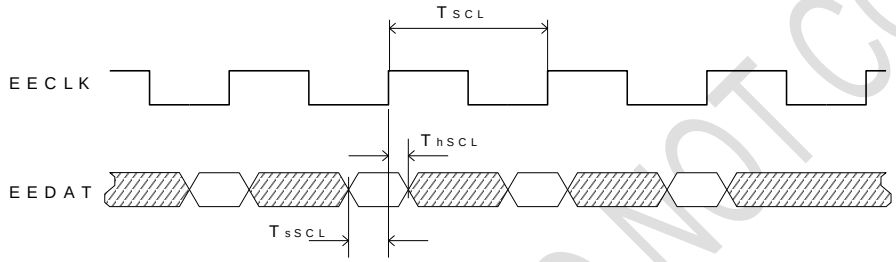
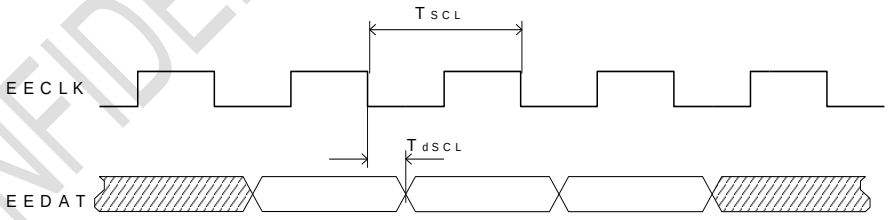


Table 10 Command cycle Specifications

EEPROM Timing Tx Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	EECLK falling edge to EEDAT	-	-	5200	ns

Command Cycle



6.2.5 SMI Timing

MDC/MDIO Timing Requirements

Table 11 SMI Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time.	180	-	-	ns
T_{cl}	MDC Low Time.	180	-	-	ns
T_{cm}	MDC period.	400	-	-	ns
T_{md}	MDIO output delay (read from PHY).	5	-	15	ns
T_{mh}	MDIO setup time (write to PHY).	10	-	-	ns
T_{ms}	MDIO hold time (write to PHY).	10	-	-	ns

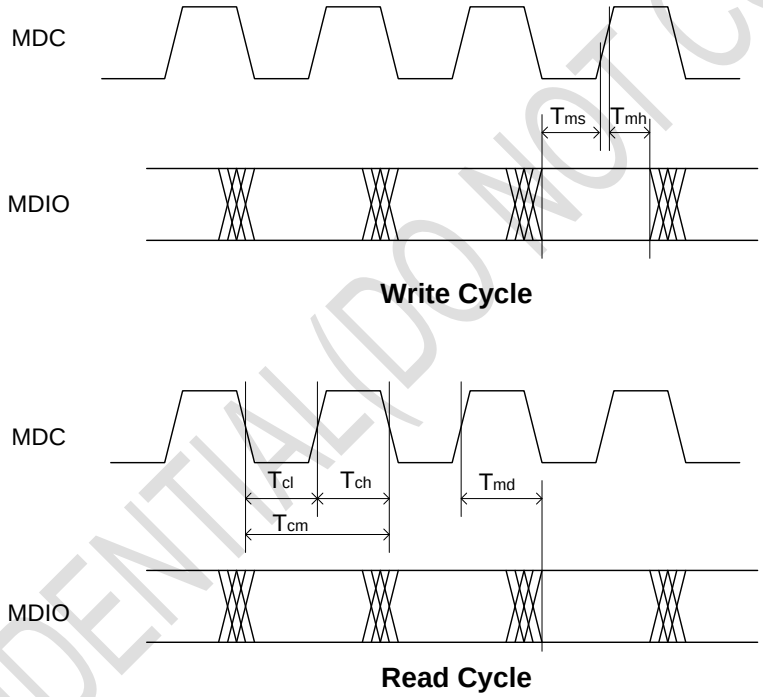


Figure 8 SMI Timing Requirements

6.3 DC Characteristics

6.3.1 DC Characteristic

Table 12 DC Characteristic

Symbol	Description	Minimum	Typical	Maximum	Remark
AVDD33	Supply voltage of analog circuit	3.2V	3.3V	3.63V	
AVDD10	Supply voltage of analog circuit	---	1.08V	---	
DVDD10	Supply voltage of digital circuit	---	1.08V	---	
DVDD_IO_3.3V	I/O_3.3V supply voltage	2.97V	3.3V	3.63V	The I/O voltage of both IP1001C and MAC come from the same power source.
DVDD_IO_2.5V	I/O_2.5V supply voltage	2.25V	2.5V	2.75V	
DVDD_IO_1.8V	I/O_1.8V supply voltage	1.8V		2.0V	

6.3.2 Crystal Specifications

Table 13 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Frequency Tolerance at 25℃	+/- 25 ppm
3	Temperature Characteristics	+/- 25 ppm
4	Operating Temperature Range	0℃ ~ +70℃
5	Load Capacitance	20 pF, or Specify
6	Equivalent Series Resistance	40 ohm Max.
7	Shunt Capacitance	7 pF Max
8	Insulation Resistance	Mega ohm Min./DC 100V
9	Aging Rate A Year	+/- 5 ppm/year

6.3.3 I/O Electrical Characteristics table

Table 14 I/O Electrical Characteristics

Symbol	Specific Name	Minimum	Typical	Maximum
I/O_3.3V	VIH (Input High Voltage)	2.5	---	---
	VIL (Input Low Voltage)	---	---	1.32
I/O_2.5V	VIH (Input High Voltage)	2.0	---	---
	VIL (Input Low Voltage)	---	---	1
I/O_1.8V	VIH (Input High Voltage)	1.7	---	---
	VIL (Input Low Voltage)	---	---	0.8
I/O (3.3V/2.5V/1.8V)	VOH (Output High Voltage)	0.9*DVDD_IO	---	---
	VOL (Output Low Voltage)	---	---	0.1*DVDD_IO
LED/ CLK_OUT	VOH (Output High Voltage)	0.9*DVDD33	---	---
	VOL (Output Low Voltage)	---	---	0.1*DVDD33
X1/OSC	VIH (Input High Voltage)	0.8* DVDD33	---	3.3V +0.5V
	VIL (Input Low Voltage)	-0.5V	---	0.2*DVDD33
RESET#	VIH (Input High Voltage)	0.8*DVDD33	---	---
	VIL (Input Low Voltage)	---	---	0.2*DVDD33

6.3.4 I/O internal pull high/low resistance

DVDD_IO	Pull-high	Pull-low
1.8V	184k ohm	185k ohm
2.5V	241k ohm	253k ohm
3.3V	303k ohm	325k ohm

*According DVDD_IO Voltage different, with different I/O internal resistance

6.3.5 Power consumption table of Green Power

Item	Mode	1000BASE-T (@25 °C)
1	Active	TBD
2	802.3az LPI	TBD
3	Smart EEE LPI	TBD
4	Auto Power Saving	TBD

6.3.6 Thermal Data

Table 15 Thermal Data

Theta Ja	Theta Jc	Conditions	Units
55	12.8	2 Layer PCB	°C/W
24.8	10.7	4 Layer PCB	°C/W

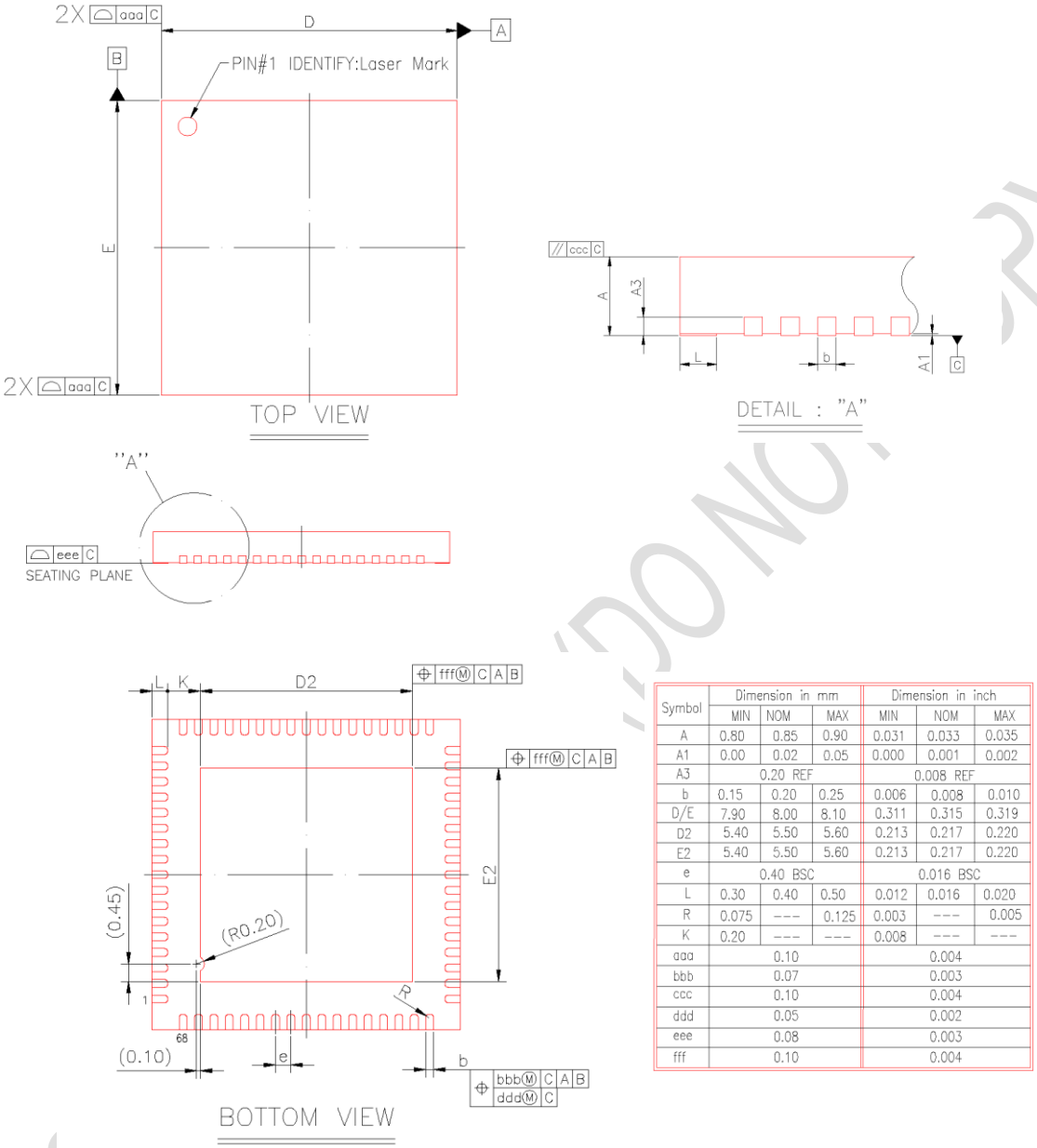
We present the thermal resistance on 2L/4L JEDEC PCB using Finite Element Molding (FEM) method

7. Order Information

Table 16 Part Number and Package

Part No.	Package	Notice
IP1001C	68Pin QFN	

8. Package Outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.90	8.00	8.10	0.311	0.315	0.319
D2	5.40	5.50	5.60	0.213	0.217	0.220
E2	5.40	5.50	5.60	0.213	0.217	0.220
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	0.125	0.003	---	0.005
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Figure 9 68-PIN QFN Dimension

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