24+1-port Management Switch Controller with 24 PHYs inside (SOC_90nm, Green & Management)

Features

- 25 Ports 10/100Mb Ethernet Layer 2 Smart Switch
  - Built-in 24 PHYs
  - One MII interface
- Store & Forward, Share Memory Non_blocking Architecture
  - Built-in 2.5Mb SRAM (1.75Mb for packet buffer)
  - Max. length 1664B
- Wire-speed Operation On Every Port
- Head Of Line Blocking Prevention
- Flow Control Support
  - 802.3x compliant flow control in full duplex
  - Collision/Carrier_snese based backpressure in half duplex
- Internal 8K MAC Address Entities
  - CRC/direct hashing algorithm
  - Aging timer programmable (55s~251.6hr) < 4 %
  - Wire speed address learning and resolution
  - CPU accessible for security and static MAC
  - Learning enable/disable
- Sniffer Function Support (in/out/in+out)
- IGMP Snooping Support
  - Version 1 , 2
  - Snooping by Switch ASIC or external CPU
- Two Trunk Group Support
  - Two trunk groups, each trunk has 4 ports (max)
  - The ports belong to trunk group are configurable
  - Load balance based on (Port ID, DA , SA, DA/SA)
  - Link fault recovery
- VLAN (32 VLAN groups)
  - Port based
  - Tagged based
  - Tag remove/add/modify support
  - Special TAG support
  - Protected VLAN
  - Q-in-Q (double tag) support
- Class Of Service (CoS) Support
  - Port based
  - 802.1Q priority based tagged based
  - IP TOS based (IPv4/IPv6)
  - TCP/UDP port number based
  - Destination MAC address based
  - IP address based
  - 4 levels per port
  - WRR/FIFS/SP/SP+WRR
  - ACL based
- Broadcast Storm Control
  - Broadcast rate control per port selectable
  - With option to drop all ARP to CPU
  - Also has ARP and ICMP storm control
- Multi-cast/unknown DA frames can be counted
- Port Security
  - MAC based
  - IP(DIP/SIP) based (IPv4 32 bit only)
  - TCP/UDP port based
  - Port based
- Bandwidth Control
  - 32K bpsxN 256 levels
  - 512K bpsxN 256 levels
  - With flow control/Without flow control
  - WAN port control support
- Support SMI Interface Auto-polling
  - Speed, Duplex, Flow control, Link
  - CPU accessible (interrupt support)
  - CPU R/W PHY register
- Out Queue Aging Function
  - From 100 ms to 6.3 sec selectable
- Spanning Tree Protocol Port State Support
  - Discard/Block/Learning/Forwarding four states support
  - Forwarding STP frame to CPU port
  - RSTP support
- Support 16 ACL Entities Based On
  - Ingress port or VLAN
  - Destination/Source IP (specific or range)
  - TCP/UDP Destination/Source port number (specific, > 1023, <=1023)
  - Action : forward, to CPU, drop, priority, Q-in-Q tag
- Configuration
  - Pin initial setting
  - 2-wire serial interface for configuration EEPROM
  - 2-wire serial interface for low cost smart system application
- Per Port 2 Counter (32 bit x 2) Selectable
  - RX/TX packet count
  - CRC error packet count
  - Drop packet count
  - Collision count
- LED
  - Direct mode
  - 2-wire serial mode
- Support Auto Test Function For Mass-production
  - Auto generate test frames
  - Shown the result on LED output
- Interrupt Pin For PHY Mode/Link/SMI R/W
  - Complete notification
- Build-in SRAM Self Test (BIST)
- Build-in Oscillator Circuit, Only One 25 MHz Crystal Needed
- IO Voltage Selectable (3 groups)
- 90 nm Process, 208 Pin EDHS-QFP

General Description

The IP1725 is a cost effective and fully integrated single chip. It integrates a 25-port switch controller, an 3X octal PHY transceiver and SSRAM. Each of PHY transceiver complies with 802.3u specification and HP-license Auto MDI/MDIX.

It supports full smart switch functions, including IGMP snooping, 4 priority queues, TOS, TCP/UDP port number priority, 802.1Q VLAN, port security, protocol filter/forwarding and bandwidth control.

Table of Contents

List of Tables

List of Figures

Revision History

Revision #	Change Description
IP1725-DS-R00	Initial release
IP1725-DS-R01	1. Add 802.1D Reserved Group mode selection (page 19/22/73) 2. Add Thermal resistor value (page 102)
IP1725-DS-R02	1. Modify I/O Electrical Characteristics (page 102) 2. Modify Power On Sequence and Reset Timing (page 105) 3. Add Thermal Data (page 108)
IP1725-DS-R03	1. Modify Power On Sequence and Reset Timing (page 105) 2. Add SCAN_MODE and SELF_TEST description (page 17) 3. Modify Input Clock (page 102/107) 4. Modify MII Pin Description (page 15/16) 5. Modify MII Interface (page 26/27) 6. Modify MII Timing (page 105/106) 7. Modify EEPROM Interface (page 30) 8. Add Auto MDI/MDIX Description (page 63/71) 9. Modify Switch Register EEPROM Map (page 73)
IP1725-DS-R04	1. Add VID Tag Based priority (page 43) 2. Modify Pin Description for pin 120/143/144 in Table 11 (page 19/20) 3. Add QoS priority description for pin 143/144 in Table 11 (page 20) 4. Add Strict Priority description for 2/4 queues mode in Table 26 (page 42) 5. Add 2 queues mode description for Strict Priority in Table 27/28 (page 42/43) 6. Add I/O input voltage V_{IH}, V_{IL} description for I/O Electrical Characteristics (page 106) 7. Add junction temperature value (page 105/113) 8. Add OSCI(X1) input voltage range value (page 106) 9. Add priority description between TCP/UDP Port Number and User-define Port Number (page 45/51) 10.Modify description for pin 149 bcst_control_dis (page 21)
IP1725-DS-R05	1. Modify pin 151 auto_slew description for initial pin setting when direct LED mode (page 21/35) 2. Modify TCP/UDP port number setting for 1863, 4000/8000, 5190 and 5050 (page 78/79/80) 3. Add PHY Spec. Control Register (page 71) 4. Modify description for register 0x82[13] (page 95) 5. Modify Figure 18 TCP/UDP Port Number Based Priority Selection Table (page 46) 6. Modify description for rg_xen_on (page 19) 7. Modify core voltage Maximum (page 106) 8. Modify description for Restart Auto-Negotiation (page 65) 9. Swap PHY/MAC mode register description (page 26, 15, 16) 10. Add description for to CPU and drop of TCP/UDP port number are global setting. (page 79, 80) 11. Pin Diagram pin 80 modify (page 12) 12. Add PHY Management Timing (page 111) 13. Add MII speed and duplex description (page 26) 14. Modify External Clock Specifications (page 114) 15. Modify DVDD supply voltage (page 107)
IP1725-DS-R06	Add a few detail value for power on sequence (page 112)

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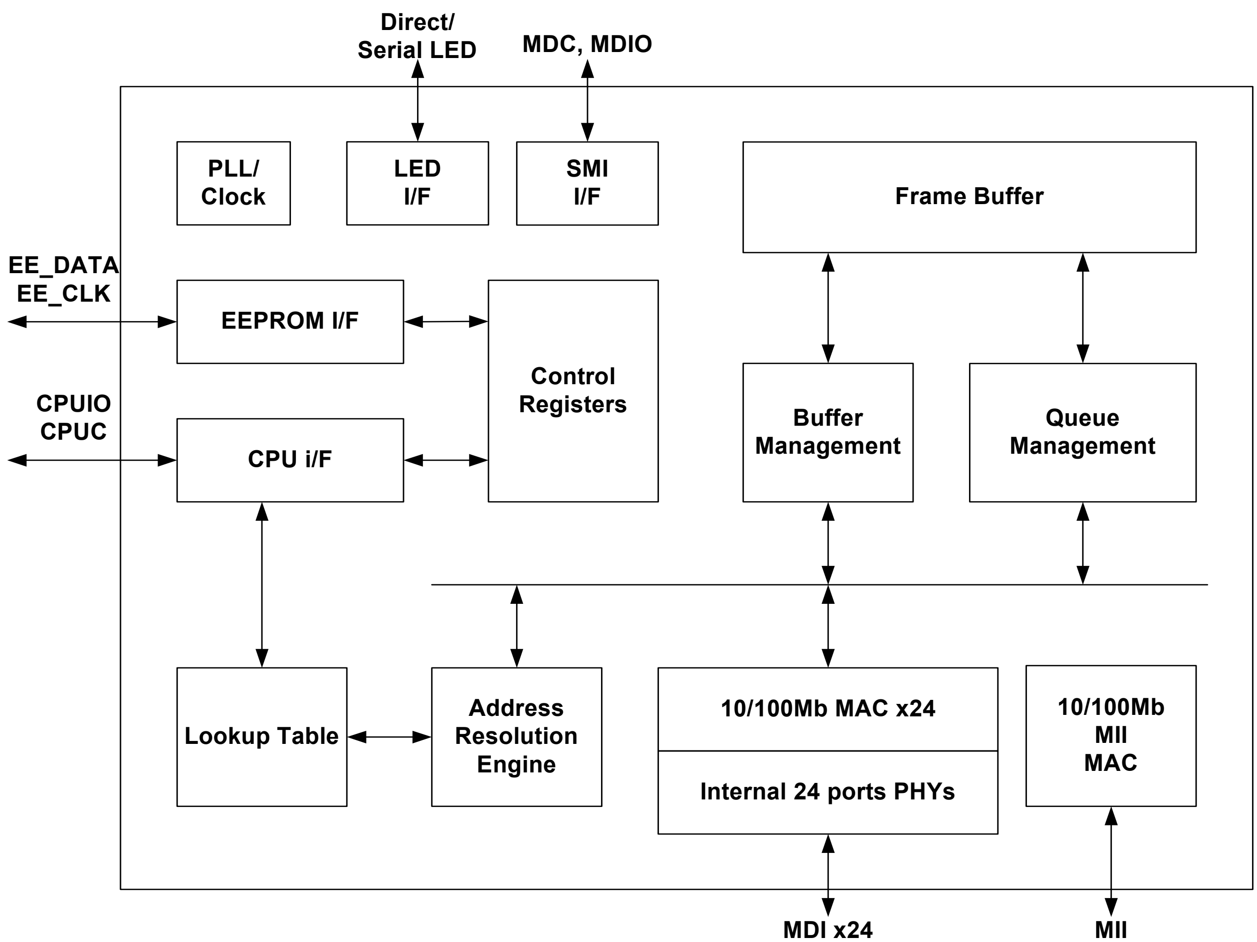
1 Block Diagram

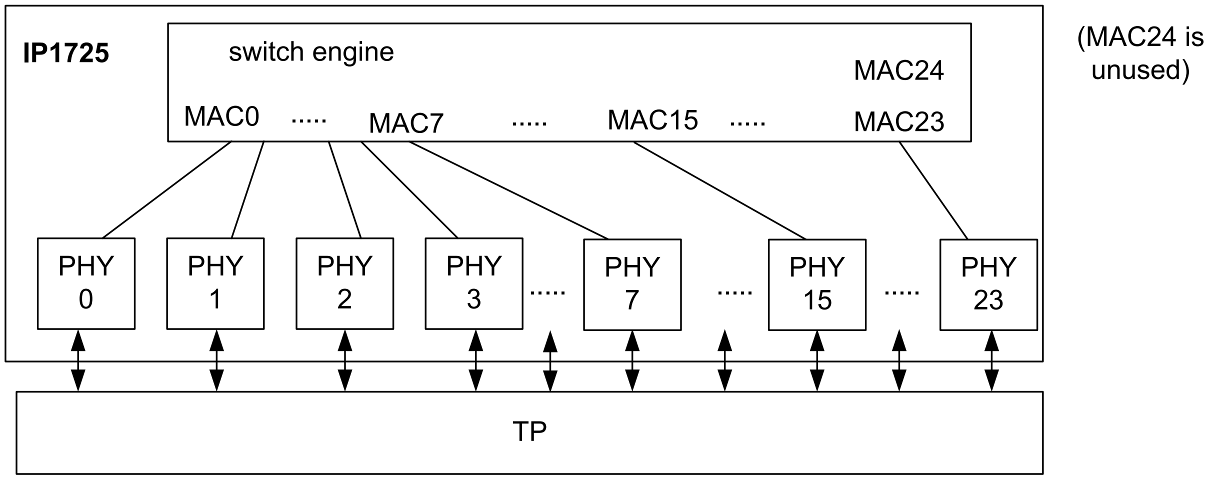
Figure 1 Block Diagram



2 Application Diagram

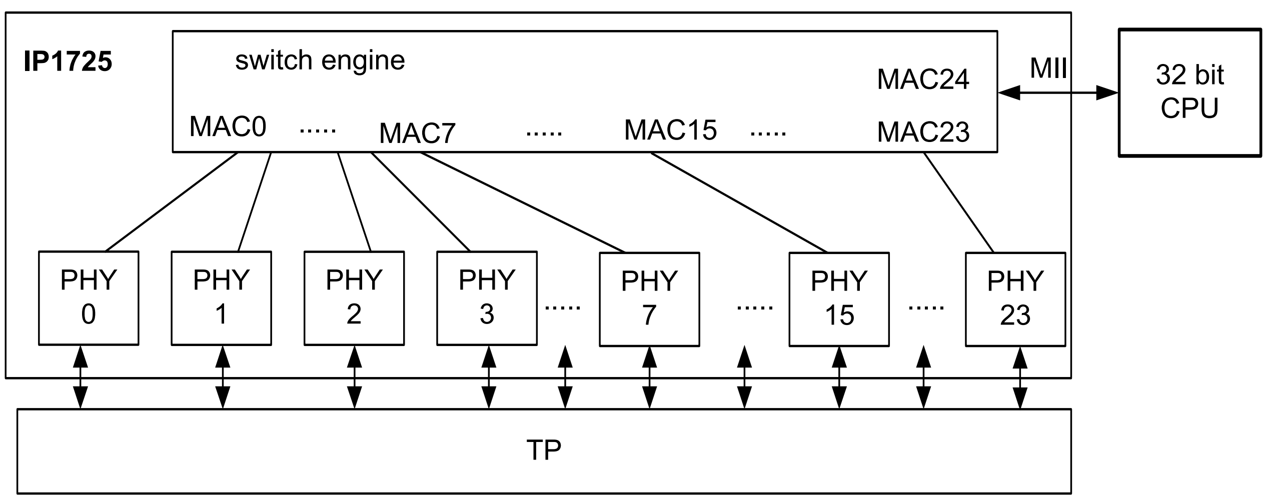
2.1 Dumb Switch Application

Figure 2 Dumb Switch Application



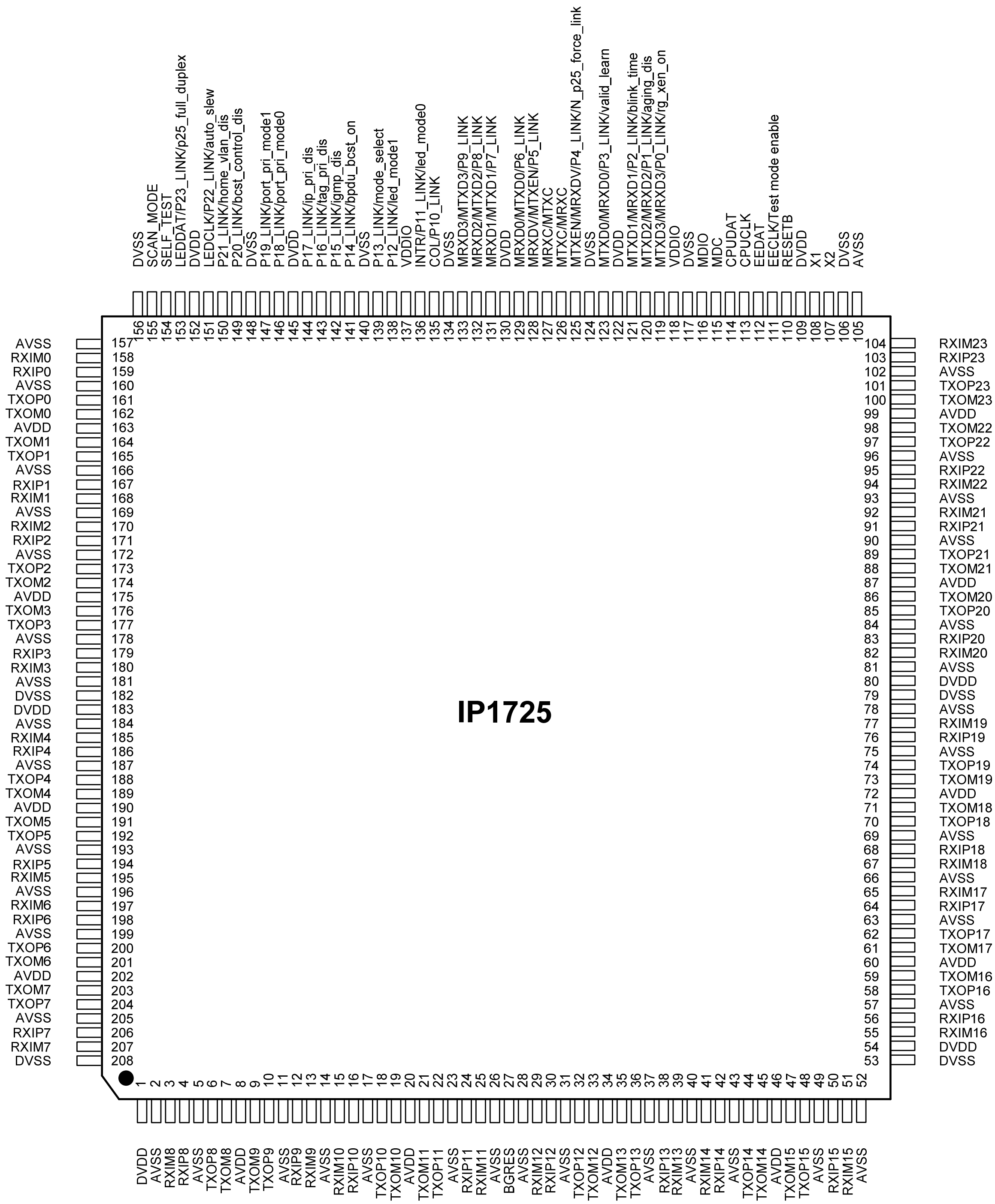
2.2 Smart/Management Switch Application

Figure 3 Smart/Management Switch Application



3 Pin Diagram

Figure 4 Pin Diagram



4 Pin Description

Table 1 Pin Symbol Abbreviations

Type	Description	Type	Description
I	Input pin	IL	Input latched upon reset
O	Output pin	PD	Pulled down with internal resistor
I/O	Bi-direction input/output	PU	Pulled up with internal resistor
P	Power or ground		

4.1 MDI Pin Description

Table 2 MDI Pin

Pin No.	Label	Type	Description
161 162 159 158	TXOP0 TXOM0 RXIP0 RXIM0	O O I I	**Port 01 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 01. Auto MDI/MDIX can reverse the pairs TXOP0/TXOM0 and RXIP0/RXIM0.
165 164 167 168	TXOP1 TXOM1 RXIP1 RXIM1	O O I I	**Port 02 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 02. Auto MDI/MDIX can reverse the pairs TXOP1/TXOM1 and RXIP1/RXIM1.
173 174 171 170	TXOP2 TXOM2 RXIP2 RXIM2	O O I I	**Port 03 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 03. Auto MDI/MDIX can reverse the pairs TXOP2/TXOM2 and RXIP2/RXIM2.
177 176 179 180	TXOP3 TXOM3 RXIP3 RXIM3	O O I I	**Port 04 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 04. Auto MDI/MDIX can reverse the pairs TXOP3/TXOM3 and RXIP3/RXIM3.
188 189 186 185	TXOP4 TXOM4 RXIP4 RXIM4	O O I I	**Port 05 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 05. Auto MDI/MDIX can reverse the pairs TXOP4/TXOM4 and RXIP4/RXIM4.
192 191 194 195	TXOP5 TXOM5 RXIP5 RXIM5	O O I I	**Port 06 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 06. Auto MDI/MDIX can reverse the pairs TXOP5/TXOM5 and RXIP5/RXIM5.
200 201 198 197	TXOP6 TXOM6 RXIP6 RXIM6	O O I I	**Port 07 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 07. Auto MDI/MDIX can reverse the pairs TXOP6/TXOM6 and RXIP6/RXIM6.
204 203 206 207	TXOP7 TXOM7 RXIP7 RXIM7	O O I I	**Port 08 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 08. Auto MDI/MDIX can reverse the pairs TXOP7/TXOM7 and RXIP7/RXIM7.

Pin No.	Label	Type	Description
6 7 4 3	TXOP8 TXOM8 RXIP8 RXIM8	O O I I	**Port 09 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 09. Auto MDI/MDIX can reverse the pairs TXOP8/TXOM8 and RXIP8/RXIM8.
10 9 12 13	TXOP9 TXOM9 RXIP9 RXIM9	O O I I	**Port 10 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 10. Auto MDI/MDIX can reverse the pairs TXOP9/TXOM9 and RXIP9/RXIM9.
18 19 16 15	TXOP10 TXOM10 RXIP10 RXIM10	O O I I	**Port 11 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 11. Auto MDI/MDIX can reverse the pairs TXOP10/TXOM10 and RXIP10/RXIM10.
22 21 24 25	TXOP11 TXOM11 RXIP11 RXIM11	O O I I	**Port 12 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 12. Auto MDI/MDIX can reverse the pairs TXOP11/TXOM11 and RXIP11/RXIM11.
32 33 30 29	TXOP12 TXOM12 RXIP12 RXIM12	O O I I	**Port 13 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 13. Auto MDI/MDIX can reverse the pairs TXOP12/TXOM12 and RXIP12/RXIM12.
36 35 38 39	TXOP13 TXOM13 RXIP13 RXIM13	O O I I	**Port 14 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 14. Auto MDI/MDIX can reverse the pairs TXOP13/TXOM13 and RXIP13/RXIM13.
44 45 42 41	TXOP14 TXOM14 RXIP14 RXIM14	O O I I	**Port 15 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 15. Auto MDI/MDIX can reverse the pairs TXOP14/TXOM14 and RXIP14/RXIM14.
48 47 50 51	TXOP15 TXOM15 RXIP15 RXIM15	O O I I	**Port 16 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 16. Auto MDI/MDIX can reverse the pairs TXOP15/TXOM15 and RXIP15/RXIM15.
58 59 56 55	TXOP16 TXOM16 RXIP16 RXIM16	O O I I	**Port 17 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 17. Auto MDI/MDIX can reverse the pairs TXOP16/TXOM16 and RXIP16/RXIM16.
62 61 64 65	TXOP17 TXOM17 RXIP17 RXIM17	O O I I	**Port 18 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 18. Auto MDI/MDIX can reverse the pairs TXOP17/TXOM17 and RXIP17/RXIM17.
70 71 68 67	TXOP18 TXOM18 RXIP18 RXIM18	O O I I	**Port 19 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 19. Auto MDI/MDIX can reverse the pairs TXOP18/TXOM18 and RXIP18/RXIM18.
74 73 76 77	TXOP19 TXOM19 RXIP19 RXIM19	O O I I	**Port 20 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 20. Auto MDI/MDIX can reverse the pairs TXOP19/TXOM19 and RXIP19/RXIM19.

Pin No.	Label	Type	Description
85 86 83 82	TXOP20 TXOM20 RXIP20 RXIM20	O O I I	**Port 21 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 21. Auto MDI/MDIX can reverse the pairs TXOP20/TXOM20 and RXIP20/RXIM20.
89 88 91 92	TXOP21 TXOM21 RXIP21 RXIM21	O O I I	**Port 22 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 22. Auto MDI/MDIX can reverse the pairs TXOP21/TXOM21 and RXIP21/RXIM21.
97 98 95 94	TXOP22 TXOM22 RXIP22 RXIM22	O O I I	**Port 23 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 23. Auto MDI/MDIX can reverse the pairs TXOP22/TXOM22 and RXIP22/RXIM22.
101 100 103 104	TXOP23 TXOM23 RXIP23 RXIM23	O O I I	**Port 24 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 24. Auto MDI/MDIX can reverse the pairs TXOP23/TXOM23 and RXIP23/RXIM23.

4.2 MII Pin Description

Table 3 MII Pin

Pin No.	Label	Type	Description
MII PHY Mode In this mode, LED should be entered serial mode when power on reset and register 0x70[1] is set to '1'.			
135	COL	O	**MII Collision Detect** Collision detect when operation on 10/100 half duplex mode.
125	MRXDV	O	**MII Receive Valid** Transmit data enable that is sent synchronously at the falling edge of MRXC.
123 121 120 119	MRXD0 MRXD1 MRXD2 MRXD3	O	**MII Receive Data Bus** Transmit data output bus that is sent synchronously at the falling edge of MRXC.
128	MTXEN	I	**MII Transmit Enable** Receive data valid that is sent synchronously at the rising edge of MTXC.
129 131 132 133	MTXD0 MTXD1 MTXD2 MTXD3	I	**MII Transmit Data Bus** Receive data input bus that is sent synchronously at the rising edge of MTXC.
126	MRXC	O	**MII Transmit Clock** In 100Mbps, the pin is 25MHz clock input. In 10Mbps, the pin is 2.5MHz clock input.
127	MTXC	O	**MII Receive Clock** In 100Mbps, the pin is 25MHz clock input. In 10Mbps, the pin is 2.5MHz clock input.

Pin No.	Label	Type	Description
MII MAC Mode In this mode, LED should be entered serial mode when power on reset and register 0x70[1] is set to ‘0’.			
135	COL	I	**MII Collision Detect** Collision detect when operation on 10/100 half duplex mode.
125	MTXEN	O	**MII Transmit Enable** Transmit data enable that is sent synchronously at the rising edge of MTXC.
123 121 120 119	MTXD0 MTXD1 MTXD2 MTXD3	O	**MII Transmit Data Bus** Transmit data output bus that is sent synchronously at the rising edge of MTXC.
128	MRXDV	I	**MII Receive Valid** Receive data valid that is sent synchronously at the rising edge of MRXC.
129 131 132 133	MRXD0 MRXD1 MRXD2 MRXD3	I	**MII Receive Data Bus** Receive data input bus that is sent synchronously at the rising edge of MRXC.
126	MTXC	I	**MII Transmit Clock** In 100Mbps, the pin is 25MHz clock input. In 10Mbps, the pin is 2.5MHz clock input.
127	MRXC	I	**MII Receive Clock** In 100Mbps, the pin is 25MHz clock input. In 10Mbps, the pin is 2.5MHz clock input.

4.3 SMI Pin Description

Table 4 SMI Pin

Pin No.	Label	Type	Description
115	MDC	O	**Serial management bus clock output** It’s recommended to add a 30pF capacitor to ground for noise filtering.
116	MDIO	I/O	**Serial management bus data input/output** It’s recommended to add a 4.7K ohm pull up resistor connecting to 3.3V VCC and a 30pF capacitor connecting to ground.

4.4 EEPROM Pin Description

Table 5 EEPROM Pin

Pin No.	Label	Type	Description
111	EECLK	O	**Serial EEPROM clock output**
112	EEDAT	I/O	**Serial EEPROM data input/output**

4.5 CPU Pin Description

Table 6 CPU Pin

Pin No.	Label	Type	Description
113	CPUCLK	I	**Serial CPU access clock input**
114	CPUDAT	I/O	**Serial CPU data input/output**

4.6 Serial LED Pin Description

Table 7 Serial LED Pin

Pin No.	Label	Type	Description
151	LEDCLK	O	**Serial LED clock output**
153	LEDDAT	I/O	**Serial LED data input/output**

4.7 Direct LED Pin Description

Table 8 Direct LED Pin

Pin No.	Label	Type	Description
119,120, 121,123, 125,128, 129,131, 132,133, 135,136, 138,139, 141,142, 143,144, 146,147, 149,150, 151,153	P0_LINK ~ P23_LINK	O	**Direct LED link/activity for port 01~24** The LED should be connected to 3.3V VCC through a 220 ohm resistor.

4.8 Miscellaneous Pin Description

Table 9 Miscellaneous Pin

Pin No.	Label	Type	Description
108	X1	I	**Crystal/Oscillator 25MHz input**
107	X2	O	**Crystal output**
110	RESETB	I	**System reset (low active)** Should be kept at “low” for at least 10 microseconds. The input voltage should be not higher than VDDIO.

Pin No.	Label	Type	Description
136	INTR	O	**Interrupt output. Active low**
155	SCAN_MODE	I, PD	**Scan mode for testing** 0 : disable (default) 1 : enable If an external pull up resistor is used, it should be connected to VDDIO.
154	SELF_TEST	I, PD	**Self test for switch mass production test** 0 : disable (default) 1 : enable If an external pull up resistor is used, it should be connected to VDDIO. The detail refer to chapter 5.14
27	BGRES	I	**Band gap reference voltage** It must be pull down by 6.19K ohm resistor.

4.9 Power & Ground Pin Description

Table 10 Power & Ground Pin

Pin No.	Label	Type	Description
1,54,80, 109,122, 130,145, 152,183	DVDD	P	**1V power for Core circuit**
8,20,34, 46,60,72, 87,99,163, 175,190, 202	AVDD	P	**1.9V power for analog circuit**
118,137	VDDIO	P	**3.3V power of I/O PAD**
53,79,106, 117,124, 134,140, 148,156, 182,208	DVSS	P	**Core Ground**

Pin No.	Label	Type	Description
2,5,11,14, 17,23,26, 28,31,37, 40,43,49, 52,57,63, 66,69,75, 78,81,84, 90,93,96, 102,105, 157,160, 166,169, 172,178, 181,184, 187,193, 196,199, 205	AVSS	P	**Analog Ground**

4.10 Power on Setting

The state of these pins will be latched upon reset.

Table 11 Power on Setting

Pin No.	Label	Type	Description
111	Test mode enable	IL, PD	**Test mode function** 0 : disable (default) 1 : enable If an external pull up resistor is used, it should be connected to VDDIO.
123	valid_learn	IL, PU	**LUT entry overwrite method select** 0 : write when entry is empty 1 : overwrite (default) The setting can be updated with register 0x8B[8]
121	blink_time	IL, PU	**LED blink time select** 0 : 120 ms 1 : 40ms (default) The setting can be updated with register 0x54[3]
120	oq_aging_dis	IL, PU	**Output queue aging time** 0 : enable 1 : disable (default) The setting can be updated with register 0x44[8]
119	rg_xen_on	IL, PU	**Flow control function** 0 : disable 1 : enable (default) The setting can be updated with registers 0x5B~0x60

Pin No.	Label	Type	Description
125	N_p25_force_link	IL, PU	**Port 25 force link** 0 : port 25 force to link 1 : port 25 is not force to link (default) The setting can be updated with register 0x61[5]
136 138	led_mode0 led_mode1	IL, PU	**LED mode select** led_mdoe1 led_mode0 0 0 : 2-bit serial LED mode 0 1 : 3-bit serial LED mode 1 0 : 3-bit serial bi-color LED mode 1 1 : direct LED mode (default) The setting can be updated with register 0x54[1:0]
139	mode_select	IL, PU	**802.1D Reserved Group mode selection** 0 : special mode 1 : normal mode (default) The function can be updated with register 0x02[12]
141	bpdu_bcst_on	IL, PU	**Broadcast the packet with MAC destination address 01-80-c2-00-00-04~01-80-c2-00-00-0F** 0 : do not broadcast BPDU packets 1 : broadcast BPDU packets (default) The function can be updated with register 0x01[2]
142	igmp_dis	IL, PU	**IGMP function** 0 : enable IGMP function 1 : disable IGMP function (default) The setting can be updated with register 0x94[0].
143	tag_pri_dis	IL, PU	**VLAN Tag base priority for all port** 0 : enable If enable, register 0x22 and 0x23 will be set to 0xFFFF and 0x1FF for all port, and register 0x42 equal to 0x6, register 0x43 equal to 0x1248 1 : disable (default) The setting can be updated with registers 0x22 and 0x23.
144	ip_pri_dis	IL, PU	**IP CoS base priority for all port** 0 : enable If enable, register 0x24 and 0x25 will be set to 0xFFFF and 0x1FF for all port, and register 0x42 equal to 0x6, register 0x43 equal to 0x1248 1 : disable (default) The setting can be updated with registers 0x24 and 0x25.

Pin No.	Label	Type	Description
146 147	port_pri_mode0 port_pri_mode1	IL, PU	**Port priority mode select** port_pri_mdoe1 port_pri_mode0 0 0 : p25 is high priority 0 1 : p01~p04 are high priority 1 0 : p21~p24 are high priority 1 1 : none The setting can be updated with registers 0x1E~0x21
149	bcst_control_dis	IL, PU	**Broadcast storm control for all port** 0 : enable 1 : disable (default) The setting can be updated with registers 0x86 and 0x87.
150	home_vlan_dis	IL, PU	**Home VLAN function** Port 01~24 are all individual VLAN and only send to CPU port. 0 : enable 1 : disable (default) The setting can be updated with registers 0xAD~0xDC.
151	auto_slew	IL, PU	**PAD auto slew rate** 0 : disable 1 : enable (default) If direct LED mode is selected, this pin must be connected to ground through a 4.7K ohm resister. The setting can be updated with register 0x76[3].
153	p25_full_duplex	IL, PU	**Port 25 duplex mode select** 0 : half duplex 1 : full duplex The setting can be updated with register 0x5A[8].

5 Function Description

5.1 Switch Engine and Queue Management

5.1.1 Packet Forwarding

IP1725 utilizes the “store & forward” method to handle packet transfer. IP1725 begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

5.1.2 Address Learning and Hashing

Related registers	0x82[0], 0x8A, 0x8B

IP1725 can handle up to 8192 MAC address entries for 2 layers, 4096 MAC address entries per layer. It provides two kinds of hashing method to maintain the MAC address table. One is the direct mapping and the other is the CRC algorithm. When the direct mapping method is selected, register 0x82[0] is set to “0”. IP1725 recognizes the least significant 12 bits of the MAC address. When the CRC algorithm is used, register 0x82[0] is set to “1” IP1725 uses 48-bit MAC address to hash out 12bits access address.

The MAC address learning function for each port can be either enabled or disabled by setting the registers 0x8A[15:0] and 0x8B[7:0], and all zero pattern with MAC address can choose learning to MAC address table or not by setting register 0x8B[10] if the MAC address learning function is enabled.

IP1725 provide 2 layers LUT table with three methods can be selected. The first method is overwrite LUT even when the entry is valid, which can be enabled by programming register 0x8B[9:8] to ‘00’. The second method is do not overwrite LUT before aging out, which can be enabled by programming register 0x8B[9:8] to ‘01’ or ‘10’. The third method is only overwrite the second layer LUT before aging out, which can be enabled by programming register 0x8B[9:8] to ‘11’.

The packet with any the following conditions will not be stored in MAC address table.

- Erroneous packet
- 802.3x pause packet(option)
- 802.1D Reserved Group packet(option)
- Multicast source MAC address

5.1.3 Aging Time

5.1.3.1 Address Aging

Related registers	0x82[1], 0x89[14:0]

IP1725 supports programmable aging time to meet various system requirements, ranging from 27.6 sec to 904396.8 sec ±3.8%. The designer can program aging time by writing register 0x89[14:0]. The address aging function can be disabled by programming register 0x82[1] to “1”.

5.1.3.2 Packet Aging

Related registers	0x44[5:0], 0x44[8]

IP1725 supports packet aging (out queue aging). If a packet stays in IP1725 longer than the aging time defined in register 0x44[5:0]. IP1725 will drop the packet to improve the efficiency of packet buffer. The packet aging function can be enabled by programming register 0x44[8] to "1".

5.1.4 802.1D Packet Forwarding

Related registers	0x01[2], 0x02[1:0]

Besides the erroneous packet and the IEEE802.3x pause packet, the 802.1D Reserved Group packet with MAC address from 01-80-c2-00-00-04 to 01-80-c2-00-00-0f can be optionally dropped when register 0x01[2] is set to "0". A packet with MAC address equal to 01-80-c2-00-00-00 can be forwarded to CPU or be dropped according to the setting in register 0x02[0]. A packet with MAC address equal to 01-80-c2-00-00-03 can be forwarded to CPU or be dropped according to the setting in register 0x02[1]. A packet with MAC address equal to 01-80-c2-00-00-02 can be forwarded to CPU or be dropped according to the setting in register 0x02[2].

IP1725 provides another option to forward the special 802.1D Reserved Group when register 0x02[12] is set to "1". The detail configuration is shown in the table below.

Table 12 802.1D Reserved Group Packet Forwarding

Multicast MAC address	Normal mode Reg 0x02[12]=0	Special mode Reg 0x02[12]=1
01 80 C2 00 00 00	Pass Through	Pass Through
01 80 C2 00 00 01	Drop	Drop
01 80 C2 00 00 02	Drop	Drop
01 80 C2 00 00 03	Pass Through	Pass Through
01 80 C2 00 00 04~0D	Pass Through	Drop
01 80 C2 00 00 0E	Pass Through	Pass Through
01 80 C2 00 00 0F	Pass Through	Drop
01 80 C2 00 00 10	Pass Through	Drop
01 80 C2 00 00 21	Pass Through	Drop
01 80 C2 00 00 30~3F	Pass Through	Pass Through

5.1.5 Inter Frame Gap Compensation

Related registers	0x01[1:0]

IP1725 supports an option to transmit a packet with IPG shrank 40 ppm, 80 ppm or 160 ppm to compensation the data accumulation due to TX clock frequency difference between local machine and link partner. Programming register 0x01[1:0] can turn on this function.

5.1.6 Flow Control

IP1725 supports two kinds of flow control mechanisms, backpressure for half duplex operation and IEEE802.3x pause frame mechanism for full duplex operation.

5.1.6.1 IEEE802.3x

Related registers	0x5B~0x5E

When operating in full duplex mode, IP1725 supports IEEE802.3x flow control with both symmetric pause and asymmetric pause function. Each port's flow control function can be enabled individually by programming registers 0x5B~0x5E. When packets in the buffer reach the threshold, IP1725 generates a "Xoff" pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner stops transmission for a period of time defined in the pause packet. This prevents the buffer of IP1725 from overflow. When the packets in buffer lower than threshold, IP1725 generates a "Xon" pause packet to notify the link partner the receive buffer is available.

5.1.6.2 Backpressure

Related registers	0x5F, 0x60, 0x01[4:3]

In half duplex mode, the IP1725 supports backpressure flow control. Each port's backpressure function can be enabled individually by programming registers 0x5F and 0x60. When the packets in buffer reach the threshold, IP1725 generates a jam pattern to back off the link partner. IP1725 supports the collision based and carrier-sense based backpressure. When the collision based backpressure is enabled, setting register 0x01[3] to "1", IP1725 generates a jam pattern only when the link partner is transmitting data and the receive buffer in IP1725 is not available. When detecting a collision on line, the link partner stops transmission until a back off time expires. When the carrier-sense based backpressure is enabled, register 0x01[3] is set to "0", and IP1725 transmits null packets continuously to prevent link partner's transmission when the buffer is not available.

To prevent the packet loss due to excessive collision caused by backpressure mechanism, designer can clear bit 4 of register 0x01 to disable the 16 consecutive collisions drop function defined in IEEE802.3.

5.1.6.3 Flow Control Off For High Priority Packet

Related registers	0x01[7]

To prevent the flow control function from blocking the high priority traffic, each port of IP1725 can turn off flow control function for a period of time automatically when receiving a high priority packet. This function can be enabled by writing "0" to register 0x01[7].

5.1.6.4 Pause Frame with Invalid Uni-case DA

Related registers	0x02[8], 0x3A~0x3C

IP1725 provide one option that can be selected for pause frame type. If an incoming packet with pause frame type, however, the destination is not equal to the pause frame DA (01-80-c2-00-00-01) and the MAC address defined in registers 0x3A~0x3C. The designer can select two kinds of method. One is that the packet will be dropped by programming register 0x02[8] to '0'; the other is that the packet will be transmitted by programming register 0x02[8] to '1'.

5.1.7 Bandwidth Control

Related registers	0x05~0x1D, 0x01[6]

IP1725 implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress and the egress data rate, IP1725 provides a variety of bandwidth configurations. It limits the maximum byte counts, for each port to send or receive packets. If the transmit byte counter or receive byte counter of a port reaches a pre-defined threshold, it will stop transmitting or receiving data.

Each port's egress/ingress data rate can be programmed individually. The maximum rate of port 1 to port 25 is defined in registers 0x05~0x1D. The higher byte of the registers defines the reception rate and the lower byte defines the transmission rate. The register 0x01[6] defines the high/low throttle value used in bandwidth control function. It should be noticed that once the rate has been set, it would be independent of the status of link speed and flow control. The detail configuration is shown in the table below.

Table 13 Bandwidth Throttle Selection Table

H/L throttle	Maximum output rate (transmit rate)	Maximum input rate (receive rate)
0x01[6]=0	Bit[7:0] * 32 kbps	Bit[15:8] * 32 kbps
0x01[6]=1	Bit[7:0] * 512 kbps	Bit[15:8] * 512 kbps

5.1.8 Broadcast Storm Control

Related registers	0x82[3:2], 0x86, 0x87

To prevent the broadcast storm, the IP1725 implements a broadcast storm control mechanism. By enabling this function, a port begins to drop the incoming broadcast packets if the received broadcast packet counter reaches the threshold defined in register 0x87[14:9]. Besides the DA equaling ff-ff-ff-ff-ff-ff, IP1725 supports broadcast storm type selection. The multicast patterns can also be regarded as broadcast packets when register 0x82[2] is set to "1", and the unknown DA patterns can also be regarded as broadcast packets when register 0x82[3] is set to "1". Each port's broadcast storm protection function can be enabled individually by programming registers 0x86 and 0x87[8:0]. IP1725 also provides two kinds of period to be selected with register 0x87[15]. The detailed configuration is shown in the following table.

Table 14 Broadcast Storm Counter Clear Period Selection Table

0x87[15]	100Mbps	10Mbps
0	500us	5ms
1	10ms	100ms

5.1.9 Block Broadcast Frames to CPU Port

Related registers	0x70[0], 0x82[4], 0x82[6]

IP1725 supports an option to block broadcast frames to CPU port. To enable the function, the designer has to assign port 25 as a CPU port by programming register 0x70[0], and then turn on the function by programming register 0x82[4] to "1". When this function is enabled, IPv4 can be still forwarded to CPU port, if register 0x82[6] is set to "1".

5.1.10 ARP and ICMP Storm Control

Related registers	0x88

To prevent the ARP and ICMP storm, IP1725 implement ARP and ICMP storm control mechanism. When these function is enabled by programming registers 0x88[3] and 0x88[11], a port begins to drop incoming ARP packets if the received ARP packet counts reach the threshold defined in register 0x88[2:0]; a port begins to drop the incoming ICMP packets if the received ICMP packet counts reach the threshold in register 0x88[10:8]. Besides, IP1725 provides two kinds of period to be selected with registers 0x88[4] and 0x88[12].

5.1.11 Block ARP to CPU Port

Related registers	0x70[0], 0x82[5]

IP1725 supports an option to block ARP frames to CPU port. To enable the function, the designer has to assign port 25 as a CPU port by programming register 0x70[0], and then turn on the function by programming register 0x82[5] to “1”.

5.1.12 Reduce IPG And Preamble For CPU Port

Related registers	0x02[11:10]

At some time, for example while transmitting the packets to CPU port and add special tag. Make IP1725 difficult to transmit packets to CPU at wire speed. IP1725 provides two alternatives for solving this problem. One alternative is to reduce the IPG of packets transmitted to CPU port, from 96 bit time to 64 bit time by programming register 0x02[10] to ‘1’. The other alternative is to reduce the preamble of packets transmitted to CPU port, from 8 bytes to 4 bytes by programming register 0x02[11] to ‘1’.

5.2 The Speed and Duplex of MII

Related registers	0x70[1], 0x5A[8], 0x58[8], 0x61[6]

In MII mode, LED should be entered serial mode when power on reset.

When works in PHY Mode by programming register 0x70[1] is set to '1', IP1725 sends out data MRXDV and MRXD[3:0] at the falling edge of MRXC. By recognizing the MRXDV and MRXD[3:0], an external CPU can capture the correct data stream. Port 25’s speed and duplex can be updated by programming registers 0x58[8](for speed) and 0x5A[8](for duplex), and disable auto negotiation.

When works in MAC Mode by programming register 0x70[1] is set to '0', IP1725 sends out data MTXEN and MTXD[3:0] at the rising edge of MTXC. By recognizing the MTXEN and MTXD[3:0], an external PHY can capture the correct data stream. Port 25’s speed and duplex can be updated by programming registers 0x58[8](for speed) and 0x5A[8](for duplex) or polling status.

Table 15 MII Speed and Duplex Selection Table

MII speed/duplex select 0x61[6]	MII works in PHY mode 0x70[1]=b'1	MII works in MAC mode 0x70[1]=b'0
0	-	polling status
1	0x58[8] for speed 0x5A[8] for duplex	0x58[8] for speed 0x5A[8] for duplex

Figure 5 MII PHY Mode Interface

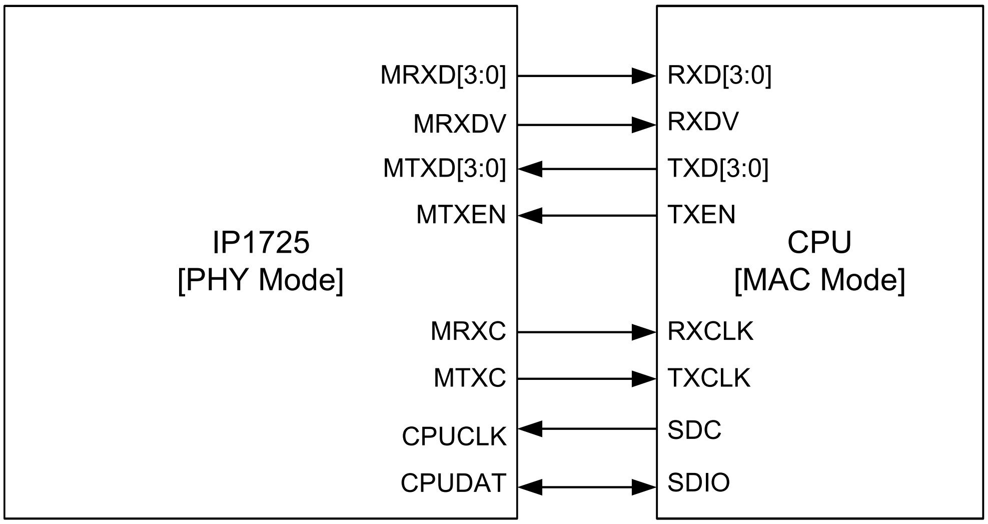
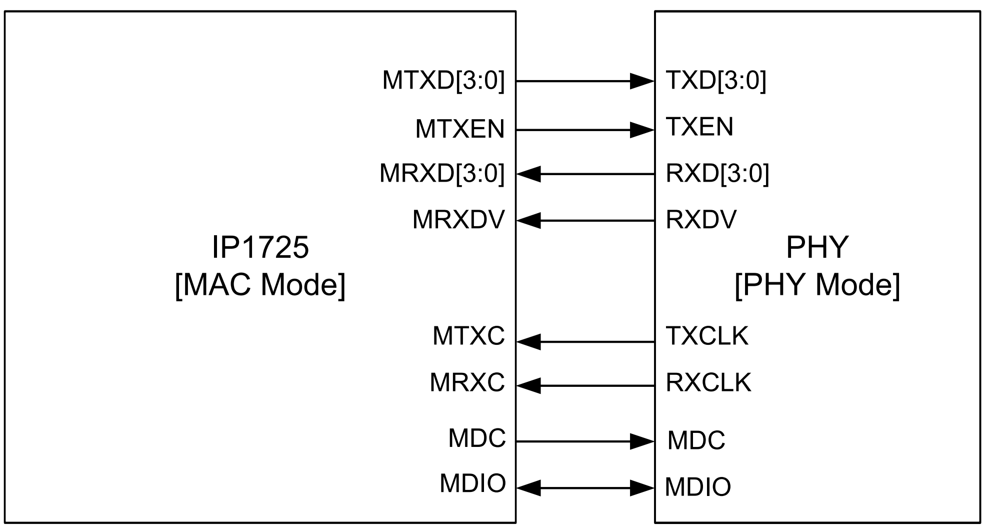


Figure 6 MII MAC Mode Interface



5.3 CPU Interface

There is no need to program the register of the IP1725 for the generic application. However it's probably necessary to program the internal register to fit some special applications. The interface between the IP1725 and the CPU is a serial bus, which comprises a clock and an I/O signal. Like the access cycle of the serial management interface, the serial interface comprises the switch ID, the read/write command, the address and the data. The access cycle is depicted as below.

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide.

Figure 7 CPU Read Data Format

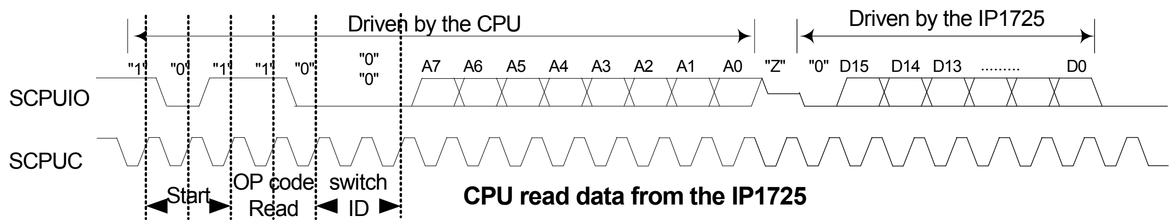
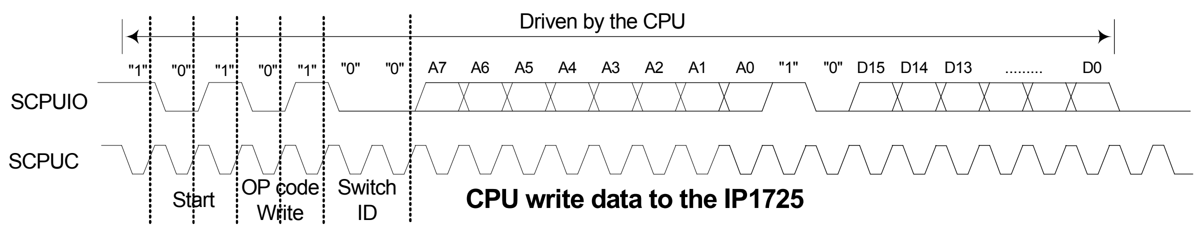


Figure 8 CPU Write Data Format



5.4 Configure the Port Properties

Related registers	0x55~0x60, 0x65~0x6D

The designer can configure properties of each port through the CPU interface. The designer can set the auto-negotiation, speed, duplex, pause, and backpressure function by writing registers 0x55~0x60.

The designer can get the status of a port by reading registers 0x65~0x6D. These registers provide the status of asymmetric pause, pause, duplex, speed and link of each port.

5.5 Force Link

Related registers	0x61[6:0], 0x58[8], 0x5A[8]

IP1725 supports force link function for port 25. Port 25 can be configured individually by programming register 0x61[5], and can access CPU port PHY address by programming register 0x61[4:0]. This function is useful when IP1725 is connected to a CPU, which doesn't support SMI. In this case, IP1725 can't get the link status and will not transmit/receive packets through this port. The force link function will keep this port active regardless of the link status. Besides, IP1725 provides other operation mode, which can be enabled with register 0x61[6] to judge link status by polling status or by registers 0x58[8] and 0x5A[8] of port 25 with link partner.

5.6 Read/Write Address Table (LUT)

Related registers	0xF5~0xF8

The designer can access IP1725's MAC address table, including 8192 entries. To write an entry to the MAC address table, the designer has to fill the 47-bit data to registers 0xF6~0xF8 and then specifies the address of the entry and issues a write command by programming register 0xF5. To read an entry from MAC address table, the designer has to specify the address of the entry and issues a read command by programming register 0xF5. The entry can be read from registers 0xF6~0xF8.

Because IP1725 builds and accesses the MAC address table with the address derived with hashing algorithm, designer has to calculate the address of an entry in the same way before accessing the table. That is, if direct hashing is selected, the address of an entry is the 12 LSB of a MAC address. If CRC hashing is selected, the address of an entry is the 12 LSB of CRC calculation result of a MAC address.

5.7 Read/Write PHY Register

Related registers	0x63, 0x64

The designer can access the register of a PHY connected to IP1725 through CPU I/F. To read a register of a PHY, the designer has to specify the PHY address and the MII register address and then issues a read command by programming register 0x63. The content of the register can be read from register 0x64. To write a register of a PHY, the designer has to specify the PHY address and the MII register address and then issues a write command by programming register 0x63. The write data should be written by programming register 0x64 before issuing a write command.

The associated PHY address from port 1 to port 24 is "8" to "31", the port 25 PHY address is "1" by default.

5.8 Read/Write EEPROM

Related registers	0x78, 0x79

The designer can access the EEPROM through CPU I/F. To read one byte from EEPROM, the designer has to specify the byte address and device address and then issues a read command by programming register 0x78. The data can be read from register 0x79. To write one byte to EEPROM through CPU I/F, designer has to specify the byte address and device address and then issues a write command by programming registers 0x78. The write data should be written by programming register 0x79 before issuing a write command.

5.9 EEPROM Interface

IP1725 supports EEPROM I/F to access 24C02/04/08/16. After detecting the rising edge of a reset input, IP1725 will start to read the content of EEPROM (acting like an EEPROM master). Being an EEPROM master, IP1725 provides two kinds of mode to download the content of EEPROM. The content of the first byte should be "25h" to be identified as IP1725 EEPROM. If the content of the second byte is "0x0A", it runs with continuous mode. If the content of the second byte is "0x0B", it runs with command mode.

In the continuous mode, IP1725 will read the EEPROM address from 00h to 1FFh and map the read data into correspond registers.

In the command mode, one command occupies 4 EEPROM bytes. The content includes 2 bytes address and 2 bytes data. The address byte equaling to “0xFF” means the end of command and IP1725 will stop the EEPROM reading. If the end of command is not set, IP1725 will read EEPROM until no acknowledge.

The mapping relationship between the IP1725 registers and the EEPROM address are depicted as the following table.

Table 16 Continuous Mode Format of EEPROM

Continuous mode		
EEPROM address	**EEPROM content**	**IP1725's Register**
0x00	0x25	XX
0x01	0x0A	XX
0x02	Expected value	0x01[15:8]
0x03	Expected value	0x01[7:0]
0x04	Expected value	0x02[15:8]
0x05	Expected value	0x02[7:0]
---	---	---
0x1FC	Expected value	0xFE[15:8]
0x1FD	Expected value	0xFE[7:0]
0x1FE	Expected value	0xFF[15:8]
0x1FF	Expected value	0xFF[7:0]

Table 17 Command Mode Format of EEPROM

Command mode		
EEPROM address	**EEPROM content**	**IP1725's Register**
0x00	0x25	XX
0x01	0x0B	XX
0x02	Expected value	0x00
0x03	Expected value	Addr[a]
0x04	Expected value	Data[15:8]
0x05	Expected value	Data[7:0]
0x06	Expected value	0x00
0x07	Expected value	Addr[b]
0x08	Expected value	Data[15:8]
0x09	Expected value	Data[7:0]
---	---	---
XX	Expected value	0x00
XX	Expected value	0xFF

Note:
1. EEPROM ID should be set to "3'b000"; i.e. A2=0; A1=0; A0=0
2. IP1725 downloads the content of EEPROM ranging from address 0x00 to 0x1FF; i.e. the register beyond this range is not recognized by IP1725.
3. The ID for IP1725 recognition should be set at address 0x00 as shown in the table.
4. In command mode, only one byte is used to be the address data. The extra address byte can be used by user defined.

5.10 Statistic Counter

Related registers	0x01[9:8], 0x3D~0x41

IP1725 provides 50 statistic counters, two counters for each port. These counters are enabled if register 0x01[9] is set to "1". The designer can select the function of counters to be RX packet count, TX packet count, collision count, packet drop count, or CRC error count by programming register 0x01[8], and registers 0x40 and 0x41. Each bit of registers 0x40 and 0x41 is corresponding to one port individually as shown in the following table.

Table 18 Port Statistic Counter Selection Table

The function of counters of one port		
0x01[8], one bit of 0x40 and 0x41	**Counter 0(even addr)**	**Counter 1(odd addr)**
0,0	Receive packet count	Transmit packet count
0,1	Transmit packet count	Collision count
1,0	Receive packet count	Packet drop count (MAC)
1,1	Receive packet count	CRC error packet count

To read the content of a counter, the designer has to specify the address of counter in register 0x3D[5:0] and issues a read command by setting register 0x3D[8]. The content of the counter can be read by accessing registers 0x3E and 0x3F. The address of counter of each port is shown in the following table.

Table 19 Address Format of Port Statistic Counter

Address of counter (0x3D[5:0])	Location of counter
0	Port 1 counter 0
1	Port 1 counter 1
2	Port 2 counter 0
3	Port 2 counter 1
---	---
46	Port 24 counter 0
47	Port 24 counter 1
48	Port 25 counter 0
49	Port 25 counter 1

5.11 Interrupt

Related registers	0x74, 0x75

IP1725 provides one interrupt pin to indicate status change. When one of the following conditions happen, IP1725 will asserts the interrupt pin if the function is enabled.

1. A CPU R/W SMI command is completed
2. A CPU R/W EEPROM command is completed
3. Link status changes on the PHY of any port

By programming the corresponding bit of register 0x74, the interrupt mask register, can enable an interrupt function. The designer can read register 0x75 to identify the interrupt source.

5.12 802.3 OAM LoopBack

Related registers	0xFE, 0xFF

IP1725 provides two kinds of 802.3 OAM loopback modes; one is the passive mode and the other is the active mode.

When the passive mode is selected, register 0xFF[8] is set to '0'. The packets with the following features:

1. In the OAM loopback ports, every frame received is transmitted back on that same port except pause frames and OAM frames.
2. Other ports send frame to OAM loopback port will be dropped.
3. CPU port can send OAM packets to specific OAM loopback port if CPU port is enabled.
4. OAM loopback ports send OAM packet to CPU port only.

When the active mode is selected, register 0xFF[8] is set to '1'. In the OAM loopback ports, the general packets will be dropped; OAM packets will be forwarded to CPU port only if register 0x02[2] is set to '1'.

Each bit of registers 0xFE and 0xFF[7:0] is corresponding to one port can be enabled individually.

Figure 9 802.3 OAM Frame Format

		6 byte	6 byte	2 byte	1 byte		
Preamble	SFD	**DA=01-80-c2-00-00-02**	SA	**TYPE=8809**	**03**	DATA	FCS

5.13 LED Description

5.13.1 LED Mode Setting

Related registers	0x54

IP1725 supports serial LED mode and direct LED mode for display statuses of each port. The formats of LED display mode are shown below controlled by setting register 0x54[1:0]. All LED statuses are represented as active-low under 3 bit and 2 bit serial modes, except Link/Act whose polarity depends on speed status in bi-color mode or those LED pins whose polarity depends on the initial setting of pin under direct mode.

Table 20 LED Display Selection Table

Reg 0x54[1:0]	Mode	Output sequences (pins)
11	Direct mode	Link/Act
10	3-bit for serial mode bi-color mode	Col/Dupx, (Link/Act)/(Spd)
01	3-bit for serial mode	Col/Dupx, Link/Act, Spd
00	2-bit for serial mode	Spd, Link/Act

Table 21 LED Indication Table

LED indication	Description
Col/Dupx	Collision and Duplex Indicator. This LED blink rate depends on led_blink_rate setting by register 0x54[3:2] when collision happens. This function can disable by register 0x54[6] is set to “1”. In duplex indicator, low for full duplex mode, and high for half duplex mode.
Link/Act	Link and Activity Indicator. For 3-bit serial stream mode, low for link established. For 3-bit bi-color LED mode and 100Mb/s, the Link/Act is high for link established. For 3-bit bi-color LED mode @ 10Mb/s, the Link/Act is low for link established. This LED blink rate depends on led_blink_rate setting by register 0x54[3:2] when the corresponding port is transmitting or receiving. This function can disable by register 0x54[7] is set to “1”.
Spd	Speed Indicator. Low for 100Mb/s, and high for 10Mb/s.

5.13.2 LED Blink Rate Setting

IP1725 provides four kinds of LED blink rate setting through register 0x54[3:2]. The LED’s blink rate of the Col/Dupx and the Link/Act will change according to register 0x54[3:2] setting. The detailed configuration is shown in the following table.

Table 22 LED Blinking Rate Selection Table

Reg 0x54[3:2]	LED blinking rate
00	40 ms
01	80 ms
10	120 ms
11	160 ms

5.13.3 LED Clock Rate Setting

IP1725 provides four kinds of clock rate setting through register 0x54[5:4]. The detailed configuration is shown in the following table.

Table 23 LED Clock Rate Selection Table

Reg 0x54[5:4]	LED clock rate
00	781 KHz
01	2.5 MHz
10	5 MHz
11	10 MHz

5.13.4 Serial Stream Mode

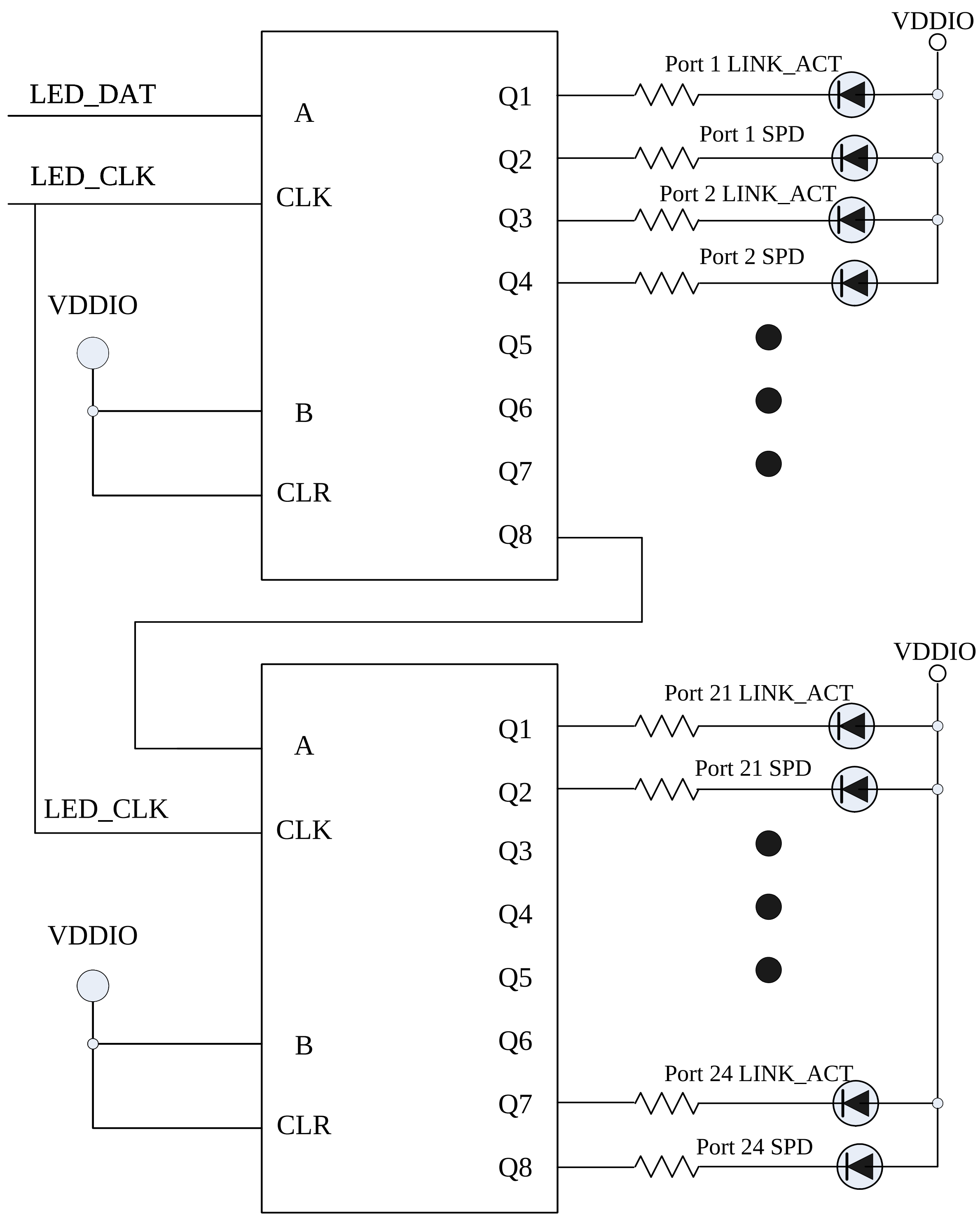
Bits stream are output sequentially from port 25 to port 1. For 2-bit serial stream mode, the sequence is Spd at first and then Link/Act. For 3-bit serial stream mode, the sequence is Col/Dupx, Link/Act, and then Spd.

5.13.5 Direct LED Mode

IP1725 also supports direct LED mode by setting register 0x54[1:0] to “11”, bits stream are output directly from port 1 to port 24.

In this mode, Pin 151 auto_slew of initial pin setting must be connected to ground through a 4.7K ohm resister when power on reset. And Link/Act is availably only.

Figure 10 External TTL for 2-bit Serial Stream LED Mode



External TTL for 2 Bit Serial Stream LED Mode

Figure 11 3-bit Bi-color Serial Stream LED Mode

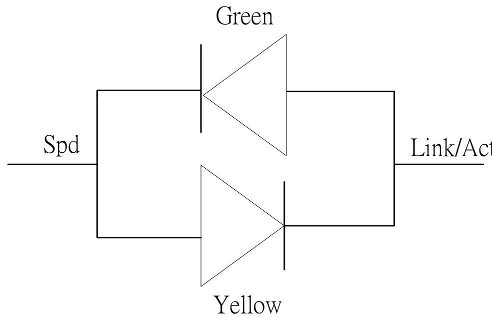


Table 24 Bi-color Serial Stream LED Status Table

Spd	Link/Act	LED indication	Bi-color state
0	0	Unlink	Dark
1	1	Unlink	Dark
0	1	100Mbps Link	Green is light
0	1-0-1-0…	100Mbps Link and Active	Green is blinking
1	0	10Mbps Link	Yellow is light
1	0-1-0-1…	10Mbps Link and Active	Yellow is blinking

5.14 Selftest Mode

IP1725 implements a selftest mode mechanism, which is very useful for switch mass production test. When this function is triggered by switch hardware pin of 155, IP1725 physical ports are connected to port-pairs loopback and then IP1725 will generator frames for TX of all ports. The test will be the light-on period changing to the light-off period for 2 seconds; show result for 4 seconds following light-off for 1.5 seconds; then finish selftest mode. For example, when port 1 and port 2 are connected to loopback and selftest function is triggered. In first time, show LED test result are light-on for port 1 and port 2. The test result is pass. If show test result are light-off. The test result is fail.

5.15 VLAN

IP1725 supports port based VLAN and tag based VLAN as the function described below.

5.15.1 Port Based VLAN

Related registers	0x82[7], 0xAD~0xDE

IP1725 provides various port-based VLAN configurations. The designer can enable the function by programming register 0x82[7] to “0”. For each port, there are two registers to describe its port-based VLAN configuration. The overall numbers of VLAN group that IP1725 can support are “25”. The VLAN group can be defined in registers from 0xAD to 0xDE.

Take the following example for the detail description. The data incoming from port 1 will be forwarded to the corresponding port defined in registers 0xAD and 0xAE. For example, if register 0xAD and 0xAE are written with 16'h000F and 16'h000F, the packet from port 1 can be forwarded to port 2/3/4 and port 17/18/19/20 only. Similarly, the forwarding rule for the data incoming from port 2 will refer to the register 0xAF and 0xB0. The forwarding rule for the data incoming from port 25 will refer to the register 0xDD and 0xDE.

Table 25 VLAN Group Definition

Packet

	Definition	Register
Port 1	The ports which port 1 can forward to	ADh, AEh
Port 2	The ports which port 2 can forward to	AFh, B0h
Port 3	The ports which port 3 can forward to	B1h, B2h
	....	
	....	
	....	
	....	
Port 22	The ports which port 22 can forward to	D7h, D8h
Port 23	The ports which port 23 can forward to	D9h, DAh
Port 24	The ports which port 24 can forward to	DBh, DCh
Port 25	The ports which port 25 can forward to	DDh, DEh

Note: The port ID is counted from 1 to 25.

5.15.2 Tag Based VLAN

Related registers	0x82[7], 0x9B~0xA3, 0xAD~0xEC, 0xFA, 0xFC

IP1725 provides a 32-entry VLAN table, including VID entries from 0 to 31, to support 32 active VLANs out of 4096 VLANs defined in IEEE802.1Q. The designer can define 32 VID entries in the VID table and enable the tag-based VLAN function by programming registers 0xFA and 0xFC, and the register 0x82[7] is set to "1". When a tagged packet is received, IP1725 compares the tag in the packet with the one defined in the VID table. If it does not match, IP1725 drops the packet. If it matches, IP1725 uses the corresponding index to check out one of the 32-entry in the VLAN table, which is defined in registers 0xAD~0xEC, as an output port mask. Finally, a set of ports to which the packet can be forwarded. IP1725 forwards the packet according to MAC address and the output port mask. If the source port is not one of the members in the VLAN table entry, refer to 1.15.7. It is note that registers 0xAD~0xEC define port-based VLAN configuration and tag-based VLAN table entries.

When an un-tagged packet is received, IP1725 uses the default PVID for the source port as an index to the VID of the packet. The default PVID index of a port is defined in the registers 0x9B~0xA3. IP1725 forwards the packet in the same way as mentioned above. For example, if port 1 receives a un-tag packet, IP1725 adopts the PVID index of port 1 defined in bit [4:0] of register 0x9B to select one of the VLAN table defined in registers 0xAD~0xEC. The priority tag packet (with VID equal to "000h") is handled as an un-tagged packet. More VLAN functions described below.

5.15.3 VLAN Function

Related registers	0x47, 0x48, 0x82[12:11], 0x97~0x9A, 0x9B~0xA3, 0xA4~0xA8 0xFA, 0xFC

5.15.3.1 Add/Modify VLAN Tag

IP1725 supports two kinds of method to insert a tag to a frame, if the tag function is enabled. One is the port-based tagging function, which is enabled if register 0x82[11] is set to '0' and the corresponding bits in registers 0x97 and 0x98 are set. The other is VID-based tagging function which is enabled if register 0x82[11] is set to '1', and the designer must go to VID_TAG entry table to set up through registers 0xFA and 0xFC.

A set port always adds a tag to a forwarding packet with "8100" + PRI + VID selected by PVID. The PRI tag information is defined in registers 0xA4~0xA8; the VID tag information must go to VID_TAG entry table to read the value through registers 0xFA and 0xFC, and the PVID for each port is defined in registers 0x9B~0xA3. A packet with VID equal to 12'b0 will be handled as un-tag frame.

When tag insertion is needed, the designer will select the insertion of PRI and PVID is according to the source port or the output port. Each bit of registers 0x47 and 0x48[8:0] is refer to each port.

5.15.3.2 Remove VLAN Tag

IP1725 supports two kinds of method to remove a tag of a frame if un-tagging function is enabled. One is the port-based un-tagging function of which is enabled if register 0x82[11] is set to '0' and the corresponding bits in registers 0x99 and 0x9A are set. The other is VID-based un-tagging function which is enabled if register 0x82[11] is set to '1', and the designer must go to VID_TAG entry table to set up through registers 0xFA and 0xFC. A set port always removes a tag from a forwarding packet.

In the VID-based tagging function mode, regardless of inserting tag or removing tag, don't modify tag if packets send to CPU port by programming register 0x82[12] to "0".

The operation is illustrated as follows. It is note that the VID defined in VLAN entry table for tagging is also used for 802.1Q tag-based VLAN.

Table 26 Forward the Packet with VLAN Configuration Table

Frame type of the received packet	The operation on a switch with VLAN configuration	
	Forward to a untagged filed	**Forward to a tagged field**
Untagged	Forward the packet without modification	1. Insert a tag using the default VLAN tag value of the source or output port 2. Calculate new CRC 3. The default VLAN tag value is defined in the registers 0x9B~0xA3.
Priority-tagged (VLAN ID=0)	1. Strip tag 2. Calculate new CRC	1. Keep priority field. 2. Replace the tag with the default VLAN tag value of the source or output port 3. Calculate new CRC 4. The default VLAN tag value is defined in the registers 0x9B~0xA3.
VLAN-tagged	1. Strip tag 2. Calculate new CRC	Forward the packet without modification

Figure 12 Frame Format of Inserting VLAN or Special Tag

An packet without tag

DA	SA	data	CRC

An packet with VLAN tag

DA	SA	8100	VID	data	CRC

An packet with special tag and VLAN tag

DA	SA	9126	Port Info.	8100	VID	data	CRC

5.15.4 Packets across a VLAN

Related registers	0x82[8]

In the normal case, a packet is not allowed to be forward across a VLAN. That is, if the destination port does not belong to the same VLAN, the packet will be dropped. IP1725 provides a VLAN option to allow uni-cast packets to stride across a VLAN. This function is enabled by set bit 8 of the register 0x82.

5.15.5 VLAN up Link

Related registers	0x82[9], 0x8D, 0x8E

Under the normal operation, if a destination port and a source port are in different VLAN, the packet will be dropped.

IP1725 supports an option to allow this dropped packet be sent to the specified up-link port if register 0x82[9] is set to “1”. The up-link port is defined in registers 0x8D and 0x8E.

5.15.6 Force The Incoming Packet Use PVID

Related registers	0xA9, 0xAA

IP1725 provides another kind of the mechanism for the packet forwarding. The designer can force the incoming to use the PVID which port he wants by setting registers 0xA9 and 0xAA. Each bit of registers 0xA9 and 0xAA is corresponding to one port can be enabled individually.

5.15.7 VLAN Ingress Check

Related registers	0xAB, 0xAC

For packets forwarding, IP1725 provides a mechanism to check the ingress port, which is in or out of the VLAN group by setting registers 0xAB and 0xAC. For packets forwarding to the port, as long as the corresponding bit in register 0xAB or 0xAC is asserted, IP1725 will check the VLAN group; if the VID are not in VLAN group, IP1725 will drop those packets.

5.16 Q-in-Q Tag

Related registers	0x27, 0x4A~0x4F, 0x82[15]

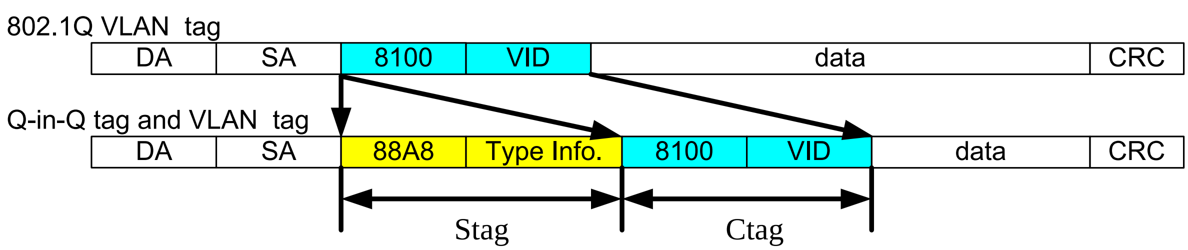
The "Q-in-Q" tag is purpose to expand the VLAN space by tagging the tag packets, thus producing a double tag frame. "Q-in-Q" tag feature provides the encapsulation of double VLAN tags within an Ethernet frame, with the inner VLAN tag being the 802.1Q VLAN tag is defined "Ctag", while the outer one being the "Q-in-Q" VLAN tag assigned is defined "Stag". Frames are forwarded based on the outer VLAN tag only, while the 802.1Q VLAN tag is shielded during data transmission.

IP1725 provides ingress packets control of Ctag/Stag by programming register 0x27 configurations.

If the incoming packets comprise "Q-in-Q double" tag, IP1725 will don't modify Ctag by programming register 0x82 to '0'.

IP1725 insert or remove a "Q-in-Q" tag of a frame by programming registers 0x4C~0x4E and 0x4B[10:9] when add/remove "Q-in-Q" tag function is enabled. Each bit of registers 4Ah and 0x4B[8:0] is corresponding to one port individually. The Q-in-Q double tag information is defined in register 4Fh.

Figure 13 Frame Format of Inserting Q-in-Q Tag



5.17 Class Of Service (CoS)

5.17.1 Output Queue Schedule Mode with Priority

Related registers	0x01[7], 0x42, 0x43

IP1725 implements four levels of priority queues (priority queue 0 to 3). The priority for each packet is based on the following schemes:

1. Physical port
2. 802.1Q VLAN tag
3. IP TOS/DS
4. TCP/UDP port number
5. Supreme priority (include ACL result, IP address, MAC address)

When CoS function is enabled, the following three schedule modes are selectable. When CoS function is not enabled, the first-in/first-out forwarding method is used. The detailed configuration is shown in the following table. The weight function, for the transmitting ratio from high to low priority, is defined in register 43h.

Table 27 Output Queue Schedule Mode Description Table

Reg 0x42[1:0]	Mode	Function description
00	Fist In Fist Out Schedule	All output packets are queued to one queue, first comes first outs.
01	Strict Priority	In 2 queues mode, packets are classified into high/low queues, unless the high priority queue is empty, low priority cannot transmit packets. And in 4 queues mode, packets are classified into Q0/Q1/Q2/Q3, unless Q0 is empty, Q1/Q2/Q3 cannot transmit packets, the sequence is Q0>Q1>Q2>Q3.
10	WRR	Packets are classified into four queues. The transmit weighting is based on the packet count defined in register 0x43.
11	WRR/Strict Priority Mixed	Packets are classified into four queues. The highest priority queue transmits packets when queue is not empty. The other three queues follow the weighting defined in register 0x43.

IP1725 provides five kinds of CoS priority described above. The precedence is Supreme priority > TCP/UDP port number base priority > IP CoS base priority > VLAN tag base priority > port base priority.

IP1725 provides an option to pause flow control function to prevent the extra delay for a high priority packet. A port's flow control function is disabled for 1.5s automatically when it receives a high priority packet. This function can be enabled by writing "0" to register 0x01[7].

5.17.2 Port Based Priority

Related registers	0x1E~0x21

The port-based priority only concerns the physical port location in a switch. A packet received by a high priority port is handled as a high priority packet. Each port of IP1725 can be configured as a high priority port individually by programming registers 0x1E~0x21. For example, the bit 0 and bit 1 of register 0x1E corresponds to port 1 and the bit 0 and bit 1 of register 0x21 corresponds to port 25.

5.17.3 802.1Q VLAN Tag Based Priority

Related registers	0x22, 0x23

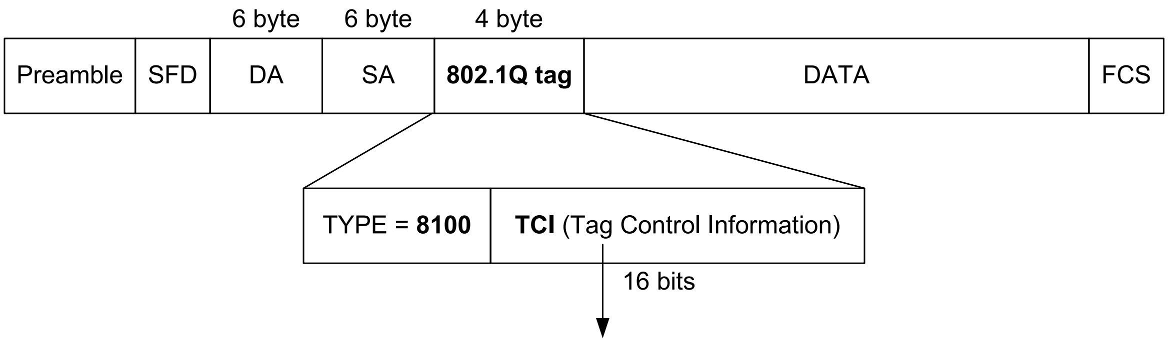
When the CoS for 802.1Q VLAN tag-base priority is enabled, IP1725 will examine 3 bits of the priority field carried by a VLAN tag and map it to the corresponding priority. The priority tag is shown in the following table. The CoS function of each port can be enabled individually by programming registers 0x22 and 0x23. For example, the bit 0 of register 0x22 corresponds to port 1 and the bit 0 of register 0x23 corresponds to port 17.

Table 28 QoS Selection Table

Priority tag bit [15:13]	2 queues mode	4 queues mode
00X	To low queue	To queue 3
01X		To queue 2
10X	To high queue	To queue 1
11X		To queue 0

Note: X means "don't care"

Figure 14 Frame Format of 802.1Q Priority



Bit[15:13]: Priority
IP1725 uses these bits to define priority.
Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.

5.17.4 VID Tag Based Priority

Related registers	0x23[9], 0xFA, 0xFC

IP1725 provides one kind to judge the mechanism of priority by VID. This function can be enabled by writing bit 9 of register 0x23 to '1'. IP1725 will recognize the VID of incoming packets, and then checking VID Table to finds out corresponding priority queue. Each VID priority of VID Table can be configured individually by programming registers 0xFA and 0xFC. The VID Table is shown in the following table.

Table 29 VID Table

VID priority enable	VID priority queue			Bit [11:0]
Bit [14]	**Bit [13:12]**	**2 queues mode**	**4 queues mode**	
1 : Enable 0 : Disable	00	To low queue	To queue 3	**VID value**
	01		To queue 2	
	10	To high queue	To queue 1	
	11		To queue 0	

5.17.5 IP CoS Based Priority

Related registers	0x24~0x26

IP1725 provides the IP layer CoS function by recognizing the priority octet and mapping it to the corresponding priority. For an IPv4 packet, it is embedded in the TOS (Type of Service) Octet. For an IPv6 data packet, the Traffic Class Octet is used to differentiate the Class of Service. When this function is enabled, IP1725 will automatically recognize the IP version and capture either the TOS field (IPv4) or the Traffic Class field (IPv6).

Figure 15 Frame Format of IPv4 CoS Priority

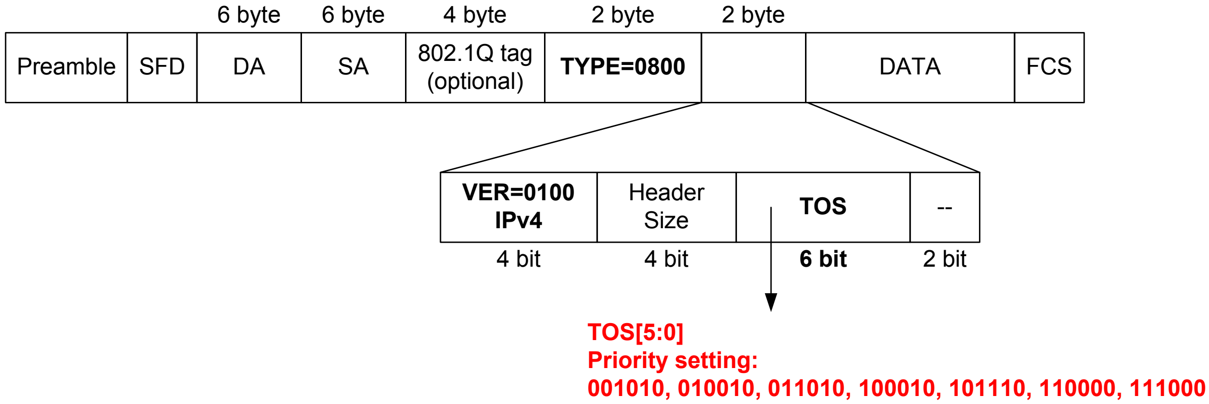
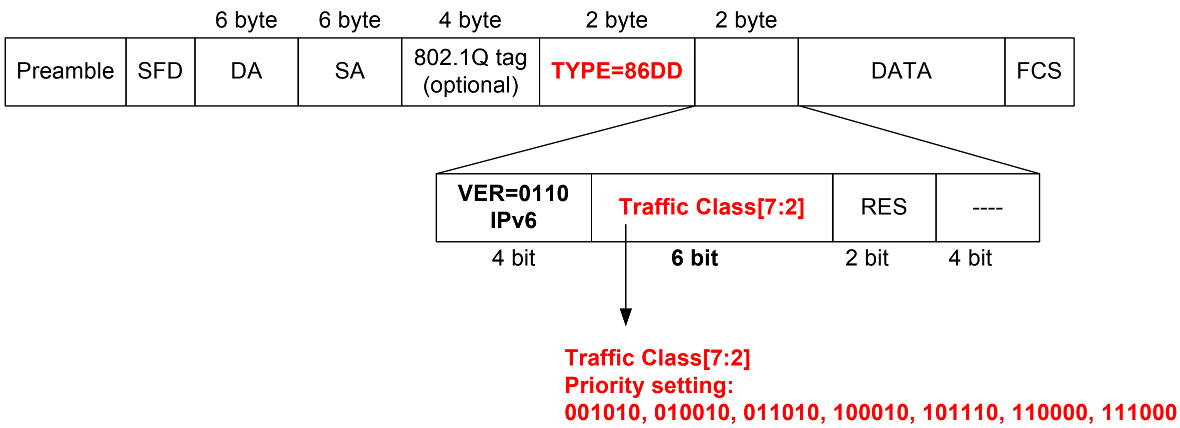


Figure 16 Frame Format of IPv6 CoS Priority



The IP TOS/DS priority function of each port can be enabled individually by programming registers 0x24 and 0x25, and designer can defines IP TOS/DS priority setting for seven kinds of CODEPOINT. If receive a packet with IP TOS/DS CODEPOINT which is not defined, IP1725 provides two kinds of method to handle. One is the zero priority method, the packet will be treated as a lowest priority by programming register 0x26[14] to '0'. The other is the Tag/Port based method, and the packet will be assigned a priority according to its priority setting on tag/port by programming register 0x26[14] to '1'. For example, the bit 0 of register 0x24 corresponds to port 1 and the bit 0 of register 0x25 corresponds to port 17.

5.17.6 TCP/UDP Port Number Based Priority

Related registers	0x2B~0x37

When the CoS based on TCP/UDP port number function is enabled, IP1725 will examine the TCP/UDP destination port number in a packet to decide its priority.

The designer can define the priority of protocols, based on TCP/UDP port number, by programming registers 0x33~0x37. A packet with TCP/UDP port number matched what are listed in registers 0x33~0x37 will be treated as a priority packet according to the corresponding setting in the registers. For example, a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a high priority packet if the register 0x33[2:0] is set to 3b'011. A packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a low priority packet if the register 0x33[2:0] is set to 3b'000.

A packet with TCP/UDP port number matched the user-defined port number range in register 0x2B to 0x30 will be treated as a priority packet according to the setting in the register 0x37. IP1725 provides three groups for user-define port number range. For example, a packet with TCP/UDP port number matched what are defined from register 0x2B to 0x2C will be handled as a high priority packet if the register 0x37[2:0] is set to 3b'011. The TCP/UDP port number base priority function of each port can be enabled individually by programming registers 0x31 and 0x32. For example, the bit 0 of register 0x31 corresponds to port 1 and the bit 0 of register 0x32 corresponds to port 17.

For the setting of TCP/UDP port number, the setting of registers 0x33~0x36 have precedence over user-defined setting. For example, if the priority of FTP (20, 21) is set to low and the priority of the port number (1~21) is set to high for user-defined setting, the priority of port number (20, 21) will be treated as low priority rather than high priority.

Figure 17 TCP/UDP Port Number Based Priority Block Diagram

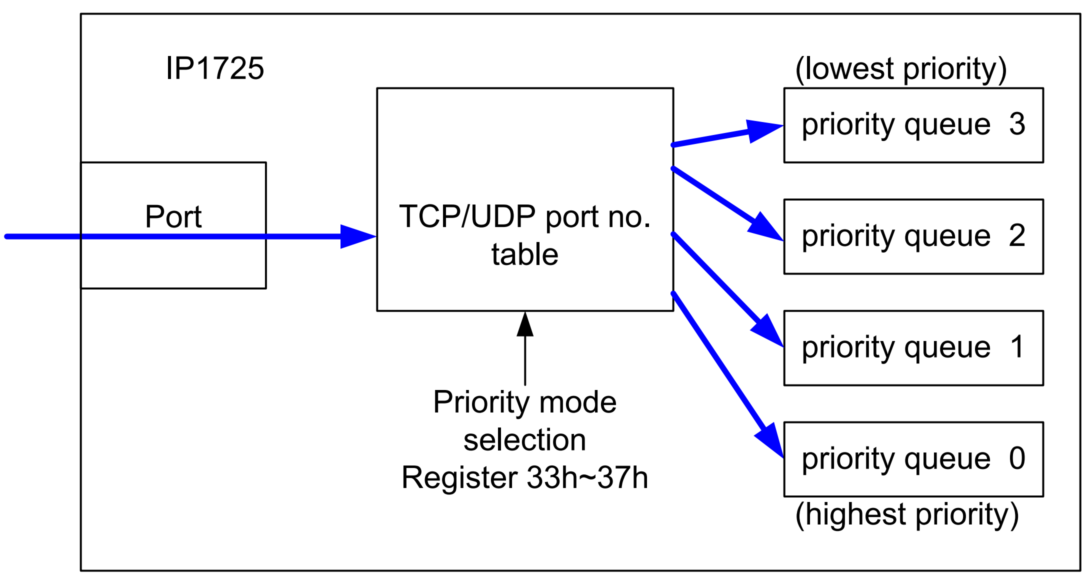


Figure 18 TCP/UDP Port Number Based Priority Selection Table

Register 0x33

bit	14:12	11:9	8:6	5:3	2:0
Protocol	53	25	23	22	20, 21
definition	000: to queue 3 (TCP/UDP port number based Cos function disabled) 001: to queue 2 010: to queue 1 011: to queue 0				

Register 0x34

bit	14:12	11:9	8:6	5:3	2:0
Protocol	123	119	110	80, 8080	69
definition	000: to queue 3 (TCP/UDP port number based Cos function disabled) 001: to queue 2 010: to queue 1 011: to queue 0				

Register 0x35

bit	14:12	11:9	8:6	5:3	2:0
Protocol	1863	443	161, 162	143, 220	137, 138, 139
definition	000: to queue 3 (TCP/UDP port number based Cos function disabled) 001: to queue 2 010: to queue 1 011: to queue 0				

Register 0x36

bit	14:12	11:9	8:6	5:3	2:0
Protocol	67, 68	5050	5190	4000, 8000	3389
definition	000: to queue 3 (TCP/UDP port number based Cos function disabled) 001: to queue 2 010: to queue 1 011: to queue 0				

Register 0x37

bit	8:6	5:3	2:0
Protocol	user define port no. C in register 2Fh and 30h	user define port no. B in register 2Dh and 2Eh	user define port no. A in register 2Bh and 2Ch
definition	000: to queue 3 (TCP/UDP port number based Cos function disabled) 001: to queue 2 010: to queue 1 011: to queue 0		

5.17.7 Supreme Priority

Related registers	0x01[15:13]

When the CoS based supreme function is enabled by programming register 0x01[15] writing to "1", the designer can select one of the three rules by programming register 0x01[14:13]. The configuration is shown in the following table. The detail settings refer to the configuration of the ACL result table, IP address table or MAC address table.

Table 30 Supreme CoS Selection Table

Reg 0x01[14:13]	Supreme CoS
00	ACL result
01	IP address
10	MAC address

5.18 ACL Function

IP1725 supports 16-entry ACL rules. When a packet is received, its Source port number/VLAN entry number, Source IP address, Destination IP address, TCP/UDP Source port or TCP/UDP destination port are recorded and compared to application ACL entry.

When a received packet matched multiple entries, the action table will be applied. If the action table is 'Forward', the packet will be forwarded to destination port. If the action table is 'To CPU', the packet will be forwarded to CPU port only. If the action table is 'Drop', the packet will be dropped. If the action table is 'To Queue 0~3', the packet will be assigned to relative priority mechanism. If the action table is 'Q-in-Q tag 1~4', the packet will be added relative Q-in-Q tag, and then be forwarded to destination port. If the packet doesn't match any entries, it will be treated as 'Forward'. The ACL table is shown in the following table. The detail settings refer to application note.

Table 31 ACL Configuration Table

Entry	Source port/ VLAN entry	Source IP	Destination IP	TCP/UDP Source Port	TCP/UDP Destinatio n Port	Action
Entry 0	15	128.001.002.003	111.222.033.044	0	61	1
Entry 1	0	001.002.003.004	005.006.007.008	1111	1234	2
…	…	…	…	…	…	…
Entry 15	14	192.168.111.123	192.168.001.002	999	500	3

Note: Action = 1: forward; Action = 2: drop; …

5.19 Capture Ethernet Protocol Frame and IP Packet to CPU Port

IP1725 recognize the following type of packets by examining the field listed in the following table.

Table 32 Frame Format of Ethernet Protocol

Protocol	DA	Type	Op code	PPP Protocol	Protocol no. In IP header	Note
In-band management	IP1725's MAC address	--	--	--	--	Global setting
BPDU	01-80-C2-00-00-**00**	--	--	--	--	Global setting
MPCP	01-80-C2-00-00-**01**	--	02~06	--	--	Global setting
Slow	01-80-C2-00-00-**02**	--	--	--	--	Global setting
802.1x	01-80-C2-00-00-**03**	888E	--	--	--	Global setting
LLDP	01-80-C2-00-00-**0E**	--	--	--	--	Global setting
GVRP, GMRP	01-80-C2-00-00-**20~21**	--	--	--	--	Global setting
PPPoE	--	8864	--	0021	--	Global setting
OSPF	--	0800	--	--	89	Global setting
ARP	--	0806	--	--	--	Global setting
ICMP	--	0800	--	--	01	Global setting
IGMP	01-00-5E-XX-XX-XX	0800	--	--	02	Global setting
TCP	--	0800	--	--	06	Global setting
UDP	--	0800	--	--	17	Global setting

Note:
1. **"--" means "don't care".**
2. **Pause frame is not forwarded to CPU.**

5.19.1 In Band Management Frame

Related registers	0x01[10], 0x70[0], 0x3A~0x3C

IP1725 has a default MAC address 00-90-c3-00-00-00. If an incoming packet with DA equaling to IP1725's MAC address, it will be forwarded to the CPU port as long as the register 0x01[10] is set to "1" and register 0x70[0] is set to "1". IP1725's MAC address can be edited by programming registers 0x3A~0x3C.

5.19.2 Layer Two Protocol Frame Capture

Related registers	0x01[2], 0x02[5:0], 0x02[9], 0x05[7], 0x70[0]

IP1725 recognizes layer two protocol frames (BPDU, 802.1x, MPCP, Slow Protocol, GxRP and ARP) as showing in the following table and will decide to forward it to CPU port or drop it according to the setting in registers 0x01[2], 0x02[5:0] and 0x02[9]. The register 0x70[0] defines the port 25 to be the CPU port.

Table 33 Layer Two Protocol Frames Selection Table

Register		BPDU (01-80-C2-00-00-00)	BPDU (01-80-C2-00-00-04~0F)
0x01[2]	0x02[0]		
0	0	Drop	Drop
	1	To CPU port only	
1	X	Broadcast	Broadcast

Note: X means "don't care"

Register		802.1x
0x02[1]	0	Drop or broadcast
	1	To CPU port only

Register		Slow Protocol
0x02[2]	0	Drop
	1	To CPU port only

Register		MPCP	
		0x02[7]=0	0x02[7]=1
0x02[3]	0	Drop	Forward
	1	To CPU port only	

Register		GxRP
0x02[4]	0	Broadcast
	1	To CPU port only

Register		ARP
0x02[5]	0	Forward depend on DA
	1	To DA and CPU port

Register		LLDP	
		0x01[2]=0	0x01[2]=1
0x02[9]	0	Drop	Broadcast
	1	To CPU port only	

5.19.3 Layer Three Protocol Frame Capture

Related registers	0x03, 0x04, 0x70[0]

IP1725 recognizes an incoming ICMP, TCP, UDP, and OSPF packets and will decide to forward it to CPU port or drop it according to the setting in register 0x03[7:0]. The register 0x70[0] defines the port 25 to be the CPU port. The detailed configuration is shown in the following table.

IP1725 also provides two layer three protocols for user to define by editing the register 0x04.

Table 34 Layer Three Protocol Frames Selection Table

Protocol	ICMP	TCP	UDP	OSPF	User define 1	User define 2
	Reg 0x03[1:0]	Reg 0x03[3:2]	Reg 0x03[5:4]	Reg 0x03[7:6]	Reg 0x03[9:8]	Reg 0x03[11:10]
Definition	00: send to its destination port only. 01: send to CPU port and its destination port. 10: send to CPU port only. 11: drop					

5.19.4 PPPoE Protocol Check

Related registers	0x02[6]

IP1725 provides an option to check the PPPoE packets when register 0x02[6] is set to “1”. (This function only work when the layer three protocol is IP protocol)

5.20 Security

5.20.1 MAC Address Based Security

Related registers	0x8A, 0x8B[7:0], 0x8C

IP1725 supports MAC address based security function if register 0x8C[1] is set to “0”. When this function is enabled, IP1725 drops the packet with a SA not found in the address table. This function is valid only if programming registers 0x8A and 0x8B[7:0] disables the address learning function.

IP1725 provides an option to forward the un-known SA packets to CPU when the function is enabled. An un-known SA packet is forwarded to CPU, when bit 0 of register 0x8C is cleared.

IP1725 also supports SA associated with source port if register 0x8C[2] is set to “1”, for example, if packets with specific SA learnt on port 1, when the packets SA that port 2 sent is the same port 1, the packets will not be forwarded. The packets with specific SA can send from any port if register 0x8C[2] is set to “0”.

5.20.2 802.1x Port Base Security

Related registers	0x01[2], 0x01[10], 0x02[1], 0x29, 0x2A

IP1725 supports 802.1x port base security function. If this function is enabled, IP1725 only forwards 802.1x EAPOL packets (DA=01 80 C2 00 00 03 and packet type=88 8E or DA= switch’s MAC address, packet type=88 8E and 0x01[10]=1) to CPU port and drops other types of packets. ARP packets are not affected by this function and are forwarded according to their destination address.

This function can be enabled for each port individually by programming registers 0x29 and 0x2A. Designer has to write “1” to register 0x02[1] to enable 802.1x security function. If bit 1 of register 0x02 is writing to “0”, then all EAPOL packets will be dropped or broadcast depending on 0x01[2].

5.20.3 IP Address Base Security

Related registers	0x83~0x85

IP1725 supports IP address base security function by examining the IP address and source port of an incoming packet. Designer can instruct IP1725 to check source IP address or destination IP address by programming register 0x83[3] and select one of the four matching modes by programming register 0x83[1:0] as shown in the following table. Programming registers 0x84 and 0x85 enables this function, port 1 is corresponding to register 0x84[0] and port 17 is corresponding to register 0x85[0].

For example, if register 0x83[3:0] is writing to 4'b1001, mode 2 is selected. A packet will be dropped by IP1725 if its destination IP doesn't match.

To perform IP security, designer has to fulfill the IP entries, which contains the source port and IP information. There are two ways to decide the location of an IP entry, hashing result and source port by programming register 0x83[2] configuration.

IP1725 supports an option to shift the location of IP entry. If register 0x83[6] is set to "1", IP1725 will add the address of an entry derived from the algorithm mention above by 1~3 according to the setting of register 0x83[5:4] to prevent entry collision in IP address table.

5.20.4 TCP/UDP Port Number Based Security

Related registers	0x31~0x37

IP1725 supports TCP/UDP port number based security function by examining the port number in an incoming packet. Designer can enable the function by setting registers 0x31 and 0x32, port 1 is corresponding to bit 0 of register 0x31 and port 17 is corresponding to bit 0 of register 0x32.

When this function is enabled, a packet with TCP/UDP port number matched that listed in registers 0x33~0x37 will be dropped or forwarded to CPU port. For example, a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be dropped if the register 0x33[2:0] is set to "101". A packet with TCP/UDP port number equal to 25 (SMTP) will be forwarded to CPU if the register 0x33[11:9] is set to "100".

A packet with TCP/UDP port number matched the user-defined port number range in register 0x2B to 0x30 will be dropped or forwarded to CPU port according to the setting in the register 0x37. IP1725 provides three groups for user-define port number range. For example, a packet with TCP/UDP port number matched what are defined from register 0x2B to 0x2C will be dropped if the register 0x37[2:0] is set to 3b'101. The TCP/UDP port number base priority function of each port can be enabled individually by programming registers 0x31 and 0x32. For example, the bit 0 of register 0x31 corresponds to port 1 and the bit 0 of register 0x32 corresponds to port 17.

For the setting of TCP/UDP port number, the setting of registers 0x33~0x36 have precedence over user-defined setting. For example, if the security of FTP (20, 21) is set to drop and the security of the port number (1~21) is set to forward to CPU port for user-defined setting, a packet with port number (20, 21) will be dropped rather than forwarded to CPU port.

Figure 19 TCP/UDP Port Number Based Security Selection Table

Register 0x33

bit	14:12	11:9	8:6	5:3	2:0
Protocol	53	25	23	22	20, 21
definition	100: to CPU 101: to drop				

Register 0x34

bit	14:12	11:9	8:6	5:3	2:0
Protocol	123	119	110	80, 8080	69
definition	100: to CPU 101: to drop				

Register 0x35

bit	14:12	11:9	8:6	5:3	2:0
Protocol	1863	443	161, 162	143, 220	137, 138, 139
definition	100: to CPU 101: to drop				

Register 0x36

bit	14:12	11:9	8:6	5:3	2:0
Protocol	67, 68	5050	5190	4000, 8000	3389
definition	100: to CPU 101: to drop				

Register 0x37

bit	8:6	5:3	2:0
Protocol	user define port no. C in register 2Fh and 30h	user define port no. B in register 2Dh and 2Eh	user define port no. A in register 2Bh and 2Ch
definition	100: to CPU 101: to drop		

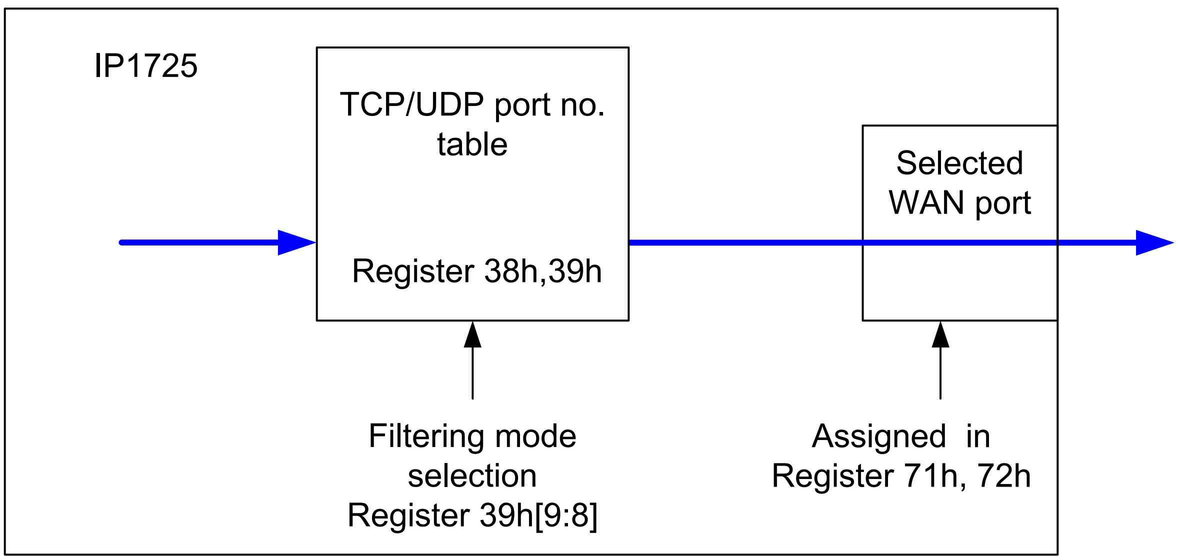
5.21 WAN Port Filtering

Related registers	0x2B~0x30, 0x38, 0x39, 0x71, 0x72

IP1725 supports a function to enable/disable a WAN port to send out packets with specific TCP/UDP port number by programming register 0x39[9] to '1'. Each port can be configured to be WAN port individually by programming registers 0x71 and 0x72. When this function is enabled, IP1725 will forward or drop a packet with TCP/UDP port number defined in registers 0x38 and 0x39[6:0] to WAN port according to the setting of 0x39[8].

If designer defined TCP/UDP port number is selected, 0x39[6:4], IP1725 handles packets according to the TCP/UDP port number defined in registers 0x2B~0x30.

Figure 20 WAN Port Filtering Block Diagram



5.22 Port Mirroring Security

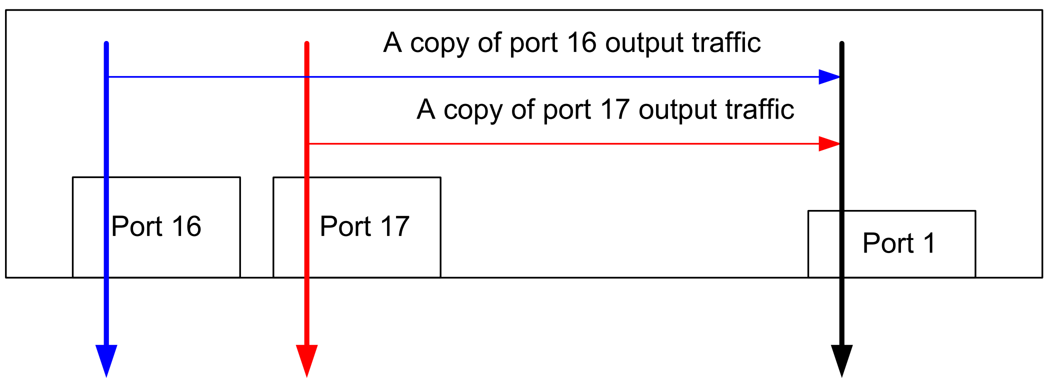
Related registers	0x90~0x93

In some circumstances, the network administrator requires to monitor the network status. The port mirroring function helps the network administrator diagnose the network.

A port mirroring function is accomplished by assigning monitored ports (source ports), snooping ports (destination ports) and snooping method. IP1725 will copy the traffic of monitored ports to all snooping ports. The IP1725 supports three kinds of mirroring methods: the ingress, the egress and ingress plus egress. It is defined in register 0x93[10:9], registers 0x92 and 0x93[8:0] define the ports to be monitored (mirroring source), registers 0x90 and 0x91 specifies the ports to snoop (mirroring destination).

For example, if designer wants to monitor the output traffic of port 16 and port 17 from port 1 as shown in the following figure. He has to write “01” to register 0x93[10:9] to choose monitor method to be output traffic, write 0x8000 and 0x0001 to registers 0x92 and 0x93[8:0] to select port 16 and port 17 to be monitored ports, write 0x0001 and 0x0000 to registers 0x90 and 0x91 to select port 1 as a monitoring port. IP1725 will copy the traffic out of port 16 and port 17 to port 1.

Figure 21 Port Mirroring Security Block Diagram



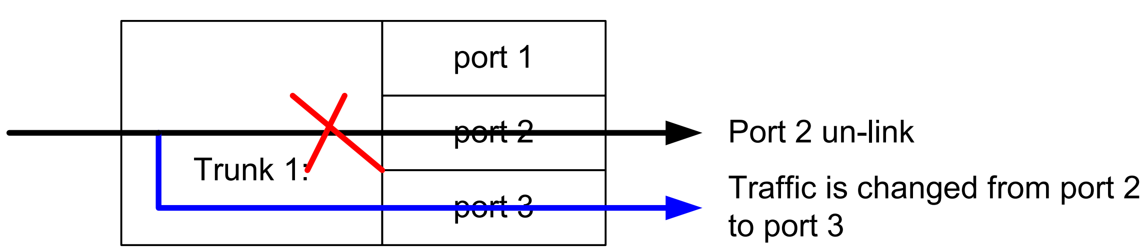
5.23 Trunk Channel

Related registers	0x8F

5.23.1 Trunk Channel Behavior

IP1725 supports two kinds of trunk channels consisting of trunk 1 group and trunk 2 group by programming registers 0x8F[10:8] and 0x8F[13:11]. Each trunk group may comprise 2 to 4 ports. Designer can configure the trunk group members individually by writing non-zero values to the corresponding bits of a port in the registers 0x8F[3:0] and 0x8F[7:4] for trunk 1 groups and trunk 2 groups. A trunk channel works as if a “big” port with multiple times of bandwidth. If the destination port of a packet is un-link, IP1725 forwards the packet to the other port of the trunk(auto recovery).

Figure 22 Trunk Channel Behavior Block Diagram



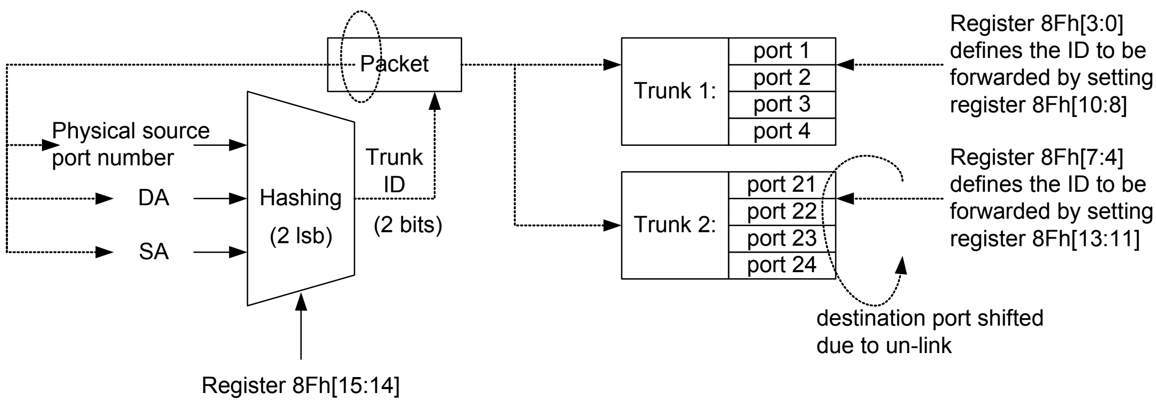
5.23.2 Load Balance

To fully utilize the bandwidth in a trunk channel, IP1725 supports load balance function. A physical port of a trunk forwards a packet only if the trunk ID of the packet matches the ID setting of the port. That is, when a packet is forwarded to a port in a trunk, its destination port is according to trunk ID.

IP1725 performs a hashing algorithm to calculate a 2-bit trunk ID of a packet. It is used to select one of the trunk ports to forward packets. Designer can select the least significant 2 bits hashing algorithm to be based on physical port number, SA, DA, or SA XOR DA by programming register 0x8F[15:14].

If the destination port of a trunk is un-link, the packet will be forward the port shifted by 2. If the port is un-link, too, the packet will be forward the port shifted by 3. For example, if port 1 is un-link, its packet will be forwarded to port 3. If port 3 is un-link, too, the packet will be forwarded to port 4.

Figure 23 Load Balance Block Diagram



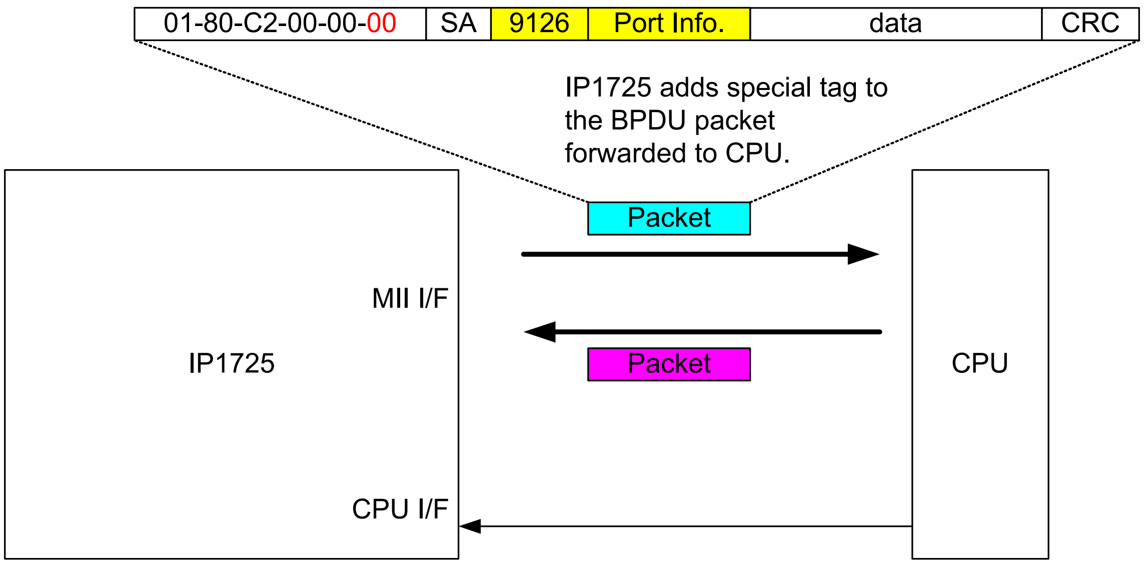
5.24 Spanning Tree

Related registers	0x01[2], 0x02[0], 0x46, 0x49, 0x70[0], 0xEF~0xF2

5.24.1 BPDU Packet Forwarding

IP1725 supports spanning tree function with the following features:
1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU through port 25 and add special tag for source port information(optional), and special tag type is defined in register 0x49. The function is enabled by writing “1” to register 0x02[0], writing “0” to register 0x01[2], writing “1” to register 0x46 and writing “1” to register 0x70[0].

Figure 24 BPDU Packet Forwarding Block Diagram



5.24.2 Port States

To support IEEE802.1D spanning tree protocol, each port of IP1725 supports four states, as shown in the following table. Each port of IP1725 can be set in one of the four spanning tree states individually by programming registers 0xEF to 0xF2.

Table 35 Port States Selection Table

	Discard state	Block state	Learning state	Forwarding state
Corresponding bit 0 of register 0xEF or 0xF0	0	1	0	1
Corresponding bit 1 of register 0xF1 or 0xF2	0	0	1	1

5.25 Non-association Port

Related registers	0xED, 0xEE

IP1725 provide an option to support non-association port function, these ports will not receive packets from each other if the function is enabled, even if the ports belong to same VLAN. The non-association port can be enabled by writing “1” to corresponding bit of registers 0xED and 0xEE. For example, port 1 and port 17 of IP1725 will not be forwarded packets to each other if registers 0xED and 0xEE are written to 16’h0001 and 16’h0001.

5.26 Port Base Address Flush

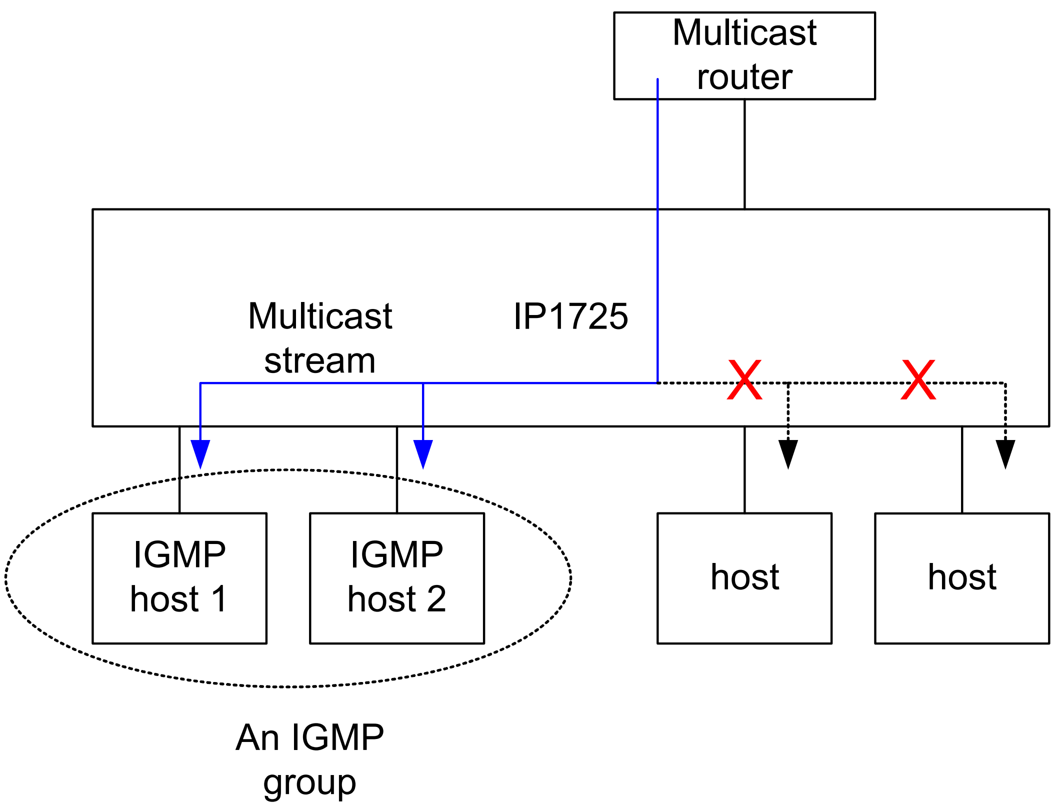
Related registers	0xF3, 0xF4

IP1725 can clear the address learnt by specific port. The specific port can be enabled by writing “1” to corresponding bit of registers 0xF3 and 0xF4[8:0], and trigger the port base address flush function by writing “1” to register 0xF4[9].

5.27 IGMP Snooping

For a switch without IGMP snooping, a multicast packet is forwarded to all ports, that is, it is treated as a broadcast packet. With IGMP snooping, a multicast packet of a group is only forwarded to ports that are members of that group. IGMP (Internet Group Management Protocol) is used to establish membership in a Multicast group. It significantly reduces multicast traffic in the LAN.

Figure 25 IGMP Snooping Block Diagram

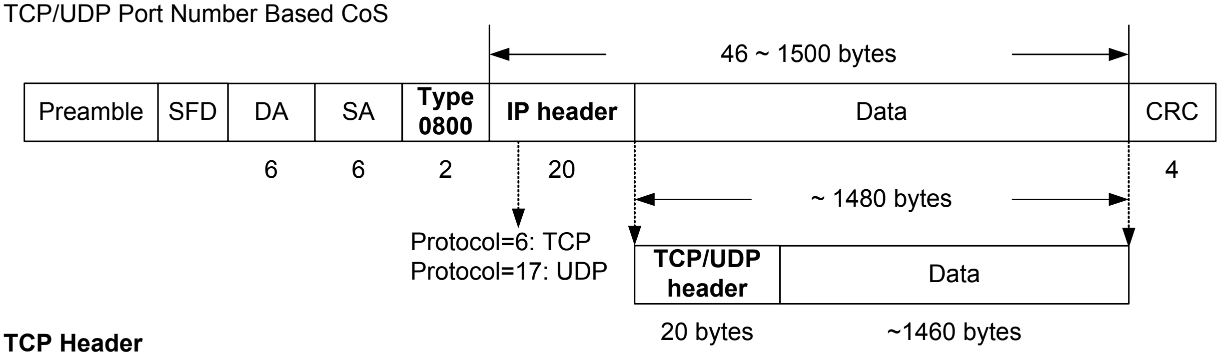


5.28 Frame Format

5.28.1 Frame Format of TCP/UDP Header

Figure 26 TCP/UDP Header Frame Format

TCP/UDP Port Number Based CoS



TCP Header

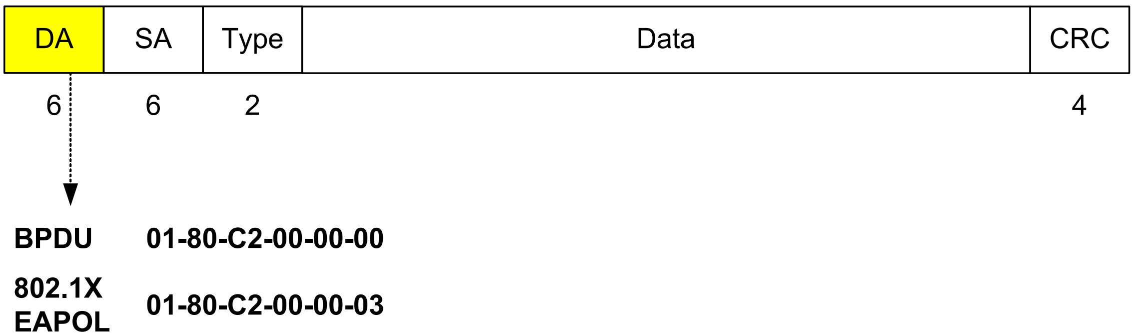
<table>
<tr><td>0</td><td></td><td colspan="3">8</td><td colspan="3"></td><td>16</td><td>24</td><td>31</td></tr>
<tr><td colspan="8">Source port</td><td colspan="2">Destination port</td></tr>
<tr><td colspan="10">Sequence number</td></tr>
<tr><td colspan="10">Acknowledge number</td></tr>
<tr><td>HLEN</td><td>Reserved</td><td>URG</td><td>ACK</td><td>PSH</td><td>RST</td><td>SYN</td><td>FIN</td><td colspan="2">Window</td></tr>
<tr><td colspan="8">Check Sum of TCP header (16)</td><td colspan="2">Urgent pointer</td></tr>
<tr><td colspan="9">Options</td><td>Padding</td></tr>
</table>

UDP Header

0	8	16	24	31
Source port		**Destination port**		
Length		Check Sum of UDP header		

5.28.2 Frame Format of BPDU and 802.1X

Figure 27 BPDU and 802.1X Frame Format



5.28.3 Frame Format of ARP, Slow Protocol, MPCP, GVRP, GMRP, and LLDP

Figure 28 ARP Frame Format

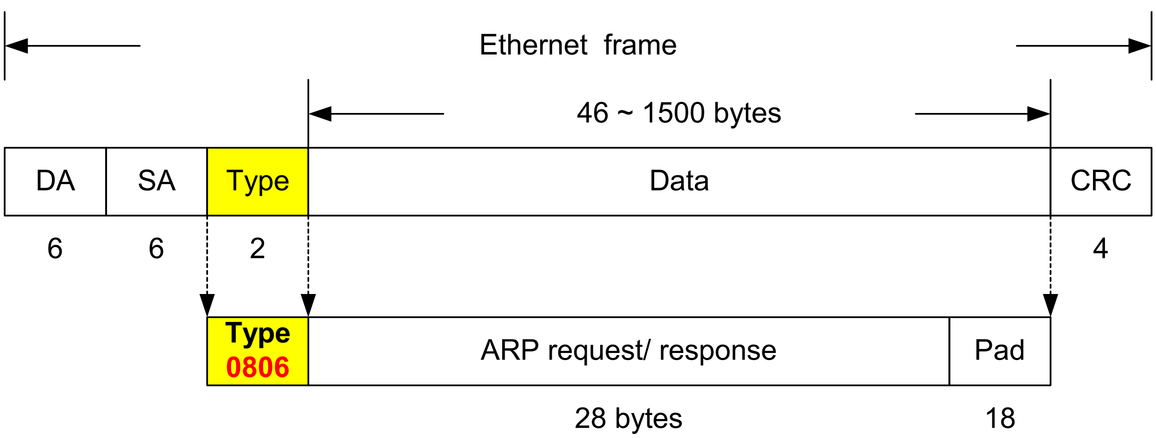


Figure 29 Slow Protocol Frame Format

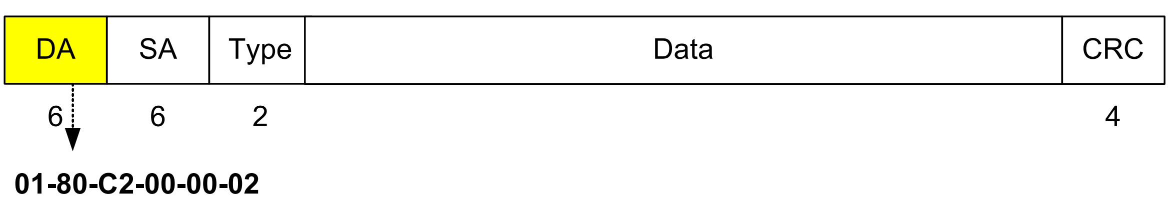


Figure 30 MPCP Frame Format

DA	SA	Type	Op code	Data	CRC
6	6	2	2		4

01-80-C2-00-00-01

Figure 31 GVRP and GMRP Frame Format

DA	SA	Type	Data	CRC
6	6	2		4

01-80-C2-00-00-20~21

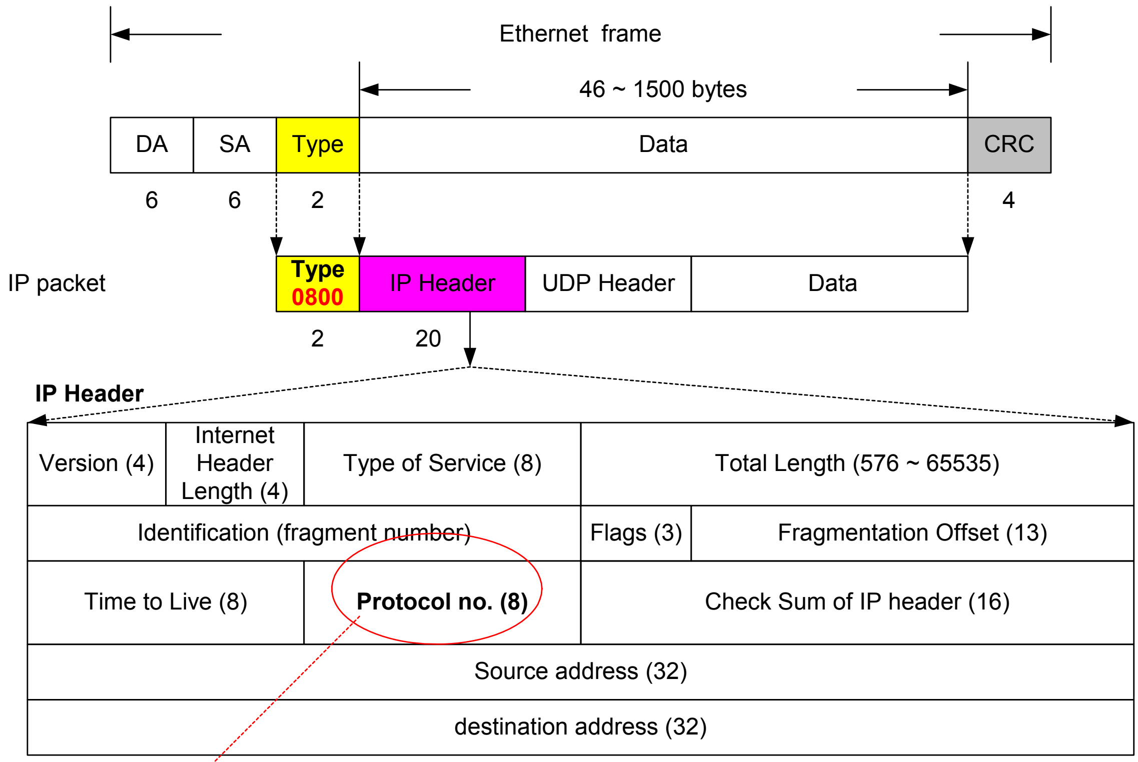
Figure 32 LLDP Frame Format

DA	SA	Type	Data	CRC
6	6	2		4

01-80-C2-00-00-0E

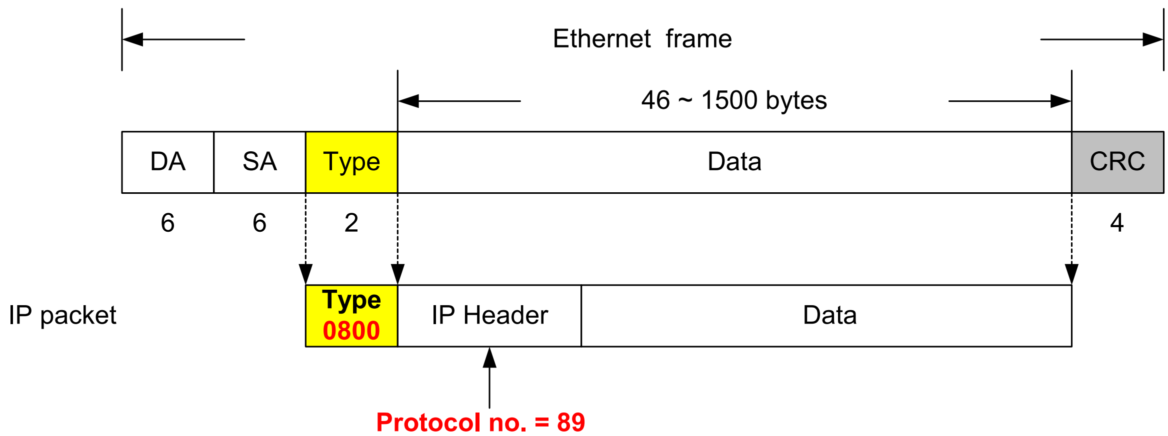
5.28.4 Frame Format of ICMP, IGMP, TCP, UDP, and OSPF

Figure 33 ICMP, IGMP, TCP, and UDP Frame Format



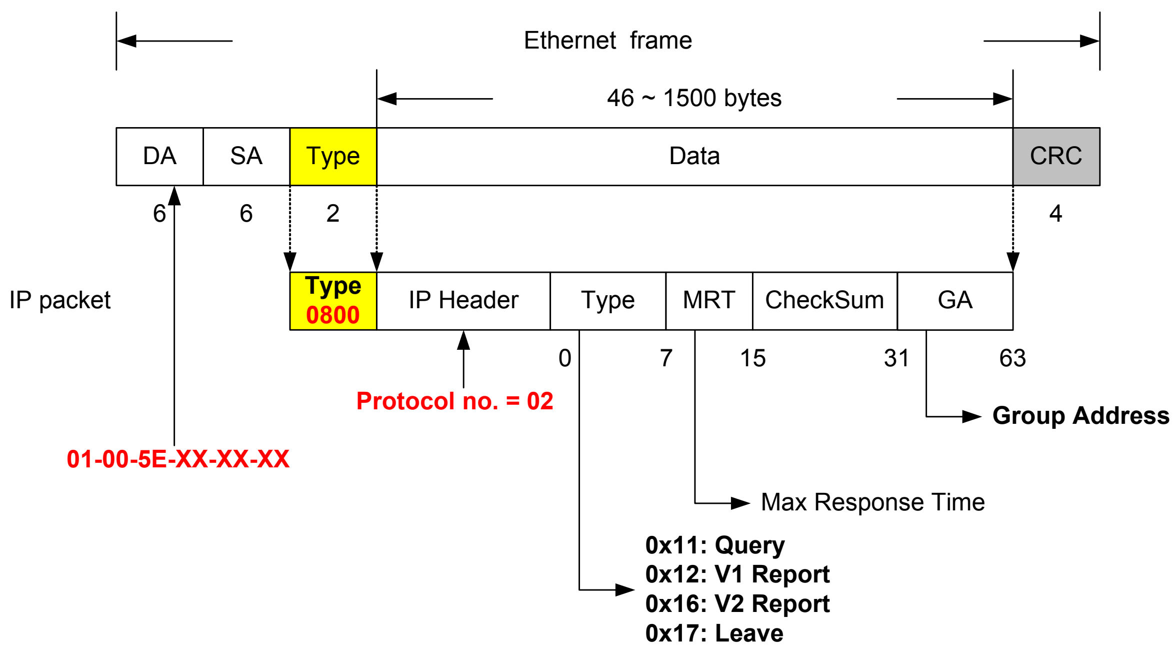
Protocol no.	Name
1	ICMP (Internet Control Message Protocol)
2	IGMP (Internet Group Management Protocol)
6	TCP (transmission Control Protocol)
17	UDP (User Datagram Protocol)

Figure 34 OSPF (Open Shortest Path First) Frame Format



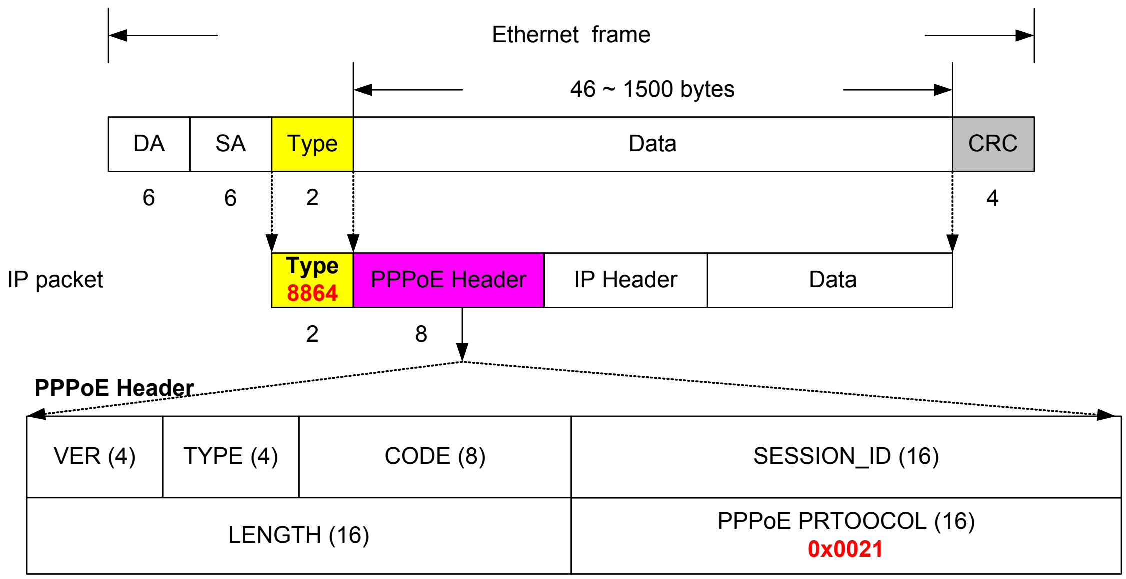
5.28.5 Frame Format of IGMP

Figure 35 IGMP Frame Format



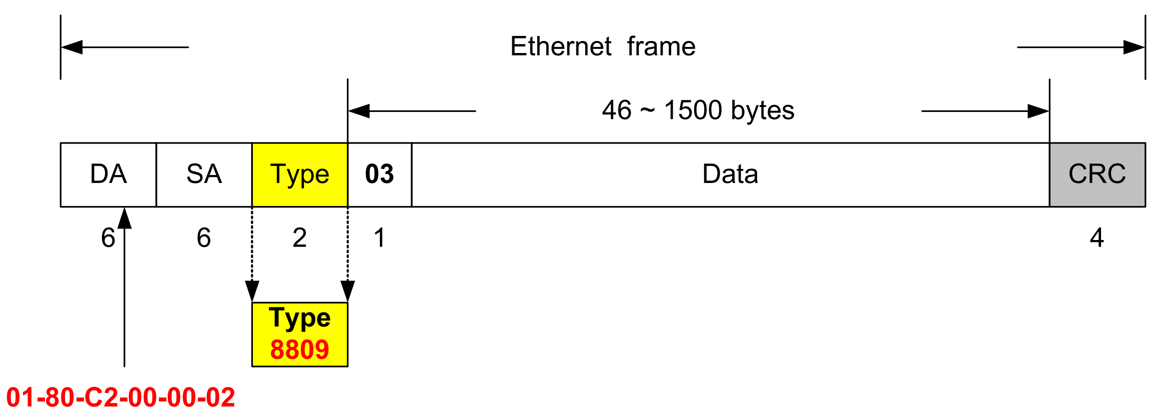
5.28.6 Frame Format of PPPoE

Figure 36 PPPoE (Point to Point Over Ethernet) Frame Format



5.28.7 Frame Format of 802.3 OAM

Figure 37 802.3 OAM Frame Format



5.29 Auto MDI/MDIX

Related registers	0x63, 0x64

In Auto MDIX mode, IP1725 detects the link activity for 80-100ms to determine whether it should swap both pairs. If no link activity is detected within this time, IP1725 waits a random time longer than 80ms and swap transmit/receive pair.

6 Register Description

6.1 PHY Register

6.1.1 PHY Register Map

Table 36 PHY Register Map

Register	Description	Default	Note
0	Control Register	16h3000	X24
1	Status Register	16h7849	X24
2	PHY Identifier 1 Register	16h0243	X1
3	PHY Identifier 2 Register	16h0D80	X1
4	Auto-Negotiation Advertisement Register		X24
5	Auto-Negotiation Link Partner Ability Register	16h0000	X24
6	Auto-Negotiation Expansion Registers	16h0000	X24

X1: 24 ports share the register
X24: Each port has its individual register

Table 37 Register Symbol Abbreviations

Type	Description
R	Read
W	Write
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
LL	Latching Low
LH	Latching High

6.1.2 Control Register

Table 38 Control Register

MII register 0 of PHY8~31 (Each PHY has its own MII register 0 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	0.15	--	RW/ SC	Reset The PHY is reset if user write "1" to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP1725.	0
8~31	0.14	--	R/W	Loop back 1 : loop back mode 0 : normal operation When this bit set, IP1725 will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN. Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test.	0
8~31	0.13	--	RW	Speed Selection 1 : 100Mbps 0 : 10Mbps It is valid only if bit 0.12 is set to be 0.	1
8~31	0.12	--	RW	Auto-Negotiation Enable 1 : auto-negotiation enable 0 : auto-negotiation disable	1
8~31	0.11	--	R/W	Power Down 1 : power down mode 0 : normal operation	0
8~31	0.10	--		Isolate IP1725 doesn't support this function.	0
8~31	0.9	--	RW SC	Restart Auto-Negotiation 1 : re-starting auto-negotiation 0 : normal operation	0
8~31	0.8	--	R/W	Duplex mode 1 : full duplex 0 : half duplex It is valid only if bit 0.12 is set to be 0.	0
8~31	0.7	--	R/W	Collision test	0
8~31	0[6:0]	--	RO	Reserved	0

6.1.3 Status Register

Table 39 Status Register

MII register 1 of PHY8~31 (Each PHY has its own MII register 1 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	1.15	--	RO	100Base-T4 Capable 1 : 100Base-T4 capable 0 : not 100Base-T4 capable IP1725 does not support 100Base-T4. This bit is fixed to be 0.	0
8~31	1.14	--	RO	100Base-X full duplex Capable 1 : 100Base-X full duplex capable 0 : not 100Base-X full duplex capable	1
8~31	1.13	--	RO	100Base-X half duplex Capable 1 : 100Base-X half duplex capable 0 : not 100Base-X half duplex capable	1
8~31	1.12	--	RO	10Base-T full duplex Capable 1 : 10Base-T full duplex capable 0 : not 10Base-T full duplex capable	1
8~31	1.11	--	RO	10Base-T half duplex Capable 1 : 10Base-T half duplex capable 0 : not 10Base-T half duplex capable	1
8~31	1[10:7]	--	RO	Reserved	0
8~31	1.6	--	RO	MF Preamble Suppression 1 : preamble may be suppressed 0 : preamble always required	1
8~31	1.5	--	RO	Auto-Negotiation Complete 1 : auto-negotiation complete 0 : auto-negotiation in progress When read as logic 1, indicates that the auto-negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the auto-negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If auto-negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0
8~31	1.4	--	RO LH	Remote Fault 1 : remote fault detected 0 : not remote fault detected When read as logic 1, indicates that IP1725 has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP1725 reset.	0
8~31	1.3	--	RO	Auto-Negotiation Ability 1 : auto-negotiation capable 0 : not auto-negotiation capable When read as logic 1, indicates that IP1725 has the ability to perform auto-negotiation.	1

MII register 1 of PHY8~31 (Each PHY has its own MII register 1 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	1.2	--	RO LL	Link Status 1 : link pass 0 : link fail When read as logic 1, indicates that IP1725 has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
8~31	1.1	--		Jabber Detect 1 : jabber condition detected 0 : no jabber condition detected When read as logic 1, indicates that IP1725 has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP1725 reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled.	0
8~31	1.0	--	RO	Extended Capability 1 : extended register capabilities 0 : no extended register capabilities IP1725 has extended register capabilities.	1

6.1.4 PHY Identifier 1 Register

Table 40 PHY Identifier 1 Register

MII register 2 of PHY8~31 (24 PHYs share the MII register)

PHY	MII	ROM	R/W	Description	Default
8~31	2	--	RO	IP1725 OUI (Organizationally Unique Identifier) ID, the msb is 3^{rd} bit of IP1725 OUI ID, and the lsb is 18^{th} bit of IP1725 OUI ID. IP1725 OUI is 0090C3.	16'h0243

6.1.5 PHY Identifier 2 Register

Table 41 PHY Identifier 2 Register

MII register 3 of PHY8~31 (24 PHYs share the MII register)

PHY	MII	ROM	R/W	Description	Default
8~31	3[15:10]	--	RO	PHY Identifier IP1725 OUI ID, the msb is 19th bit of IP1725 OUI ID, and lsb is 24th bit of IP1725 OUI ID.	6'h03
8~31	3[9:4]	--	RO	Manufacture's Model Number IP1725 model number	6'h18
8~31	3[3:0]	--	RO	Revision Number IP1725 revision number	0

6.1.6 Auto-Negotiation Advertisement Register

Table 42 Auto-Negotiation Advertisement Register

MII register 4 of PHY8~31 (Each PHY has its own MII register 4 with different PHY address)

<table>
<tr><th>PHY</th><th>MII</th><th>ROM</th><th>R/W</th><th colspan="4">Description</th><th>Default</th></tr>
<tr><td>8~31</td><td>4.15</td><td>--</td><td>RO</td><td colspan="4">Next Page
Not supported. This bit is fixed to be 0.</td><td>0</td></tr>
<tr><td>8~31</td><td>4.14</td><td>--</td><td>RO</td><td colspan="4">Reserved by IEEE, write as 0, ignore on read.</td><td>0</td></tr>
<tr><td>8~31</td><td>4.13</td><td>--</td><td>R/W</td><td colspan="4">Remote Fault
1 : advertises that this port has detected a remote fault
0 : there is no remote fault</td><td>0</td></tr>
<tr><td>8~31</td><td>4[12:11]</td><td>--</td><td>RO</td><td colspan="4">Reserved for future IEEE use, write as 0, ignore on read.</td><td>0</td></tr>
<tr><td>8~31</td><td>4.10</td><td>--</td><td>RW</td><td colspan="4">Pause
1 : advertises that this port has implemented pause function
0 : no pause function supported</td><td>Set by X_EN</td></tr>
<tr><td>8~31</td><td>4.9</td><td>--</td><td>RO</td><td colspan="4">100BASE-T4 Not supported</td><td>0</td></tr>
<tr><td rowspan="7">8~31</td><td rowspan="7">4.8</td><td rowspan="7">--</td><td rowspan="7">R/W</td><td colspan="4">100BASE-TX Full Duplex
1 : 100BASE-TX full duplex is supported
0 : 100BASE-TX full duplex is not supported</td><td rowspan="7">*</td></tr>
<tr><td>FORCE</td><td>FORCE100</td><td>FORCE_FULL</td><td>Default</td></tr>
<tr><td>0</td><td>Don't care</td><td>Don't care</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td rowspan="2">8~31</td><td rowspan="2">4.7</td><td rowspan="2">--</td><td rowspan="2">R/W</td><td colspan="4">100BASE-TX
1 : 100BASE-TX is supported
0 : 100BASE-TX is not supported</td><td rowspan="2">*</td></tr>
<tr><td>FORCE</td><td>FORCE100</td><td>FORCE_FULL</td><td>Default</td></tr>
</table>

MII register 4 of PHY8~31 (Each PHY has its own MII register 4 with different PHY address)

PHY	MII	ROM	R/W	Description				Default
				0	Don't care	Don't care	1	
				1	0	0	0	
				1	0	1	0	
				1	1	0	1	
				1	1	1	1	
8~31	4.6	--	R/W	10BASE-T Full Duplex 1 : 10BASE-T full duplex is supported 0 : 10BASE-T full duplex is not supported				*
				FORCE	FORCE100	FORCE_FULL	Default	
				0	Don't care	Don't care	1	
				1	0	0	0	
				1	0	1	1	
				1	1	0	0	
				1	1	1	1	
8~31	4.5	--	R/W	10BASE-T 1 : 10BASE-T is supported 0 : 10BASE-T is not supported				1
8~31	4[4:0]	--	RO	Selector Field Use to identify the type of message being sent by Auto-Negotiation.				5'b00001

6.1.7 Auto-Negotiation Link Partner Ability Register

Table 43 Auto-Negotiation Link Partner Ability Register

MII register 5 of PHY8~31 (Each PHY has its own MII register 5 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	5.15		RO	Next Page 1 : next page ability is supported by link partner 0 : next page ability does not supported by link partner	0
8~31	5.14		RO	Acknowledge 1 : link partner has received the ability data word 0 : not acknowledge	0
8~31	5.13		RO	Remote Fault 1 : link partner indicates a remote fault 0 : no remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (remote fault) will set to logic 1.	0
8~31	5[12:11]	--	RO	Reserved by IEEE for future use, write as 0, read as 0.	0

MII register 5 of PHY8~31 (Each PHY has its own MII register 5 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	5.10	--	RW	Pause 1 : link partner support IEEE802.3x 0 : link partner does not support IEEE802.3x When Nway enabled, this bit reflects link partner ability. (read only) When Nway disabled, this bit can be set by SMI. (read/write) When in 100FX, this bit is set by X_EN or SMI.	0
8~31	5.9	--	RO	100BASE-T4 1 : link partner support 100BASE-T4 0 : link partner does not support 100BASE-T4	0
8~31	5.8	--	RO	100BASE-TX Full Duplex 1 : link partner support 100BASE-TX full duplex 0 : link partner does not support 100BASE-TX full duplex	0
8~31	5.7	--	RO	100BASE-TX 1 : link partner support 100BASE-TX 0 : link partner does not support 100BASE-TX For 100FX mode, this bit is set. When Nway is disabled, this bit is set if register 0.13=1.	0
8~31	5.6	--	RO	10BASE-T Full Duplex 1 : link partner support 10BASE-T full duplex 0 : link partner does not support 10BASE-T full duplex	0
8~31	5.5	--	RO	10BASE-T 1 : link partner support 10BASE-T 0 : link partner does not support 10BASE-T When Nway is disabled, this bit is set if register 0.13=0	0
8~31	5[4:0]	--	RO	Selector Field Protocol selector of the link partner.	5'b000 00

6.1.8 Auto-Negotiation Expansion Register

Table 44 Auto-Negotiation Expansion Register

MII register 6 of PHY8~31 (Each PHY has its own MII register 6 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	6[15:5]	--	RO	Reserved	0
8~31	6.4	--	RO	1 : a fault has been detected via parallel detection function 0 : a fault has not been detected via parallel detection function	0
8~31	6.3	--	RO	1 : link partner is next page able 0 : link partner is not next page able	0
8~31	6.2	--	RO	1 : IP1725 next page able 0 : IP1725 is not next page able This bit is fixed to be "0" in IP1725.	0
8~31	6.1	--	RO/ LH	1 : a new page has been received 0 : a new page has not been received	0

MII register 6 of PHY8~31 (Each PHY has its own MII register 6 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	6.0	--	RO	If Nway is enabled, this bit means: 1 : link partner is auto-negotiation able 0 : link partner is not auto-negotiation able In 100FX or Nway disabled, this bit always =0.	0 (Nway) (100FX)

6.1.9 PHY Spec. Control Register

Table 45 PHY Spec. Control Register

MII register 16 of PHY8~31 (Each PHY has its own MII register 16 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	16[15]	--	R/W	Reserved	0
8~31	16[14]	--	R/W	Reserved	0
8~31	16[13]	--	R/W	Reserved	0
8~31	16[12]	--	R/W	Reserved	0
8~31	16[11]	--	R/W	Reserved	0
8~31	16[10]	--	R/W	Reserved	0
8~31	16[9]	--	R/W	Reserved	0
8~31	16[8]	--	R/W	Reserved	1
8~31	16[7]	--	R/W	Link down power saving（LDPS） mode 1 : Enable LDPS mode, PHY will transmit link pulse in sleep mode. 0 : Disable LDPS mode,	1
8~31	16[6]	--	R/W	Reserved	0
8~31	16[5]	--	R/W	Reserved	0
8~31	16[4]	--	R/W	Far end fault function 1 : Disable far end fault function when the chip operates at fiber mode. 0 : Enable far end fault function when the chip operates at fiber mode.	0
8~31	16[3]	--	R/W	Reserved	1
8~31	16[2]	--	R/W	Reserved	1
8~31	16[1]	--	R/W	Reserved	0
8~31	16[0]	--	R/W	Reserved	0

6.1.10 MDI/MDIX Control Register

Table 46 MDI/MDIX Control Register

MII register 23 of PHY8~31 (Each PHY has its own MII register 23 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
8~31	23[15:8]	--	RW	Auto_MDIX 1 : Enable auto crossover function 0 : Disable auto crossover function	8'hFF
8~31	23[7:0]	--	RW	MDI/MDIX channel selection 1 : Select MDIX channel 0 : Select MDI channel	8'h00

6.2 Switch Register

6.2.1 Switch Register Map

Table 47 Switch Register Map (Reg. Addr. 00h~FFh)

REG ADDR	Description	REG ADDR	Description
00h	Reserved	73h	Internal Status
01h	General MAC Operation Behavior	74h~75h	Interrupt Signal Setting
02h	Layer 2 Protocol Frame capture	76h	MII Interface Signal Timing Setting
03h	Layer 3 Protocol Frame capture	77h	Reserved
04h	User Define Layer 3 Protocol Type	78h~79h	CPU Read/Write EEPROM Command
05h~1Dh	Egress/Ingress Rate Control	7Ah	Reserved
1Eh~21h	Port Base Priority	7Bh~81h	Frame Buffer Information
22h~23h	VLAN Tag Base Priority	82h	ARL Operation Setting
24h~25h	IP CoS Base Priority	83h	Source/Destination IP Address Security
26h	Differentiated Services Priority	84h~85h	IP Filter Enable
27h	Stag/Ctag Ingress Control	86h~87h	Broadcast Storm Control Setting
28h	Reserved	88h	ARP and ICMP Storm Control Setting
29h~2Ah	802.1x Port Lock	89h	Aging Timer Threshold Setting
2Bh~30h	User Define TCP/UDP Port Number A~C Range Setting	8Ah~8Bh	Enable Source MAC Address Learning
31h~37h	TCP/UDP Port Number Base Priority	8Ch	Security Configuration
38h~39h	TCP/UDP Port Number Base Filter Select to Wan Port	8Dh~8Eh	VLAN Uplink Function Support Selection
3Ah~3Ch	MAC Address	8Fh	Trunk Function Setting
3Dh~3Fh	CPU Read Statistic Counter	90h~93h	Sniffer Function Configuration
40h~41h	Port Statistic Counter Selection	94h	IGMP Snooping Function Configuration
42h~45h	Output Queue Configuration	95h~96h	Router Port
46h	CPU Port (Port 25) Special Tag	97h~9Ah	VLAN Output Port Add/Remove Tag Operation Configuration
47h~48h	Tag Inserting PVID/PRI Selection	9Bh~A3h	PVID Index Setting
49h	Special Tag Type-Length Definition	A4h~A8h	PVID Priority Setting
4Ah~53h	Q-IN-Q Double Tag	A9h~ECh	VLAN Setting
54h	LED Mode Setting	EDh~EEh	Non-association Port Setting
55h~56h	Auto Negotiation Configuration	EFh~F2h	Spanning Tree State
57h~58h	Speed Setting	F3h~ F4h	Port Base Address Flush
59h~5Ah	Duplex Setting	F5h~F8h	CPU Read/Write Address Table
5Bh~5Ch	Pause Setting	F9h	Table Address Access Method
5Dh~5Eh	Asymmetric Pause Setting	FAh~FCh	ACL/VID/VID-Tag Configuration
5Fh~60h	Backpressure Setting	FDh	Reserved
61h	CPU Port PHY Address Setting	FEh~ FFh	802.3 OAM LoopBack Enable
62h	Reserved		
63h~64h	CPU Read/Write PHY Register Command		
65h~6Dh	Port Status		
6Eh	Software Reset Information		
6Fh	Built In Self Test Information		
70h	CPU Mode Setting		
71h~72h	WAN Port Setting For TCP/UDP Port Filter setting		

6.2.2 Switch Register EEPROM Map

Table 48 Switch Register EEPROM Map (Rom. Addr. 00h~1FFh)

ROM ADDR	7	6	5	4	3	2	1	0
00h~01h	Refer Table 15/16							
02h~03h	General MAC Operation Behavior							
04h~05h	Layer 2 Protocol Frame capture							
06h~07h	Layer 3 Protocol Frame capture							
08h~09h	User Define Layer 3 Protocol Type							
0Ah~3Bh	Egress/Ingress Rate Control							
3Ch~43h	Port Base Priority							
44h~47h	VLAN Tag Base Priority							
48h~4Bh	IP CoS Base Priority							
4Ch~4Dh	Differentiated Services Priority							
4Eh~4Fh	Stag/Ctag Ingress Control							
50h~51h	Reserved							
52h~55h	802.1x Port Lock							
56h~61h	User Define TCP/UDP Port Number A~C Range Setting							
62h~6Fh	TCP/UDP Port Number Base Priority							
70h~73h	TCP/UDP Port Number Base Filter Select to Wan Port							
74h~79h	MAC Address							
7Ah~7Fh	CPU Read Statistic Counter							
80h~83h	Port Statistic Counter Selection							
84h~8Bh	Output Queue Configuration							
8Ch~8Dh	CPU Port (Port 25) Special Tag							
8Eh~91h	Tag Inserting PVID/PRI Selection							
92h~93h	Special Tag Type-Length Definition							
94h~A7h	Q-IN-Q Double Tag							
A8h~A9h	LED Mode Setting							
AAh~ADh	Auto Negotiation Configuration							
AEh~B1h	Speed Setting							
B2h~B5h	Duplex Setting							
B6h~B9h	Pause Setting							
BAh~BDh	Asymmetric Pause Setting							
BEh~C1h	Backpressure Setting							
C2h~C3h	CPU Port PHY Address Setting							
C4h~C5h	Reserved							
C6h~C9h	CPU Read/Write PHY Register Command							
CAh~DBh	Port Status							
DCh~DDh	Software Reset Information							
DEh~DFh	Built In Self Test Information							
E0h~E1h	CPU Mode Setting							
E2h~E5h	WAN Port Setting For TCP/UDP Port Filter setting							
E6h~E7h	Internal Status							
E8h~EBh	Interrupt Signal Setting							
ECh~EDh	MII Interface Signal Timing Setting							
EEh~EFh	Reserved							
F0h~F3h	CPU Read/Write EEPROM Command							
F4h~F5h	Reserved							
F6h~103h	Frame Buffer Information							
104h~105h	ARL Operation Setting							
106h~107h	Source/Destination IP Address Security							
108h~10Bh	IP Filter Enable							
10Ch~10Fh	Broadcast Storm Control Setting							
110h~111h	ARP and ICMP Storm Control Setting							
112h~113h	Aging Timer Threshold Setting							
114h~117h	Enable Source MAC Address Learning							
118h~119h	Security Configuration							
11Ah~11Dh	VLAN Uplink Function Support Selection							
11Eh~11Fh	Trunk Function Setting							
120h~127h	Sniffer Function Configuration							
128h~129h	IGMP Snooping Function Configuration							
12Ah~12Dh	Router Port							
12Eh~135h	VLAN Output Port Add/Remove Tag Operation Configuration							
136h~147h	PVID Index Setting							
148h~151h	PVID Priority Setting							
152h~1D9h	VLAN Setting							
1DAh~1DDh	Non-association Port Setting							
1DEh~1E5h	Spanning Tree State							
1E6h~1E9h	Port Base Address Flush							
1EAh~1F1h	CPU Read/Write Address Table							
1F2h~1F3h	Table Address Access Method							
1F4h~1F9h	ACL/VID/VID-Tag Configuration							
1FAh~1FBh	Reserved							
1FCh~1FFh	802.3 OAM LoopBack Enable							

6.2.3 MAC Control Register

Table 49 MAC Control Register

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
01h	02h 03h	General MAC operation behavior bit[1:0] : enable IPG compensation 00 : disable 01 : compensation 40 ppm 10 : compensation 80 ppm 11 : compensation 160 ppm bit[2] : broadcast all BPDU packets (MAC address= 0x0180C2000004~0x0180C200000F) but (0X0180C2000000 must also ref 0x02[0]) bit[3] : backpressure method 0 : carrier sense base 1 : collision base bit[4] : collision 16 times drop enable bit[5] : collision back off enable bit[6] : high/low bandwidth throttle select 0 : 32 kbps unit 1 : 512 kbps unit bit[7] : auto turn off flow control function if priority queue disable bit[8] : port statistic counter method (ref. to 0x40~0x41) bit[9] : port statistic counter enable (ref. to 0x40~0x41) bit[10] : in-band management (destination MAC address = switch MAC address) 0 : forward 1 : to CPU port (switch MAC address define in offset address 0x3A,3B,3C) bit[11] : disable Tx packets CRC recalculation bit[12] : by pass Rx packets CRC error bit[14:13] : the supreme priority selection 00 : ACL result 01 : IP address 10 : MAC address 11 : multicast group bit[15] : the supreme priority enable 0 : disable 1 : enable	R/W	16'h4AE
02h	04h 05h	Layer 2 Protocol frames capture bit[0] : spanning tree (when mg_bpdu_brcst_en = 0) 0 : drop 1 : to CPU port bit[1] : 802.1x protocol enable 0 : drop or broadcast 1 : to CPU port bit[2] : slow protocol 0 : drop	R/W	12'h80

MAC Control Register				
Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		1 : send to port 25 (CPU) only bit[3] : MPCP protocol 0 : drop 1 : send to port 25 (CPU) only bit[4] : GxRP 0 : broadcast 1 : send to port 25 (CPU) only bit[5] : ARP 0 : forward depend on DA 1 : to DA and CPU port bit[6] : PPPoE protocol check enable 0 : don't check PPPoE type 1 : check PPPoE type (only useful when the L3 protocol is IP) bit[7] : MPCP drop disable 0 : drop MPCP packet when bit[3] is 1'b0 1 : don't drop MPCP packet when bit[3] is 1'b0 bit[8] : pass pause frame with DA not equal to 01-80-C2-00-00-01 and address defined in 0x3A~0x3C 0 : drop the pause frame 1 : transmit the pause frame bit[9] : LLDP protocol 0 : drop 1 : send to port 25 (CPU) only bit[10] : reduce IPG for port 25 (CPU) enable 0 : disable 1 : reduce IPG to 64 bit-time bit[11] : reduce preamble for port 25 (CPU) enable 0 : disable 1 : reduce 4 bytes preamble bit[12] : special mode for 802.1D Reserved Group 0 : normal mode 1 : special mode		
03h	06h 07h	Layer 3 Protocol frame capture bit[1:0] : ICMP bit[3:2] : TCP bit[5:4] : UDP bit[7:6] : OSPF bit[9:8] : user define 1 bit[10:11] : user define 2 bit[13:12] : others 00 : send to ports only 01 : send to port 25 (CPU) and ports 10 : send to port 25 (CPU) only 11 : drop	R/W	14'h0
04h	08h 09h	User define Layer 3 Protocol type bit[7:0] : User define protocol 1	R/W	16'h0

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		bit[15:8] : User define protocol 2		
05h ~ 1Dh	0Ah ~ 3Bh	Egress/Ingress Rate control bit[7:0] : output rate control bit[15:8] : input rate control The max. input/output bytes no. in one period time (500 ms) for port 01~port 25 (ref. to 0x01 bit[6]) = rate control x 32K bps : low bandwidth = rate control x 512K bps : high bandwidth	R/W	16'h0
1Eh	3Ch 3Dh	Port base priority enable for port 01~port 08, 2 bit per port Ex. bit[1:0] : port base priority setting for port 1 00 : to queue 3 (lowest priority) 01 : to queue 2 10 : to queue 1 11 : to queue 0 (highest priority)	R/W	16'h0
1Fh	3Eh 3Fh	Port base priority enable for port 09~port 16, 2 bit per port	R/W	16'h0
20h	40h 41h	Port base priority enable for port 17~port 24, 2 bit per port	R/W	16'h0
21h	42h 43h	Port base priority enable for port 25	R/W	2'h0
22h	44h 45h	VLAN tag base priority enable for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable 1 : enable	R/W	16'h0
23h	46h 47h	VLAN tag base priority enable for port 17~port 25, 1 bit per port bit[8:0] : 0 : disable 1 : enable bit[9] : VID base priority enable 0 : disable 1 : enable	R/W	10'h0
24h	48h 49h	IP CoS base priority enable for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable 1 : enable	R/W	16'h0
25h	4Ah 4Bh	IP CoS base priority enable for port 17~port 25, 1 bit per port bit[8:0] : 0 : disable 1 : enable	R/W	9'h0

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
26h	4Ch 4Dh	Differentiated Services (DS) priority setting bit [1:0] : priority setting for CODEPOINT 6'b001010 bit [3:2] : priority setting for CODEPOINT 6'b010010 bit [5:4] : priority setting for CODEPOINT 6'b011010 bit [7:6] : priority setting for CODEPOINT 6'b100010 bit [9:8] : priority setting for CODEPOINT 6'b101110 bit [11:10] : priority setting for CODEPOINT 6'b110000 bit [13:12] : priority setting for CODEPOINT 6'b111000 bit[14] : the undefined CODEPOINT priority handling 0 : undefined CODEPOINT treat as priority “0” 1 : priority based on TAG/PORT setting	R/W	15’h7FFF
27h	4Eh 4Fh	Stag/Ctag ingress control bit[0] : admit only Ctag packet enable bit[1] : admit only Stag packet enable 0 : disable 1 : enable	R/W	2’h0
29h	52h 53h	802.1x port lock enable (port 01~port 16) bit[15:0] : 0 : normal operation 1 : drop all frames except ARP & 802.1x EAPOL packet	R/W	16'h0
2Ah	54h 55h	802.1x port lock enable (port 17~port 24) bit[7:0] : 0 : normal operation 1 : drop all frames except ARP & 802.1x EAPOL packet	R/W	8'h0
2Bh	56h 57h	User define TCP/UDP port number A upper range setting	R/W	16'h0
2Ch	58h 59h	User define TCP/UDP port number A lower range setting IP1725 will check if the port number A in the following range lower ranger ≦ port number A ≦ upper ranger	R/W	16'h0
2Dh	5Ah 5Bh	User define TCP/UDP port number B upper range setting	R/W	16'h0
2Eh	5Ch 5Dh	User define TCP/UDP port number B lower range setting IP1725 will check if the port number B in the following range lower range ≦ port number B ≦ upper range	R/W	16'h0
2Fh	5Eh 5Fh	User define TCP/UDP port number C upper range setting	R/W	16’h0
30h	60h 61h	User define TCP/UDP port number C lower range setting IP1725 will check if the port number C in the following range lower range ≦ port number C ≦ upper range	R/W	16'h0

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
31h	62h 63h	TCP/UDP port number base priority for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable 1 : enable Note: these bits only for TCP/UDP priority setting per port.	R/W	16'h0
32h	64h 65h	TCP/UDP port number base priority for port 17~port 25, 1 bit per port bit[8:0] : 0 : disable 1 : enable Note: these bits only for TCP/UDP priority setting per port.	R/W	9'h0
33h	66h 67h	TCP/UDP port number based priority setting : bit[2:0] : 20,21 (common by FTP) bit[5:3] : 22 (common by SSH) bit[8:6] : 23 (common by TELNET) bit[11:9] : 25 (common by SMTP) bit[14:12] : 53 (common by DNS) 000 : to queue 3 (disable) 001 : to queue 2 010 : to queue 1 011 : to queue 0 100 : to CPU (global setting) 101 : drop (global setting) To CPU and drop are global setting, not accept 31h and 32h set.	R/W	15'h0
34h	68h 69h	TCP/UDP port number based priority setting : bit[2:0] : 69 (common by TFTP) bit[5:3] : 80,8080 (common by HTTP_0,1) bit[8:6] : 110 (common by POP3) bit[11:9] : 119 (common by NEWS) bit[14:12] : 123 (common by NTP) 000 : to queue 3 (disable) 001 : to queue 2 010 : to queue 1 011 : to queue 0 100 : to CPU 101 : drop To CPU and drop are global setting, not accept 31h and 32h set.	R/W	15'h0

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
35h	6Ah 6Bh	TCP/UDP port number based priority setting : bit[2:0] : 137,138,139 (common by NETBIOS0,1,2) bit[5:3] : 143,220 (common by IMAP_0,1) bit[8:6] : 161,162 (common by SNMP_0,1) bit[11:9] : 443 (common by HTTPS) bit[14:12] : 1863 000 : to queue 3 (disable) 001 : to queue 2 010 : to queue 1 011 : to queue 0 100 : to CPU 101 : drop To CPU and drop are global setting, not accept 31h and 32h set.	R/W	15'h0
36h	6Ch 6Dh	TCP/UDP port number based priority setting : bit[2:0] : 3389 (common by XRD_RDP) bit[5:3] : 4000,8000 bit[8:6] : 5190 bit[11:9] : 5050 bit[14:12] : 67,68 (common by BOOTP/DHCP) 000 : to queue 3 (disable) 001 : to queue 2 010 : to queue 1 011 : to queue 0 100 : to CPU 101 : drop To CPU and drop are global setting, not accept 31h and 32h set.	R/W	15'h0
37h	6Eh 6Fh	TCP/UDP user defined port number based priority setting: bit[2:0] : tcp/udp_num_a bit[5:3] : tcp/udp_num_b bit[8:6] : tcp/udp_num_c 000 : to queue 3 (disable) 001 : to queue 2 010 : to queue 1 011 : to queue 0 100 : to CPU 101 : drop To CPU and drop are global setting, not accept 31h and 32h set.	R/W	9'h0

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
38h	70h 71h	TCP/UDP port number based filter select to WAN port bit[0] : 20, 21 (common by FTP) bit[1] : 22 (common by SSH) bit[2] : 23 (common by TELNET) bit[3] : 25 (common by SMTP) bit[4] : 53 (common by DNS) bit[5] : 69 (common by TFTP) bit[6] : 80, 8080 (common by HTTP_0,1) bit[7] : 110 (common by POP3) bit[8] : 119 (common by NEWS) bit[9] : 123 (common by NTP) bit[10] : 137, 138, 139 (common by NETBIOS0,1,2) bit[11] : 143, 220 (common by IMAP_0,1) bit[12] : 161, 162 (common by SNMP_0,1) bit[13] : 443 (common by HTTPS) bit[14] : 1863 bit[15] : 3389 (common by XRD_RDP) 0 : don't care 1 : select (corresponding to offset address 0x33~0x37)	R/W	16'h0
39h	72h 73h	TCP/UDP port number based filter select to WAN port bit[0] : 4000, 8000 bit[1] : 5190 bit[2] : 5050 bit[3] : 67, 68 (common by BOOP/DHCP) bit[4] : tcp/udp_num_a bit[5] : tcp/udp_num_b bit[6] : tcp/udp_num_c 0 : don't care 1 : select bit[7] : reserved bit[8] : filter method to WAN port 0 : negative list, the setting “1”s above which routed to WAN port will be filtered 1 : positive list, the setting “1”s above which routed to WAN port can be passed, otherwise be filtered bit[9] : filter function enable 1 : enable (0x38, 0x39 setting take effect) 0 : disable (bit[9:8] : ref. to offset address 0x71, 0x72)	R/W	10'h0
3Ah	74h 75h	Switch's MAC address[15:0]	R/W	16'h0
3Bh	76h 77h	Switch's MAC address[31:16]	R/W	16'hC300

MAC Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
3Ch	78h 79h	Switch's MAC address[47:32]	R/W	16'h90
3Dh	7Ah 7Bh	CPU Read statistic counter command [5:0] : statistic counter read address (from 0~49) [6] : statistic counter data updating stop [7] : statistic counter reset [8] : statistic counter read (after read, counter will reset to 0) [9] : command enable	W SC	9'h0
3Eh	7Ch 7Dh	CPU Read low 16 bits statistic counter data	R	16'h0
3Fh	7Eh 7Fh	CPU Read high 16 bits statistic counter data	R	16'h0
40h	80h 81h	Port statistic counter selection (port 01~port 16) **ref. : 0x01[8]= (Port statistic counter method)** addr even odd {method, selection} : counter 0 counter 1 0 0 , receive packet count, transmit packet count 0 1 , transmit packet count, collision count 1 0 , receive packet count, packet drop count (mac) 1 1 , receive packet count, CRC error packet count ex : port 1 : addr = 0 (even addr) , counter 0 1 (odd addr) , counter 1 port 2 : addr = 2 (counter 0) , 3 (counter 1) … port 25 : addr = 48 (counter 0) , 49 (counter 1)	R/W	16'h0
41h	82h 83h	Port statistic counter selection (port 17~port 25)	R/W	9'h0

6.2.4 Output Queue Register

Table 50 Output Queue Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
Output Queue Register				
42h	84h 85h	Out queue schedule mode/weight selection bit[1:0] : Schedule mode 00 : fist come fist schedule All output packets are queued to 1 queue, first comes first outs. 01 : strict Priority Packets are classified into high/low queues. Unless the high priority queue is empty, low priority can not transmit packets. 10 : WRR Packets are classified into 4 queues. The transmit weighting is based on the packet count defined in reg 0x43. 11 : WRR/Strict priority MIXED mode Packets are classified into 4 queues. The highest priority queue transmit packets when queue is not empty. The other 3 queues follow the weighting defined in reg 0x43. bit[2] : Indicates the SP mode is 2 or 4 queues, only meaningful when bit[1:0]=01 0 : 2 queues 1 : 4 queues	R/W	3'h4
43h	86h 87h	Out queue schedule weight selection bit[3:0] : Priority queue 0 weight number when in WRR and MIXED mode, the first priority packets are queued to this queue. 1~16 packets count is settable. (Note : 0 stands for 16) bit[7:4] : Priority queue 1 weight number, the second priority packets are queued to this queue. 1~16 packets count is settable. (Note : 0 stands for 16) bit[11:8] : Priority queue 2 weight number , the third priority packets are queued to this queue. 1~16 packets count is settable. (Note : 0 stands for 16) bit[15:11] : Priority queue 3 weight number, the lowest priority packets are queued to this queue. 1~16 packets count is settable. (Note : 0 stands for 16)	R/W	16'h0
44h	88h 89h	Out queue Aging timer configuration bit[5:0] : output queue aging time = (1~2) x (value+1) x 100ms for example : if “3” is set, the output queue aging time is from : 1 x (3+1) x 100ms = 400ms to : 2 x (3+1) x 100ms = 800ms bit[7:6] : (unused)	R/W	9'h0

Output Queue Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		bit[8] : output queue aging function enable 0 : output queue aging function is disable 1 : output queue aging function is enable		
45h	8Ah 8Bh	Out queue pause off/on threshold* bit[8:0] : output queue pause on threshold (default = 0x1b4 for 1 queue mode, = 0x0b4 for 2 queue mode, = 0x05e for 4 queue mode) bit[15:9] : the number of output queue pause off threshold which bigger than pause on threshold (default = 0x16) *Note : the output queue pause on threshold parameter will be re-set while register 44h schedule mode changed in datasheet, this register is reserved for test	R/W	16'h2DCF

6.2.5 TxDMA Register

Table 51 TxDMA Register

TxDMA Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
46h	8Ch 8Dh	CPU port (port 25) special tag enable bit[0] : port 25 can recognize the special tag frame 1 : enable 0 : disable Note : (a) the minimum byte count of special tag frame Rx. from CPU should be (64B + 6B) = 70B (b) the minimum byte count of special tag frame Tx. to CPU should be (64B + 4B) = 68B	R/W	1'h0
47h	8Eh 8Fh	When tag insertion is needed, the inserting PVID/PRI is according to source port or output port. 1bit per port for port 01~port 16 bit[15:0] : 0 : base on source port 1 : base on output port	R/W	16'h0
48h	90h 91h	When tag insertion is needed, the inserting PVID/PRI is according to source port or output port. 1bit per port for port 17~port 25 bit[8:0] : 0 : base on source port 1 : base on output port When priority tag is modified, the PRI bit in tag is modified or not bit[9] : 0 : do not modified 1 : modified by the mg_ins_tag_cfg setting	R/W	10'h0
49h	92h 93h	Special tag Type-length definition [15:0] Used to recognize the special tag frame.	R/W	16'h9126
4Ah	94h 95h	Q-in-Q double tag enable for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable, this port can not identify Q-in-Q packet and can not add/remove Q-in-Q tag 1 : enable, this port will identify Q-in-Q packet and can add/remove Q-in-Q tag according to reg 0x4B~ 0x53	R/W	16'h0
4Bh	96h 97h	Q-in-Q double tag enable for port 17~port 25 and port 25 Q-in-Q tag egress processing configuration bit[8:0] : 0 : disable 1 : enable bit[10:9] : 00 : port 25 does not modify Q-in-Q of Tx. packets x1 : port 25 adds Q-in-Q tag to Tx. packets 10 : port 25 removes Q-in-Q tag from Tx. packets	R/W	11'h0

TxDMA Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
4Ch	98h 99h	Q-in-Q tag egress processing configuration for port 08~port 01 bit[15:14] : 00 : port 08 does not modify Q-in-Q of Tx. packets x1 : port 08 adds Q-in-Q tag to Tx. packets 10 : port 08 removes Q-in-Q tag from Tx. packets bit[13:12] : port 07 Q-in-Q tag egress processing configuration : bit[1:0] : port 01 Q-in-Q tag egress processing configuration	R/W	16'h0
4Dh	9Ah 9Bh	Q-in-Q tag egress processing configuration for port 16~port 09 bit[15:14] : port 16 Q-in-Q tag egress processing configuration bit[13:12] : port 15 Q-in-Q tag egress processing configuration : bit[1:0] : port 09 Q-in-Q tag egress processing configuration	R/W	16'h0
4Eh	9Ch 9Dh	Q-in-Q tag egress processing configuration for port 24~port 17 bit[15:14] : port 24 Q-in-Q tag egress processing configuration bit[13:12] : port 23 Q-in-Q tag egress processing configuration : bit[1:0] : port 17 Q-in-Q tag egress processing configuration	R/W	16'h0
4Fh	9Eh 9Fh	Q-in-Q double tag Type-length definition [15:0] Used to recognize the Q-in-Q tag frame.	R/W	16'h88A8
50h	A0h A1h	Q-in-Q double tag VID definition [15:0] for classified as school “0” by ACL rule. Used to inserted into frames which should added a double tag.	R/W	16'h0
51h	A2h A3h	Q-in-Q double tag VID definition [15:0] for classified as school “1” by ACL rule. Used to inserted into frames which should added a double tag.	R/W	16'h0
52h	A4h A5h	Q-in-Q double tag VID definition [15:0] for classified as school “2” by ACL rule. Used to inserted into frames which should added a double tag.	R/W	16'h0
53h	A6h A7h	Q-in-Q double tag VID definition [15:0] for classified as school “3” by ACL rule. Used to inserted into frames which should added a double tag.	R/W	16'h0

6.2.6 SMI Control Register

Table 52 SMI Control Register

SMI Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
54h	A8h A9h	LED mode settings bit[1:0] : LED mode 11 : direct mode (L/A) (default) 10 : 3-bit for serial mode bi-color (C/F, L/A, Spd) 01 : 3-bit for serial mode (C/F, L/A, Spd) 00 : 2-bit for serial mode (Spd, L/A) bit[3:2] : LED blink time 00 : 40 ms 01 : 80 ms 10 :120 ms 11 :160 ms bit[5:4] : LED clock rate 00 : 781 KHz 01 : 2.5 MHz 10 : 5 MHz 11 : 10 MHz bit[6] : LED Col blink disable 0 : will blink when Col 1 : don't blink when Col bit[7] : LED act (Tx/Rx) blink disable 0 : will blink when act 1 : don't blink when act bit[8] : LED port number control in fiber mode 0 : normal 1 : 19 ports mode	R/W	9'h23
55h	AAh ABh	Auto negotiation configuration for port 01~port 16 bit[15:0] : auto negotiation for each port 0 : disable auto negotiation 1 : enable auto negotiation	R/W	16'hFFFF
56h	ACh ADh	Auto negotiation configuration for port 17~port 25 bit[8:0] : auto negotiation for each port 0 : disable auto negotiation 1 : enable auto negotiation	R/W	9'h1FF
57h	AEh AFh	Speed setting for port 01~port 16, 1 bit per port bit[15:0] : 0 : 10 MBps 1 : 100 MBps	R/W	16'hFFFF
58h	B0h B1h	Speed setting for port 17~port 25, 1 bit per port bit[8:0] : 0 : 10 MBps 1 : 100 MBps	R/W	9'h1FF

SMI Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
59h	B2h B3h	Duplex setting for port 01~port 16, 1 bit per port bit[15:0] : 0 : half duplex 1 : full duplex	R/W	16'hFFFF
5Ah	B4h B5h	Duplex setting for port 17~port 25, 1 bit per port bit[8:0] : 0 : half duplex 1 : full duplex	R/W	9'h1FF
5Bh	B6h B7h	Pause setting for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable pause 1 : enable pause	R/W	16'hFFFF
5Ch	B8h B9h	Pause setting for port 17~port 25, 1 bit per port bit[8:0] : 0 : disable pause 1 : enable pause	R/W	9'h1FF
5Dh	BAh BBh	Asymmetric pause setting for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable asymmetric pause 1 : enable asymmetric pause	R/W	16'hFFFF
5Eh	BCh BDh	Asymmetric pause setting for port 17~port 25, 1 bit per port bit[8:0] : 0 : disable asymmetric pause 1 : enable asymmetric pause	R/W	9'h1FF
5Fh	BEh BFh	Backpressure setting for port 01~port 16, 1 bit per port bit[15:0] : 0 : backpressure function disable 1 : backpressure function enable	R/W	16'hFFFF
60h	C0h C1h	Backpressure setting for Port 17~Port 25, 1 bit per port bit[8:0] : 0 : backpressure function disable 1 : backpressure function enable	R/W	9'h1FF
61h	C2h C3h	CPU port PHY address setting bit[4:0] : CPU port PHY address bit[5] : CPU port force link disable 0 : CPU port force link 1 : not force link bit[6] : selection method of port 25 operation mode (speed/duplex) 0 : judge by polling status 1 : judge by reg 0x58 and 0x5A setting only	R/W	7'h21
63h	C6h C7h	CPU read/write PHY register command bit[4:0] : PHY address bit[9:5] : MII register address bit[12:10] : reserved bit[13] : 0 : command not complete	R/W	16'h0

SMI Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		1 : command complete bit[14] : 0 : read operation 1 : write operation this bit also indicates what the data is when 0x64 reading 0 : the data read back from PHY 1 : the data want to write to PHY bit[15] : the read/write command trigger 0 : idle or command complete 1 : start command		
64h	C8h C9h	CPU read/write PHY register command data bit[15:0] : in read command – the read back data in write command – data want to write	R/W	16'h0
65h	CAh CBh	The port status of port 01~port 03, 5 bit per port bit[4:0] : port 1 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 2 status bit[14:10] : port 3 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
66h	CCh CDh	The port status of port 04~port 06, 5 bit per port bit[4:0] : port 4 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 5 status bit[14:10] : port 6 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
67h	CEh CFh	The port status of port 07~port 09, 5 bit per port bit[4:0] : port 7 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 8 status bit[14:10] : port 9 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
68h	D0h D1h	The port status of port 10~port 12, 5 bit per port bit[4:0] : port 10 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 11 status bit[14:10] : port 12 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
69h	D2h D3h	The port status of port 13~port 15, 5 bit per port bit[4:0] : port 13 status	R	15'h7BDE

SMI Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		{enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 14 status bit[14:10] : port 15 status flow_ctrl include backpressure in half duplex		
6Ah	D4h D5h	The port status of port 16~port 18, 5 bit per port bit[4:0] : port 16 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 17 status bit[14:10] : port 18 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
6Bh	D6h D7h	The port status of port 19~port 21, 5 bit per port bit[4:0] : port 19 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 20 status bit[14:10] : port 21 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
6Ch	D8h D9h	The port status of port 22~port 24, 5 bit per port bit[4:0] : port 22 status {enable pause receive, enable pause transmit, duplex, speed, link} bit[9:5] : port 23 status bit[14:10] : port 24 status flow_ctrl include backpressure in half duplex	R	15'h7BDE
6Dh	DAh DBh	The port status of port 25 bit[4:0] : port 25 status {enable pause receive, enable pause transmit, duplex, speed, link} flow_ctrl include backpressure in half duplex	R	5'h1E

6.2.7 Miscellaneous Control Register

Table 53 Miscellaneous Control Register

Miscellaneous Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
6Eh	DCh DDh	bit[0] :software reset 1 : software reset 0 : normal bit[1] : reset mask for mg_bist_rst 1 : do not reset when BIST finished 0 : reset when BIST finished bit[2] : reset mask for mg_ou_rst 1 : do not reset when over-flow observed 0 : reset when over-flow observed bit[3] : reset mask for oq_sw_reset_trig 1 : do not reset when out-queue op mode changed 0 : reset when out-queue op mode changed	RW / SC R/W	4'h0
6Fh	DEh DFh	Build in self test information bit[3:0] : BIST enable {OQ, FB, BM, LUT} LUT : look up table BM : buffer management FB : frame Buffer OQ : output queue bit[7:4] : BIST is busy {OQ, FB, BM, LUT} bit[11:8] : BIST is OK or not {OQ, FB, BM, LUT} bit[12] : frame buffer BIST repair function enable bit[13] : block/non-block MDC control in test mode 0 : don't block 1 : block bit[15] : fast test mode set 1 : switch is in fast test mode 0 : normal mode	 R/W R/O R/O R/W R/W R/W	16'h3F0F
70h	E0h E1h	CPU mode setting bit[0] : port 25 linked to CPU bit[1] : CPU interface RvMII mode	R/W	2'h2
71h	E2h E3h	WAN port setting for TCP/UDP port filter setting bit[15:0] : port 16~port 01 port filter Ref offset address 0x39[8] : 0 : negative filtering list (if TCP/UDP number matched, packet sent to filter setting port will be dropped)	R/W	16'h0

Miscellaneous Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		1 : positive filtering list (if TCP/UDP port number matched, packet sent to filter setting port will be allowed, others will be dropped) 0x39[9] : filter enable		
72h	E4h E5h	WAN port setting for TCP/UDP port filter setting bit[8:0] : port 25~port 17 port filter (same definition as above)	R/W	9'h0
73h	E6h E7h	Internal Status : bit[2:0] : port page count under-flow counter indicates the number of under-flow condition after power on (port page under flow trigger) bit[3] : reserved bit[6:4] : out queue over flow counter indicates the number of overflow condition after power on bit[7] : reserved bit[8] : share page count is not equal to setting value indication	R	9'h0
74h	E8h E9h	Interrupt signal setting bit[0] : enable interrupt for CPU R/W SMI command complete bit[1] : enable interrupt for PHY link status notification bit[2] : (reserved, should be 0) bit[3] : enable interrupt for CPU R/W EPROM command complete bit[4] : interrupt pin active mode 0 : Low active 1 : High active	R/W	5'h2
75h	EAh EBh	Interrupt signal setting bit[0] : interrupt of CPU R/W SMI command complete bit[1] : PHY link status change notification bit[2] : (reserved) bit[3] : interrupt of PU R/W EPROM command complete Note : interrupt signal that is triggered by any event will assert until user read this register	R/C	4'h0
76h	ECh EDh	MII Interface signal timing setting bit[2:0] : the driving current setting for MII interface 000 : minimum current 011 : 5mA (default) 111 : maximum current bit[3] : auto driving current enable 1 : IP1725 will auto adjust the driving current by loading 0 : the driving current is based on bit[2:0] bit[5:4] : (D_SEL, reserved for test) bit[6] : (custom_sr, reserved for test)	R/W	7'h13

Miscellaneous Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
77h	EEh EFh	(reserved)		
78h	F0h F1h	CPU read/write EEPROM command bit [7:0] : byte address bit [10:8] : device address bit [12:11] : reserved bit [13] : 0 : command not complete 1 : command complete bit [14] : 0 : read operation 1 : write operation bit [15] : the read/write command trigger 0 : idle or command complete 1 : start command	R/W	16'h0
79h	F2h F3h	CPU read/write EEPROM command data bit [7:0] : in read command - the read back data in write command - data want to write	R/W	8'h0

6.2.8 Buffer Management Control Register

Table 54 Buffer Management Control Register

Buffer Management Control Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
7Ah	F4h F5h	(reserverd)	R/O	
7Bh	F6h F7h	bit[6:0] : the dedicate frame buffer threshold for flow control on	R/W	7'h32
7Ch	F8h F9h	bit[6:0] : the dedicate frame buffer threshold for flow control off	R/W	7'h62
7Dh	FAh FBh	bit[7:0] : the dedicate frame buffer threshold for drop packet on	R/W	8'h1
7Eh	FCh FDh	bit[6:0] : the dedicate frame buffer threshold for drop packet off	R/W	7'h19
7Fh	FEh FFh	bit[10:0] : frame buffer share pool page count bit[11] : 1 : use present share page count as read back data 0 : use register setting share page count as read back data	R/W	12'h46E
80h	100h 101h	bit[6:0] : frame buffer per port allocated memory page count (port 01~port 24, CPU) bit[7] : (reserved) bit[8] : rd_port_page_cnt_err (if 0xC5[12] = 1)	R/W R/O	9'h64
81h	102h 103h	bit[9:0] : the max. page count that one port can get from share memory bit[10] : 1 : the max. share page count is static equal to bit[9:0] 0 : the max. share page count is allocated dynamically by switch	R/W R/O	11'h380

6.2.9 Address Resolution Logic Register

Table 55 Address Resolution Logic Register

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
82h	104h 105h	ARL operation setting bit[0] : hash algorithm selection 0 : direct map base 1 : CRC map base bit[1] : address table aging function disable 0 : aging enable 1 : aging disable bit[3:2] : broadcast storm type selection [2] : multicast also regard as Bcst [3] : unknow DA also regard as Bcst bit[4] : block broadcast frames to CPU port 0 : disable blocking 1 : enable blocking bit[5] : block ARP to CPU port 0 : don't block 1 : block bit[6] : pass all IPv4 packet when block broadcast frame to CPU port 0 : disable pass 1 : enable pass bit[7] : VLAN type 0 : port based VLAN 1 : 802.1Q tag based VLAN bit[8] : unicast packet stride across VLAN bit[9] : VLAN blocked packet forward to uplink port enable (uplink port setting establish at offset address 0x8D,8E) bit[10] : drop priority tag enable 0 : don't drop 1 : drop bit[11] : select the tag/untag method 0 : base on Ports (ref. reg 0x97~0x9A) 1 : base on VIDs (ref. reg 0xFA and 0xFC) bit[12] : modify tag in VID_TAG mode for CPU port 0 : do not modify tag 1 : modify tag by setting register 0xFA and 0xFC bit[13] : CPU route enable, if enable, the packets will route according to special tag assignment bit[14] : CPU route function do not care VLAN and trunk result bit[15] : Ctag remove/modify enable 0 : don't change Ctag 1 : remove/modify Ctag enable	R/W	16'h1
83h	106h 107h	Source/Destination IP address security setting bit[1:0] : IP address filter mode cfg	R/W	16'h0

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		00 : IP dis-match can pass 01 : IP match can pass 10 : IP match and source port match can pass 11 : IP match and source port not match can pass bit[2] : IP address filter subnet mode 0 : IP address in LUT will base on hashing result 32 bits IP should match exactly 1 : IP address in LUT will base on source port ex : packets from port 0 will check LUT address 12'h000, and IP should match the correspond subnet mask setting bit[3] : IP selection 0 : source IP 1 : destination IP bit[5:4] : IP address shift in LUT 00 : none 01 : add 1 10 : add 2 11 : add 3 bit[6] : IP address shift in LUT enable bit[7] : IP address equal to 0.0.0.0 can pass bit[15:8] : IP subnet mask setting for IP filter function the subnet mask will be 255.255.bit[15:8].0		
84h	108h 109h	IP filter enable for port 01~port 16 0 : disable 1 : enable	R/W	16'h0
85h	10Ah 10Bh	IP filter enable for port 17~port 25 0 : disable 1 : enable	R/W	9'h0
86h	10Ch 10Dh	Broadcast storm control setting (port 01~port 16) bit[15:0] : broadcast storm control 0 : disable 1 : enable	R/W	16'h0
87h	10Eh 10Fh	Broadcast storm control setting (port 17~port 25) bit[8:0] : broadcast storm control 0 : disable 1 : enable bit[14:9] : broadcast storm control threshold bit[15] : broadcast storm counter clear period selection 0 : 100M : 500 us 10M : 5 ms 1 : 100M : 10 ms 10M : 100 ms	R/W	16'h7E00

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
88h	110h 111h	ARP and ICMP storm control settings bit[2:0] : ARP storm control threshold bit[3] : ARP storm control enable 0 : disable 1 : enable bit[4] : ARP storm counter clear period selection 0 : 1 ms 1 : 10 ms bit[7:5] : reserved bit[10:8] : ICMP storm control threshold bit[11] : ICMP storm control enable 0 : disable 1 : enable bit[12] : ICMP storm counter clear period selection 0 : 1 ms 1 : 10 ms	R/W	13'h0
89h	112h 113h	Aging timer threshold setting bit[14:0] : aging timer, the aging time is about : (mg_aging_time + 1) x 27.6 sec. (+/-3.8%)	R/W	15'hA
8Ah	114h 115h	Enable Source MAC address learning function for port 01~port 16 bit[15:0] : 0 : disable learning 1 : enable learning	R/W	16'hFFFF
8Bh	116h 117h	Enable Source MAC address learning function for port 17~port 24 bit[7:0] : 0 : disable learning 1 : enable learning bit[9:8] : LUT entry overwrite method select 00 : overwrite even when the entry is valid 01 : don't overwrite before aging out 10 : the same as 01 11 : only overwrite second lut before aging out bit[10] : null (all zero) MAC address is learning disable 0 : learn to LUT 1 : not learn to LUT	R/W	11'hFF
8Ch	118h 119h	Security configuration bit[0] : disable forward unknown SA frame to CPU port 0 : forward 1 : not forward bit[1] : forward unknown SA frame if source address learning function is disable 0 : drop the unknown SA frame 1 : forward the unknown SA frame bit[2] : indicates the SA of input frame should match the original learnt port or not 0 : SA will not binding the port	R/W	8'h6

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
		1 : SA will binding to the original learnt port bit[3] : unknown IGMP type behavior 0 : broadcast 1 : to CPU port bit[5:4] : unregister Multicast packets behavior 00 : broadcast 01 : drop 10 : to Router port 11 : to CPU port bit[7:6] : unknown VID behavior 00 : drop 01 : default all Group 10 : broadcast 11 : to CPU port		
8Dh	11Ah 11Bh	VLAN uplink function support selection for port 01~port 16 bit[15:0] : uplink port configuration 0 : normal port 1 : uplink port	R/W	16'h0
8Eh	11Ch 11Dh	VLAN uplink function support selection for port 17~port 25 bit[8:0] : uplink port configuration 0 : normal port 1 : uplink port	R/W	9'h0
8Fh	11Eh 11Fh	Trunk function setting bit[3:0] : for trunk 1 member selection bit[7:4] : for trunk 2 member selection 0 : port is not in trunk group 1 : port is in trunk group bit[10:8] : for trunk 1 group set selection bit[13:11] : for trunk 2 group set selection ex : 001 – port 01~port 04 010 – port 05~port 08 … 110 – port 20~port 24 bit[15:14] : trunk hash algorithm selection 2'b00 : Port ID 2'b01 : SA 2'b10 : DA 2'b11 : Both SA/DA	R/W	16'h0
90h	120h 121h	Sniffer function configuration for port 01~port 16 bit[15:0] : the sniffering port select	R/W	16'h0
91h	122h 123h	Sniffer function configuration for port 17~port 25 bit[8:0] : the sniffering port select	R/W	9'h0

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
92h	124h 125h	Sniffer function configuration for port 01~port 16 bit[15:0] : sniffered port config 0 : this port is not be sniffered 1 : this port is sniffered	R/W	16'h0
93h	126h 127h	Sniffer function configuration for port 17~port 25 bit[8:0] : sniffered port config 0 : this port is not be sniffered 1 : this port is sniffered bit[10:9] : sniffer method 00 : disable 01 : egress 10 : ingress 11 : egress/ingress	R/W	11'h0
94h	128h 129h	IGMP snooping function configuration bit[0] : enable IGMP snooping function bit[1] : multicast table make by CPU (leave will send to CPU port) bit[2] : disable MAC address 01:00:5e:00:00:xx broadcast (except IGMP packet) bit[3] : ***"Report"*** packet also send to host port (work in hardware mode) bit[4] : ***"Leave"*** packet send to router port (work in hardware mode) bit[5] : router port list configure by CPU only bit[6] : disable ***"Leave"*** function (work in hardware mode) bit[7] : multicast data to CPU port (DA equal to multicast DA, IP protocol not equal to IGMP) bit[8] : send query to CPU port when table make by CPU bit[9] : send report to CPU port when table make by CPU bit[10] : enable IGMP with DA not equal to multicast DA bit[11] : regard Mcst entry as invalid if group member is empty bit[12] : multicast DA use default all group VLAN enable bit[13] : multicast DA does not regard as broadcast storm 0 : multicast is counted into broadcast counter 1 : multicast is not counted into broadcast counter	R/W	13'h0
95h	12Ah 12Bh	Indicates which port is router port for port 01~port 16, 1 bit per port bit[15:0] : 0 : this port is a normal port 1 : this port is a router port	R/W	16'h0
96h	12Ch 12Dh	Indicates which port is router port for port 17~port 25, 1 bit per port bit[8:0] : 0 : this port is a normal port 1 : this port is a router port	R/W	9'h0
97h	12Eh 12Fh	VLAN output port add tag operation configuration for port 01~port 16, 1 bit per port	R/W	16'h0

Address Resolution Logic Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		bit[15:0] : output frame add tag 0 : disable 1 : add VLAN tag to output frame		
98h	130h 131h	VLAN output port add tag operation configuration for port 17~port 25, 1 bit per port bit[8:0] : output frame add tag 0 : disable 1 : add VLAN tag to output frame	R/W	9'h0
99h	132h 133h	VLAN output port remove tag operation configuration for port 01~port 16, 1 bit per port bit[15:0] : output frame remove tag 0 : disable 1 : remove VLAN tag to output frame	R/W	16'h0
9Ah	134h 135h	VLAN output port remove tag operation configuration for port 17~port 25, 1 bit per port bit[8:0] : output frame remove tag 0 : disable 1 : remove VLAN tag to output frame	R/W	9'h0
9Bh	136h 137h	PVID index setting for port 01~port 03 bit[4:0] : PVID configuration for port 01 bit[9:5] : PVID configuration for port 02 bit[14:10] : PVID configuration for port 03	R/W	15'h0
9Ch	138h 139h	PVID index setting for port 04~port 06 bit[4:0] : PVID configuration for port 04 bit[9:5] : PVID configuration for port 05 bit[14:10] : PVID configuration for port 06	R/W	15'h0
9Dh	13Ah 13Bh	PVID index setting for port 07~port 09 bit[4:0] : PVID configuration for port 07 bit[9:5] : PVID configuration for port 08 bit[14:10] : PVID configuration for port 09	R/W	15'h0
9Eh	13Ch 13Dh	PVID index setting for port 10~port 12 bit[4:0] : PVID configuration for port 10 bit[9:5] : PVID configuration for port 11 bit[14:10] : PVID configuration for port 12	R/W	15'h0
9Fh	13Eh 13Fh	PVID index setting for port 13~port 15 bit[4:0] : PVID configuration for port 13 bit[9:5] : PVID configuration for port 14 bit[14:10] : PVID configuration for port 15	R/W	15'h0

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
A0h	140h 141h	PVID index setting for port 16~port 18 bit[4:0] : PVID configuration for port 16 bit[9:5] : PVID configuration for port 17 bit[14:10] : PVID configuration for port 18	R/W	15'h0
A1h	142h 143h	PVID index setting for port 19~port 21 bit[4:0] : PVID configuration for port 19 bit[9:5] : PVID configuration for port 20 bit[14:10] : PVID configuration for port 21	R/W	15'h0
A2h	144h 145h	PVID index setting for port 22~port 24 bit[4:0] : PVID configuration for port 22 bit[9:5] : PVID configuration for port 23 bit[14:10] : PVID configuration for port 24	R/W	15'h0
A3h	146h 147h	PVID index setting for port 25 bit[4:0] : PVID configuration for port 25	R/W	5'h0
A4h	148h 149h	PVID priority bits setting for port 01~port 05 bit[2:0] : PVID priority bit configuration for port 01 bit[5:3] : PVID priority bit configuration for port 02 bit[8:6] : PVID priority bit configuration for port 03 bit[11:9] : PVID priority bit configuration for port 04 bit[14:12] : PVID priority bit configuration for port 05	R/W	15'h0
A5h	14Ah 14Bh	PVID priority bits setting for port 06~port 10 bit[2:0] : PVID priority bit configuration for port 06 bit[5:3] : PVID priority bit configuration for port 07 bit[8:6] : PVID priority bit configuration for port 08 bit[11:9] : PVID priority bit configuration for port 09 bit[14:12] : PVID priority bit configuration for port 10	R/W	15'h0
A6h	14Ch 14Dh	PVID priority bits setting for port 11~port 15 bit[2:0] : PVID priority bit configuration for port 11 bit[5:3] : PVID priority bit configuration for port 12 bit[8:6] : PVID priority bit configuration for port 13 bit[11:9] : PVID priority bit configuration for port 14 bit[14:12] : PVID priority bit configuration for port 15	R/W	15'h0
A7h	14Eh 14Fh	PVID priority bits setting for port 16~port 20 bit[2:0] : PVID priority bit configuration for port 16 bit[5:3] : PVID priority bit configuration for port 17 bit[8:6] : PVID priority bit configuration for port 18 bit[11:9] : PVID priority bit configuration for port 19 bit[14:12] : PVID priority bit configuration for port 20	R/W	15'h0
A8h	150h	PVID priority bits setting for port 21~port 25	R/W	15'h0

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
	151h	bit [2:0] : PVID priority bit configuration for port 21 bit [5:3] : PVID priority bit configuration for port 22 bit [8:6] : PVID priority bit configuration for port 23 bit [11:9] : PVID priority bit configuration for port 24 bit [14:12] : PVID priority bit configuration for port 25		
A9h	152h 153h	Force the incoming packet use PVID as 802.1Q VLAN check for port 01~port 16 bit[15:0] : 0 : don't force 1 : force to use PVID	R/W	16'h0
AAh	154h 155h	Force the incoming packet use PVID as 802.1Q VLAN check for port 17~port 25 bit[8:0] : 0 : don't force 1 : force to use PVID	R/W	9'h0
ABh	156h 157h	Check if the input port is in the VLAN group for port 01~port 16 (ingress check) bit[15:0] : 0 : don't check if the input port is in the group 1 : check if the input port is in the group. If not, drop.	R/W	16'hFFFF
ACh	128h 159h	Check if the input port is in the VLAN group for port 17~port 25 (ingress check) bit[8:0] : 0 : don't check if the input port is in the group 1 : check if the input port is in the group. If not, drop.	R/W	9'h1FF
ADh	15Ah 15Bh	VLAN member configuration for VLAN table entry 0 or port 01 port base VLAN setting. bit[15:0] : 0 : not in VLAN group 1 : in VLAN group	R/W	16'hFFFF
AEh	15Ch 15Dh	VLAN member configuration for VLAN table entry 0 or port 01 port base VLAN setting. bit[8:0] : 0 : not in VLAN group 1 : in VLAN group	R/W	9'h1FF
AFh ~ ECh	15Eh 15Fh ~ 1D8h 1D9h	VLAN member configuration for VLAN table entry 01 ~ 31 (entry 01~24 for port 02~25 port base VLAN) (same definition as 0xAD and 0xAE)	R/W	16'hFFFF 9'h1FF
EDh	1DAh 1DBh	Non-association port setting for port 01~port 16 bit[15:0] : indicate which ports are non-association port If a port is the non-association port, it will not send packets to other non-association ports.	R/W	16'h0

Address Resolution Logic Register

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
EEh	1DCh 1DDh	Non-association port setting for port 17~port 25 bit[8:0] : indicate which ports are non-association port If a port is the non-association port, it will not send packets to other non-association ports.	R/W	9'h0
EFh	1DEh 1DFh	Spanning Tree state configure bit 0 for port 01~port 16	R/W	16'hFFFF
F0h	1E0h 1E1h	Spanning Tree state configure bit 0 for port 17~port 24	R/W	8'hFF
F1h	1E2h 1E3h	Spanning Tree state configure bit 1 for port 01~port 16 {bit 1, bit 0} 00 : discard state 01 : block state 10 : learning state 11 : forwarding state	R/W	16'hFFFF
F2h	1E4h 1E5h	Spanning Tree state configure bit 1 for port 17~port 24 {bit 1, bit 0} 00 : discard state 01 : block state 10 : learning state 11 : forwarding state	R/W	8'hFF
F3h	1E6h 1E7h	Port base address flush for port 01~port 16 bit[15:0] : indicate that the address learnt by the selected port should be flushed	R/W	16'h0
F4h	1E8h 1E9h	Port base address flush for port 17~port 25 bit[8:0] : indicate that the address learnt by the selected port should be flushed bit[9] : port base address flush function trigger	R/W	10'h0
F5h	1EAh 1EBh	CPU read/write address table configuration bit[11:0] : the address table address bit[12] : select first/second LUT 0 : first LUT 1 : second LUT bit[13] : read/write configuration 0 : read 1 : write bit[14] : command enable 0 : disable 1 : read/write address table enable bit[15] : command complete	R/W	16'h0
F6h	1ECh 1EDh	CPU read/write address table data[15:0] If the command is read, store the read back data.	R/W	16'h0

Address Resolution Logic Register				
Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		If the command is write, write this data to address table.		
F7h	1EEh 1EFh	CPU read/write address table data[31:16] If the command is read, store the read back data. If the command is write, write this data to address table.	R/W	16'h0
F8h	1F0h 1F1h	CPU read/write address table data[46:32] If the command is read, store the read back data. If the command is write, write this data to address table.	R/W	15'h0
F9h	1F2h 1F3h	bit[1:0] : table address access method 00 : address calculated by CPU 01 : address calculated by HW for normal MAC entry 10 : address calculated by HW for IGMP entry 11 : address calculated by HW for IP entry	R/W	2'h0
FAh	1F4h 1F5h	ACL/VID/VID_TAG register group access command for ACL entry | for VID/VID_TAG [15] : trigger | [15] : trigger [14] : read/write | [14] : read/write [13:10] : reserved | [13:10] : reserved [9] : type select (0) | [9] : type_select (1) [8] : high/Llow for IP | [6] : VLAN_ID/VID_TAG (1) [7:4] : select | [5] : high/low for VID_TAG [3:0] : entry | [4:0] : entry When write ACL/VID/VID_TAG register, the data register must be written first, then write the command register. When read ACL/VID/VID_TAG register, the command register must be written first, then read back the data register.	R/W	16'h0
FBh	1F6h 1F7h	ACL data If the command is read, store the read back data. If the command is write, write this data to related ACL column.	R/W	16'h0
FCh	1F8h 1F9h	VID/VID _TAG data If the command is read, store the read back data. If the command is write, write this data to related VID/VID_TAG register.	R/W	16'h0
FDh	1FAh 1FBh	(reserved)	R/W	
FEh	1FCh 1FDh	802.3 OAM LoopBack enable for port 01~port 16, 1 bit per port bit[15:0] : 0 : disable 1 : enable	R/W	16'h0

Address Resolution Logic Register				
Reg Addr.	**ROM Addr.**	**Register Description**	**R/W**	**Default value**
FFh	1FEh 1FFh	802.3 OAM LoopBack enable for port 17~port 24 1 bit per port, and OAM mode setting bit[7:0] : 0 : disable 1 : enable bit[8] : for OAM mode setting 0 : passive mode 1 : active mode	R/W	9'h0

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

Table 56 Absolute Maximum Rating

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage	I/O	$V_{DDI/O}$	-0.5	+3.6	V
	Core	V_{DDCore}	-0.5	+1.26	V
Input Voltage		V_I	-0.5	$V_{DDI/O}$	V
Output Voltage		V_O	-0.5	$V_{DDI/O}$	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	70	°C
Junction Temperature		Tj	0	+125	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

7.2 DC Characteristics

7.2.1 Operating Conditions

Table 57 Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Power Consumption		4.06	4.2	W	10Mbps Full duplex active
		2.34	2.5	W	100Mbps Full duplex active

7.2.2 I/O Electrical Characteristics

Table 58 I/O Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output low voltage	V_{OL}	-	-	0.4	V
Output high voltage	V_{OH}	3.0	-	-	V
Input low voltage	V_{IL}	-	-	0.6	V
Input high voltage	V_{IH}	1.2	-	-	V
Low level output current	I_{OL}	-	-	TBD	mA
High level output current	I_{OH}	TBD	-	-	mA
DVDD supply voltage	V_{DVDD}	1.05	1.1	1.15	V
AVDD supply voltage	V_{AVDD}	1.8	1.9	2.09	V
VDDIO supply voltage	$V_{DDI/O}$	2.97	3.3	3.63	V
Pull-down resistor	R_{PD}	51	-	127	KΩ
RESETB threshold voltage	V_{RST}	0.6*$V_{DDI/O}$	-	0.8* $V_{DDI/O}$	V
OSCI(X1) input low voltage		-	-	0.6	V
OSCI(X1) input high voltage		1.5	-	-	V

7.3 AC Characteristics

7.3.1 CPU Serial Bus Timing

Table 59 CPU Serial Bus Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{S_C}	CPUCLK cycle time	400		-	ns
T_{SIO_SU}	CPUDAT set up time	10	-		ns
T_{SIO_H}	CPUDAT hold time	10	-	-	ns
T_{SIO_D}	CPUDAT output delay time	-	-	20	ns

Figure 38 Serial I/O Input Cycle

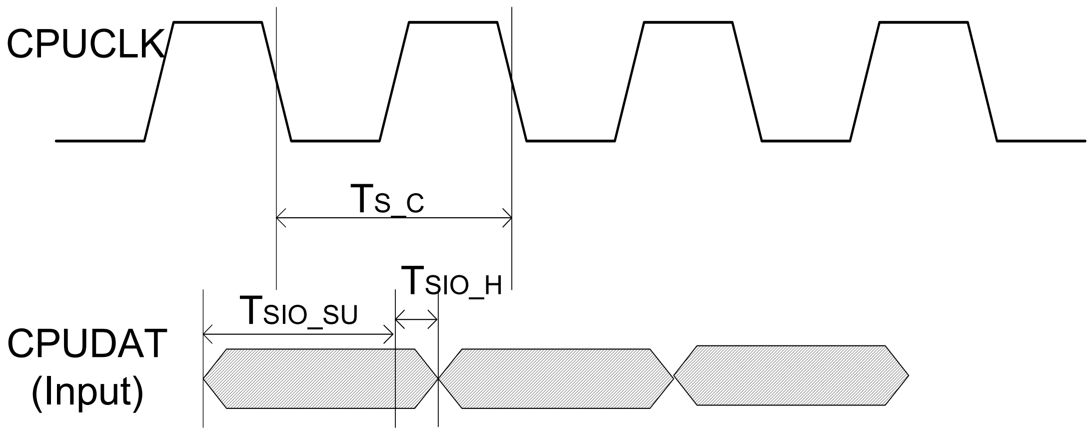
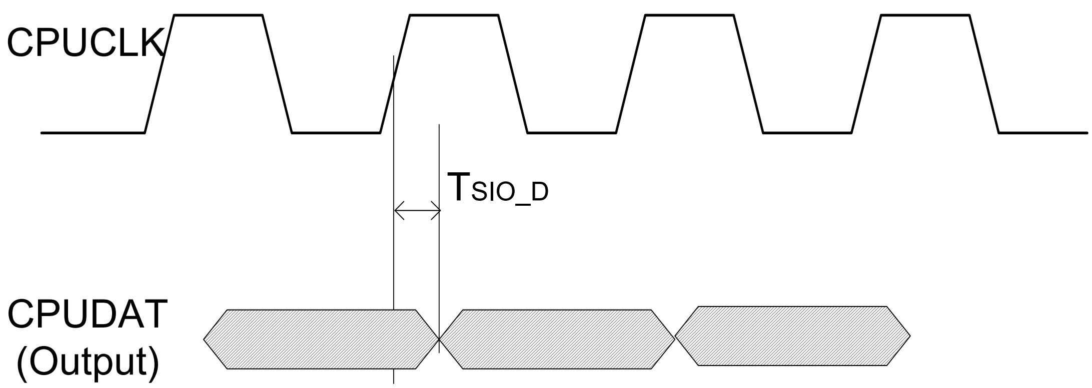


Figure 39 Serial I/O Output Cycle



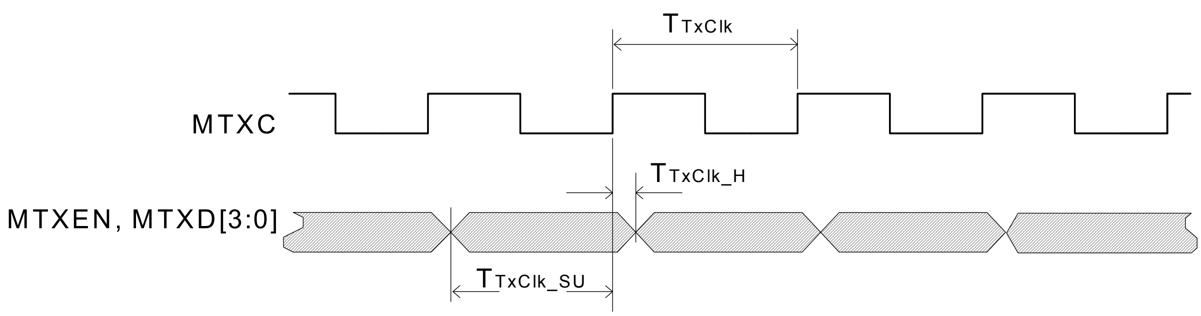
7.3.2 MII PHY Mode Timing

7.3.2.1 PHY Mode Transmit Timing Requirements

Table 60 PHY Mode Transmit Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100Mbps MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10Mbps MII	-	400	-	ns
T_{TxClk_SU}	MTXEN, MTXD to MTXC setup time	2	-	-	ns
T_{TxClk_H}	MTXEN, MTXD to MTXC hold time	0.5	-	-	ns

Figure 40 PHY Mode Transmit Timing

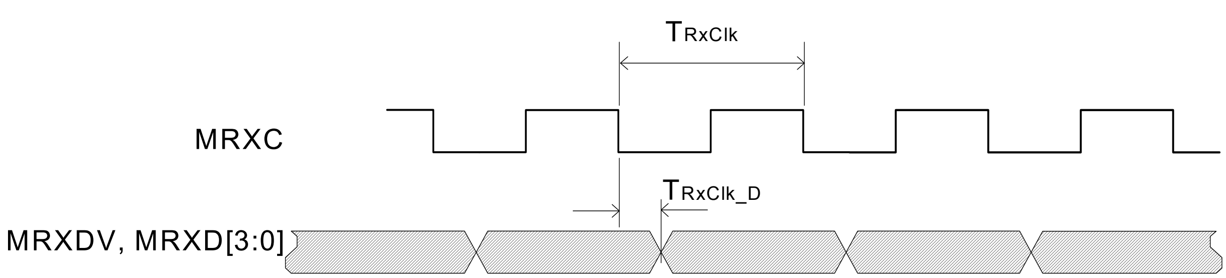


7.3.2.2 PHY Mode Receive Timing Requirements

Table 61 PHY Mode Receive Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100Mbps MII	-	40	-	ns
T_{RxClk}	Receive clock period 10Mbps MII	-	400	-	ns
T_{RxClk_D}	MRXC falling edge to MRXDV, MRXD	1	-	4	ns

Figure 41 PHY Mode Receive Timing



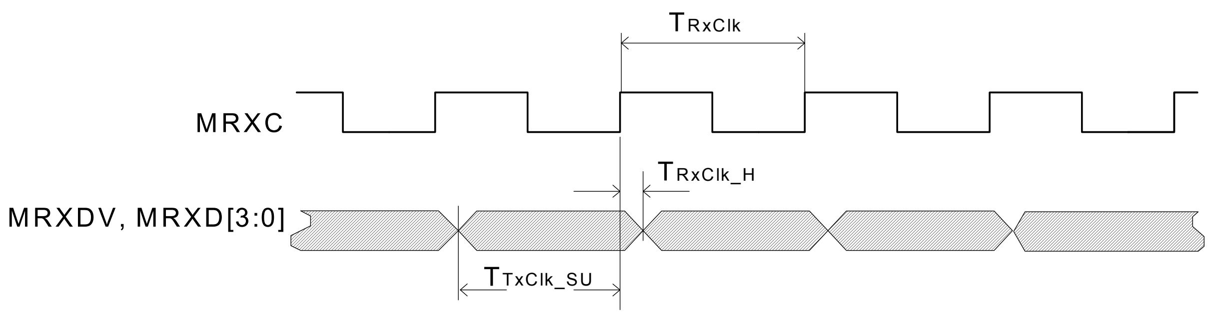
7.3.3 MII MAC Mode Timing

7.3.3.1 MAC Mode Receive Timing Requirements

Table 62 MAC Mode Receive Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100Mbps MII	-	40	-	ns
T_{RxClk}	Receive clock period 10Mbps MII	-	400	-	ns
T_{RxClk_SU}	MRXDV, MRXD to MRXC setup time	2	-	-	ns
T_{RxClk_H}	MRXDV, MRXD to MRXC hold time	0.5	-	-	ns

Figure 42 MAC Mode Receive Timing

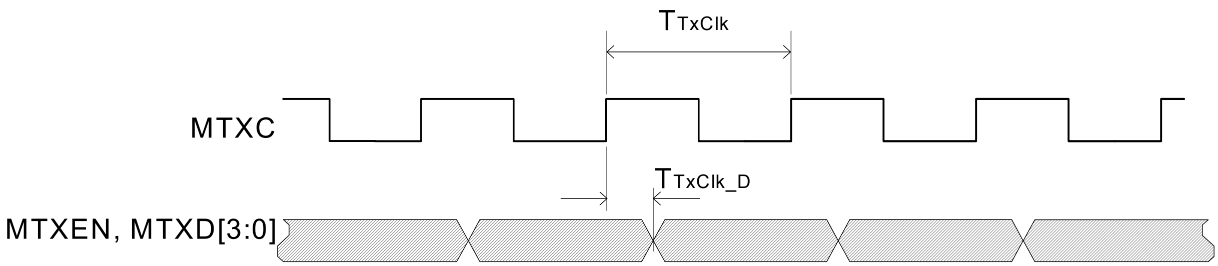


7.3.3.2 MAC Mode Transmit Timing Requirements

Table 63 MAC Mode Transmit Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100Mbps MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10Mbps MII	-	400	-	ns
T_{TxClk_D}	MTXC rising edge to MTXEN, MTXD	5	-	25	ns

Figure 43 MII Transmit Timing



7.3.4 PHY Management Timing

Table 64 PHY Management Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time	-	200	-	ns
T_{cl}	MDC Low Time	-	200	-	ns
T_{cm}	MDC cycle time	-	400	-	ns
T_{MD_SU}	MDIO set up time	10	-	-	ns
T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns

Figure 44 MDIO Receive Timing

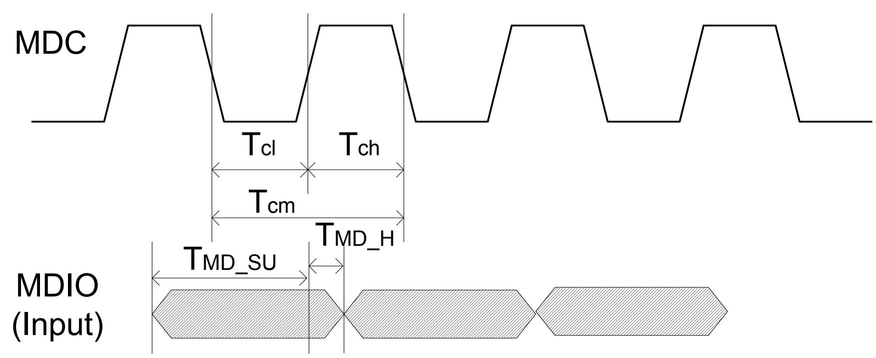
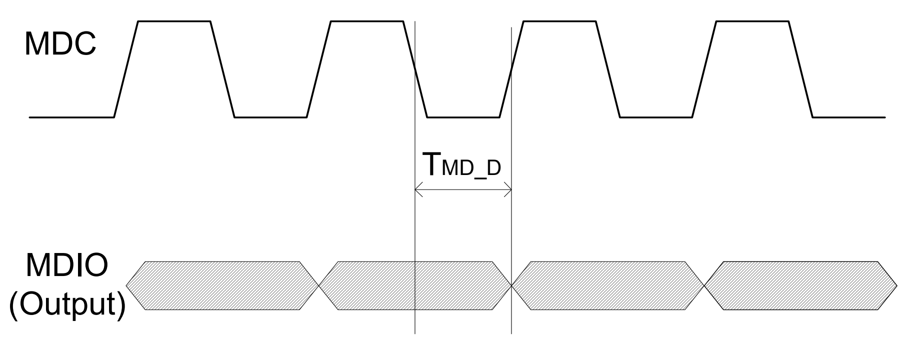


Figure 45 MDIO Transmit Timing



7.3.5 Power On Sequence and Reset Timing

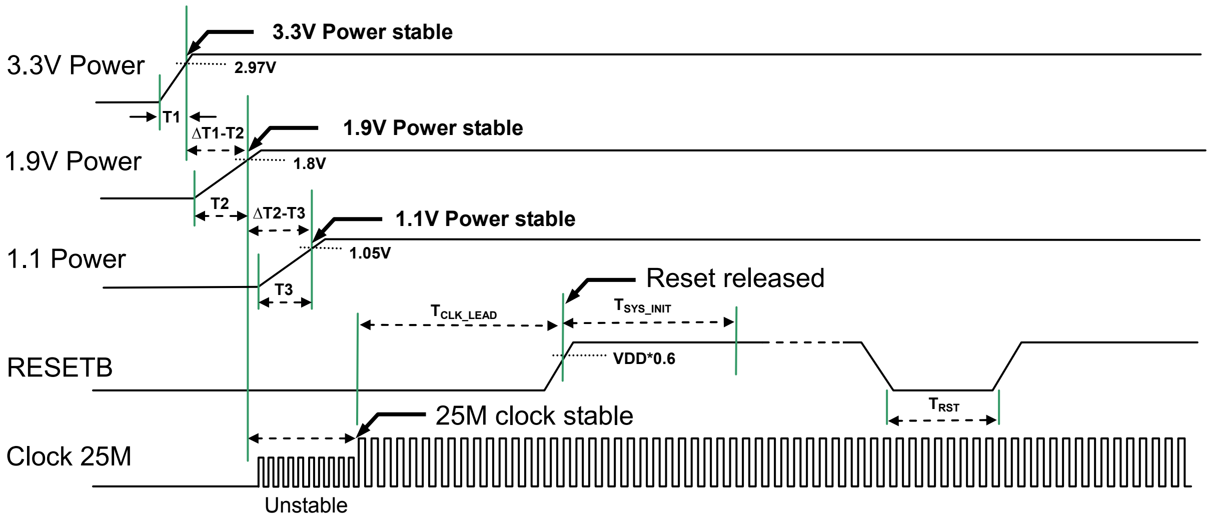


Table 65 Power on and Reset Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T1	Rising time of 3.3V Power	1	-	-	ms
T2	Rising time of 1.9V Power	1	-	-	ms
T3	Rising time of 1.1V Power	1	-	-	ms
ΔT1-T2	Time difference between 3.3V and 1.9V	0	-	10	ms
ΔT2-T3	Time difference between 1.9V and 1.1V	0	-	10	ms
T_{CLK_LEAD}	X1 valid period before reset released	5	-	-	ms
T_{SYS_INIT}	System initial completed, this time to keep silence.	100	-	-	ms
T_{RST}	Reset period for reset switch	3	20	-	ms

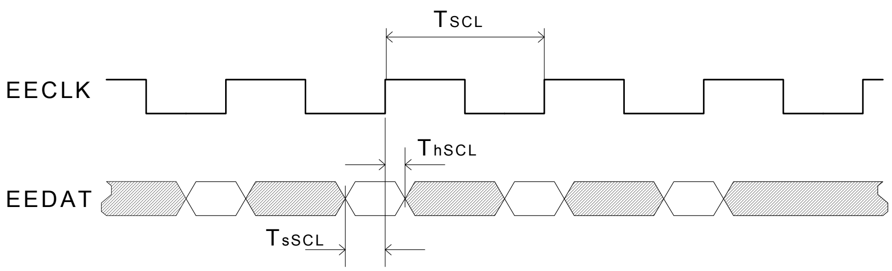
7.3.6 EEPROM Timing

7.3.6.1 Read data cycle

Table 66 EEPROM Timing Rx Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	EEDAT to EECLK setup time	20	-	-	ns
T_{hSCL}	EEDAT to EECLK hold time	20	-	-	ns

Figure 46 Read Data Cycle

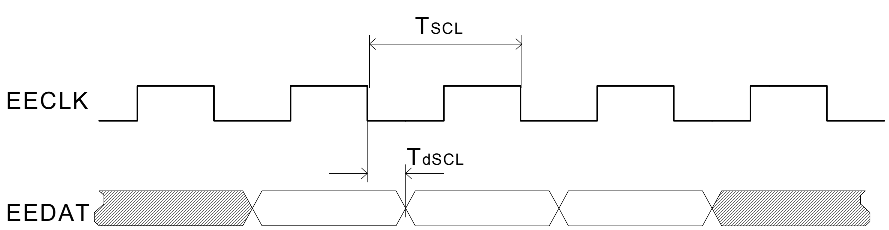


7.3.6.2 Command cycle

Table 67 EEPROM Timing Tx Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	EECLK falling edge to EEDAT	-	-	5200	ns

Figure 47 Command Cycle



7.4 External Clock Specifications

7.4.1 Crystal Specifications

Table 68 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25℃	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10°C ~ +70°C
6	Equivalent Series Resistance	40 ohm Max.
7	Load Capacitance	15 pF
8	Shunt Capacitance	7 pF Max

Parameter	Symbol	Min.	Typ.	Max.	Unit	Cconditions
Frequency		-	25	-	MHz	
Duty cycle		40	-	60	%	
Rise time	T_R	-	-	14	ns	
Fall time	T_F	-	-	14	ns	
Swing voltage (X2)		-	-	2.3	V	
Jitter		-	400	-	ps	
Frequency Tolerance		-50	-	+50	PPM	

7.4.2 External Oscillator Specifications

Table 69 External Oscillator Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Cconditions
Frequency		-	25	-	MHz	
Duty cycle		40	-	60	%	
Rise time	T_R	-	-	4	ns	
Fall time	T_F	-	-	4	ns	
Swing voltage		-	-	2	V	
Jitter		-	300	-	ps	
Frequency Tolerance		-50	-	+50	PPM	

7.5 Thermal Data

The junction temperature of chip (Tj) is a well-known key factor of IC characteristics and life time. There are there thermal resistance coefficients, $_{JA}$, ψ_{JT}, and $_{Jc}$, which are defined in JEDEC 51-2 and 51-6, will be provided to estimate Tj. If the Tj is over maximum limit, it is necessary to disperse heat by extra dissipation device, such as heat sink and electrical fan.

Thermal resistance represents the capability of an IC package to carry out the heat inside an IC chip. It is a complex function of package structure, material property, input power, environment variables such as air flow speed and PCB layers. The major thermal dissipation paths can be illustrated as following,

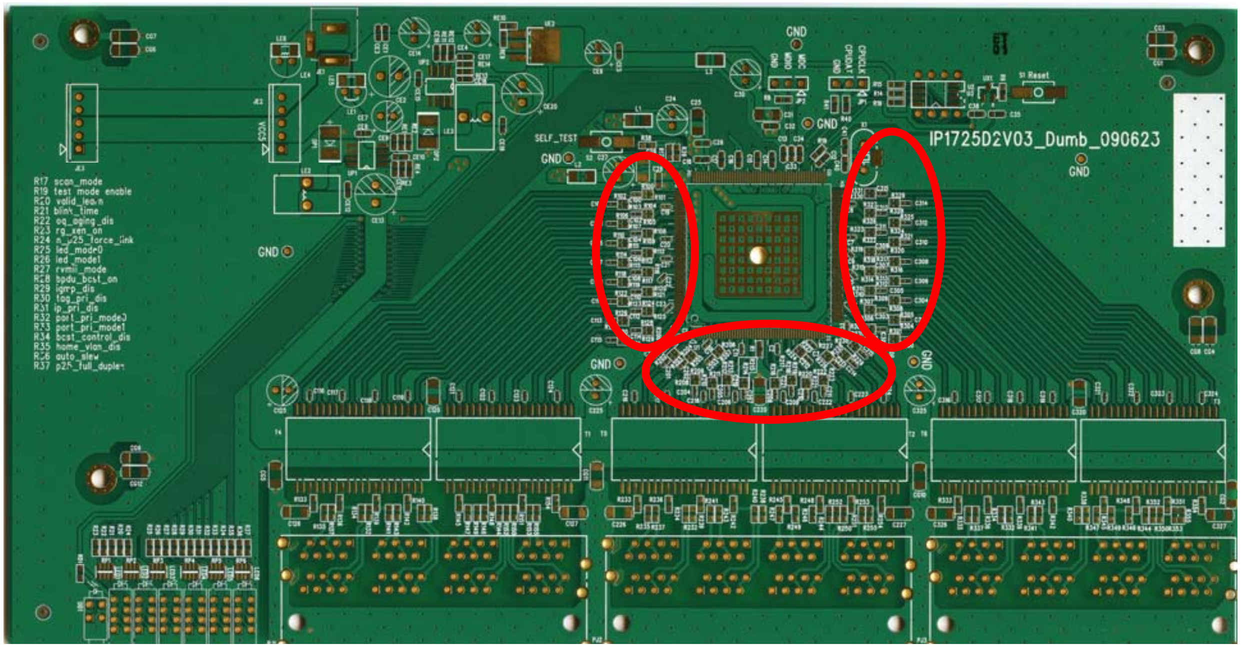
Table 70 Operation Range

Parameter	Min	Typical	Max	unit
Tj	0	-	125	℃
Ta	0	25	70	℃

Table 71 Thermal Resistance

Parameter	Condition	Value	Unit
Θ_{JA}	0 ft/s Air flow 2 layers PCB	15.3	℃/W
ψ_{JT}	0 ft/s Air flow 2 layers PCB	2.0	℃/W

8 Design and Layout Guide



Note: 49.9 ohm must be close to IP1725.

The detail descriptions refer to application note.

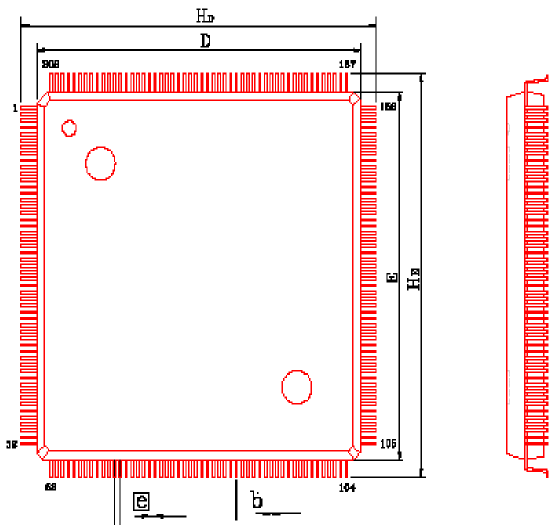
9 Order Information

Table 72 Order Information

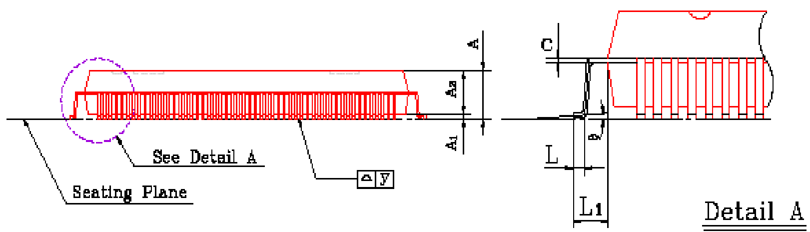
Part No.	Package	Notice
IP1725	208 Pin EDHS-QFP	-

10 Package Detail

208 EDHS-QFP Outline Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.154	—	0.160	3.92	—	4.07
A_1	0.010	—	—	0.25	—	—
A_2	0.124	0.127	0.130	3.15	3.23	3.30
b	0.007	—	0.011	0.18	—	0.28
c	0.005	—	0.009	0.13	—	0.23
D	1.098	1.102	1.106	27.90	28.00	28.10
E	1.098	1.102	1.106	27.90	28.00	28.10
e	0.020 BSC			0.50 BSC		
H_D	1.195	1.205	1.215	30.35	30.60	30.85
H_E	1.195	1.205	1.215	30.35	30.60	30.85
L	0.014	0.020	0.026	0.35	0.50	0.65
L_1	0.051 REF			1.30 REF		
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°



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