

N-Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4454 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

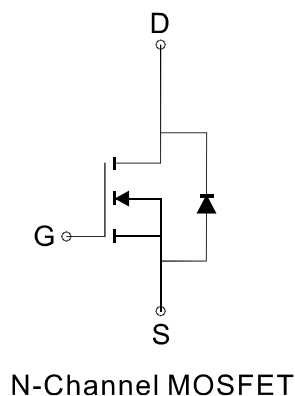
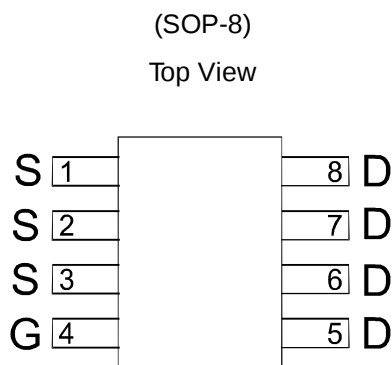
FEATURES

- $R_{DS(ON)} \leq 13m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 18m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION



Ordering Information: ME4454 (Pb-free)

ME4454-G (Green product- Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current($T_J = 150^\circ C$)*	$T_A = 25^\circ C$	I_D	10.6	A
	$T_A = 70^\circ C$		8.5	
Pulsed Drain Current		I_{DM}	43	A
Maximum Power Dissipation*	$T_A = 25^\circ C$	P_D	2.5	W
	$T_A = 70^\circ C$		1.6	
Operating Junction Temperature		T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	50	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	40			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V			1	μA
R _{DS(on)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =10A		11	13	mΩ
		V _{GS} =4.5V, I _D =5A		14	18	
V _{SD}	Diode Forward Voltage	I _S =2.3A, V _{GS} =0V		0.7	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =10V, I _D =10A		28		nC
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =4.5V, I _D =10A		14		
Q _{gs}	Gate-Source Charge			5.8		
Q _{gd}	Gate-Drain Charge			6.5		
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, f=1.0MHz		1259		pF
C _{oss}	Output Capacitance			139		
C _{rss}	Reverse Transfer Capacitance			93		
t _{d(on)}	Turn-On Delay Time	V _{DS} =20V, R _L =20Ω V _{GS} =10V, R _G =3.3Ω I _D =1A		18		ns
t _r	Turn-On Rise Time			11		
t _{d(off)}	Turn-Off Delay Time			50		
t _f	Turn-Off Fall Time			6		

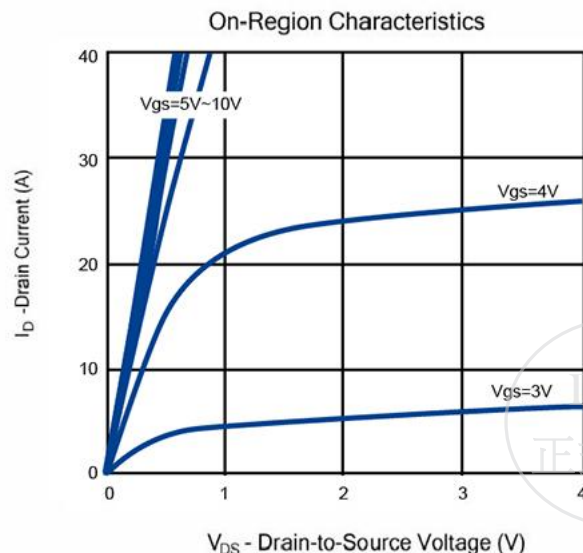
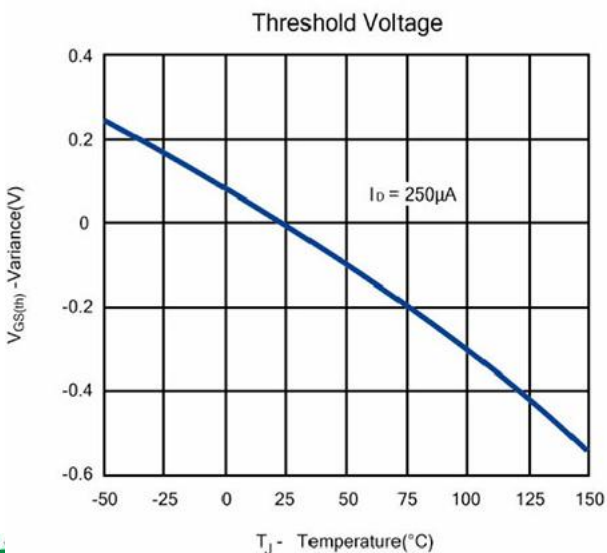
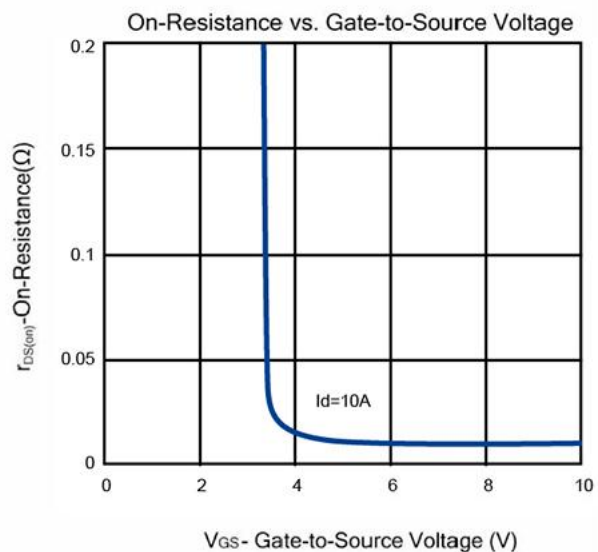
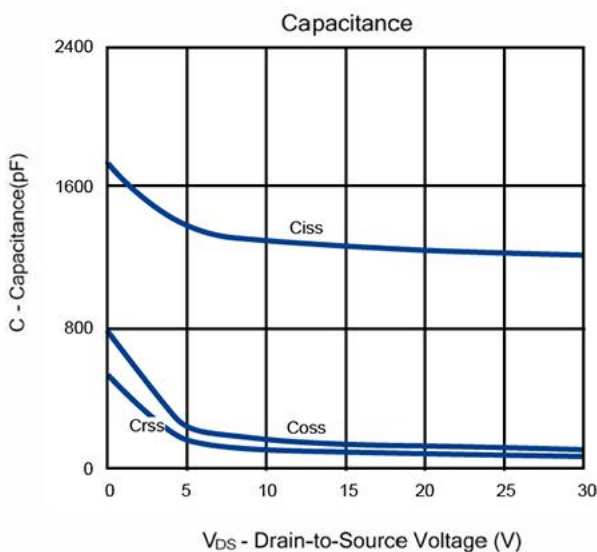
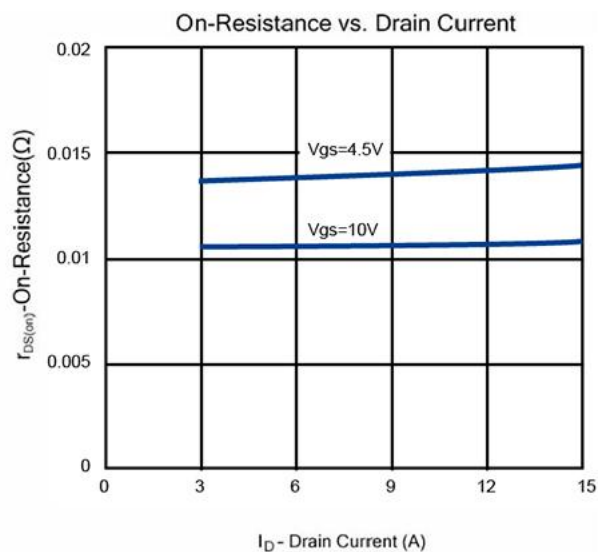
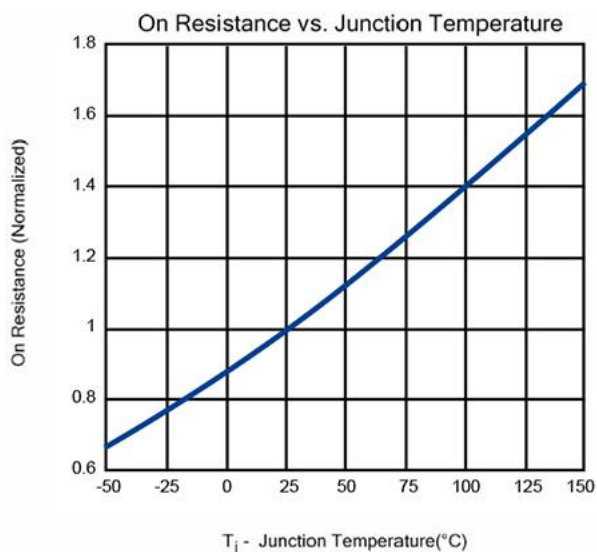
Notes: a. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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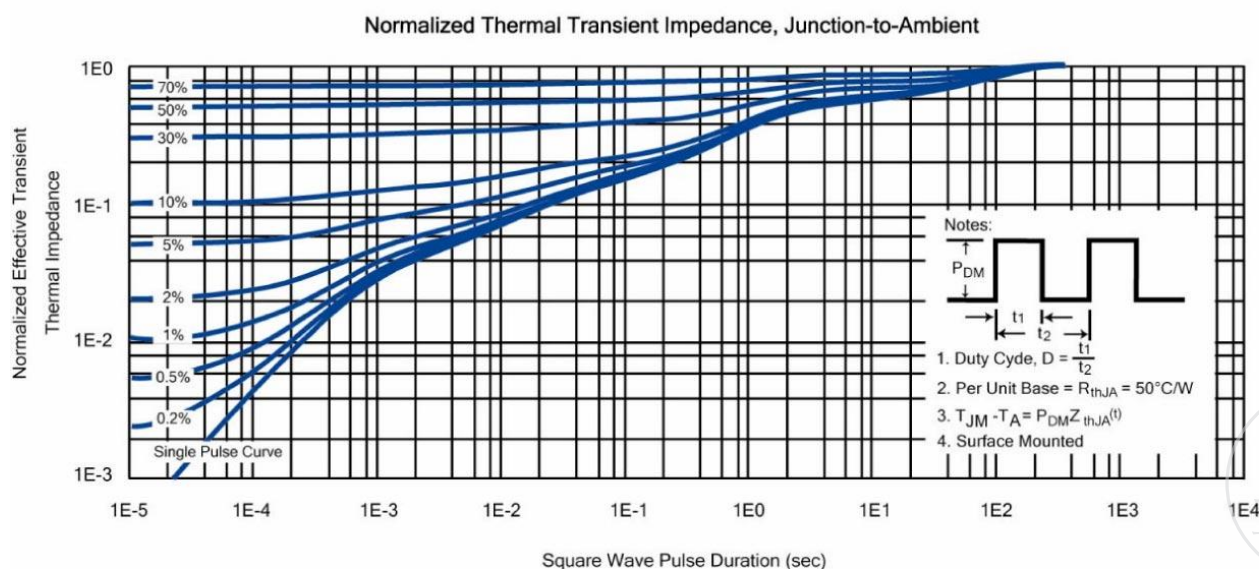
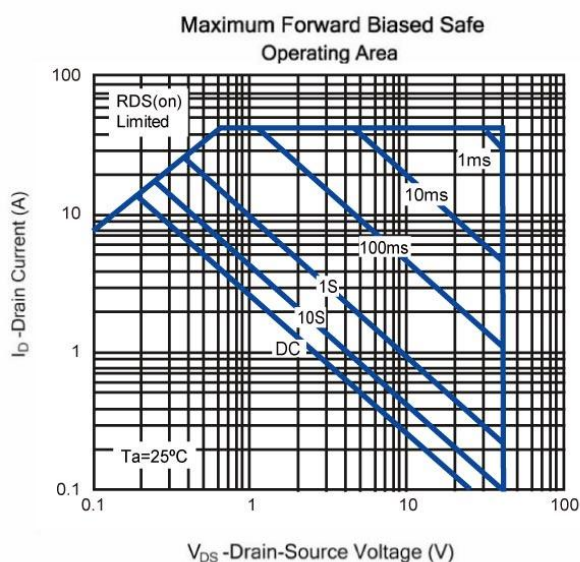
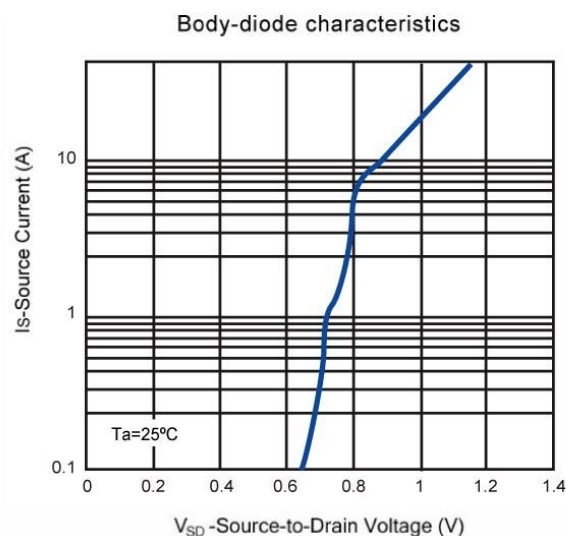
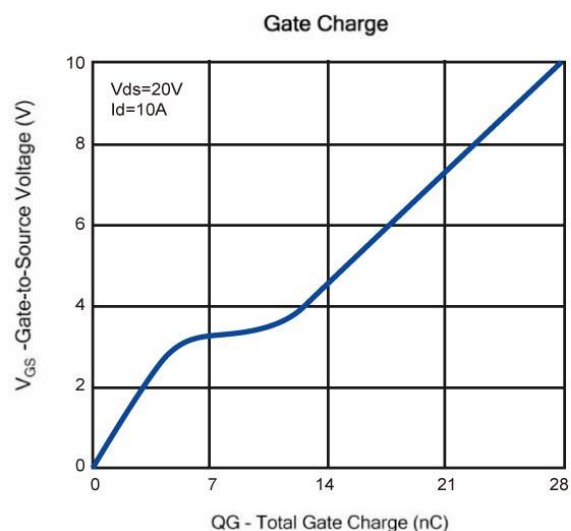
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Typical Characteristics (T_J = 25°C Noted)

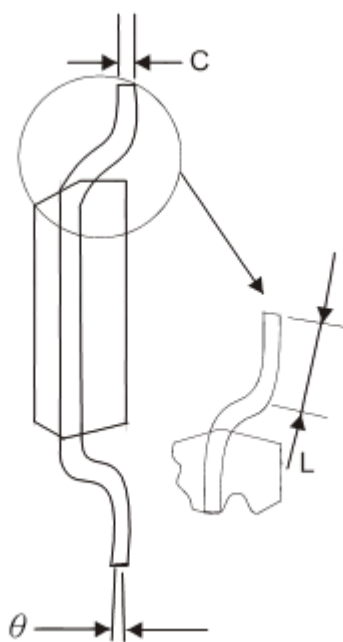
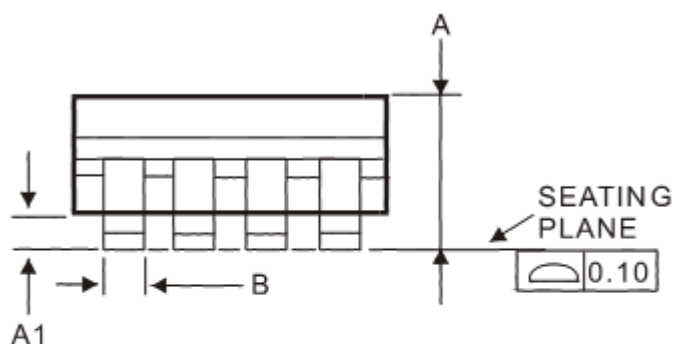
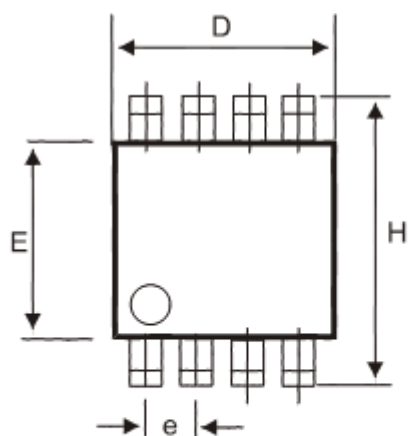


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SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°