

**Dual P-Channel 30V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME4953 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and low in-line power loss are needed in a very small outline surface mount package.

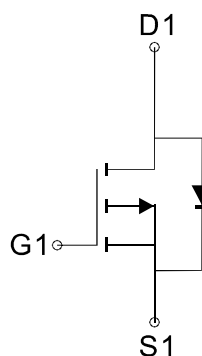
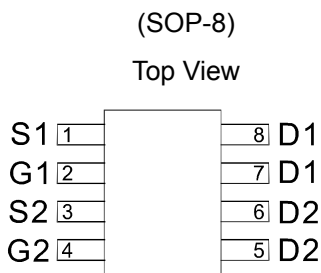
**FEATURES**

- R<sub>DS(ON)</sub> 60mΩ@V<sub>GS</sub>=-10V
- R<sub>DS(ON)</sub> 90mΩ@V<sub>GS</sub>=-4.5V
- Super high density cell design for extremely low R<sub>DS(ON)</sub>
- Exceptional on-resistance and maximum DC current capability

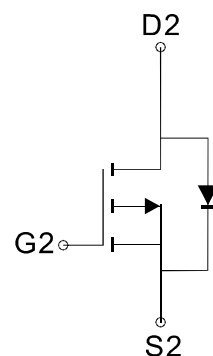
**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

**PIN CONFIGURATION**



P-Channel MOSFET



P-Channel MOSFET

Ordering Information: ME4953 (Pb-free)

ME4953-G (Green product-Halogen free)

**Absolute Maximum Ratings (T<sub>A</sub>=25 Unless Otherwise Noted)**

| Parameter                                       | Symbol           | Limit              | Unit |
|---|------------------|--------------------|------|
| Drain-Source Voltage                            | V <sub>DSS</sub> | -30                | V    |
| Gate-Source Voltage                             | V <sub>GSS</sub> | ±20                | V    |
| Continuous Drain Current (T <sub>j</sub> =150 ) | I <sub>D</sub>   | T <sub>A</sub> =25 | -5.3 |
|   |                  | T <sub>A</sub> =70 | -4.3 |
| Pulsed Drain Current                            | I <sub>DM</sub>  | -30                | A    |
| Continuous Source Current (Diode Conduction)    | I <sub>S</sub>   | -1.7               | A    |
| Maximum Power Dissipation                       | P <sub>D</sub>   | T <sub>A</sub> =25 | 2.0  |
|   |                  | T <sub>A</sub> =70 | 1.3  |
| Operating Junction Temperature                  | T <sub>J</sub>   | -55 to 150         |      |
| Storage Temperature Range                       | T <sub>stg</sub> | -55 to 150         |      |
| Thermal Resistance-Junction to Ambient*         | R <sub>θJA</sub> | T 10 sec           | 47   |
|   |                  | Steady State       | 75   |
| Thermal Resistance-Junction to Case             | R <sub>θJC</sub> | 45                 |      |

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

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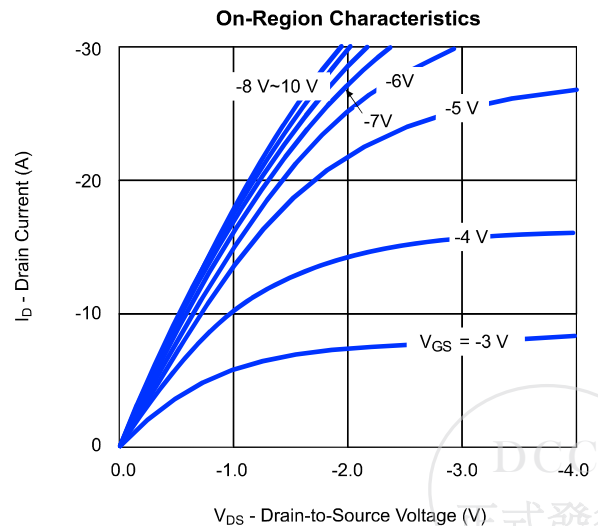
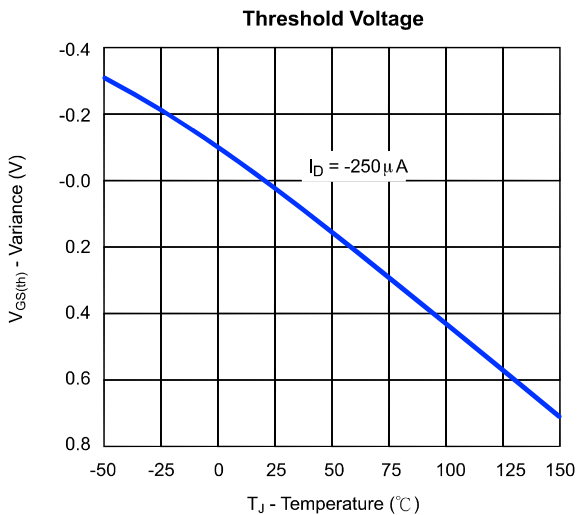
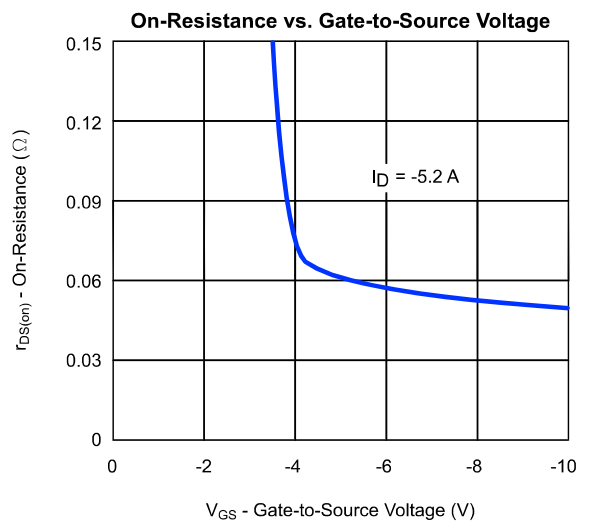
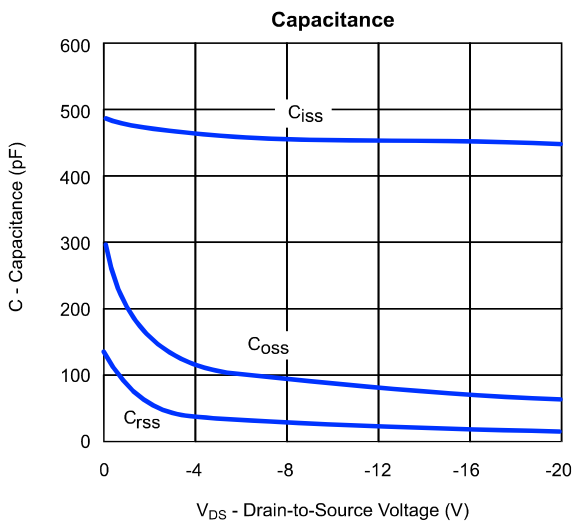
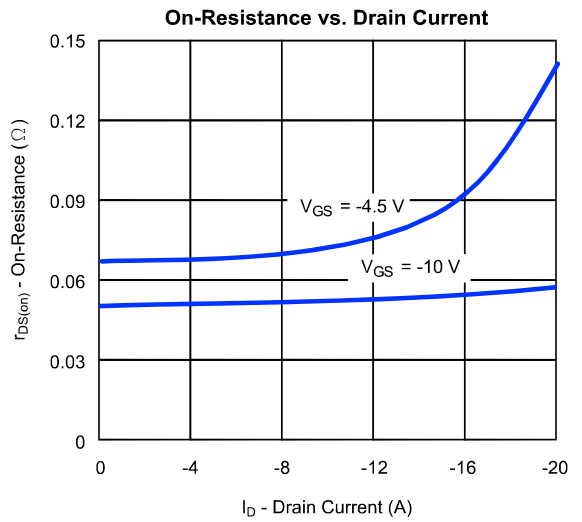
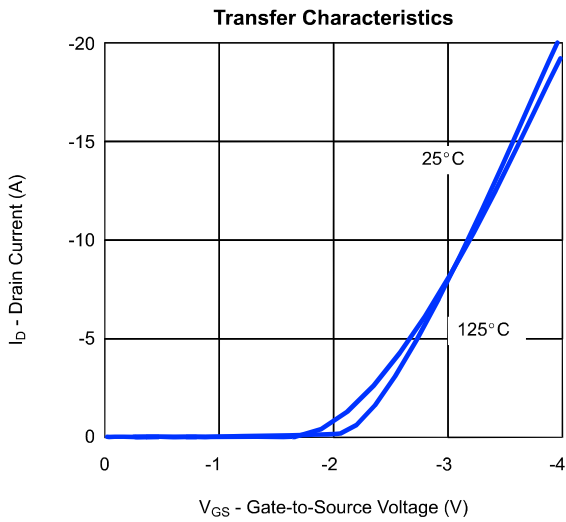
Electrical Characteristics (T<sub>A</sub> = 25 Unless Otherwise Specified)

| Symbol              | Parameter                       | Limit   | Min | Typ  | Max  | Unit |
|---------------------|---------------------------------|---|-----|------|------|------|
| <b>STATIC</b>       |                                 |   |     |      |      |      |
| V <sub>GS(th)</sub> | Gate Threshold Voltage          | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA  | -1  | -1.4 | -3   | V    |
| I <sub>GSS</sub>    | Gate Leakage Current            | V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V  |     |      | ±100 | nA   |
| I <sub>DSS</sub>    | Zero Gate Voltage Drain Current | V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V  |     |      | -1   | μA   |
|                     |                                 | V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V<br>T <sub>J</sub> =55  |     |      | -25  |      |
| R <sub>DS(ON)</sub> | Drain-Source On-Resistance      | V <sub>GS</sub> =-10V, I <sub>D</sub> = -5.3A   |     | 50   | 60   | m    |
|                     |                                 | V <sub>GS</sub> =-4.5V, I <sub>D</sub> = -4.2A  |     | 69   | 90   |      |
| V <sub>SD</sub>     | Diode Forward Voltage           | I <sub>S</sub> =-1.7A, V <sub>GS</sub> =0V  |     | -0.8 | -1.2 | V    |
| <b>DYNAMIC</b>      |                                 |   |     |      |      |      |
| R <sub>g</sub>      | Gate resistance                 | V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz  |     | 3.5  |      | Ω    |
| C <sub>iss</sub>    | Input capacitance               | V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1.0MHz  |     | 450  | 490  | pF   |
| C <sub>oss</sub>    | Output Capacitance              |   |     | 70   |      |      |
| C <sub>rss</sub>    | Reverse Transfer Capacitance    |   |     | 20   |      |      |
| Q <sub>g</sub>      | Total Gate Charge               | V <sub>DS</sub> =-15V, V <sub>GS</sub> =-10V,<br>I <sub>D</sub> =-5.3A  |     | 14   | 17   | nC   |
| Q <sub>gs</sub>     | Gate-Source Charge              |   |     | 4    |      |      |
| Q <sub>gd</sub>     | Gate-Drain Charge               |   |     | 3    |      |      |
| t <sub>d(on)</sub>  | Turn-On Delay Time              | V <sub>DD</sub> =-15V, R <sub>L</sub> =15Ω<br>I <sub>D</sub> =-1.0A, V <sub>GEN</sub> =-10V<br>R <sub>G</sub> =6Ω |     | 27   | 33   | ns   |
| t <sub>r</sub>      | Turn-On Rise Time               |   |     | 11   | 15   |      |
| t <sub>d(off)</sub> | Turn-Off Delay Time             |   |     | 40   | 52   |      |
| t <sub>f</sub>      | Turn-Off Fall Time              |   |     | 4    | 6    |      |

Notes: a. Pulse test; pulse width 300us, duty cycle 2%

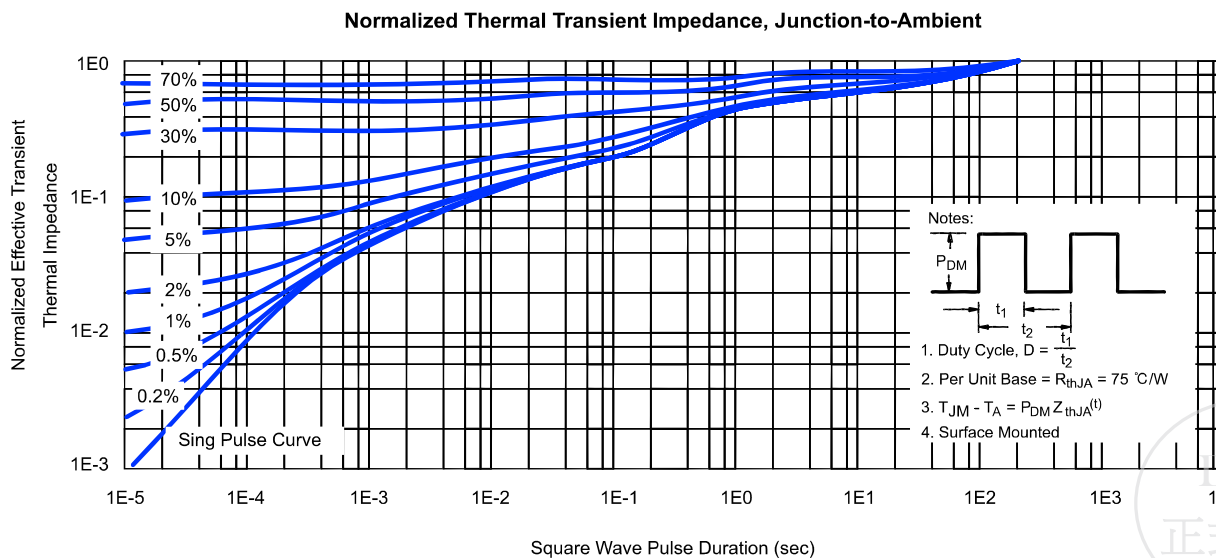
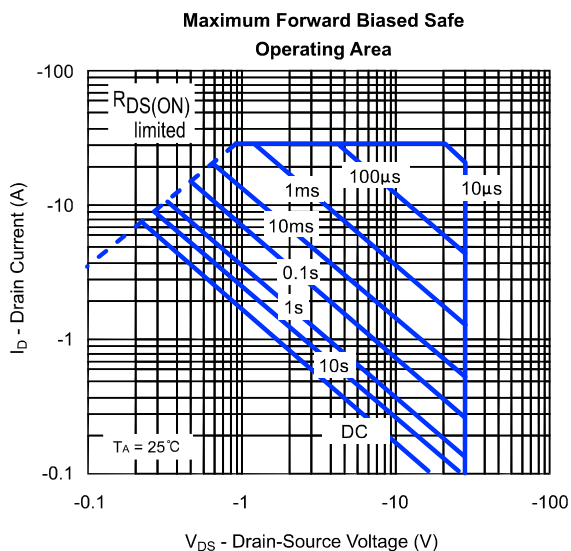
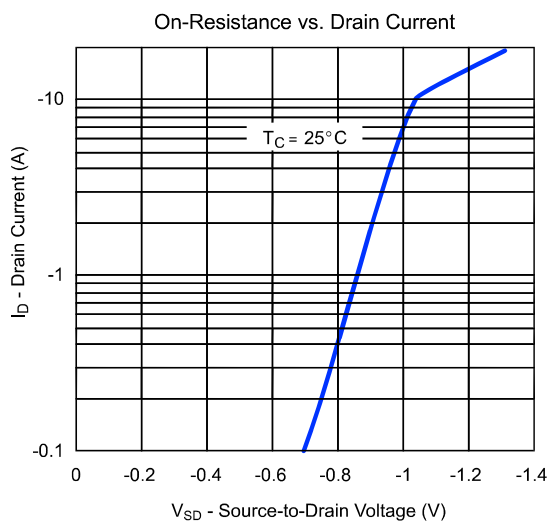
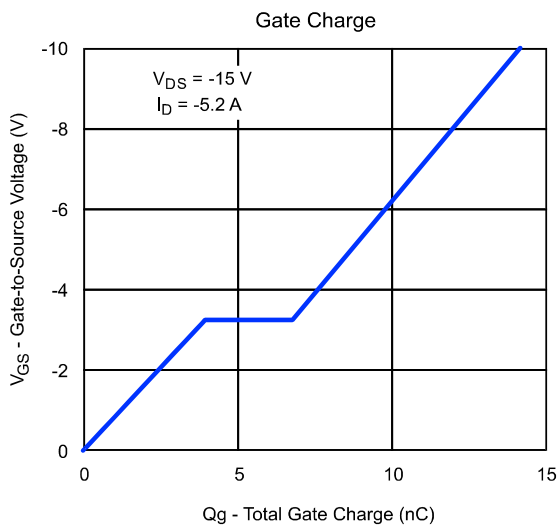


Typical Characteristics (T<sub>J</sub> = 25    Noted)

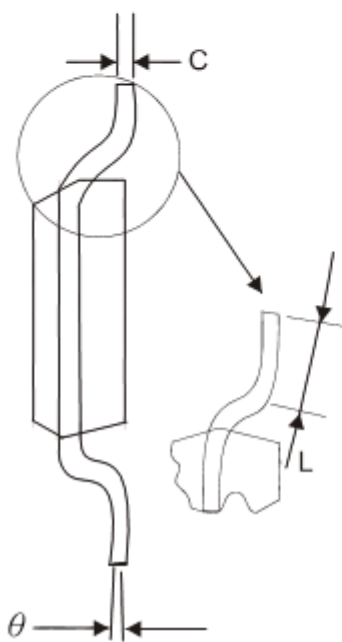
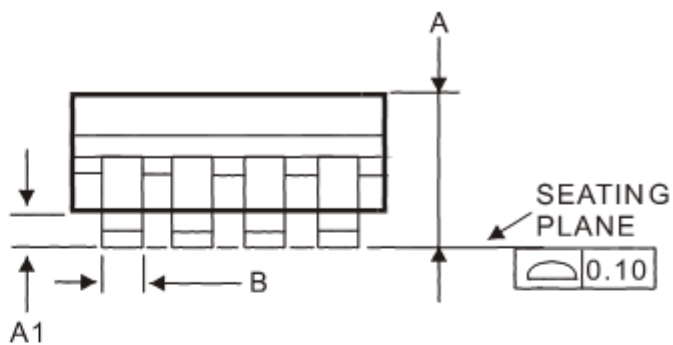
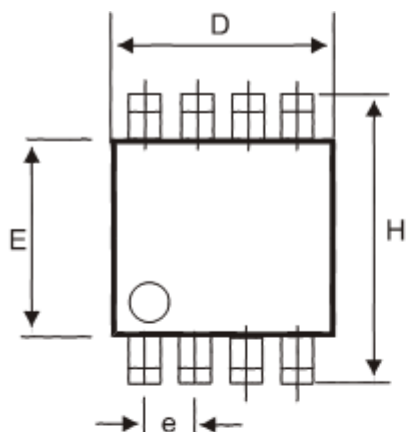


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Typical Characteristics (T<sub>J</sub> = 25 °C Noted)



**SOP-8 Package Outline**



| DIM | MILLIMETERS (mm) |      |
|-----|------------------|------|
|     | MIN              | MAX  |
| A   | 1.35             | 1.75 |
| A1  | 0.10             | 0.25 |
| B   | 0.35             | 0.49 |
| C   | 0.18             | 0.25 |
| D   | 4.80             | 5.00 |
| E   | 3.80             | 4.00 |
| e   | 1.27 BSC         |      |
| H   | 5.80             | 6.20 |
| L   | 0.40             | 1.25 |
|     | 0°               | 7°   |

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

