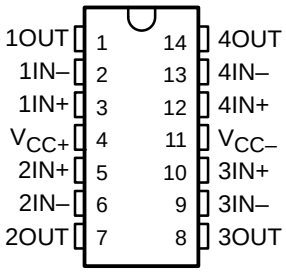
- **Wide Range of Supply Voltages, Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**

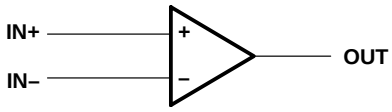
(TOP VIEW)



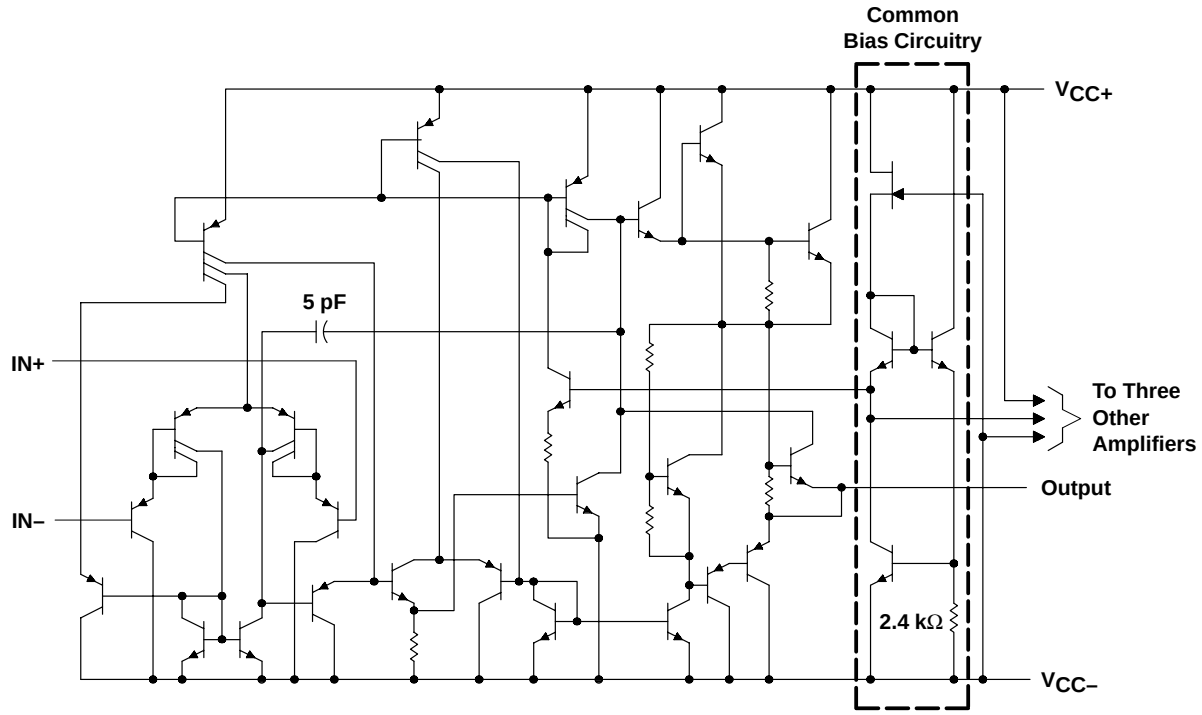
description

XDXL3403 quadruple operational amplifiers similar in performance to the XD741, but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to VCC – 1.5 V. Quiescent supply currents are less than one-half those of the XD741.
and the XDXL3403 is characterized for operation from 0°C to 70°C.

logic diagram (each amplifier)



schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+}	18 V
V_{CC-}	–18 V
Supply voltage, V_{CC+} with respect to V_{CC-}	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage (see Notes 1 and 3)	±18 V
Package thermal impedance, θ_{JA} (see Note 4): 3403	80°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, Tstg	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-}.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		5	30	V
	Dual-supply voltage	V_{CC+}	2.5	15	V
		V_{CC-}	–2.5	–15	V
T_A	Operating free-air temperature	XDXL3403	0	70	°C

electrical characteristics at specified free-air temperature, V_{CC+} = 14 V, V_{CC-} = 0 V for $V_{CC\pm}$ = ±15 V for XDXL3403 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		XDXL3403			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 5	25°C		2	10	mV
			Full range			12	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	See Note 5	Full range		10		µV/°C
I_{IO}	Input offset current	See Note 5	25°C		30	50	nA
			Full range			200	
$\alpha_{I_{IO}}$	Temperature coefficient of input offset current	See Note 5	Full range		50		pA/C
I_{IB}	Input bias current	See Note 5	25°C		–0.2	–0.5	µA
			Full range			–0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		V
		R_L = 2 kΩ	25°C	±10	±13		
		R_L = 2 kΩ	Full range	±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		V/mV
			Full range	15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1		MHz
ϕ_m	Phase margin	C_L = 200 pF, R_L = 2 kΩ	25°C		60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±2.5 to ±15 V	25°C		30	150	µV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 5	25°C		2.8	7	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for XDXL3403.
‡ The V_{ICR} limits are linked directly, volt-for-volt, to supply voltage; the positive limit is 2 V less than V_{CC+}.
§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
NOTE 5: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_OXDXL3403.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	XDXL3403			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V		–0.2	–0.5	µA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	V_{CC+} – 1.7			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		V/mV
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V			150	µV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		2.5	7	mA
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Output will swing essentially to ground.

operating characteristics, $V_{CC\pm}$ = ±15 V for XDXL3403, T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS				TYP	UNIT
SR	Slew rate at unity gain	V_I = ±10 V,	C_L = 100 pF,	R_L = 2 kΩ,	See Figure 1	0.6	V/µs
t_r	Rise time	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ,	See Figure 1	0.35	µs
t_f	Fall time	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ,	See Figure 1	0.35	µs
	Overshoot factor	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ,	See Figure 1	20	%
	Crossover distortion	$V_{I(PP)}$ = 30 mV,	V_{OPP} = 2 V,	f = 10 kHz		1	%

PARAMETER MEASUREMENT INFORMATION

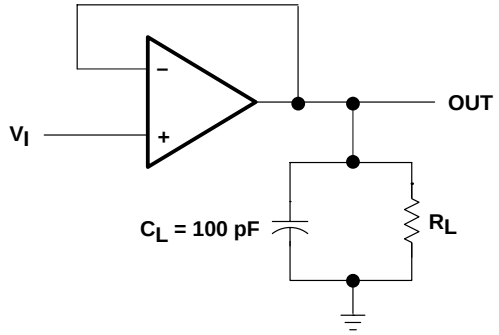


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

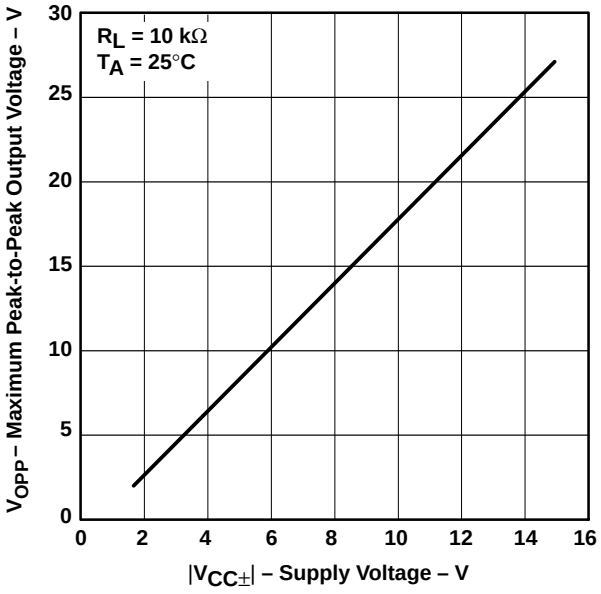


Figure 2

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

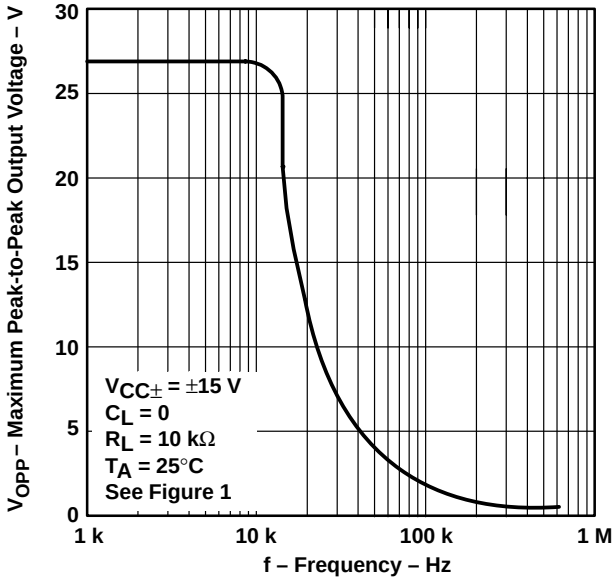


Figure 3

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

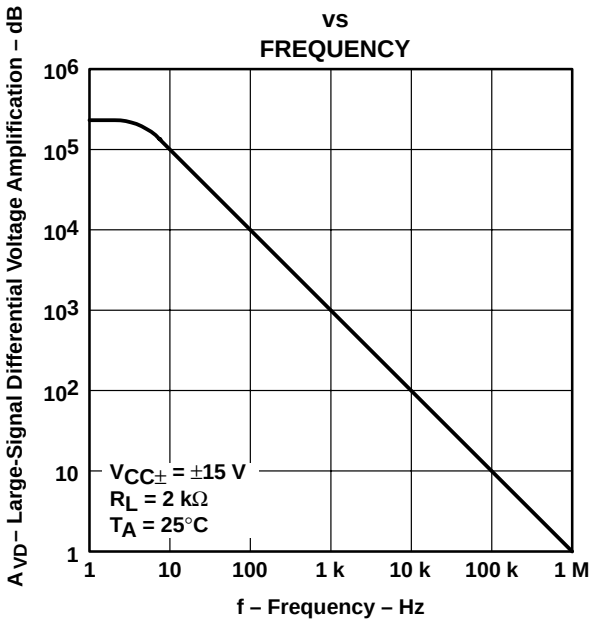


Figure 4

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

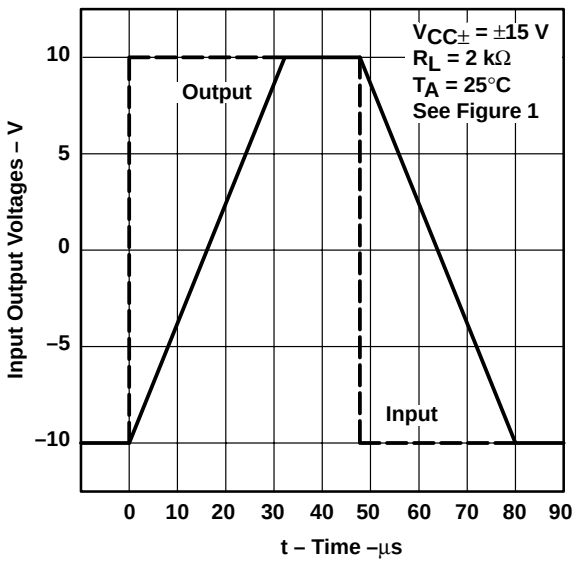


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

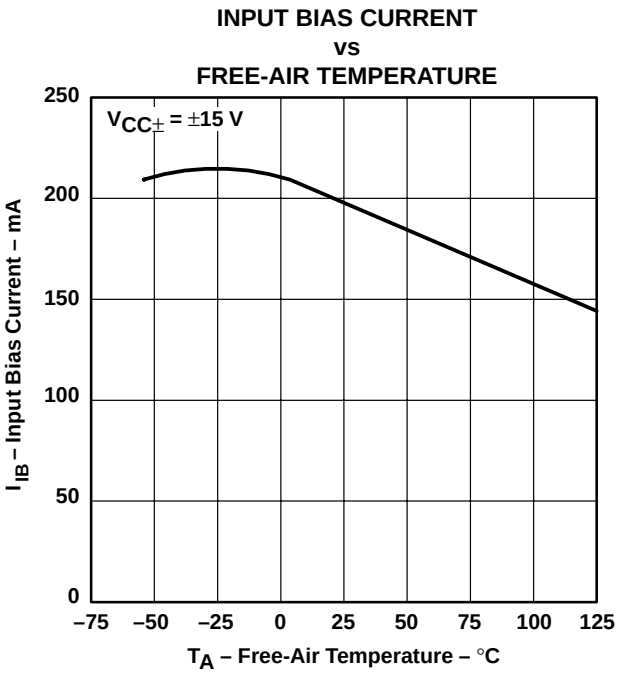


Figure 6

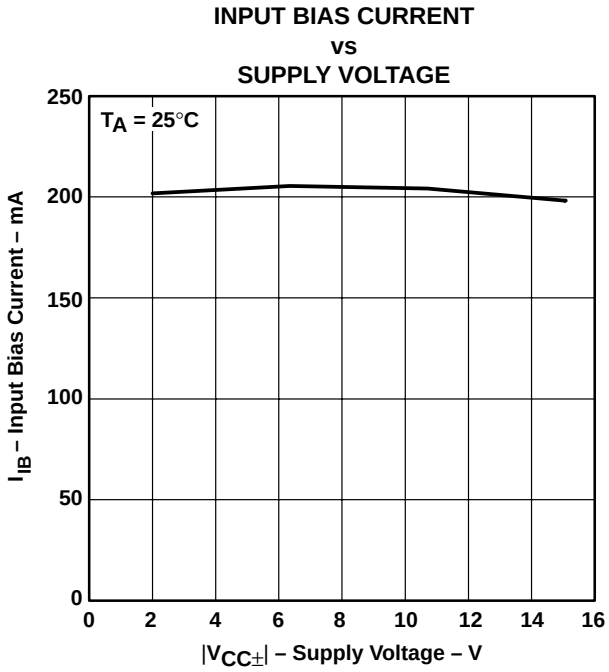


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

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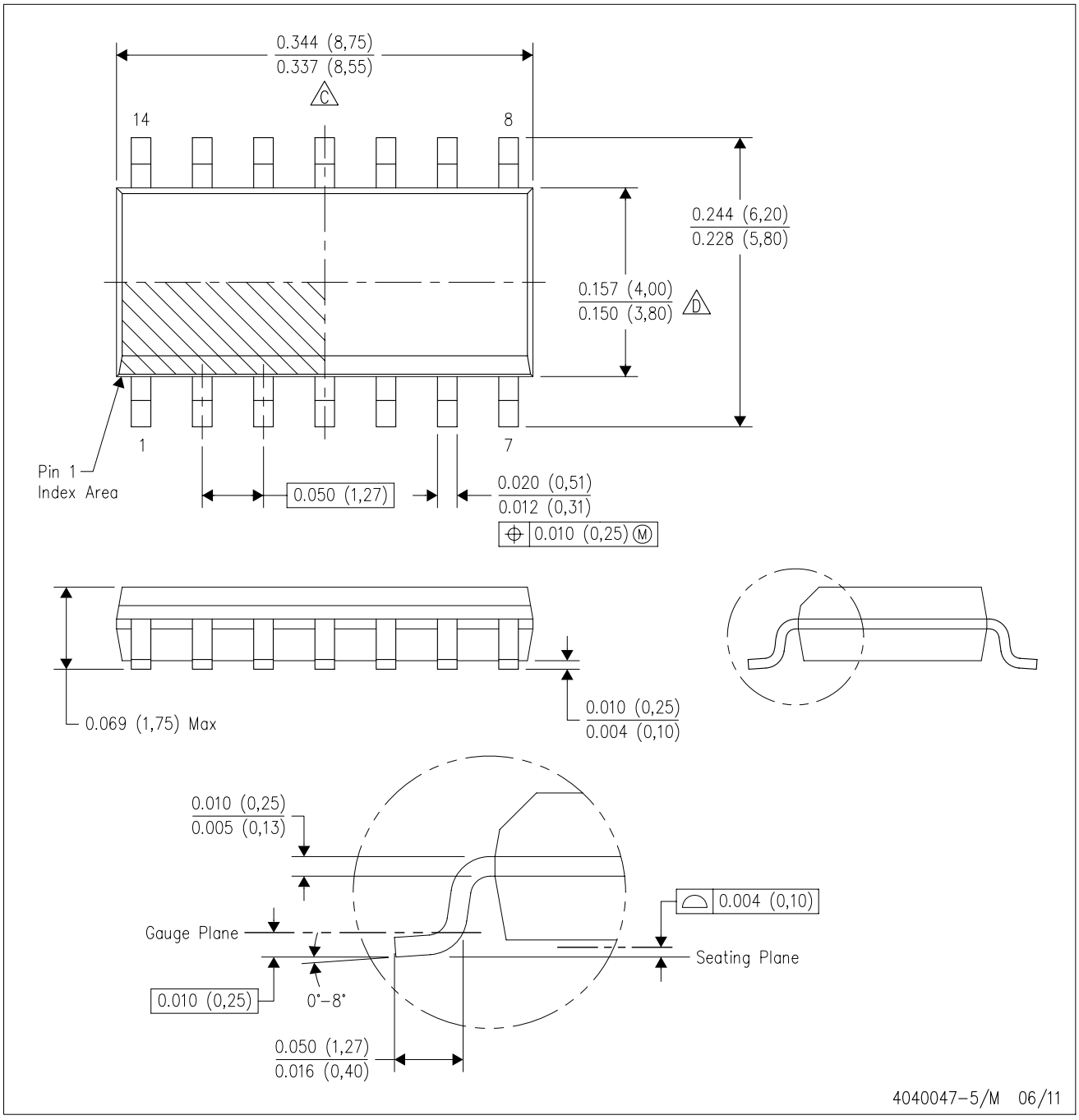
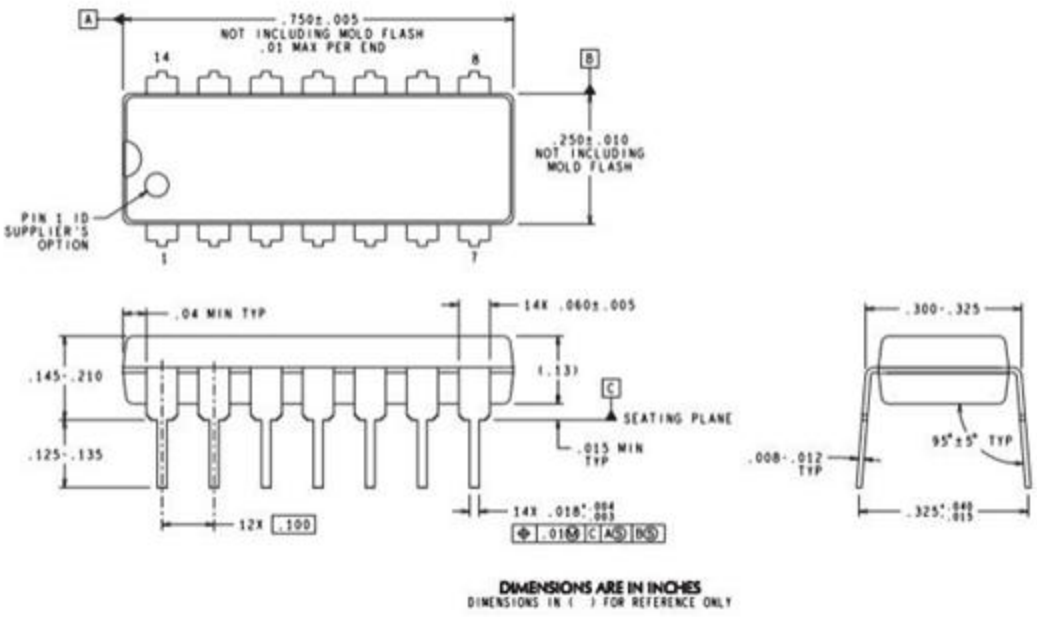


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

DIP14



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA