

## Low Noise Amplifier for LTE Low Band

### FEATURES

- Operating frequency 728MHz to 960MHz
- Noise figure(NF) =0.7dB
- High power gain =16.4dB
- In band IIP3=+2.7dBm
- Input 1dB compression point=-1dBm
- Supply voltage: 1.5V to 3.1V
- Supply current 7.6mA
- Input and output DC decoupled
- Requires only one input matching inductor
- Integrated matching for the output
- FCDFN 1.1mmX0.7mmX0.37mm -6L package
- 2kV HBM ESD protection (including RFIN and RFOUT pin)

### APPLICATIONS

- Cell phones
- Tablets
- Other RF front-end modules

### GENERAL DESCRIPTION

The AW5008L1 is a Low Noise Amplifier designed for LTE receiver applications. The AW5008L1 requires only one external input matching inductor, reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The AW5008L1 achieves low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.1V. All these features make AW5008L1 an excellent choice for LTE LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost.

The AW5008L1 is available in a small lead-free, RoHS-Compliant, FCDFN 1.1mmX0.7mmX0.37 mm -6L package.

### TYPICAL APPLICATION CIRCUIT

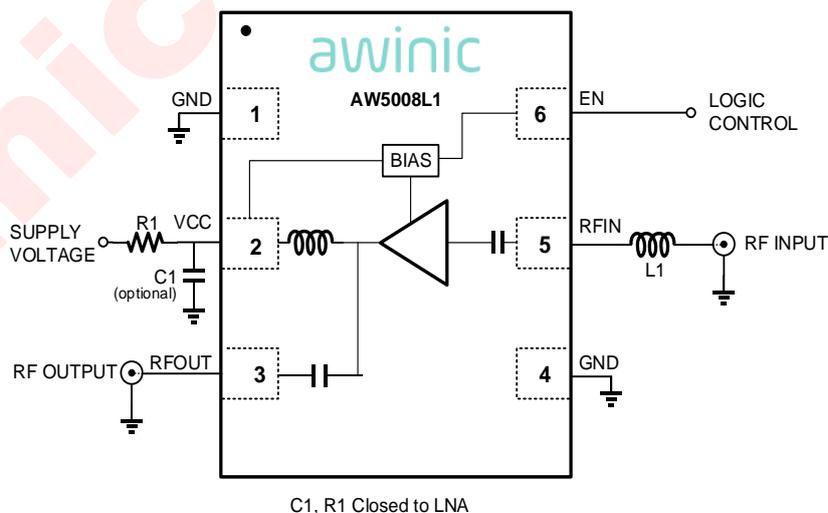


Figure 1 Typical Application Circuit of AW5008L1

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## PIN CONFIGURATION AND TOP MARK

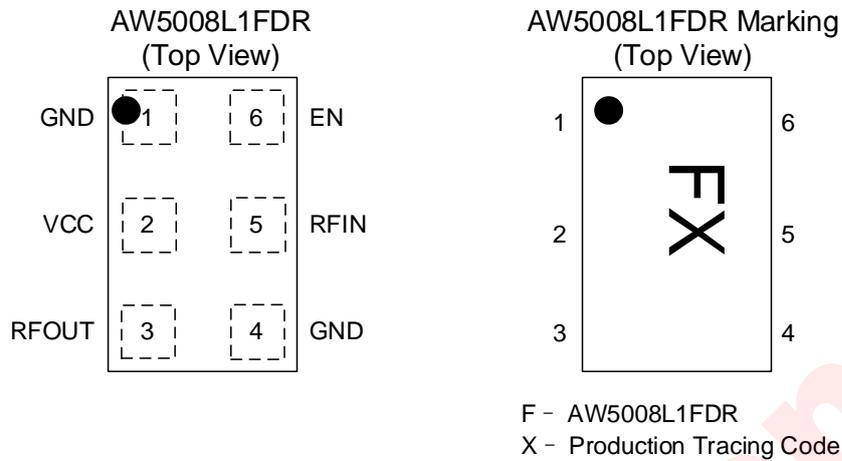


Figure 2 Pin Configuration and Top Mark

## PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground.
2	VCC	Supply connection.
3	RFOUT	RF output
4	GND	Ground
5	RFIN	RF input
6	EN	EN (high level) supports 1.8V/2.8V IO with internal 150kohm pull-down resistor.

## FUNCTIONAL BLOCK DIAGRAM

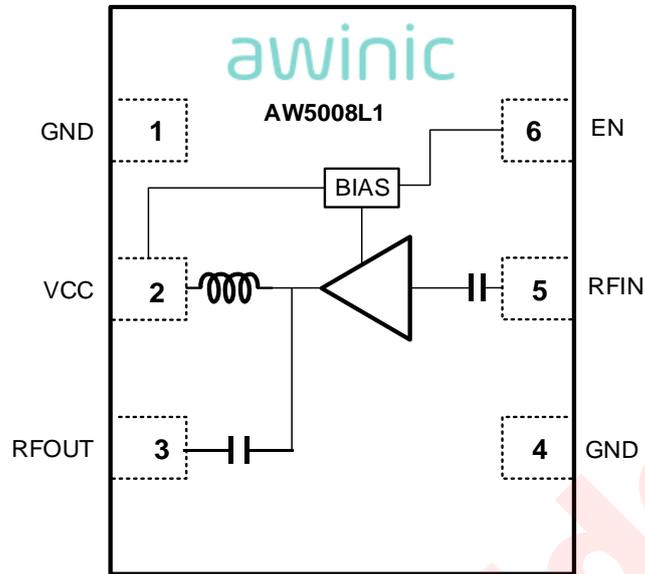
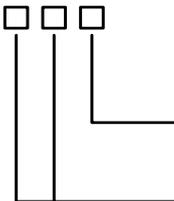


Figure 3 Functional Block Diagram

## ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW5008L1FDR	-40°C~85°C	FCDFN 1.1mmX 0.7mm -6L	F	MSL1	ROHS+HF	3000 units/Tape & Reel

AW5008L1

Shipping  
R: Tape & ReelPackage Type  
FD: FCDFN

**ABSOLUTE MAXIMUM RATINGS<sup>[1]</sup>**

PARAMETERS	RANGE
Supply voltage VCC	-0.3V to 3.6V
EN pin voltage	-0.3V to 3.6V
Supply maximum current ICC	30mA
RF input power Pin	10dBm
Maximum Junction temperature T <sub>JMAX</sub>	150°C
Storage temperature T <sub>STG</sub>	-65°C to 150°C
Operating free-air temperature range	-40°C to 85°C
Lead temperature (Soldering 10 Seconds)	260°C
ESD <sup>[2]</sup>	
HBM	±2kV
CDM	±1kV
Latch-up	
Standard: JEDEC STANDARD NO.78D NOVEMBER 2011	+IT: +200mA -IT: -200mA

[1] Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

[2] The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9. The CDM test method: JEDEC EIA/JESD22-C101F.

## ELECTRICAL CHARACTERISTICS

TA=+25°C , V<sub>CC</sub>=2.8V, EN=2.8V, frequency=728MHz to 960MHz. Input matched to 50Ω using a 18nH<sup>[3]</sup> inductor in series. (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
<b>DC Electrical Characteristic</b>						
VCC	Supply Voltage		1.5	-	3.1	V
VEN	Digital Input-Logic High		0.8			V
	Digital Input-Logic Low				0.45	V
<b>Gain Mode</b>						
ICC	Supply Current			8.6		mA
Gp	Power Gain	f=740MHz [4]		15.3		dB
		f=882MHz [5]		16.4		
		f=943MHz [6]		16.2		
RLin	Input Return Loss	f=740MHz [4]		-5.5		dB
		f=882MHz [5]		-11		
		f=943MHz [6]		-12.5		
RLout	Output Return Loss	f=740MHz [4]		-6		dB
		f=882MHz [5]		-12.0		
		f=943MHz [6]		-12.0		
ISL	Reverse Isolation	f=740MHz [4]		-34.0		dB
		f=882MHz [5]		-30.0		
		f=943MHz [6]		-30.0		
NF	Noise Figure	f=740MHz [4][7]		0.7		dB
		f=882MHz [5][7]		0.7		
		f=943MHz [6][7]		0.75		
IP1dB	In-band input 1dB-compression point	f=740MHz [4]		-1		dBm
		f=882MHz [5]		-5		
		f=943MHz [6]		-5		
IIP3ib	In-band input 3 <sup>rd</sup> -order intercept point	f=740MHz [4]		1.8		dBm
		f=882MHz [5]		2.7		
		f=943MHz [6]		2.6		
ton	turn-on time	time from V <sub>EN</sub> ON to 90% of the gain		1.5		μs
toff	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.5		μs

[3] High quality-factor 18nH inductor.

[4] E-UTRA operating band 17(734MHz to 746MHz) , input power is -25dBm.

[5] E-UTRA operating band 5(869MHz to 894MHz) , input power is -25dBm.

[6] E-UTRA operating band 8(925MHz to 960MHz) , input power is -25dBm.

[7] PCB losses are subtracted.

TA=+25°C , V<sub>CC</sub>=1.8V, EN=1.8V, frequency=728MHz to 960MHz. Input matched to 50Ω using a 18nH<sup>[3]</sup> inductor in series. (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
<b>DC Electrical Characteristic</b>						
VCC	Supply Voltage		1.5	-	3.1	V
VEN	Digital Input-Logic High		0.8			V
	Digital Input-Logic Low				0.45	V
<b>Gain Mode</b>						
ICC	Supply Current			7.6		mA
Gp	Power Gain	f=740MHz [4]		15.0		dB
		f=882MHz [5]		16.0		
		f=943MHz [6]		16.0		
RLin	Input Return Loss	f=740MHz [4]		-6.0		dB
		f=882MHz [5]		-11.0		
		f=943MHz [6]		-12.0		
RLout	Output Return Loss	f=740MHz [4]		-7.0		dB
		f=882MHz [5]		-12.5		
		f=943MHz [6]		-13.0		
ISL	Reverse Isolation	f=740MHz [4]		-33.0		dB
		f=882MHz [5]		-30.0		
		f=943MHz [6]		-29.0		
NF	Noise Figure	f=740MHz [4][7]		0.7		dB
		f=882MHz [5][7]		0.7		
		f=943MHz [6][7]		0.75		
IP1dB	In-band input 1dB-compression point	f=740MHz [4]		-8.0		dBm
		f=882MHz [5]		-9.0		
		f=943MHz [6]		-9.0		
IIP3ib	In-band input 3rd-order intercept point	f=740MHz [4]		2.0		dBm
		f=882MHz [5]		2.5		
		f=943MHz [6]		2.0		
ton	turn-on time	time from V <sub>EN</sub> ON to 90% of the gain		1.5		μs
toff	turn-off time	time from V <sub>EN</sub> OFF to 10% of the gain		0.5		μs

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[7] PCB losses are subtracted.

## AW5008L1 APPLICATION BOARD

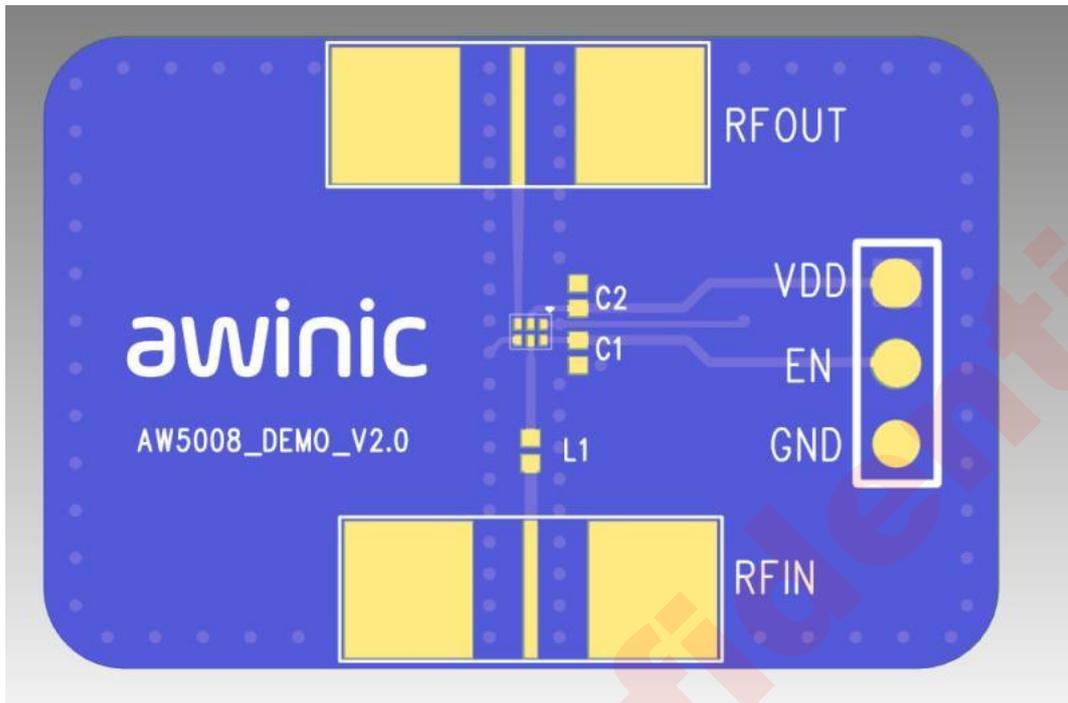


Figure 4 AW5008L1 EVB

## MEASUREMENT DIAGRAM

### Test DC Characteristics(Current & Power Consumption)

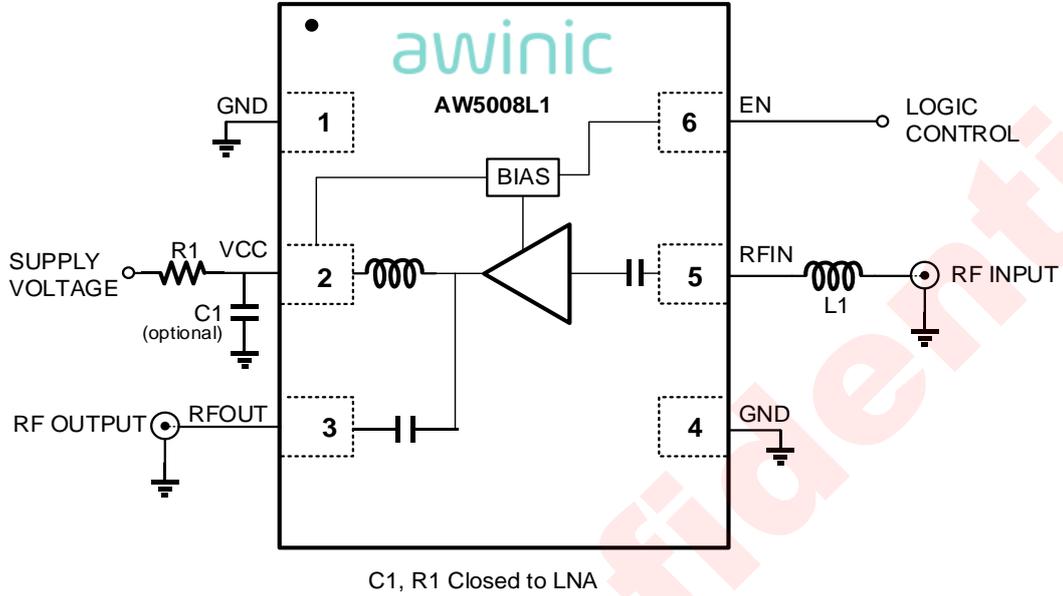


Figure 5 AW5008L1 DC Test Diagram

### Test S-Parameter

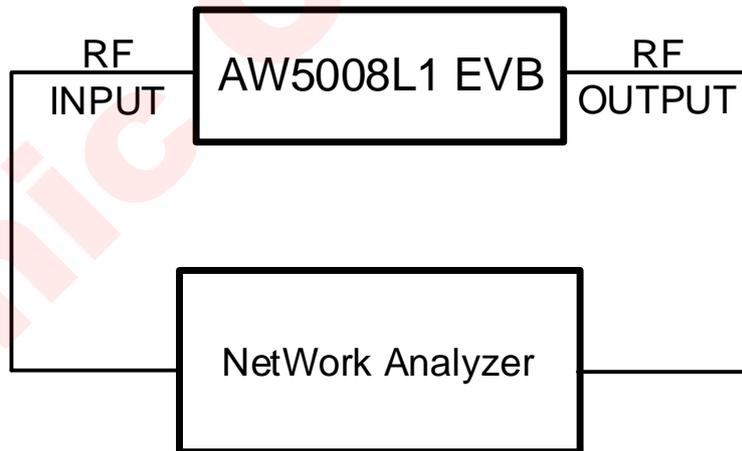


Figure 6 AW5008L1 S-parameter Measurement Diagram

## Test Noise Figure

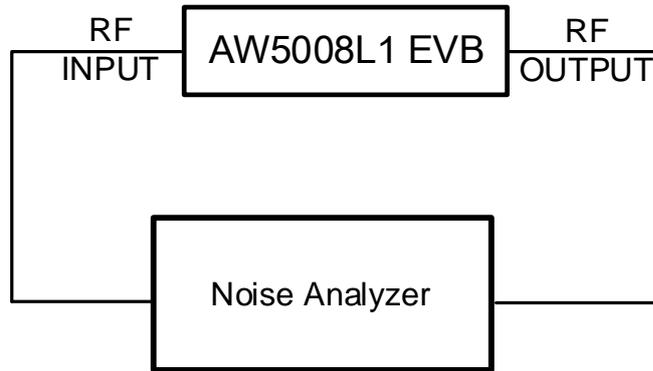


Figure 7 AW5008L1 Noise Figure Measurement Diagram

## Test IIP3

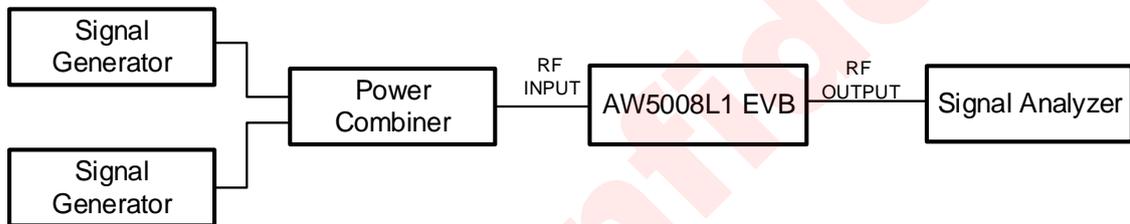


Figure 8 AW5008L1 IIP3 Measurement Diagram

## APPLICATION INFORMATION

### Choice of components

1. The AW5008L1 requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the power supply decoupling capacitor, better performance would be received, like a little higher gain, etc. The value is optimized for the key performance, such as higher power gain, lower noise figure, and better return loss. Typical value of inductor is 18nH with high quality factor, and capacitor is 1nF. The typical application circuit can refer to Figure1.

2. The output of AW5008L1 is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.

3. The AW5008L1 should be placed close to the diversity antenna with the input-matching inductor. Use 50 ohm micro-strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor need be located close to the device. For long  $V_{CC}$  lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

Following tables show recommended inductor and capacitor values.

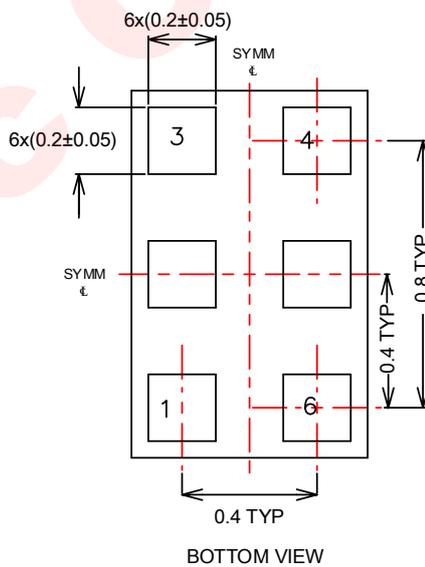
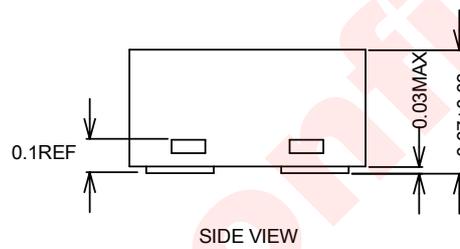
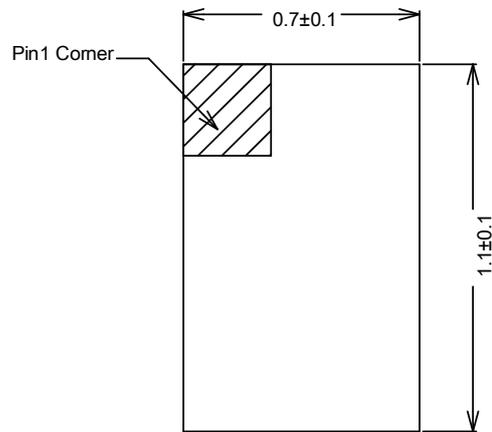
**Inductor Selection Table**

Part	Typical(nH)	Q(min)	Frequency(MHz)	MFR	Size
LQW15A	18	25	250	Murata	0402

**Capacitor Selection Table**

Part	Typical(pF)	Voltage(V)	MFR	Size
GRM155	1000	50	Murata	0402

## PACKAGE DESCRIPTION



Unit : mm

Figure 9 Package Outline

LAND PATTERN

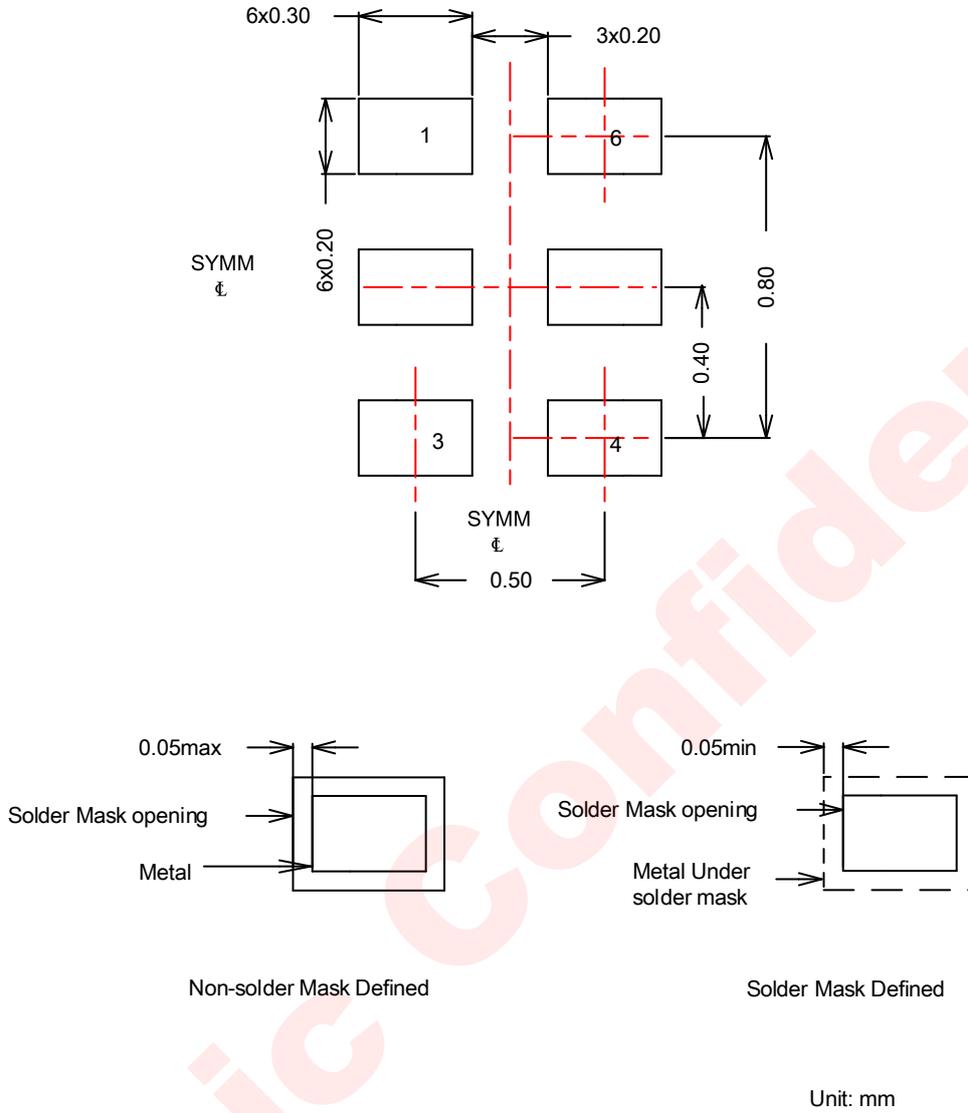
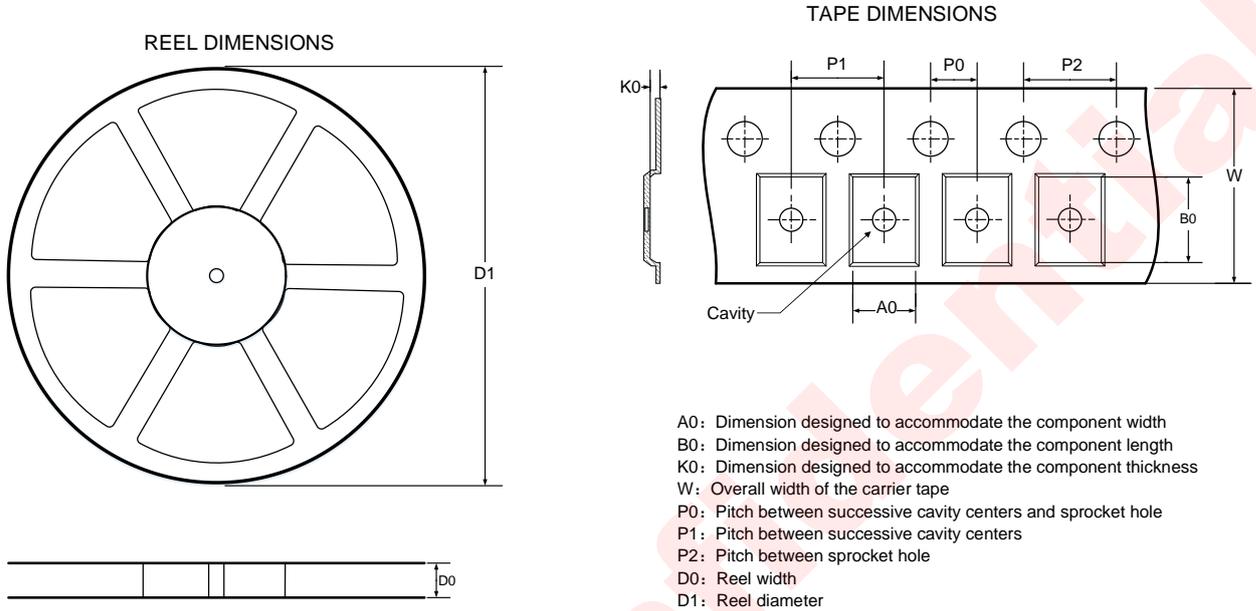
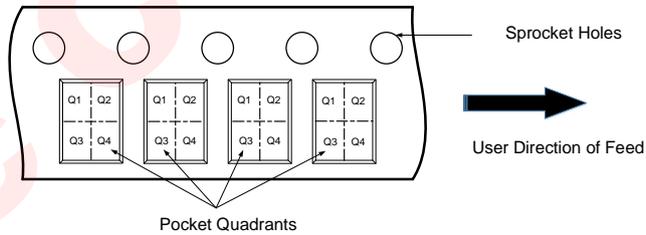


Figure 10 Land Pattern

**TAPE & REEL DESCRIPTION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.8	1.2	0.55	2	2	4	8	Q1

**Figure 11 Tape & Reel Description**

## REVISION HISTORY

Version	Date	Change Record
V1.0	Sept 2018	Officially Released
V1.1	Jan 2019	Update FCDFN

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