Features

- Dual MOSFET Drivers for Synchronous Rectified Bridge
- Adjustable Relative Constant on-time for fast dynamic response
- Programmable VOUT range
- VIN range = 3V~28V
- Support Internal Reference Voltage and External Reference Voltage
- Wide Output Load Range: 0 to 20A+
- 1% reference accuracy over load and line
- Low voltage DC current sense using low-side RDS (ON) Sensing or sense resistor
- Resistor programmable frequency
- Built-in Bootstrap Diode
- Cycle-by-cycle current limit
- 4-Step Current Limit During Soft-start
- Over-voltage/under-voltage fault protection
- Low quiescent power dissipation
- Power good indicator/ Power save option
- Integrated gate drivers with fast transmission scheme
- Over temperature protection(Non-Latch)
- TQFN16-3x3 package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Notebook computers
- CPU core/IO Supplies
- Chip/RAM Supplies

General Description

The GS7210A is small size chip with a relative constant on-time synchronous buck switching controller suitable for applications in notebook computers and other battery operated devices.

The GS7210A has a unique power save mode, which can save battery power supply by decreasing frequency when load current falls down below preset critical current point.

The fast dynamic transient response means that buck converter applications based on GS7210A will provide about 100ns-order response to load when output voltage falls down or rises up. The frequency will increase or decrease to meet the change in output load. Moreover, the GS7210A will take the same method to regulate the output voltage when input voltage changes. When transient response regulated, the controller will maintain a new steady-state operation. Both the transient response state and the new state, the GS7210A always has the same on-time.

The GS7210A supports internal 0.6V reference voltage and external reference from 0.4V to 3.0V for internal error amplifier. When the chip works external reference mode, it can deliver output voltage as low as 0.4V.

An external setting resistor and output voltage can set the on-time, duty-cycle and frequency for the controller. The integrated gate drivers feature adaptive shoot-through protection, fast signal transmission. Additional features include current limit, soft-start, over-voltage and under-voltage protection and a Power Good flag. The GS7210A is available in package TQFN16-3x3.

Typical Application

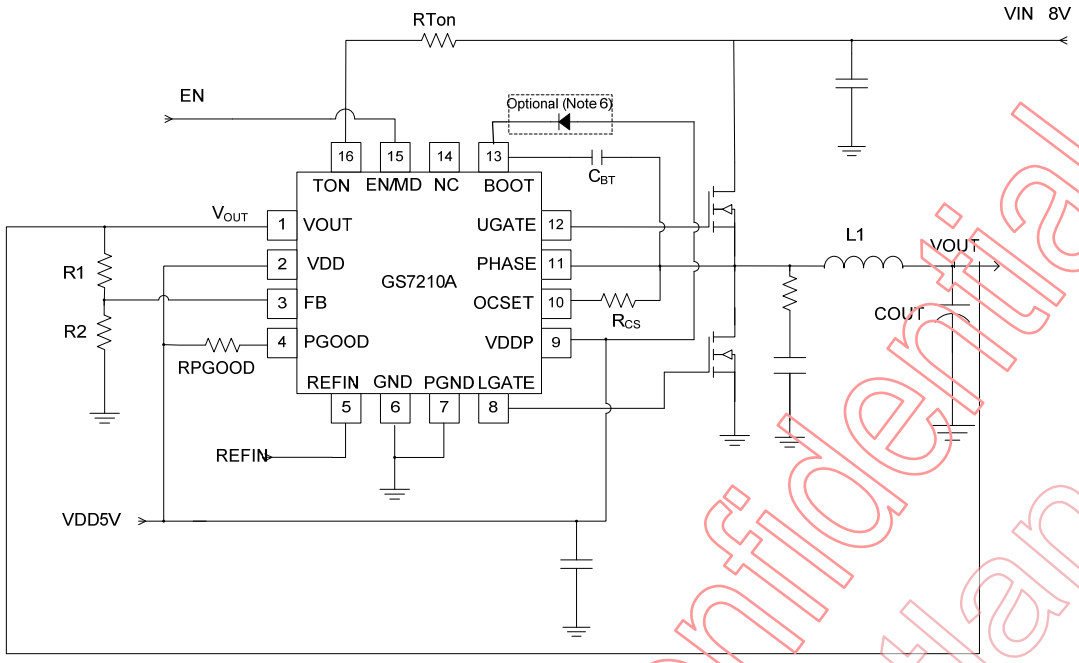


Figure 1a Typical Application of GS7210A: VIN=8V, ILOAD=18A

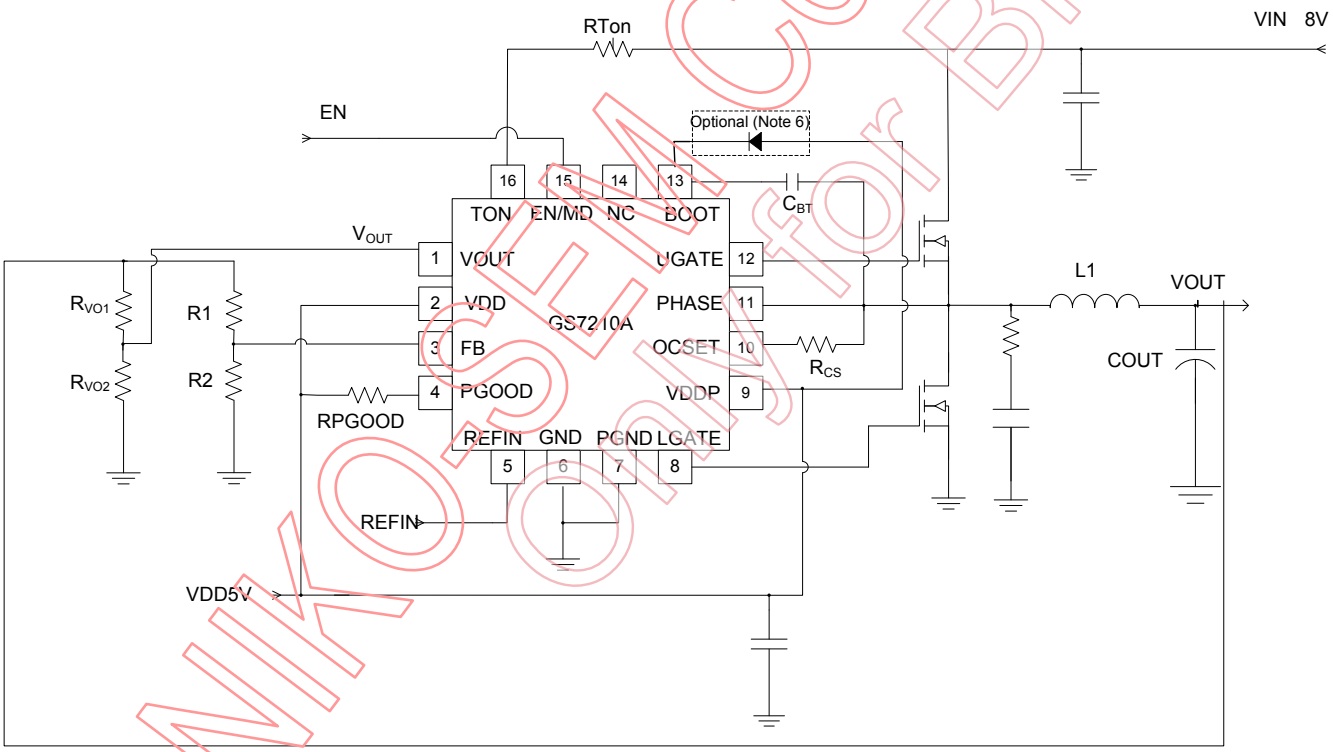


Figure 1b Typical Application of GS7210A: VIN=8V, ILOAD=18A

Function Block Diagram

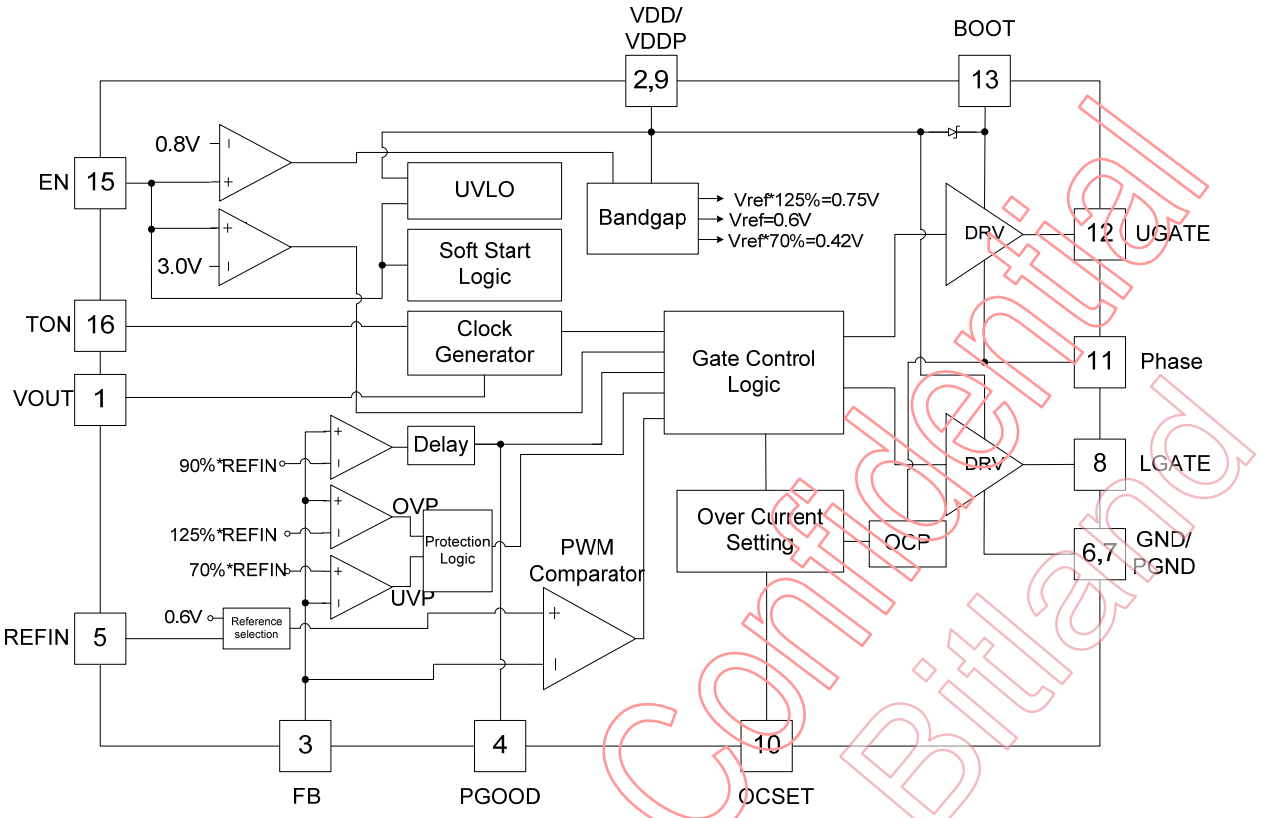


Figure 2 Function Block Diagram

Pin Configuration

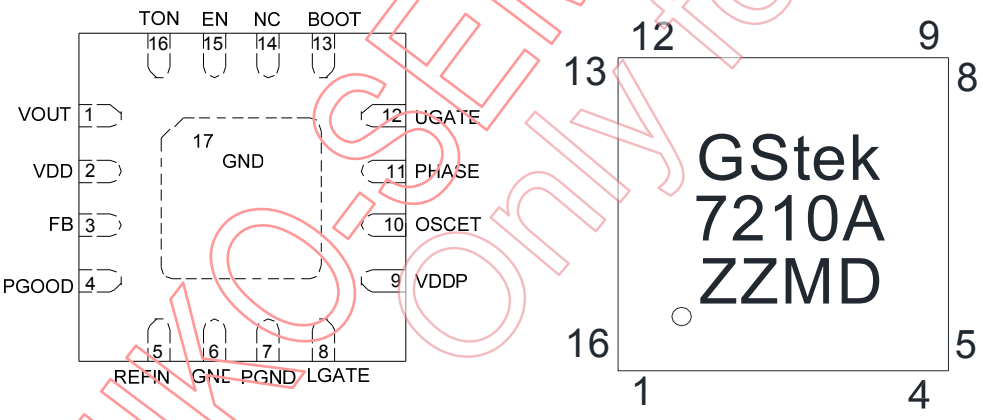


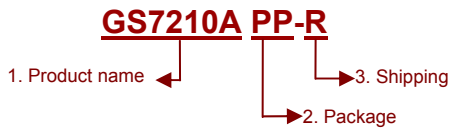
Figure3 TQFN16-3x3Package

(Top view)

Pin Descriptions

No.	Name	I/O type	Pin Function
1	VOUT	I	Buck Output Voltage (0~2.5V) Sense Input. Control the inner TON Time.
2	VDD	I	Power Supply for Analog and Digital circuits of the chip. Use a 1uF Ceramic capacitor to bypass to GND.
3	FB	I	Buck Output Voltage Feedback Input. Used to control output voltage range through a resistor voltage divider.
4	PGOOD	I/O	Buck controller power good indicator. Internal open drain structure. Connect to an external pull-up resistor. This pin will be pulled high when output voltage reaches to the target range.
5	REFIN	I	External Reference Voltage Input. This pin supports the reference voltage from 0.4V to 3.0V as the non-inverting input of the error amplifier. Pulling this pin lower than 0.3V disables the controller. Float this pin for internal 0.6V reference.
6,17	GND	O	Analog and Digital Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	PGND	O	The Power Ground for the driver circuits of the chip
8	LGATE	O	Lower gate drive output for Buck Controller. Connect to gate of low-side power MOS FET.
9	VDDP	I	Power Supply for the driver circuits of the chip. Use a 1uF Ceramic capacitor to bypass to GND.
10	OCSET	I	Current-Limit setting Input Pin for Buck Controller. Connect to PHASE pin though an external resistor to set the current limit threshold.
11	PHASE	I	Upper Driver Floating Ground for Buck Controller. Connect to an external Inductor. It is used to sense current of the inductor.
12	UGATE	O	Upper gate drive output for Buck Controller. Connect to gate of high-side power MOS FET.
13	BOOT	I	UGATE Driver Power Supply for Buck Controller. Bootstrap voltage pin. Use a ceramic capacitor connecting to the external diode with this pin.
14	NC		Useless
15	EN/MD	I	Buck Enable Control Pin. EN=Low, Shutdown; EN=High, PWM work in DEM MODE, EN=Floating or 2V, PWM work in CCM MODE.
16	TON	I	Inner Ton Time Control Pin for Buck Controller, Connect an external pull up resistor to VIN.

Ordering Information



No	Item	Contents
1	Product name	GS7210A
2	Package	TQ: TQFN16-3x3
3	Shipping	R: Tape & Reel

Example: GS7210A TQFN16-3x3 Tape & Reel ordering information is "GS7210A-TQ-R"

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VIN to GND	V_{IN}	-0.3 ~ 30	V
TON to GND	V_{TON}	-0.3 ~ 30	V
OCSET to GND	V_{OC}	-0.3 ~ 40	V
VDD, VDDP to GND	V_{SUPPLY}	-0.3 ~ 6	V
PGOOD, FB, EN, REFIN to GND		-0.3 ~ 6	V
BOOT Voltage	$V_{BOOT-GND}$	-0.3 ~ 45	V
BOOT to PHASE Voltage	$V_{BOOT-PHASE}$	-0.3 ~ 6	V
LGATE to GND	V_{GL}	-0.3 ~ 6	V
PHASE to GND GND - 8V (<400ns, 20μJ) to 40V (<200ns, VBOOT-GND<46V)	V_{PHASE}	-2 ~ 40	V
Package Power Dissipation at $T_A \leqq 25°C$	$P_{D\_TQFN16-3x3}$	1471	mW
Junction Temperature	T_J	- 45 ~ 150	°C
Storage Temperature	T_{STG}	- 55 ~ 150	°C
Lead Temperature (Soldering) 10S	T_{LEAD}	260	°C
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	$\theta_{JA\_TQFN16-3x3}$	68	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VIN to GND (NOTE 7)	V_{IN}	4.5~28	V
VDDP to GND	V_{DDP}	4.5~5.5	V
VDD to GND	V_{DD}	4.5~5.5	V
EN to GND	V_{EN}	$V_{EN}=V_{DD}$	V
Junction Temperature	T_J	- 40 ~ 125	°C
Ambient Temperature	T_A	-40 ~ 85	°C

Electrical Characteristics

(R_{TON}=300KOhms, VDD=VDDP=5V, VIN= 8V, , EN=VDD, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Power Input Voltage	VIN		3	8	28	V
Chip Supply Voltage	VDD		4.5	5	5.5	V
Reference Voltage						
FB Reference Voltage (Trimming)	VFB	VDD= 4.5V ~ 5.5V	0.594	0.6	0.606	V
Output Voltage Accuracy		| VFB –VREFIN | , VREFIN=0.4~1.0V,Tracking Mode			15	mV
		| VFB –VREFIN |/ VREFIN, VREFIN=1.0~3.0V,Tracking Mode			1.5	%
REFIN Enable Threshold	VREFIN			0.3	0.35	V
Enable Logic						
EN Logic Low Voltage	EN_L	EN Falling(2V~0V), LGATE Falling			0.8	V
EN Floating Voltage	EN_F	VDD Power On, Stable State		2		V
EN Logic High Voltage	EN_H	EN Rising(2V~5V), LGATE Falling	3.0			V
Current Parameters						
Quiescent	IQ	FB=0.65V, VDD=5V, EN=5V, PHASE=0.1V, VCS=Floating		640		uA
Shutdown Current	I_{SHTDN}	EN=0, I(VDD+VDDP)		1.43		uA
		EN=0, I(TON)			0.01	uA
		EN=0,I(EN)		-0.35		uA
Ton Operating Current	I_{TON}	RTON=300K,VIN=8V, VFB=0.65V		24		uA
Logic Input Current		EN=5V		1.04		uA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		EN=0V		-0.35		uA
FB Input Bias Current	I_{FB}	FB=0.65V			0.01	uA
System Time & Driver On-Resistance						
On-Time	T_{ON}	V_{IN}=8V,V_{FB}=0.55V, R_{TON}=300K,V_{OUT}=1.1V		350		ns
Minimum On-Time(Note5)	T_{ONMIN}			110		ns
Minimum Off-Time	T_{OFFMIN}	EN=Floating, VIN=8V, RTON=300K, FB=0.55V, PHASE=0		350		ns
Dead Time[3]	T_{DL}	UGATE Falling to LGATE Rising		45		ns
	T_{DH}	LGATE Falling to UGATE Rising		36		ns
UGATE Driver Pull Up	R_{U_UP}	BOOT-PHASE=5V, UGATE=High		1.9		ohms
LGATE Driver Pull Down	R_{L_DN}	BOOT-PHASE=5V, LGATE=Low		0.5		ohms
UGATE Driver Sink	R_{U_SINK}	BOOT-PHASE=5V, UGATE=Low		0.7		ohms
LGATE Driver Pull Up	R_{L_UP}	BOOT-PHASE=5V, LGATE=High		1.0		ohms
Current Sensing (Trimming)						
OCSET Source Current	ICS	VCS=1V		20		uA
IOCSET current temperature coefficient	TCCS	On the bias of 25C		4700		ppm/°C,
Current Limit 1 (Rising)	I_{LIM1}	GND-PHASE, RCS=18K		360		mV
Current Limit 2 (Rising)	I_{LIM2}	GND-PHASE, RCS=10K		200		mV
Current Limit 3 (Rising)	I_{LIM3}	GND-PHASE, RCS=2.5K		50		mV
Zero Crossing Threshold	V_{T_0}	GND-PHASE	-10		10	mV
Current Comparator Offset	V_{OS_VCL}	GND-CS	-10		10	mV
Voltage Fault Protection						
VDD UVLO Threshold 1	UVLO_W	Wake Up		4.22		V
VDD UVLO Threshold 2	UVLO_S	Shutdown		4.0		V
UV Threshold	UV_TH	PGOOD Falling Edge, PWM Disable		70		%
UV Blank Time (Note5)	T_UV	From EN Rising to PGOOD Rising		512CLKs		ms
UV Fault Delay (Note5)	UV_DELAY			256CLKS		ms
OVP Threshold	OV_TH	PGOOD Rising, LGATE Rising		125		%
OVP Delay	T_OV	PGOOD Falling to LGATE Rising		26		us

PGOOD Flag						
PGOOD Trip Threshold	PG_TH	PGOOD Falling, Measured at FB		90		%
PGOOD Fault Propagation Delay	T_PG_F	From FB Falling to PGOOD Falling		4.8		us
Leakage Current	I_{LEAK}	PGOOD=5V(To be Measured)			0.01	uA
PGOOD Low Voltage	VOLV	PGOOD ISINK=1mA			0.4	V
Out Voltage Discharge Resistance						
VOUT Shutdown Discharge Resistance	R_{DISC}	IOUT=10mA		12		ohms
Boost Diode Forward Voltage						
Internal Boost Charging Switch On_Resistance	R_{BT_D}	VDDP to BOOT, 10mA			100	ohms
Over Temperature Shutdown						
Thermal Shutdown start threshold	T_{TSDN}			150		°C
Thermal Shutdown Hysteresis	T_{HYS_TSDN}			20		°C

Note 1 Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2 Devices are ESD sensitive. Handling precaution recommended.

Note 3 θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4 The device is not guaranteed to function outside its operating conditions.

Note 5 Such specifics are guaranteed by circuit design.

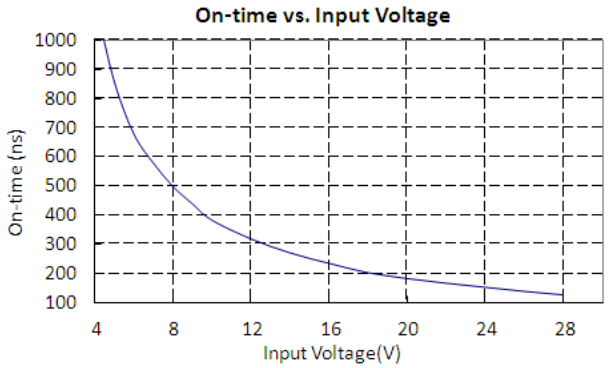
Note 6 If V(BOOT)-V(PHASE)<3.5V, a boot diode is recommended.

Note 7 Recommend the Pulse time<100ns when VIN over than 28V.

Typical Characteristics (To be continued)

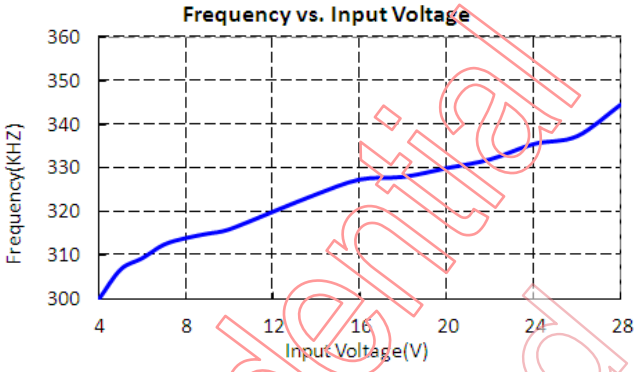
1. On-time vs. Input Voltage

(RTON=390K,ILOAD=15A,VOUT=1.1V)



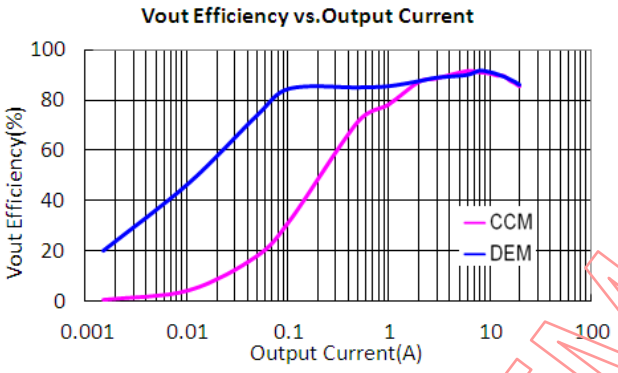
2. Frequency vs. Input Voltage

(RTON=390K,ILOAD=15A,VOUT=1.1V)



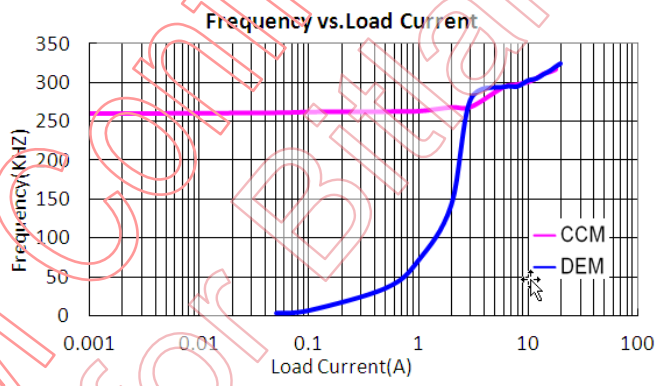
3. VOUT Efficiency vs. Load Current

(RTON=390K,VIN=8V,VOUT=1.1V)



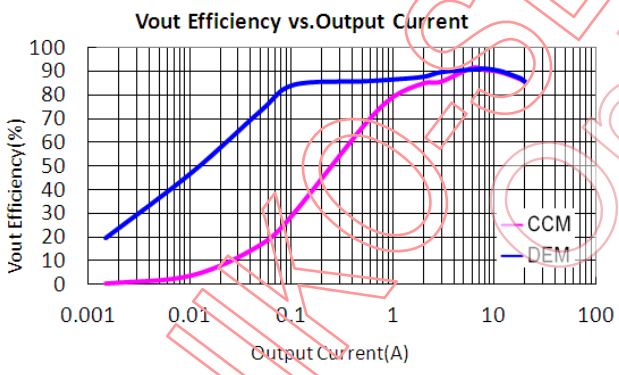
4. Frequency vs. Load Current

(RTON=390K,VIN=8V,VOUT=1.1V)



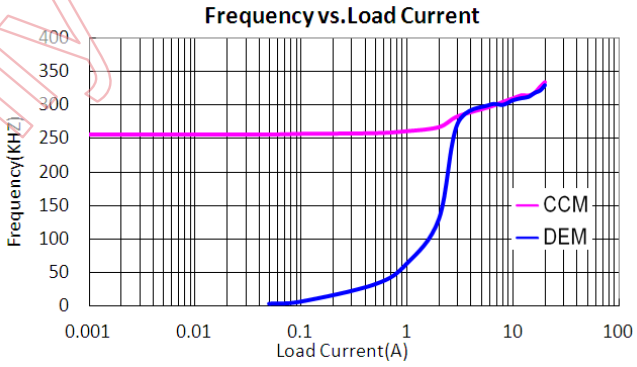
5. VOUT Efficiency vs. Load Current

(RTON=390K,VIN=12V,VOUT=1.1V)



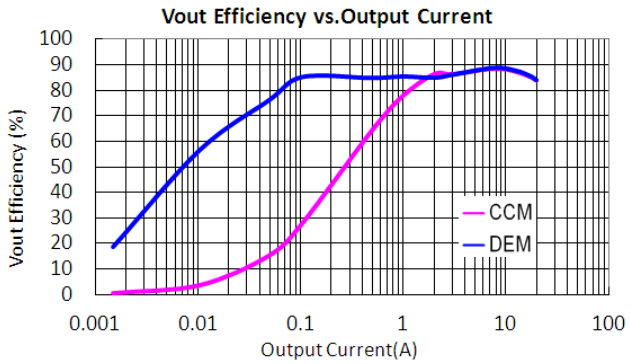
6. Frequency vs. Load Current

(RTON=390K,VIN=12V,VOUT=1.1V)



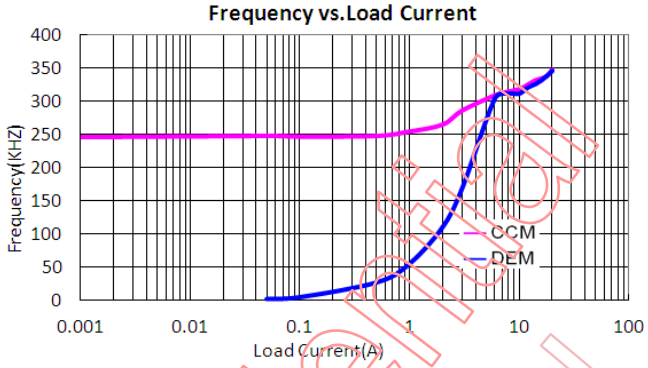
7. VOUT Efficiency vs. Load Current

(RTON=390K,VIN=20V,VOUT=1.1V)



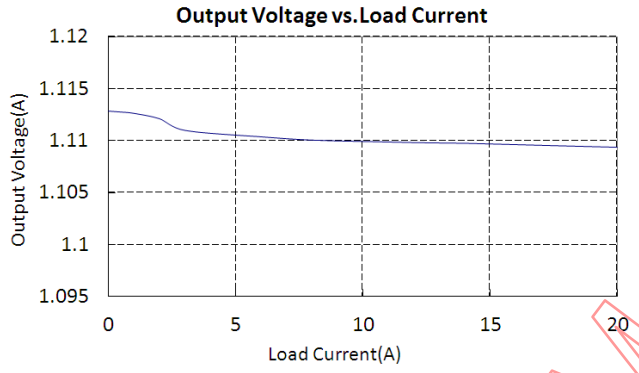
8. Frequency vs. Load Current

(RTON=390K,VIN=20V,VOUT=1.1V)



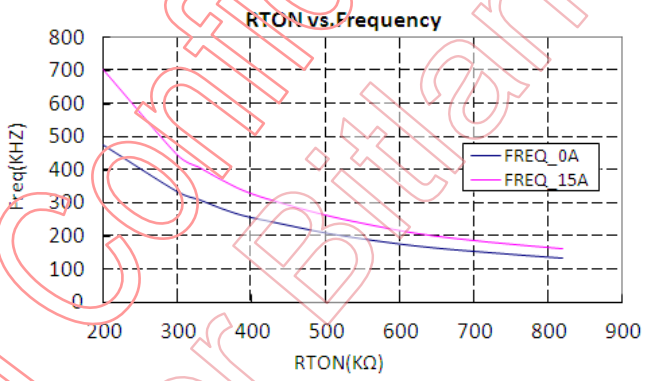
9. Output Voltage vs. Load Current

(RTON=390K,VIN=12V,VOUT=1.1V)



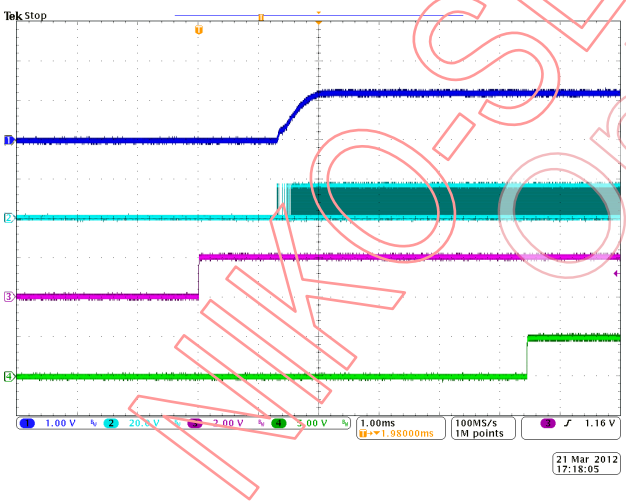
10. On-time vs. Input Voltage

(VIN=12 ,VOUT=1.1V)



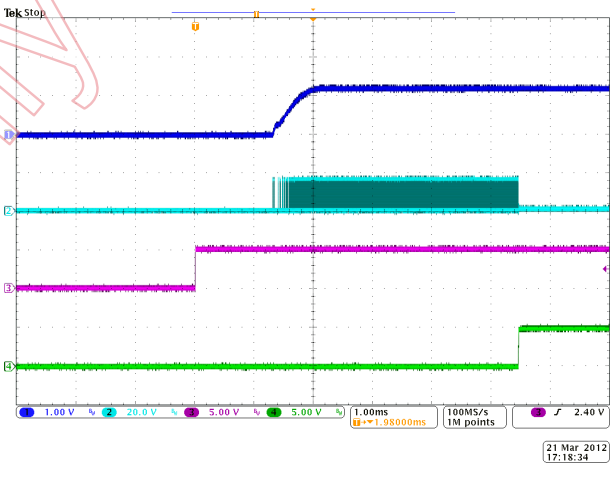
11. Power on from EN (CCM Mode, No Load)

CH1:VOUT CH2:PHASE CH3:EN CH4:PGOOD



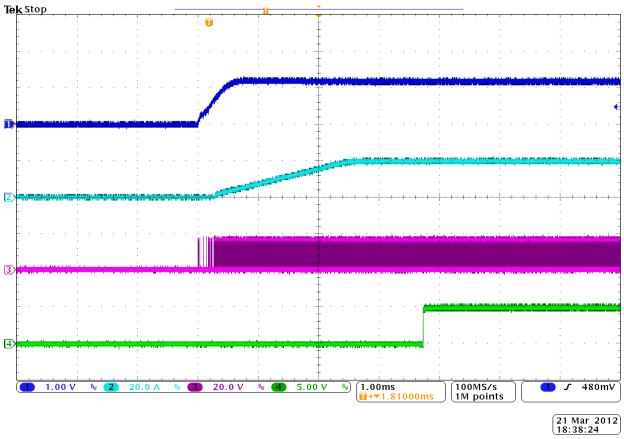
12. Power on from EN (DEM Mode, No Load)

CH1:VOUT CH2:PHASE CH3:EN CH4:PGOOD



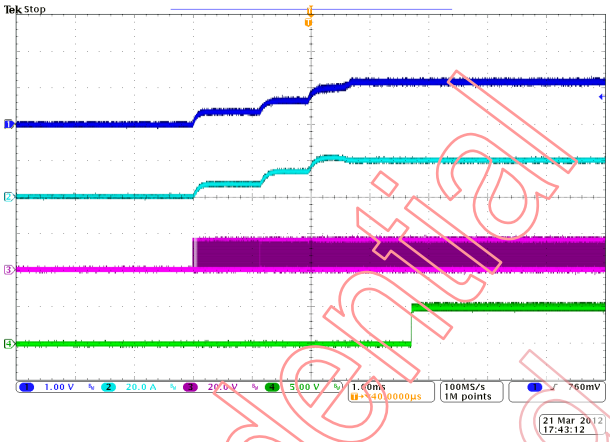
13. Power on from EN (20A Load)

CH1:VOUT CH2:IOUT CH3:UGATE CH4:PGOOD



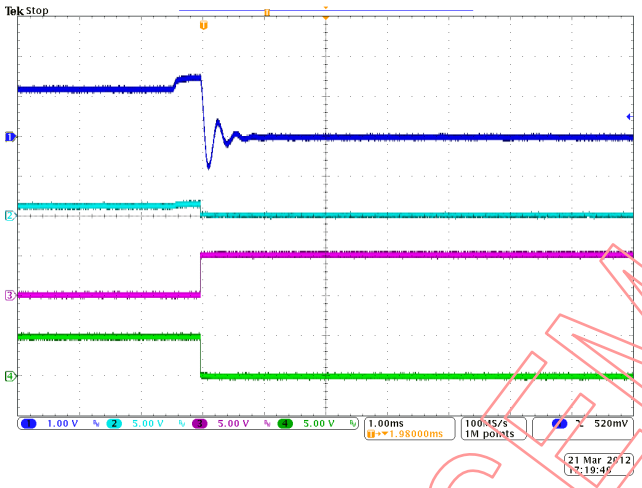
14. Power on from EN (50mohm Load)

CH1:VOUT CH2:IOUT CH3:UGATE CH4:PGOOD



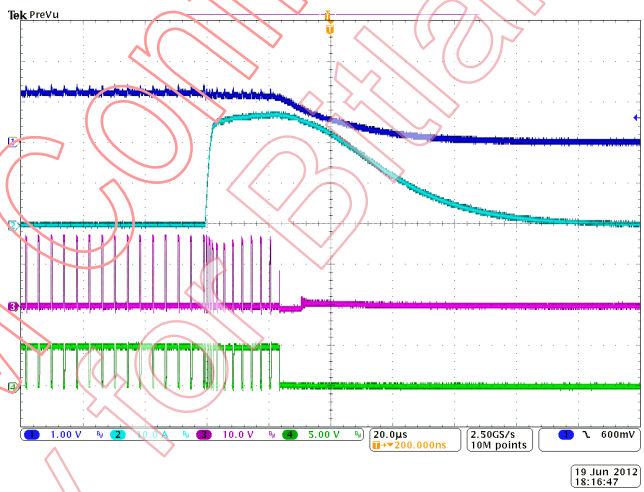
15. OVP

CH1:VOUT CH2:UGATE CH3:LGATE CH4:PGOOD



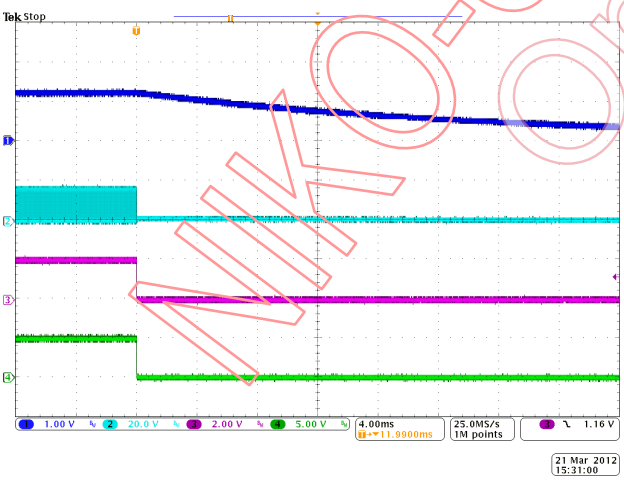
16. Output Short After Power On

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



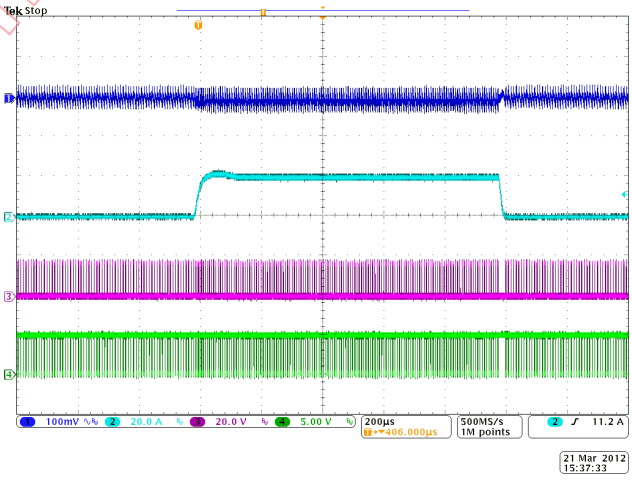
17. Power Off From EN

CH1:VOUT CH2:PHASE CH3:EN CH4:PGOOD



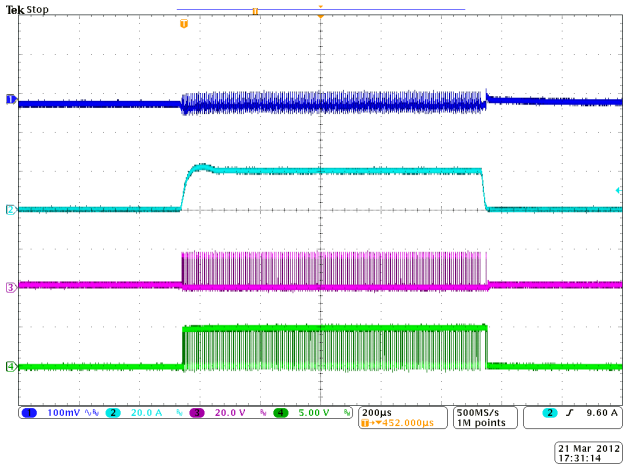
18. Load Transient CCM Mode

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



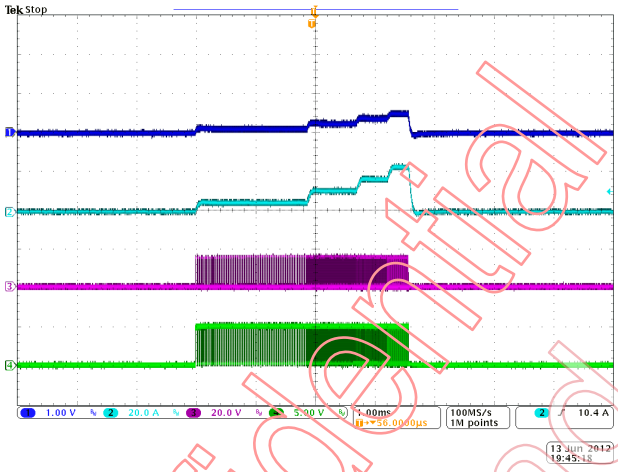
19. Load Transient DEM Mode

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



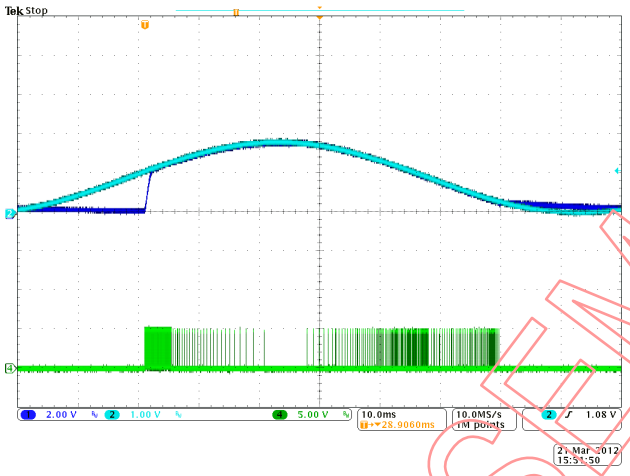
20. Power ON in Short Condition

CH1:VOUT CH2:IOUT CH3:UGATE CH4:LGATE



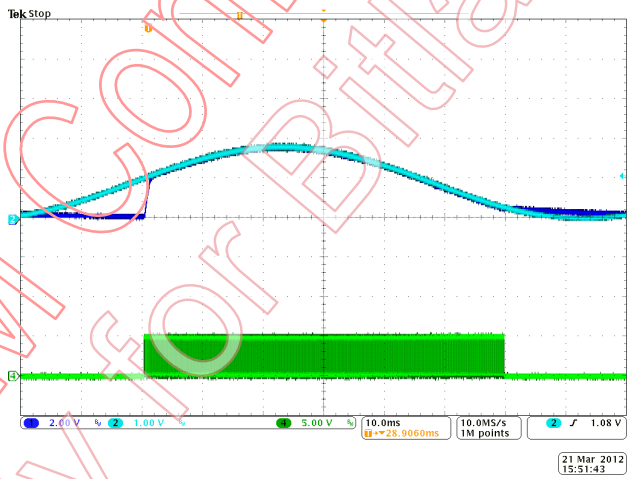
21. Vout changes with REFIN in DEM Mode

CH1:VOUT CH2:REFIN CH4:LGATE



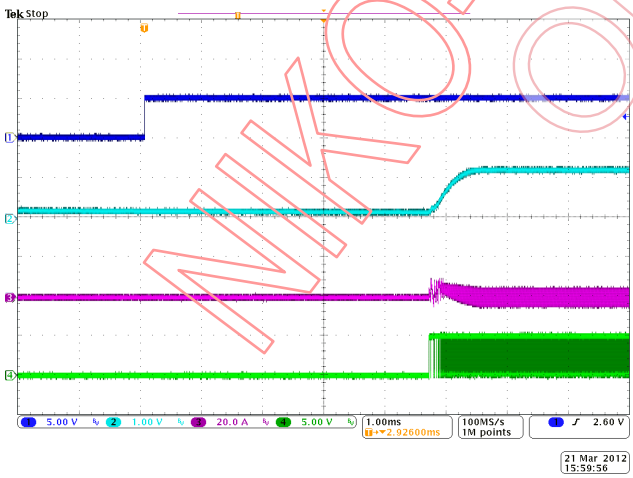
22. Vout changes with REFIN in CCM mode

CH1:VOUT CH2:REFIN CH4:LGATE



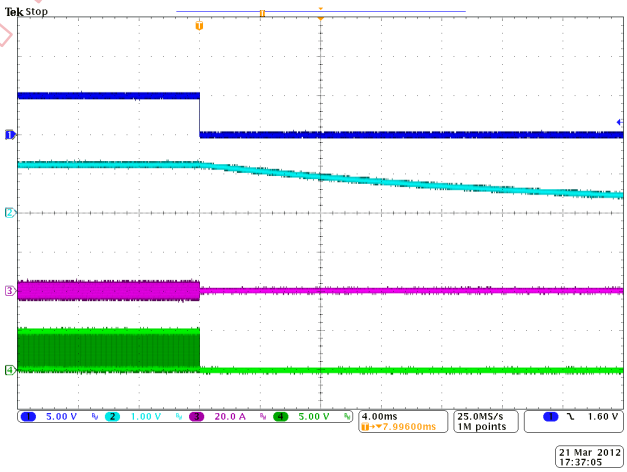
22.Power on from REFIN

CH1:REFIN CH2:VOUT CH3:IL CH4:LGATE



23.Shut down from REFIN

CH1:REFIN CH2:VOUT CH3:IL CH4:LGATE



Application Information

The GS7210A is small size chip with a relative constant on-time synchronous buck switching controller suitable for applications in notebook computers and other battery operated portable devices. Features include very wide input voltage range, high efficiency and a fast dynamic response with internal fast response scheme.

System Clock Generator and PWM Control

The on-time of GS7210A can be set by an external setting resistor from external Battery input voltage to TON pin and a sampled output voltage. The controller maintains the duty-circle as loop feedback path exists between the GS7210A controller, external power MOSFET, low pass filter and voltage divider. For a given VIN to given VOUT buck application, the feedback maintains the constant duty-cycle. Due to the constant resistor, battery voltage and relative constant sampled output voltage, the GS7210A based buck converter has the relative constant frequency. Moreover, the GS7210A can increase the duty-cycle automatically as battery voltage falls down. Because of the constant on-time in each switching period, the controller maintains the relative frequency when the battery input voltage changes.

At the beginning of each switching cycle, upper power MOSFET is turned on, after typical fixed on-time, the upper MOSFET is turned off, and then lower power MOSFET is turned on after internal dead time. The upper MOSFET will not be turned on at the beginning of next cycle until output voltage falls down below the preset voltage and the dead time passes. The same events repeat the following switching cycles. To avoid the surge inductor current during large load transient, a minimum Off-time is added. Typical minimum off-time is around 350ns.

The on-time which is too small can affect soft-start and anti-noise ability. In order to avoid the on-time is too small to be eliminated; a minimum on-time around 110ns is designed in the circuit. This should to be noted in the small duty applications.

High Side Switch On-Time Count

The on-time is decided by the external setting resistor, battery input voltage and output voltage. Looking at the TON pin, the battery input voltage is converted to current which is inversely proportional to itself by dividing the external setting resistor. Simultaneously, the sample and hold module inside the chip samples the output voltage at each switching cycle. The input voltage-proportional current is used to charge an internal capacitor from zero volts. When the voltage between two terminals of the capacitor reaches to the sampled output voltage, on-time one-shot pulse is generated, and then upper power MOSFET is turned off and lower power MOSFET is turned on.

We can count the on-time and switching frequency according to the equations below:

$T_{ON}=8.22p\times R_{TON}\times V_{OUT}/ (V_{IN}-0.8)$

Here, the V_{OUT} is the sampled output voltage of VOUT .For output voltalge VOUT<2.5V, the VOUT Voltage connects to V_{OUT} PIN directly(refers to Figure 1a), the V_{OUT} = VOUT. For output voltalge VOUT >2.5V, the output voltage for the buck system connects to V_{OUT} PIN through the dividing resistors R_{VO1} and R_{VO2}(refers to Figure 1b), the typical VOUT is set to 2.5V, choose the R_{VO1} and R_{VO2} as follows: $V_{OUT}=VOUT*R_{VO2}/(R_{VO1}+R_{VO2})$.

Then, the switching frequency is:

$F_{sw}=V_{OUT}/ (V_{IN}\times T_{ON})$

RTON is a resistor connected from the input supply (VIN) to the TON pin.

For heavy load (more than 20A) application, due to ground bounced and the high impedance of $R_{TON,}$ the TON pin should always be bypassed to GND using a several nF-order ceramic capacitor for reliable system operation.

EN/DEM, DEM Mode

The EN/DEM pin enables the power supply. When EN/DEM is tied to VDD the GS7210A controller is enabled and diode-emulated mode (DEM) which is power save mode will be also enabled. When the EN/DEM is floating or tri-stated, an internal tri-stated judged logic module will activate the controller and the DEM Mode will be disabled which means the chip works in CCM Mode. The result of Mode selection will be latched during the 1ms delay after chip enabling.

At light loads, GS7210A starts power save mode in order to maintain the on-time and decrease the system clock frequency to skip PWM pulses for better efficiency. If DEM Mode is enabled, the GS7210A zero crossing comparator will sense the inductor current and judge its value by comparing the phase node (PHASE) to PGND. Once the phase node voltage is equal to the PGND node voltage, the controller will enter the DEM Mode and turn off the low side power MOSFET. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than required the next switching cycle. The on-time is kept the same as that in the heavy-load condition.

If the EN/DEM pin is pulled low, the GS7210A internal logic will shutdown the switching clock and stop the buck controller, the related output will be discharged using a built-in switch resistor with a nominal resistance of 12ohms. This will ensure that the output is in a defined state next time when it is enabled. Since this is a soft discharge, that there are no dangerous negative voltage excursions to be concerned about. In order to maintain the correct function of the soft-discharge module, the chip power supply must be online.

To Select External Reference Voltage

Connect REFIN to a voltage source range from 0.4V to 3.0V. As the REFIN voltage rises above 0.3V threshold level, the Enable Comparator initiates the operation of the GS7210A. The REFIN voltage is compared with 3.0V voltage to select the reference voltage with 1ms time delay after chip enabling. The external reference input is selected as the REFIN voltage is lower than 3.0V. The internal 50uA current source is turn off to eliminate the load effect on the reference input. The soft-start cycle is initiated after reference selection is completed.

Note that the 50uA current source will induces load effect on the external reference input and causes the REFIN voltage slightly higher than the external reference input during the reference selection. Make sure that the external reference input is strong enough so that REFIN voltage will not higher than 3.0V.

DEM to CCM changing mechanism

When using REFIN pin as external reference voltage, DEM to CCM changing mechanism will enable if REFIN falls down to avoid over voltage protection happens. This mechanism keeps the deference between REFIN voltage and output voltage within a small range in DEM MODE when REFIN voltage becomes low. This mechanism will disable in CCM mode or internal reference voltage mode.

Output Voltage Selection

The output voltage is set by the feedback resistors R1 and R2 of Figure1 above. The internal reference is 0.6V, so the voltage at the feedback pin is also 0.6V. Therefore the output can be set by the equation

below:

VOUT= (1+R1/R2) ×0.6V

Over Current Protection

The GS7210A uses the on-state resistance of the low-side power MOSFET as a current-sense resistor. In this case, the R_{CS} resistor between the PHASE pin and OCSET pin sets the over current threshold. This resistor R_{CS} is connected to a 20uA current source within the GS7210A which is turned on when the low side power MOSFET turns on. When the voltage drops across the low side power MOSFET equals the voltage crossing the current limit resistor R_{CS}, positive current limit will activate. If this occurs for 8 times continuously, both the upper side Power MOSFET and the lower side Power MOSFET will turn off and the chip will shut down until EN pin or REFIN pin resets again. The current sensing circuit actually regulates the inductor valley current. This means that if the magnitude of the current-sense signal at OCSET pin is above the current-limit threshold, the PWM is not allowed to initiate a new switching cycle. The equation for the current limit threshold is as follows:

$I_{LLIMIT}=20uA\times R_{CS}/R_{DSON}$

While

$I_{Load\_OCP}=20uA\times R_{CS}/R_{DSON}+(VIN-VOUT)*VOUT/(2\times L\times f\times VIN)$

I_{Load_OCP} is the current load of VOUT while OCP occurs. R_{DSON} is the resistance of lower side Power MOSFET. Ensure that noise and DC errors do not corrupt the current-sense signal seen by OCSET and PGND. Mount the IC close the lower side Power MOSFET and sense resistor with short, direct traces.

Power Good Indicator

When the output voltage is 25% above or 10% below its preset value, PGOOD gets pulled low. There is a 4.8us delay built into the PGOOD module to prevent false operations. It is held low until the output voltage returns to above 93% below OVP trigger point. PGOOD flag is also held low during soft-start .It will be pulled high immediately when soft-start is over and the output reaches 93% of its preset value. The Power Good indicator is open-drain architecture and requires an external pull-up resistor connected to PGOOD pin for system applications.

Output Over Voltage Protection

When the output voltage rises up to 125% of the preset voltage, the internal fault-logic module delays about 26us and turns on the low side Power MOSFET. It stays latched on and the GS7210A is latched off until Power Reset or EN Reset or REFIN pin Reset.

Output Under Voltage Protection

When the output voltage falls down to 70% of the preset voltage, the internal fault-logic module counts 256-CLKS and turns off both the high side and low side Power MOSFETs. Both switches stay latched off and the GS7210A is latched off until Power Reset or EN Reset or REFIN pin Reset. During soft-start, the UVP will be blanked around 512CLKS. But if the output voltage rises up above the UVP threshold tolerance during the counter period, the UVP counter is released immediately.

UVLO and Soft-Start

An internal under voltage lockout (UVLO) module is used to sense the VDD power supply. The PWM controller is locked by the under voltage

lockout module until VDD rises above 4.22V. The GS7210A will initial the control logic circuitries and soft-start ramping generator after UVLO unlocks the chip. When VDD falls down to 4.0V, the PWM controller is locked again. At this time, both upper side MOSFET and lower side MOSFET will turn off.

After soft-start module starting, the GS7210A controller will limit the output current by 4-step current limiting logic cycle by cycle over a predetermined time period of 512CLKS. After UV blanking time (512CLKS), the output under voltage protection and power good indicator is enabled.

Power MOSFET Gate Drivers

The GS7210A has UGATE and LGATE drivers built-in, which can drive two large external N-type MOSFET used as high side and low side. External Boost diode and capacitor are need to power the internal floating drive module, A dead-time circuit is added to monitor the UGATE output and to prevent the high-side MOSFET from turning on until LGATE is fully off. The internal pull-down transistor that drives LGATE low is robust with a 0.5ohm typical on-resistance. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND. The dead-time circuit also monitors the LGATE output and prevents the low-side MOSFET from turning on until UGATE is fully off. The typical dead time from UGATE-falling to LGATE-rising is about 45ns.The typical dead time from LGATE-falling to UGATE-rising is about 36ns.

External Devices Selection

For loop stability, the 0 dB frequency (f0), defined in the follow equation:

$$f_0 = \frac{1}{2\pi \times RESR \times C_{OUT}} \le \frac{f_{SW}}{4}$$

The loop stability is determined by the output capacitor. Specialty polymer capacitors have C_{OUT} in the order of several 100uF and RESR in range of 10mohm is recommended. However, ceramic capacitors have f0 at more than 700 KHz, which is not recommended.

In order for the right regulate manner, the ripple voltage at the feedback pin (FB), should be approximately 15mV. This generates Vripple= (VOUT/0.6) ×15mV at the output node. The output capacitor RESR should meet this equation.

The external device selection is list below:

Choose Feedback Voltage Divider Resistor

Set R_1=1K~10K ohm

$$R_2 = \frac{0.6}{(V_{OUT} - 0.6)} \times R_1$$

For output voltage VOUT> 2.5V, Set VOUT PIN's voltage V_{OUT}=2.5V.

Choose R_{VO2}=1K~10K ohm

$$R_{VO1} = \frac{(V_{OUT} - 2.5)}{2.5} \times R_{VO2}$$

Choose RTON

$$T_{ON(Max)} = \frac{1}{f_{SW}} \times \frac{V_{OUT}}{V_{IN(Min)}}$$

$R_{ON\ (Max)}$ =T_{ON}× ($V_{IN\ (Min)}$-0.8)/ (8.22P×V_{OUT})

Choose Inductor

Set the ripple current approximately 1/4 to 1/2 of the maximum output current. 1/3 is recommended.

$$L_{IND} = \frac{1}{I_{IND(ripple)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}}$$

$$L_{IND} = \frac{3}{I_{IOUT(max)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}}$$

For applications that require fast transient response with minimum VOUT overshoot, consider a smaller inductance than above. The cost of a small

inductance value is higher steady state ripple, larger line regulation, and higher switching loss.

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimate as follows.

$$L_{IND(peak)} = \frac{1}{L \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} + \frac{V_{OC}}{R_{DS(on)}}$$

Choose Output Capacitors

$$RESR = \frac{1}{I_{ripple}} \times \frac{V_{OUT}}{0.6} \times 0.015$$

$$\approx \frac{3}{I_{OUT(max)}} \times \frac{V_{OUT}}{0.6} \times 0.015$$

$$RESR \approx \frac{V_{OUT}}{I_{OUT(max)}} \times 75(mohm)$$

Organic semiconductor capacitors or specialty polymer capacitors are recommended.

Choose Power MOSFETs

According to the GS7210A's current limit principle and its specification, the low side $R_{DS(ON)}$ times the inductor current value at the over-current point should be equal to 20uA*R_{CS}. Assuming a 20% guard band, $R_{DS\ (ON)}$ should satisfy the following equation during the full temperature range.

$$R_{DS(ON)} \le \frac{20uA \times R_{CS}}{1.2 \times I_{OUT(max)} - 0.5 \times I_{ripple}}$$

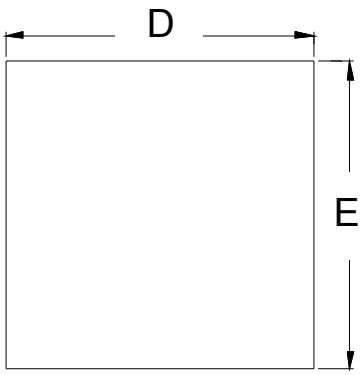
For higher efficiency application, low side power MOSFET with low $R_{DS\ (ON)}$ should be selected.

For heavy load application, two low side power MOSFETs are recommended.

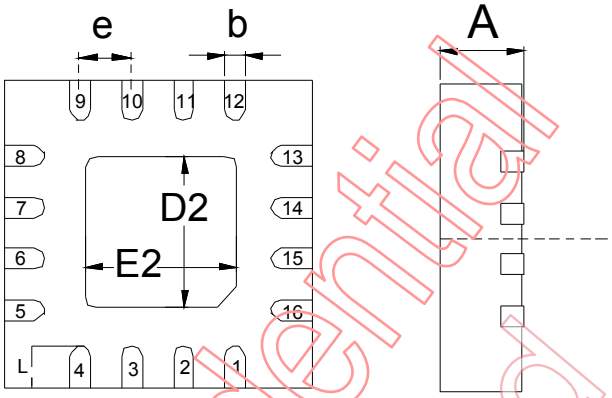
Choose RCS

Use the same equation above at “Choose Power MOSFETs”.

Package Dimensions, TQFN16-3x3



(Top view)



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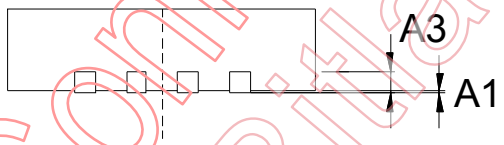

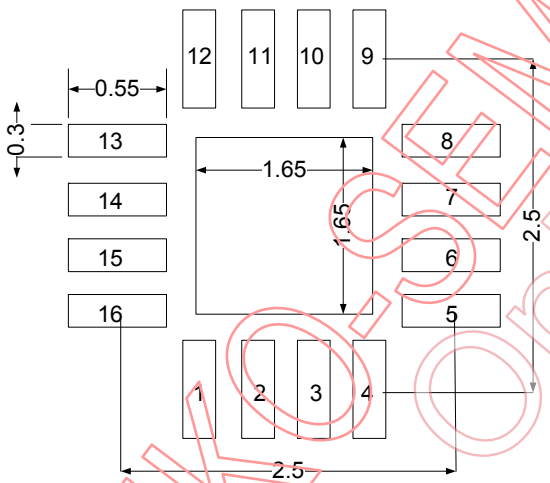

Unit: mm

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.70	0.90
A1	0.00	0.05
A3	0.20 REF.	
b	0.18	0.30
D	2.90	3.10
D2	1.65 REF.	
E	2.90	3.10
E2	1.65 REF.	
e	0.50 REF.	
L	0.30	0.50

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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