

# TLS202A1

Adjustable Linear Voltage Post Regulator

TLS202A1MBV

## Data Sheet

Rev. 1.0, 2015-06-22

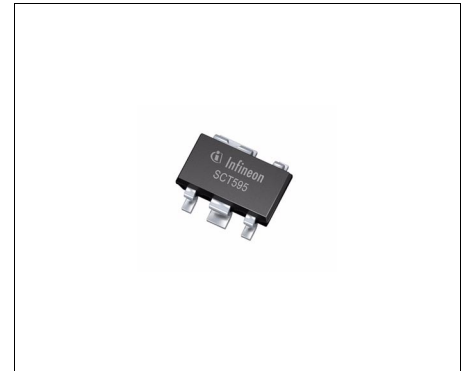
Automotive Power



## 1 Overview

### Features

- Adjustable Output Voltage from 1.2 V to 5.25 V
- Output Voltage Accuracy of  $\pm 3\%$
- Output Currents up to 150 mA
- Extended Input Voltage Operating Range of 2.7 V to 18 V
- Low Dropout Voltage: typ. 290mV
- Very Low Current Consumption: typ. 50  $\mu$ A
- Very High PSRR: typ. 65dB at 10kHz
- Output Current Limitation
- Short Circuit protected
- Overtemperature Shutdown
- Wide Temperature Range From  $-40\text{ }^{\circ}\text{C}$  up to  $150\text{ }^{\circ}\text{C}$
- Suitable for Use in Automotive Electronics as Post Regulator
- Green Product (RoHS compliant)
- AEC Qualified



**PG-SCT595**

### Functional Description

The TLS202A1 is a monolithic integrated adjustable linear voltage post regulator for load currents up to 150 mA. The IC regulates an input voltage  $V_I$  in the range of  $2.7\text{ V} \leq V_I \leq 18\text{ V}$  to an adjustable output voltage of 1.2 V to 5.25 V with a precision of  $\pm 3\%$ . The TLS202A1 is especially designed for applications requiring very low standby currents, e.g. with a permanent connection to preregulators like DCDC converters. The regulator is not designed to operate with a direct connection to the battery. The device is available in a very small surface mounted PG-SCT595 package. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLS202A1 can be also used in all other applications requiring a stabilized voltage of 1.2 V to 5.25 V.

### Choosing External Components

The input capacitor  $C_I$  is recommended for compensating line influences. The output capacitor  $C_Q$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values specified in **“Functional Range” on Page 6** within the whole operating temperature range.

Type	Package	Marking
TLS202A1MBV	PG-SCT595	20

## 2 Block Diagram

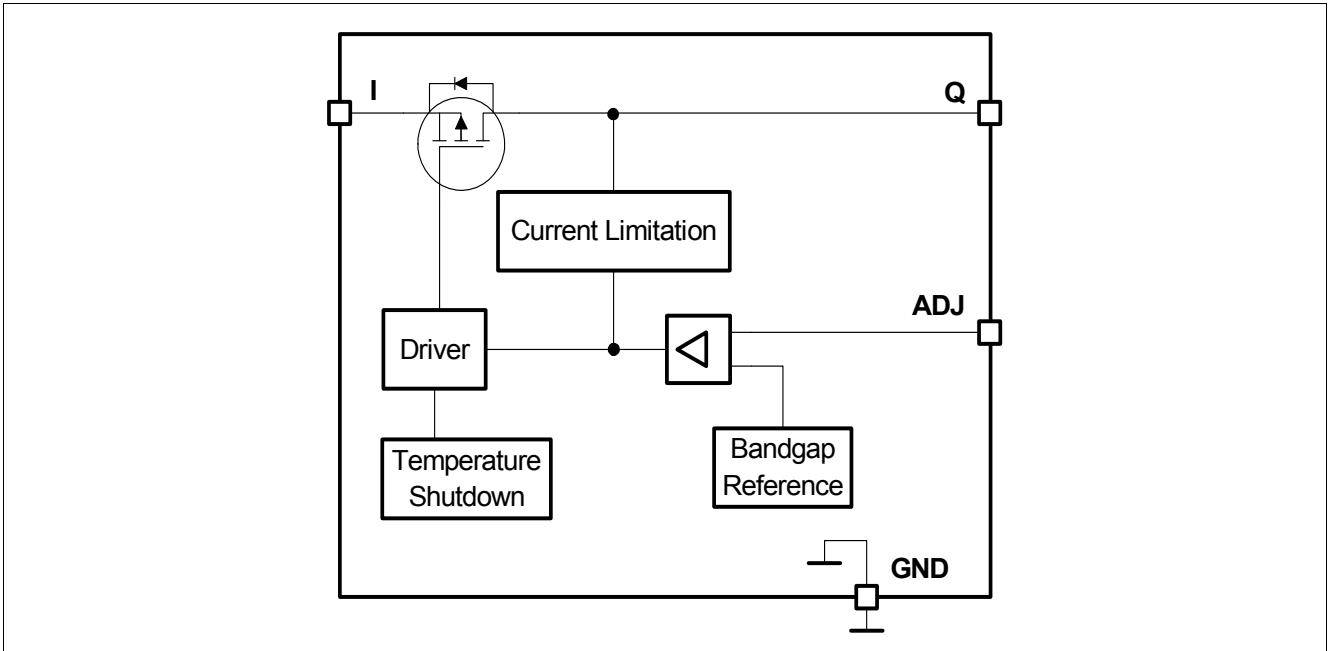


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment PG-SCT595

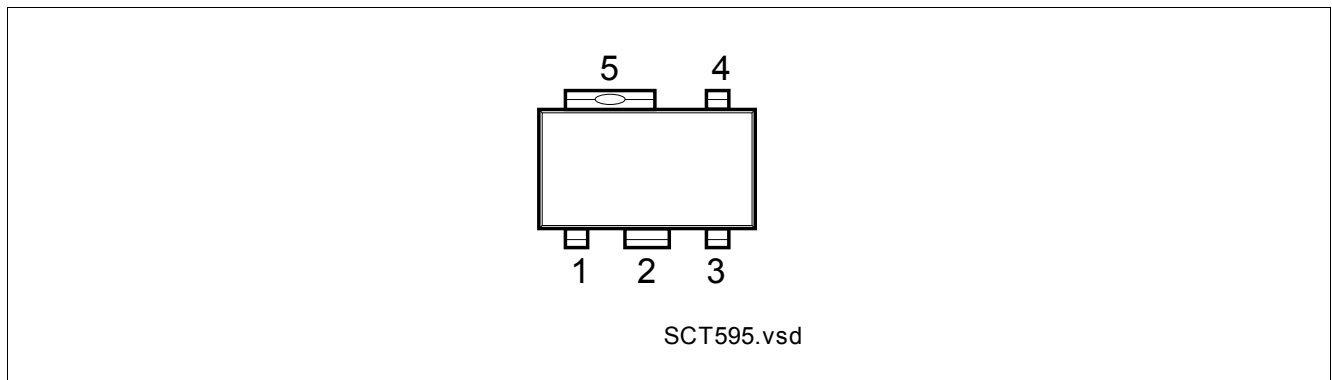


Figure 2 Pin Configuration Package PG-SCT595-5

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	I	<b>Input.</b> <b>IC supply.</b> For compensation line influences, a capacitor of 220nF close to the IC pins recommended.
2	GND	<b>Ground Reference.</b> Internally connected to Pin 5. Connect to heatsink area. For thermal reasons both ground Pins 2 and 5 have to be soldered.
3	Q	<b>Output.</b> Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the <b>“Functional Range” on Page 6</b> .
4	ADJ	<b>Adjust.</b> The reference voltage can be connected directly to the output Q or by a voltage divider for higher output voltages (see <b>“Application Information” on Page 15</b> ).
5	GND	<b>Ground Reference.</b> Internally connected to Pin 2. Connect to heatsink area. For thermal reasons both ground Pins 2 and 5 have to be soldered.

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings** <sup>1)</sup>  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Input I</b>							
Voltage	$V_I$	-0.3	–	20	V	–	P_4.1.1
<b>Output Q</b>							
Voltage	$V_Q$	-0.3	–	5.5	V	–	P_4.1.2
<b>Adjust ADJ</b>							
Voltage	$V_{ADJ}$	-0.3	–	5.5	V	–	P_4.1.3
<b>Temperature</b>							
Junction temperature	$T_j$	-40	–	150	°C	–	P_4.1.4
Storage temperature	$T_{stg}$	-50	–	150	°C	–	P_4.1.5
<b>ESD Susceptibility</b>							
ESD Absorption	$V_{ESD,HBM}$	-4	–	4	kV	Human Body Model (HBM) <sup>2)</sup>	P_4.1.6
ESD Absorption	$V_{ESD,CDM}$	-750	–	750	V	Charge Device Model (CDM) <sup>3)</sup> at all pins	P_4.1.7

1) not subject to production test, specified by design

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 2 Functional Range**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	$V_I$	2.7	–	18	V	–	P_4.2.1
Output Capacitor Requirements for Stability	$C_Q$	1	–	–	$\mu\text{F}$	<sup>1)</sup>	P_4.2.2
Output Capacitor Requirements for Stability	$ESR(C_Q)$	–	–	10	$\Omega$	<sup>2)</sup>	P_4.2.3
Junction temperature	$T_j$	-40	–	150	$^{\circ}\text{C}$	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at  $f = 10$  kHz

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 3 Thermal Resistance**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Ambient	$R_{thJA}$	–	81	–	K/W	2s2p board <sup>1)</sup>	P_4.3.1
Junction to Ambient	$R_{thJA}$	–	217	–	K/W	Footprint only <sup>2)</sup>	P_4.3.2
Junction to Ambient	$R_{thJA}$	–	117	–	K/W	300 mm <sup>2</sup> PCB heatsink area <sup>2)</sup>	P_4.3.3
Junction to Ambient	$R_{thJA}$	–	103	–	K/W	600 mm <sup>2</sup> PCB heatsink area <sup>2)</sup>	P_4.3.4
Junction to Soldering Point	$R_{thJSP}$	–	30	–	K/W	Pins 2, 5 fixed to $T_A$	P_4.3.5

1) Specified  $R_{thJA}$  value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu\text{m}$  Cu, 2 x 35 $\mu\text{m}$  Cu). Where applicable a thermal via array next to the package contacted to the first inner copper layer.

2) Package mounted on PCB FR4; 80 x 80 x 1.5 mm; 35  $\mu\text{m}$  Cu, 5  $\mu\text{m}$  Sn; horizontal position; zero airflow. Not subject to production test; specified by design.

## 5 Voltage Regulator

### 5.1 Description Voltage Regulator

The output voltage  $V_Q$  is controlled as follows: It is divided by the external resistor divider and this fraction is distributed to the ADJ Pin. The Voltage at the ADJ is then compared to an internal reference and drives the pass transistor accordingly.

By connecting the ADJ pin directly to the output Q the device will regulate to its reference voltage. In this case a minimum load resistance of less than 1 M $\Omega$  needs to be ensured for stability reasons.

The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the circuit design. To ensure stable operation, the requirements for output capacitance and equivalent series resistance ESR, given in “**Functional Range**” on Page 6, have to be maintained. For details see also the typical stability graph of ESR versus load current on Page 12. As the output capacitor also has to buffer load steps it should be sized according to the needs of the application.

An input capacitor  $C_I$  of at least 220 nF is recommended to compensate line influences. Connect the capacitors close to the terminals of the component.

In case the load current is above the specified limit, e.g. in case of a short circuit, the output current limitation limits the current. The output voltage is therefore decreasing at the same time.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC’s lifetime.

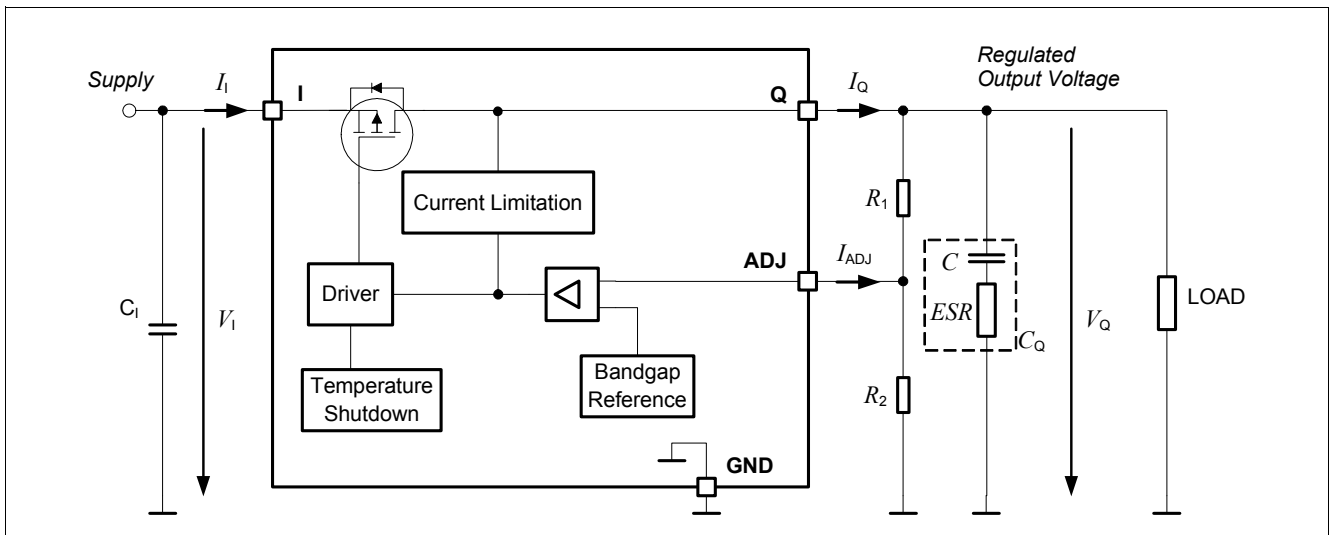


Figure 3 Block Diagram Voltage Regulator Circuit

## 5.2 Electrical Characteristics Voltage Regulator

**Table 4** Electrical Characteristics  $V_I = V_Q + 1\text{ V}$  and  $V_I \geq 2.7\text{ V}$ ;  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground (unless otherwise specified)

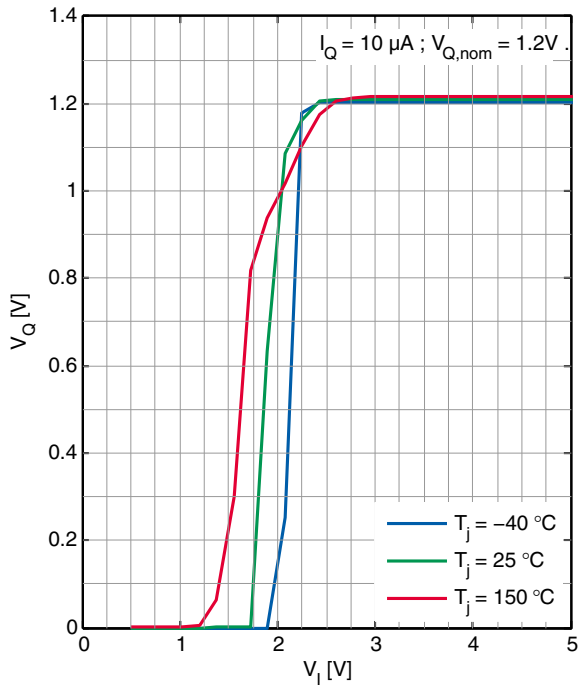
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reference Voltage	$V_{ref}$	–	1.2	–	V	–	P_5.2.1
Output Voltage <sup>1)</sup>	$V_Q$	-3%	$V_Q$	+3%	V	$I_Q = 10\text{ mA}$ ; $T_j = 25\text{ °C}$	P_5.2.2
Output Voltage <sup>1)</sup>	$V_Q$	-4%	$V_Q$	+4%	V	$I_Q = 10\text{ mA}$	P_5.2.3
Adjustable Voltage Range <sup>2)</sup>	$V_Q$	1.2	–	5.25	V		P_5.2.4
Adjust Pin Pull Up Current <sup>3)</sup>	$I_{ADJ}$	–	–	1	$\mu\text{A}$	$V_{ADJ} = V_{ref} = 1.2\text{ V}$	P_5.2.5
Dropout Voltage <sup>4)</sup>	$V_{dr}$	–	290	570	mV	$V_Q \geq 3.3\text{ V}$ ; $I_Q = 150\text{ mA}$ ;	P_5.2.6
Dropout Voltage <sup>4)</sup>	$V_{dr}$	–	350	670	mV	$V_Q \geq 2.7\text{ V}$ ; $I_Q = 150\text{ mA}$ ;	P_5.2.7
Dropout Voltage <sup>4)</sup>	$V_{dr}$		0.57	1	V	$V_Q \geq 1.8\text{ V}$ ; $I_Q = 150\text{ mA}$ ;	P_5.2.8
Load Regulation	$\Delta V_Q/V_Q$	-25	-8	–	mV/V	$I_Q = 1\text{ mA}$ to $150\text{ mA}$	P_5.2.9
Line Regulation	$(\Delta V_Q/V_Q) / \Delta V_I$	–	0.01	0.2	%/V	$V_I = (V_Q + 1\text{ V})$ to $10\text{ V}$ ; $V_I \geq 2.7\text{ V}$ ; $I_Q = 1\text{ mA}$	P_5.2.10
Output Current Limitation	$I_Q$	151	300	–	mA	$0\text{ V} \leq V_Q \leq 0.9 * V_{Q,nom}$ ; $V_I = V_Q + 2.5\text{ V}$	P_5.2.11
Power Supply Ripple Rejection <sup>2)</sup>	PSRR	–	65	–	dB	$f_f = 10\text{ kHz}$ ; $I_Q = 50\text{ mA}$ ; $T_j = 25\text{ °C}$ ; $V_{in} = V_Q + 1\text{ V}$ ; and $V_{in} \geq 3.2\text{ V}$ ; $\Delta V_I = 1\text{ V}_{pp}$ ; $C_{out} = 1\text{ }\mu\text{F}$ (Ceramic Capacitor)	P_5.2.12
Overtemperature Shutdown Threshold <sup>2)</sup>	$T_{j,sd}$	151	170	190	$^{\circ}\text{C}$	–	P_5.2.13

- 1) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation. Parameter is tested with ADJ-Pin directly connected to the output Q.
- 2) Parameter is not subject to production test, specified by design.
- 3) ADJ pin pull up current flows out of the ADJ pin.
- 4) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at  $V_{in} = V_{Q,nom} + 1\text{ V}$ ,  $I_{Load} = 150\text{ mA}$ .

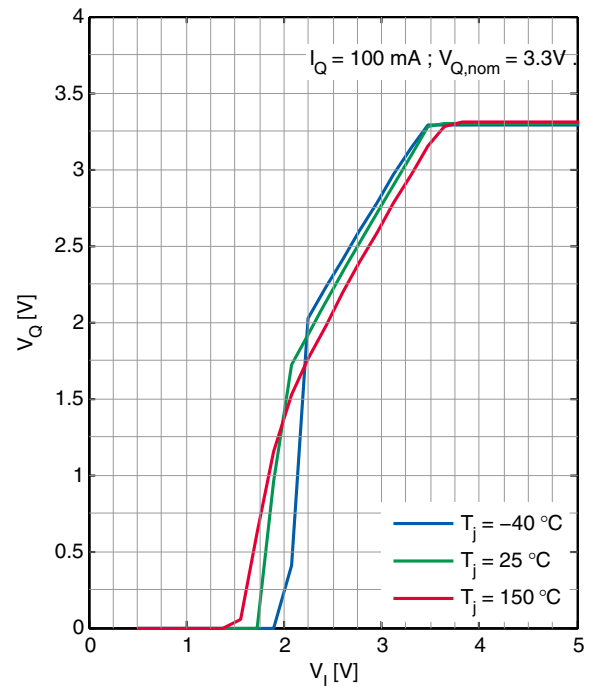


### 5.3 Typical Performance Characteristics Voltage Regulator

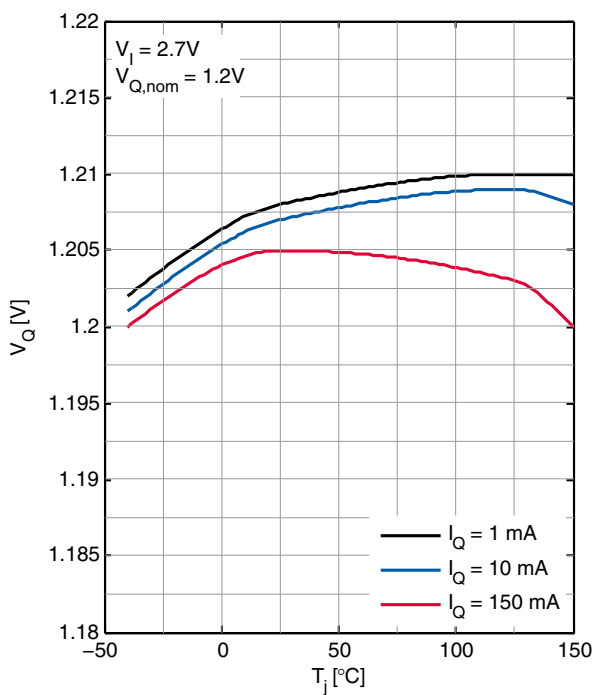
Output Voltage  $V_Q$  vs. Input Voltage  $V_I$  ( $V_{Q,nom} = 1.2\text{ V}$ )



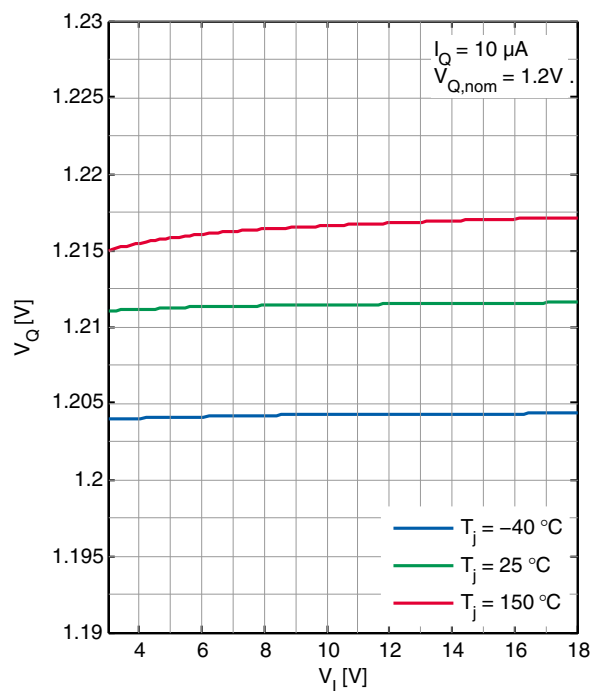
Output Voltage  $V_Q$  vs. Input Voltage  $V_I$  ( $V_{Q,nom} = 3.3\text{ V}$ )



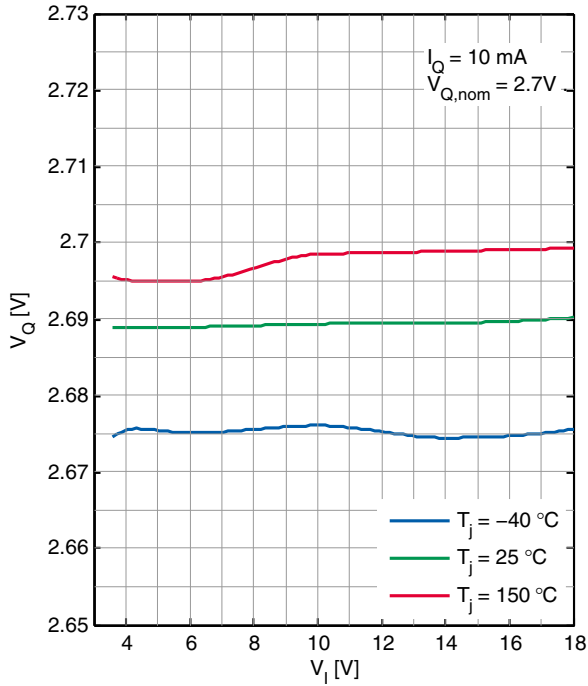
Output Voltage  $V_Q$  vs. Junction Temperature  $T_j$  ( $V_{Q,nom} = 1.2\text{ V}$ )



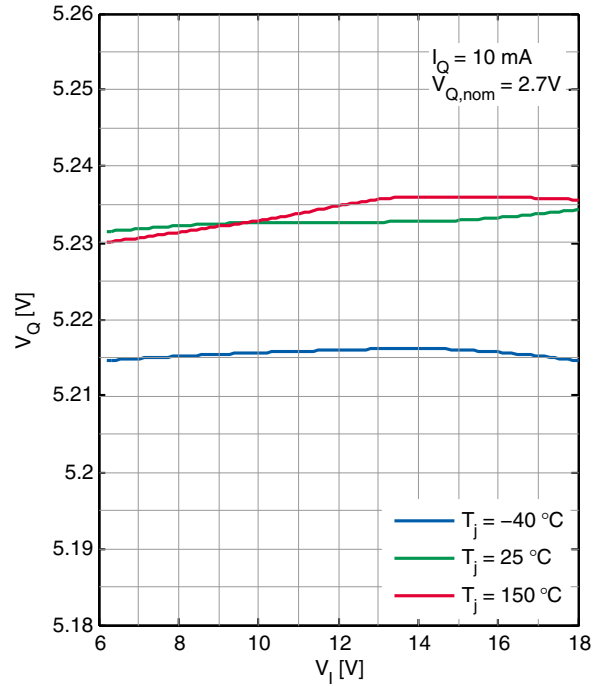
Line Regulation: Output Voltage  $V_Q$  vs. Input voltage  $V_I$  ( $V_{Q,nom} = 1.2\text{ V}$ )



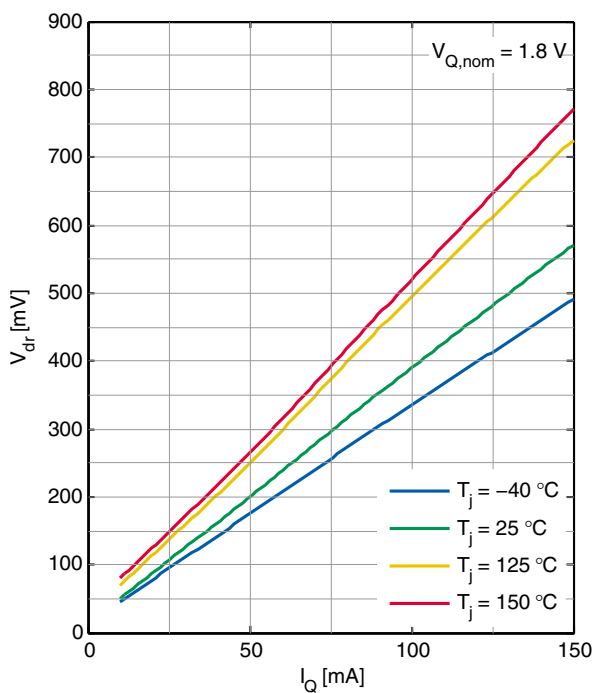
**Line Regulation: Output Voltage  $V_Q$  vs. Input voltage  $V_I$  ( $V_{Q,nom} = 2.7\text{ V}$ )**



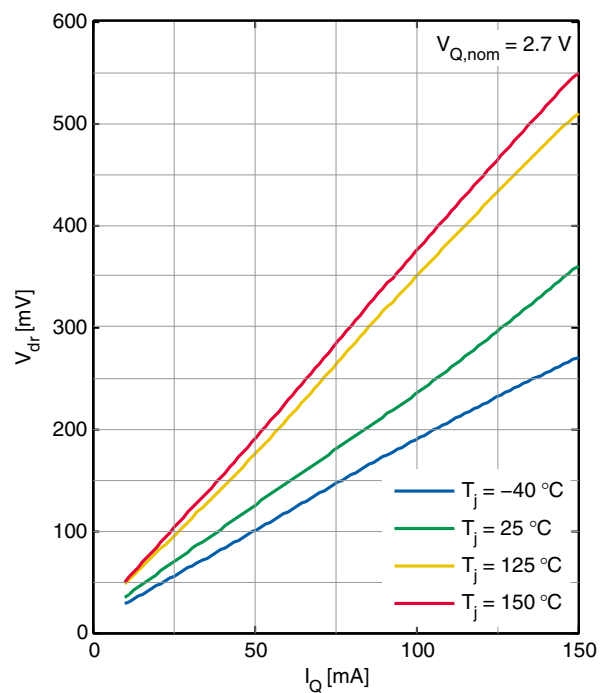
**Line Regulation: Output Voltage  $V_Q$  vs. Input voltage  $V_I$  ( $V_{Q,nom} = 5.2\text{ V}$ )**



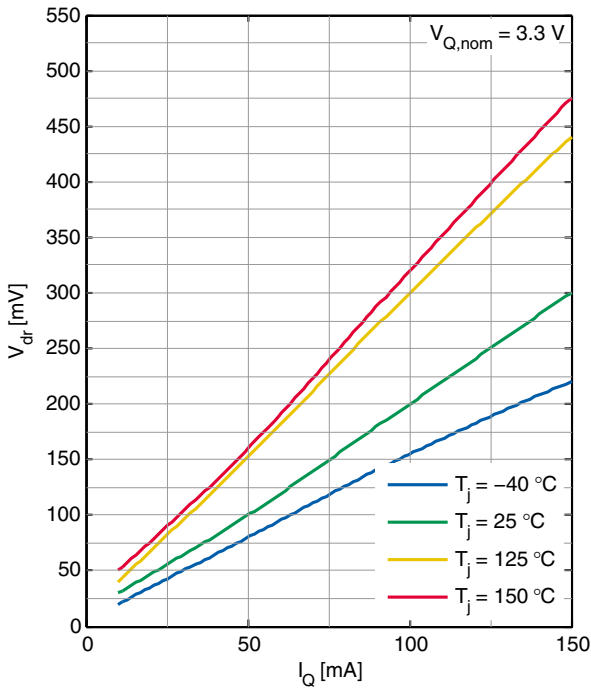
**Dropout Voltage  $V_{dr}$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 1.8\text{ V}$ )**



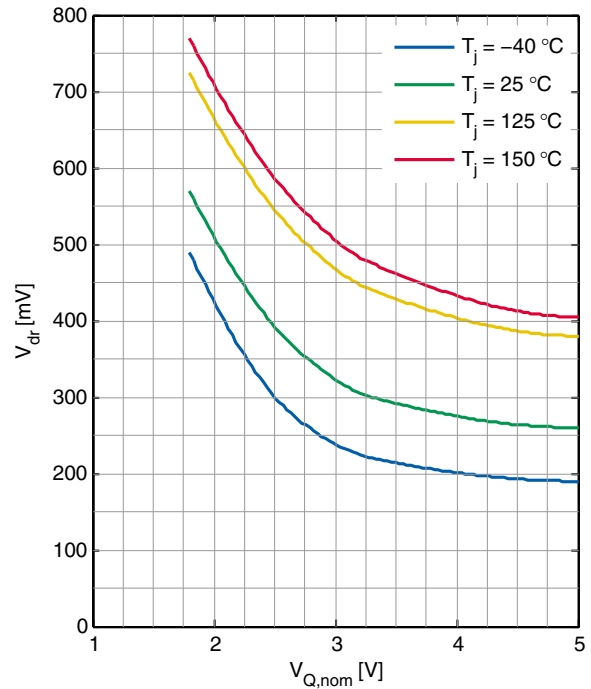
**Dropout Voltage  $V_{dr}$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 2.7\text{ V}$ )**



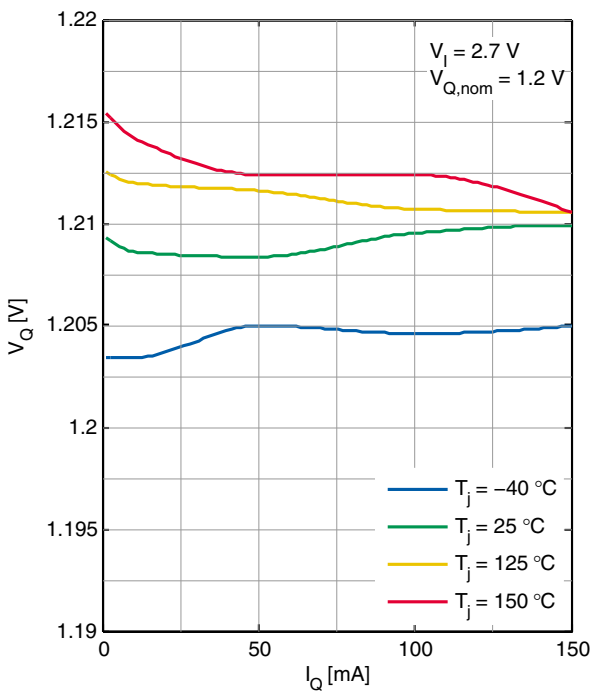
**Dropout Voltage  $V_{dr}$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 3.3\text{ V}$ )**



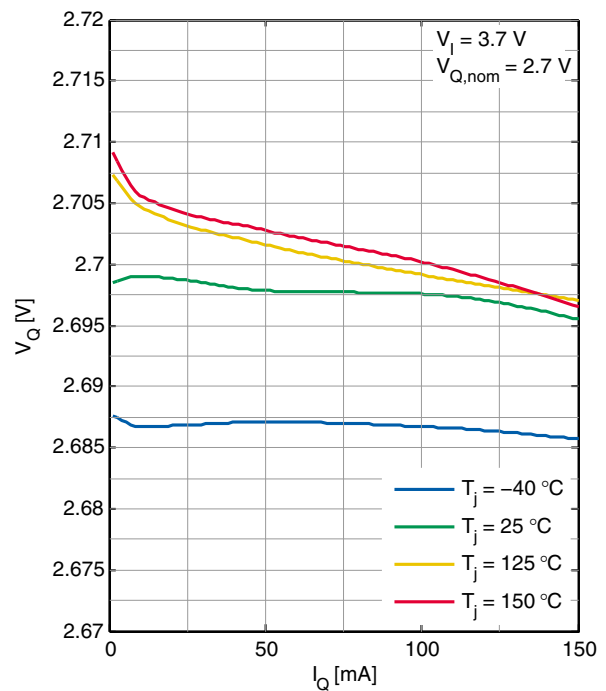
**Dropout Voltage  $V_{dr}$  vs. Nominal Output Voltage  $V_{Q,nom}$**



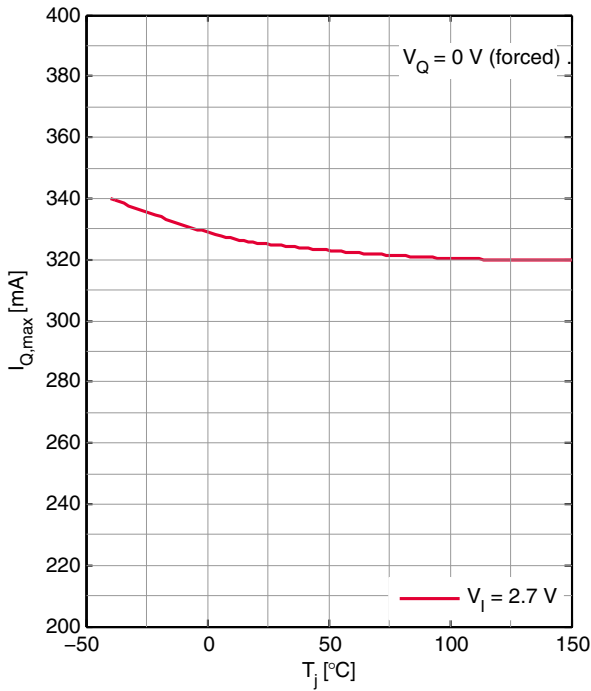
**Load Regulation: Output Voltage  $V_Q$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 1.2\text{ V}$ )**



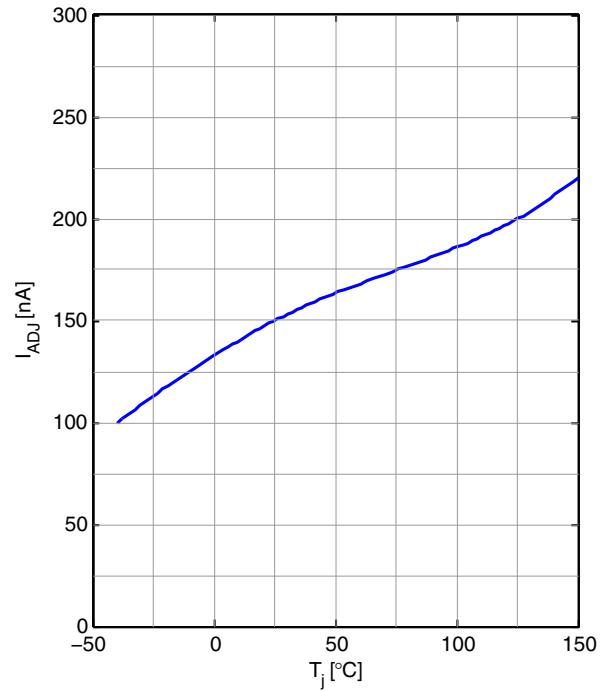
**Load Regulation: Output Voltage  $V_Q$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 2.7\text{ V}$ )**



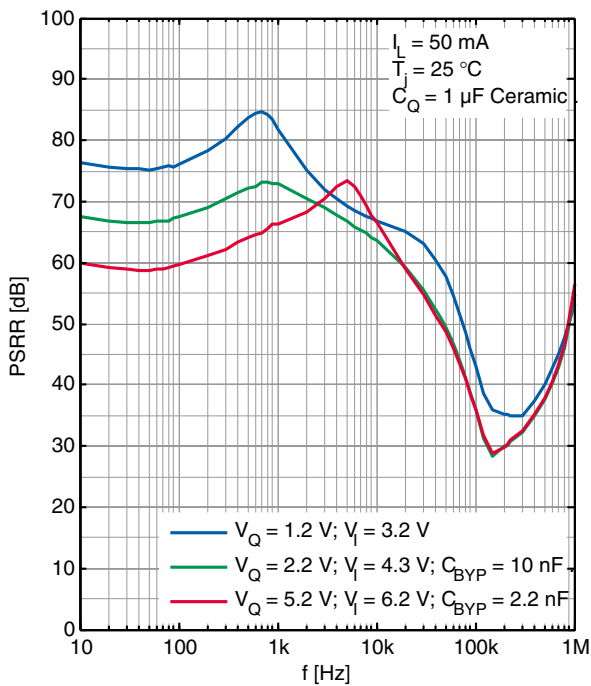
**Output Current Limitation  $I_{Q,max}$  vs. Junction Temperature  $T_j$**



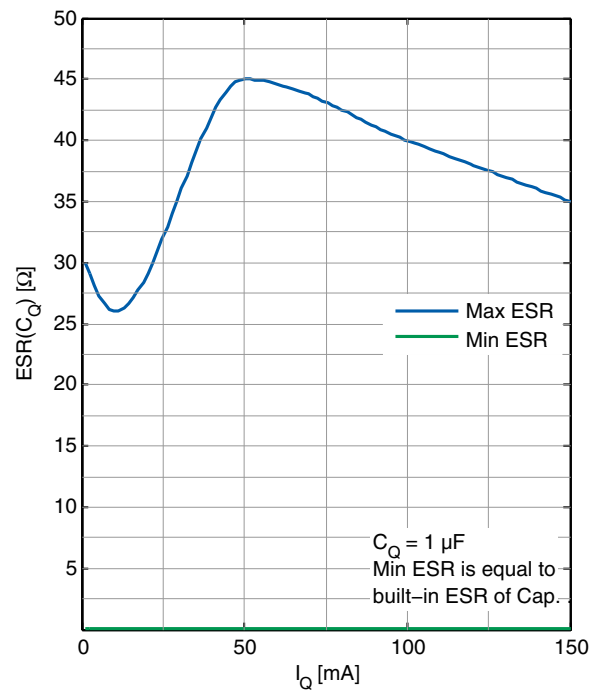
**ADJ Pin Current  $I_{ADJ}$  vs. Junction Temperature  $T_j$**



**PSRR vs. Frequency ( $V_{Q,nom} = 1.2$  V)**



**Output Capacitor Series Resistance  $ESR(C_Q)$  vs. Output Current  $I_Q$**



## 6 Current Consumption

### 6.1 Description Current Consumption

The Current Consumption of the device is characterizing the current the device needs to operate. The Quiescent Current is describing the Current Consumption in a very low load condition (e.g. the supplied microcontroller is in sleep mode). The Current Consumption of the device can be determined by measuring the Current flowing out of the GND Pin and defined as the delta between  $I_1$  and  $I_Q$ .

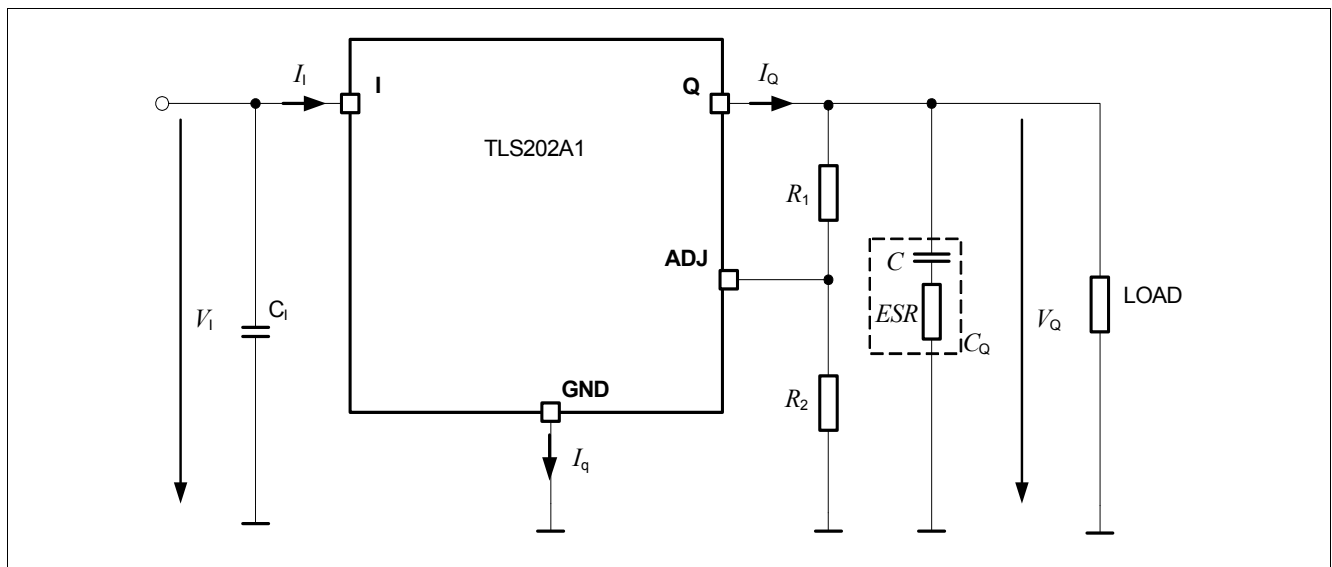


Figure 4 Parameter Definition Current Consumption

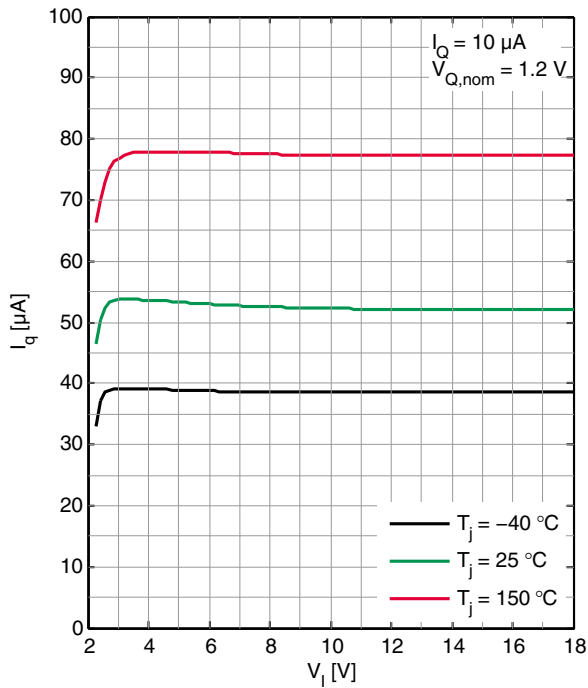
### 6.2 Electrical Characteristics Current Consumption

Table 5 Electrical Characteristics  $V_1 = V_Q + 1\text{ V}$  and  $V_1 \geq 2.7\text{ V}$ ;  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground (unless otherwise specified)

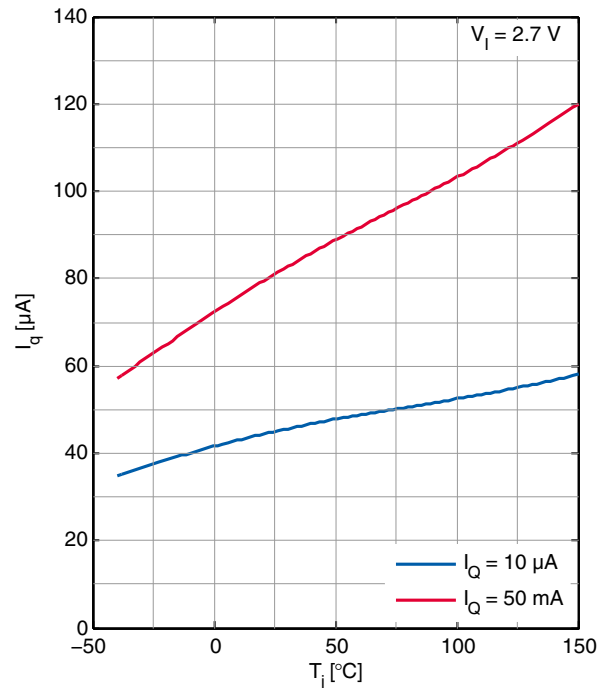
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Quiescent Current $I_q = I_1 - I_Q$	$I_q$	–	50	75	$\mu\text{A}$	$I_Q = 10\ \mu\text{A}$ ; $T_j = 25\text{ °C}$	P_6.2.1
Quiescent Current $I_q = I_1 - I_Q$	$I_q$	–	–	100	$\mu\text{A}$	$I_Q = 10\ \mu\text{A}$ ; $T_j \leq 125\text{ °C}$	P_6.2.2
Current Consumption $I_q = I_1 - I_Q$	$I_q$	–	150	200	$\mu\text{A}$	$I_Q = 50\ \text{mA}$	P_6.2.3

### 6.3 Typical Performance Characteristics Current Consumption

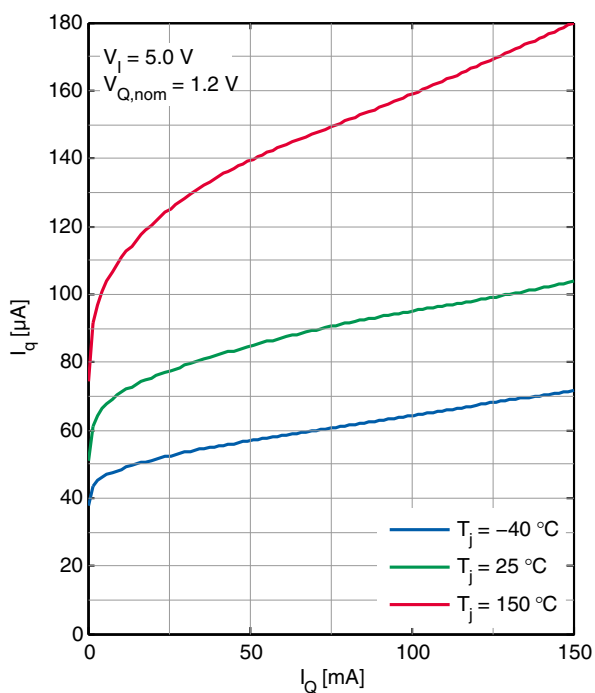
Quiescent Current  $I_q$  vs. Input Voltage  $V_I$



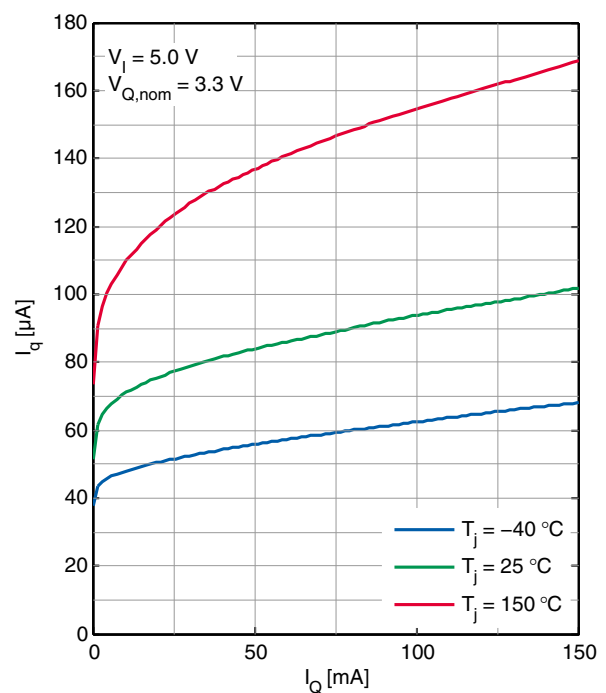
Current Consumption  $I_q$  vs. Junction Temperature  $T_j$



Current Consumption  $I_q$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 1.2 V$ )

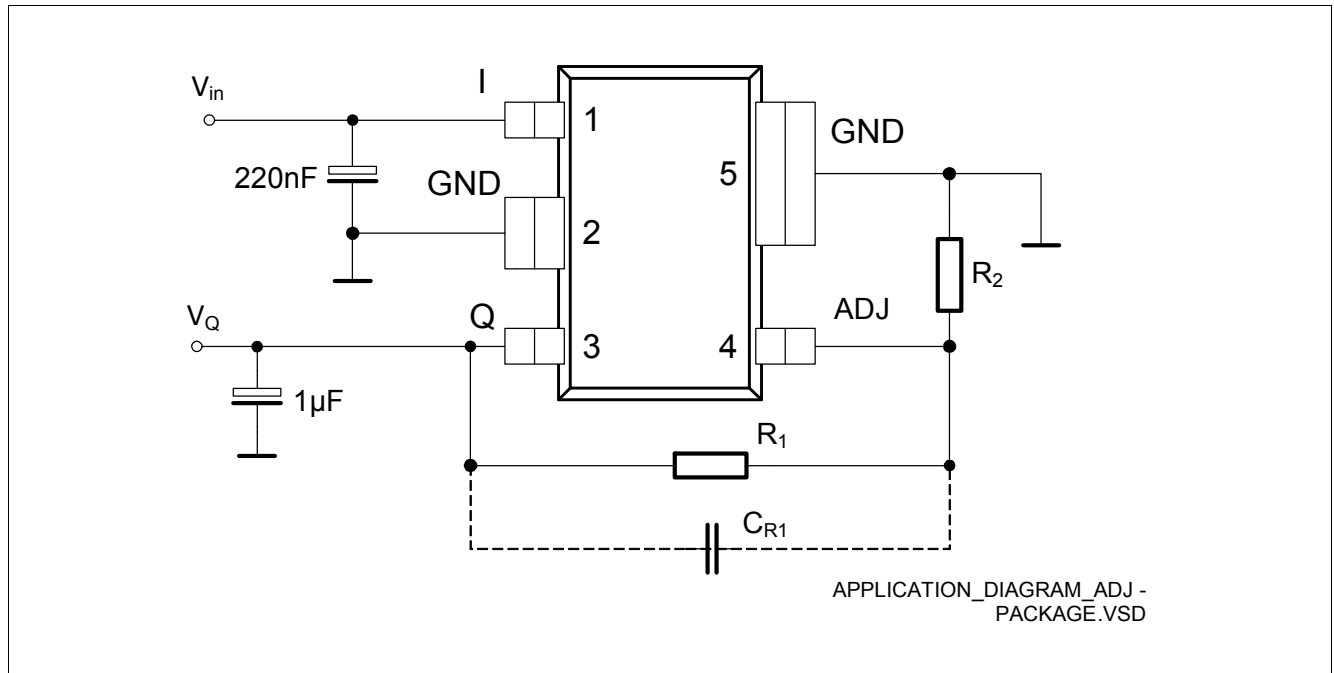


Current Consumption  $I_q$  vs. Load Current  $I_Q$  ( $V_{Q,nom} = 3.3 V$ )



## 7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.



**Figure 5** Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

The resistor divider for a specific output voltage can be calculated according to [Equation \(1\)](#). The current  $I_{ADJ}$ , which flows into the ADJ-Pin, can be neglected, if [Equation \(2\)](#) is observed.  $V_{ADJ}$  is typically 1.2 V.

$$\frac{R_1}{R_2} = \frac{V_Q}{V_{ADJ}} - 1 \quad (1)$$

$$R_2 \leq 50k\Omega \quad (2)$$

An optional Capacitor can be placed to improve the PSRR of this adjustable regulator for low currents smaller than 100  $\mu$ A. The capacitance depends strongly on the used resistance. According to [Equation \(3\)](#) the right value of the capacitance can be determined.

$$C_{R1} = \frac{1}{1 \cdot \pi \cdot R_1 \cdot 4kHz} \quad (3)$$

## 8 Package Outlines

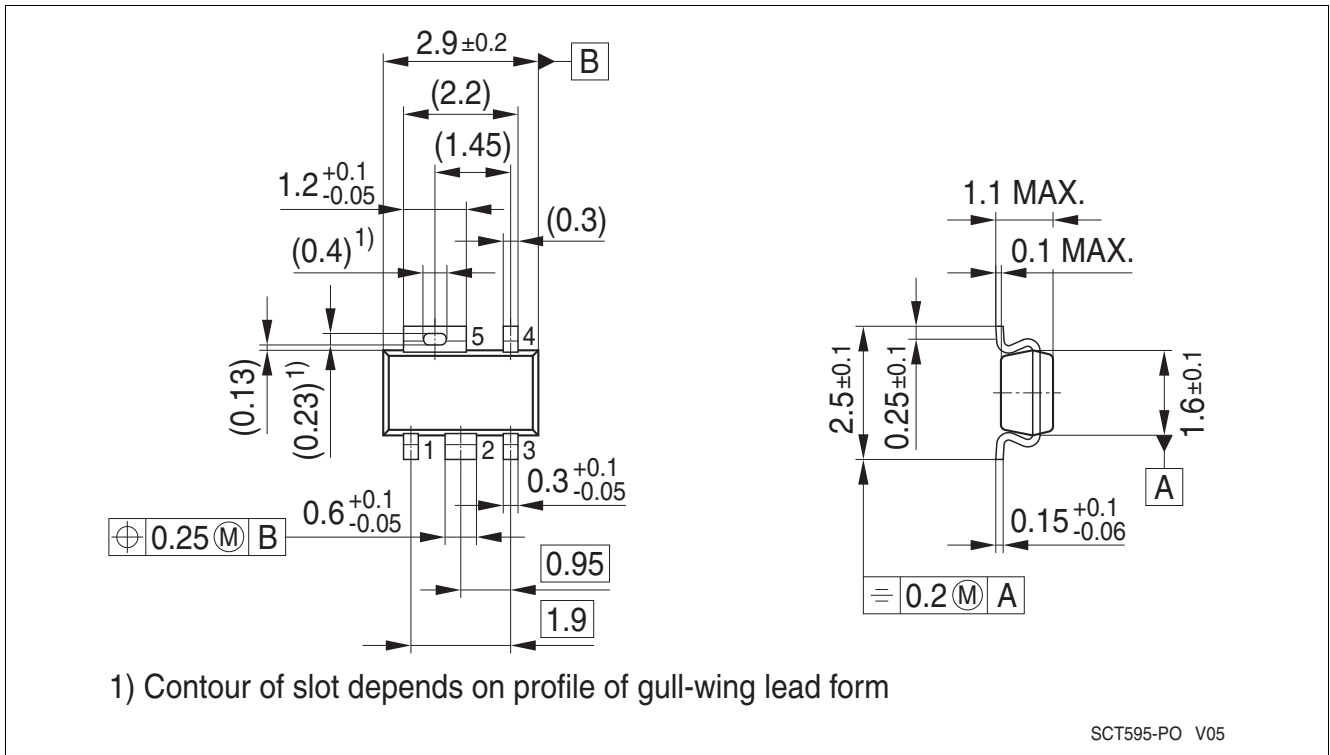


Figure 6 PG-SCT595

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:  
<http://www.infineon.com/packages>.

Dimensions in mm



## 9 Revision History

Revision	Date	Changes
1.0	2015-06-22	Initial Data Sheet.

**Edition 2015-06-22**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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### **Warnings**

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