

## YPN 438S——40V 10A N&P-Channel Power MOSFET (2 IN 1)

### General Features

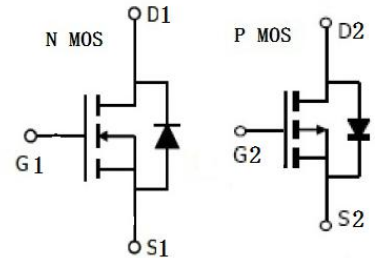
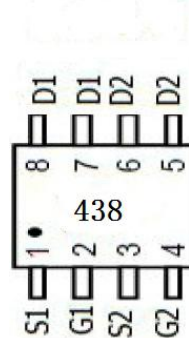
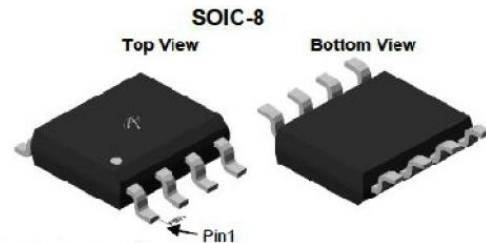
- Proprietary New Trench Technology
- Ultra-low Miller Charge
- N MOS RDS(ON),typ.=18mΩ@V<sub>GS</sub>=10V
- P MOS RDS(ON),typ.=30mΩ@V<sub>GS</sub>=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

### Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- Motor Drive

### Ordering Information

Part Number	Package	Marking
YPN 438S	SOP-8	438



### Absolute Maximum Ratings

Absolute Maximum Ratings		T <sub>A</sub> =25°C unless otherwise noted			
		Symbol	Maximum		Units
Parameter		N MOS	P MOS		
Drain-Source Voltage	V <sub>DS</sub>	+40	-40	V	
Gate-Source Voltage	V <sub>GS</sub>	±20 V	±20 V	V	
Continuous Drain Current	I <sub>D</sub>	T <sub>A</sub> =25°C	12.2	-10	A
		T <sub>A</sub> =70°C	8.5	-8	
Pulsed Drain Current	I <sub>DM</sub>	35	-30		
Maximum Power Dissipation		2.5	2.8	W	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150		°C	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device

### Thermal Characteristics

Symbol	Parameter	Value	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	4.0	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	42	

## Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D = \pm 250mA, V_{GS} = 0V$	$\pm 40$			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = \pm 40V, V_{GS} = 0V$			1	$\mu A$
$I_{GSS}$	Gate-Body leakage current	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	NMOS: $V_{DS} = V_{GS}, I_D = 250mA$	1	1.5	2.5	V
		PMOS: $V_{DS} = V_{GS}, I_D = -250mA$	-1.1	-1.7	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	NMOS: $V_{GS} = 10V, I_D = 10A$		15	18	$m\Omega$
		NMOS: $V_{GS} = 4.5V, I_D = 8A$		22	35	
		PMOS: $V_{GS} = -10V, I_D = -7.2A$		27	32	$m\Omega$
		PMOS: $V_{GS} = -4.5V, I_D = -5.6A$		32	38	
$g_{FS}$	Forward Transconductance	NMOS: $V_{DS} = 5V, I_D = 8A$	13			S
		PMOS: $V_{DS} = -5V, I_D = -5A$	20			
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sub>(Note 3)</sub>	NMOS: $V_{GS} = 0V, I_S = 8A$			1.2	V
		PMOS: $V_{GS} = 0V, I_S = -6A$				
$I_S$	Maximum Body-Diode Continuous Current <sub>(Note 2)</sub>	NMOS			10	A
		PMOS			-6.2	
$t_{rr}$	Body Diode Reverse Recovery Time	NMOS: $T_J = 25^\circ C, I_F = 10A, di/dt = 100A/\mu s$ <sub>(Note3)</sub>		35		ns
		PMOS: $T_J = 25^\circ C, I_F = -7A, di/dt = 100A/\mu s$ <sub>(Note3)</sub>		60		
<b>Dynamic Characteristics (Note4)</b>						
$C_{iss}$	Input Capacitance	NMOS		500		pf
$C_{oss}$	Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V, F = 1.0MHz$		60		
$C_{rss}$	Reverse Transfer Capacitance			25		
$C_{iss}$	Input Capacitance	PMOS		1750		
$C_{oss}$	Output Capacitance	$V_{DS} = -20V, V_{GS} = 0V, F = 1.0MHz$		215		
$C_{rss}$	Reverse Transfer Capacitance			180		

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Switching Characteristics</b> (Note 4)						
Q <sub>g</sub>	Total Gate Charge	NMOS : V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =8A		14		nC
Q <sub>gs</sub>	Gate Source Charge			2.9		
Q <sub>gd</sub>	Gate Drain Charge			5.2		
Q <sub>g</sub>	Total Gate Charge	PMOS : V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-5A		24		nC
Q <sub>gs</sub>	Gate Source Charge			3.5		
Q <sub>gd</sub>	Gate Drain Charge			6		
t <sub>d(on)</sub>	Turn-On Delay time	NMOS:  V <sub>DD</sub> =20V, I <sub>D</sub> =2A, R <sub>L</sub> =6.7Ω  V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω		5		ns
t <sub>r</sub>	Turn-On Rise Time			2.6		
t <sub>d(off)</sub>	Turn-Off Delay Time			16.1		
t <sub>f</sub>	Turn-Off Fall Time			2.3		
t <sub>d(on)</sub>	Turn-On Delay Time	PMOS:  V <sub>DD</sub> =-20V, I <sub>D</sub> =-2A, R <sub>L</sub> =2Ω,  V <sub>GS</sub> =-10V, R <sub>GEN</sub> =3Ω		9		ns
t <sub>r</sub>	Turn-On Rise Time			8		
t <sub>d(off)</sub>	Turn-Off Delay Time			28		
t <sub>f</sub>	Turn-Off Fall Time			10		

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

## Typical Electrical and Thermal Characteristics (Curves):P MOS

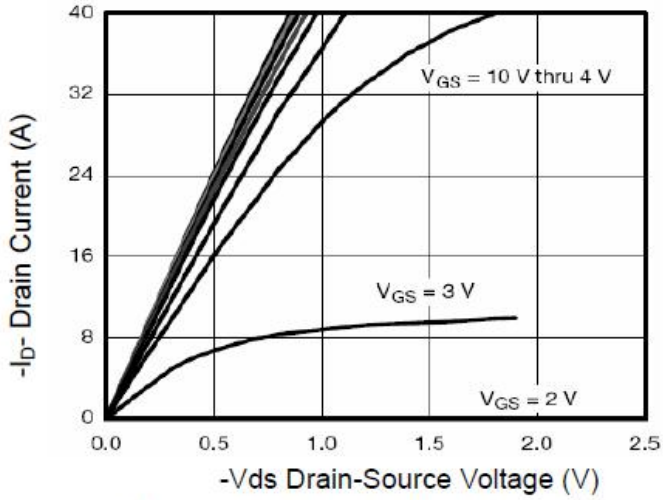


Figure 1 Output Characteristics

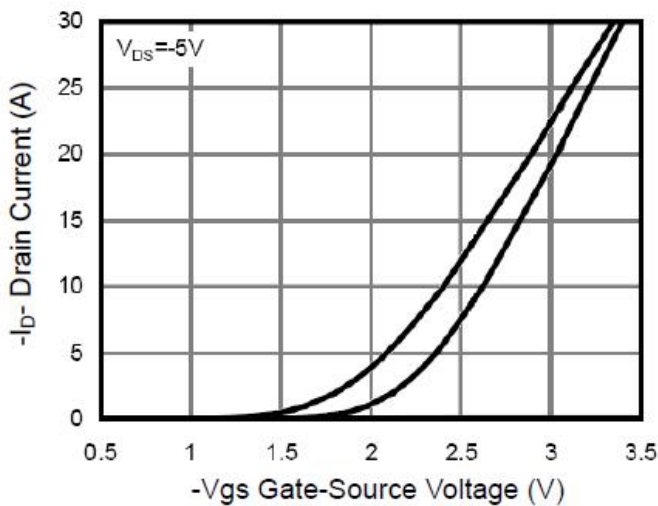


Figure 2 Transfer Characteristics

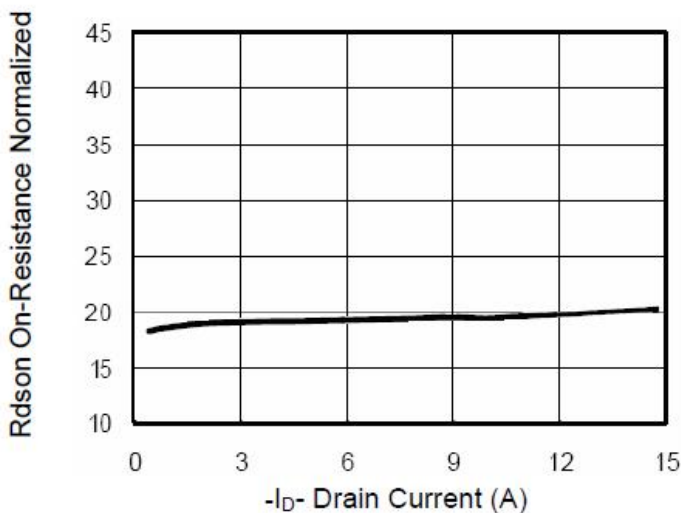


Figure 3 Rdson- Drain Current

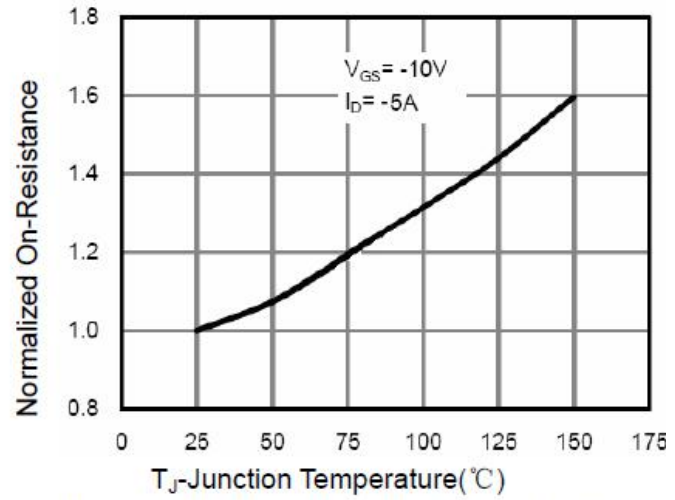


Figure 4 Rdson-Junction Temperature

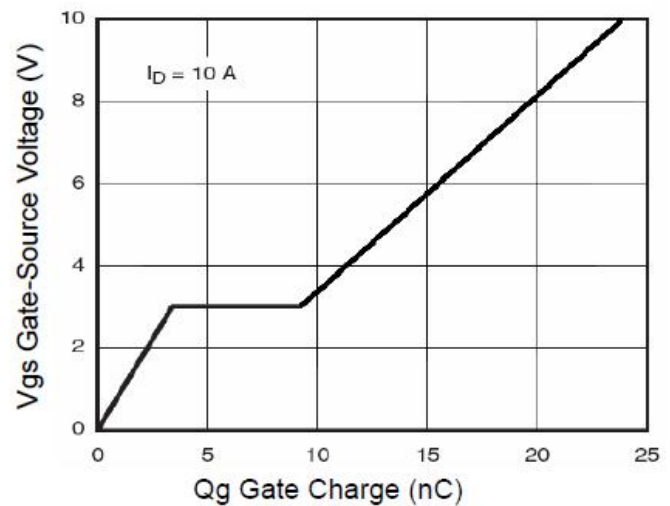


Figure 5 Gate Charge

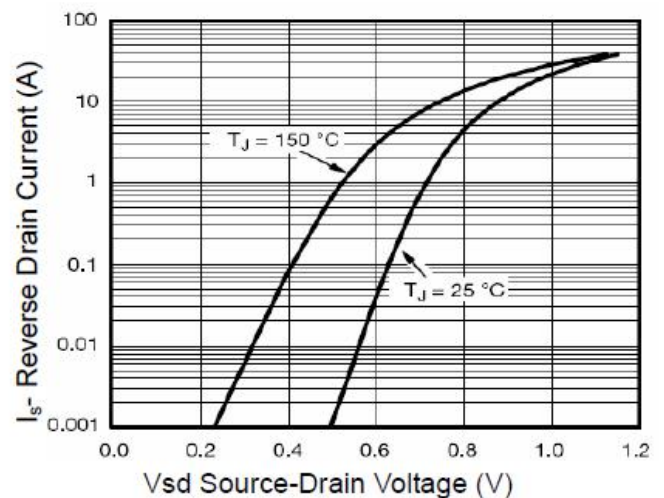


Figure 6 Source- Drain Diode Forward

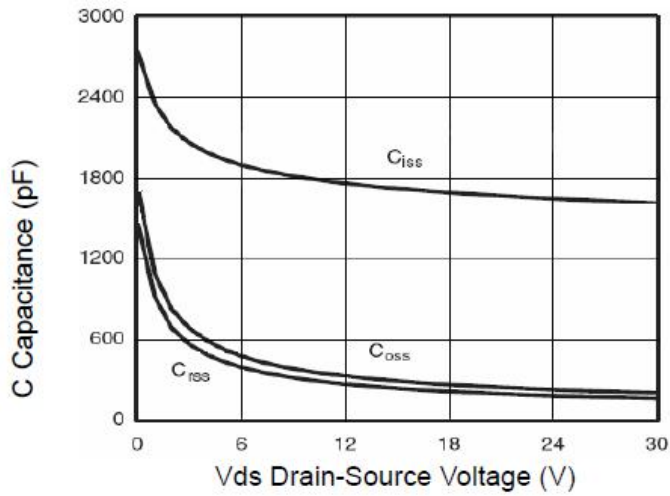


Figure 7 Capacitance vs Vds

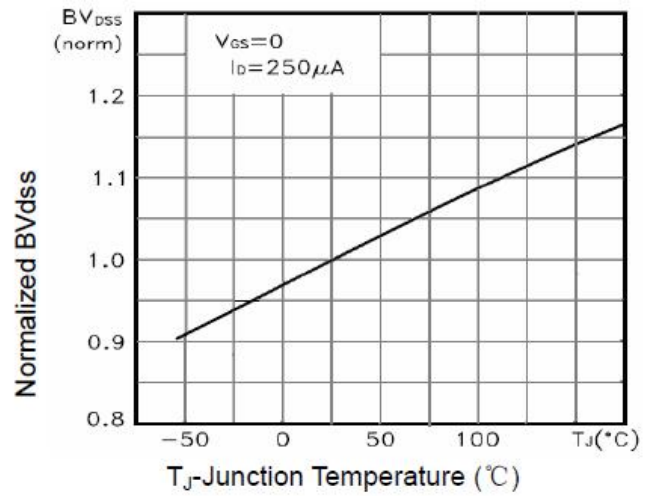


Figure 9  $BV_{DSS}$  vs Junction Temperature

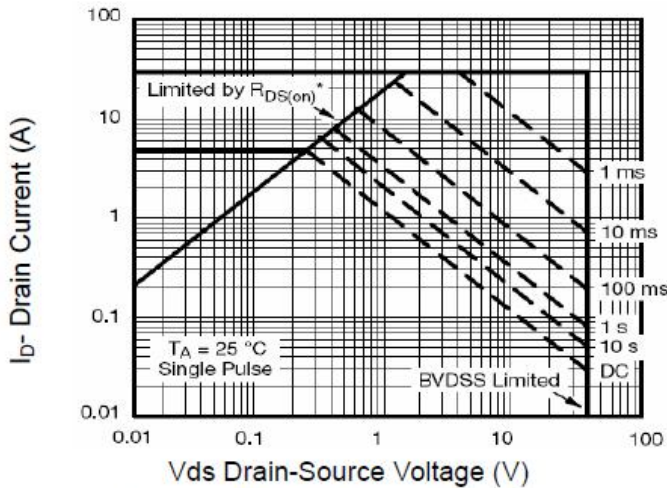


Figure 8 Safe Operation Area

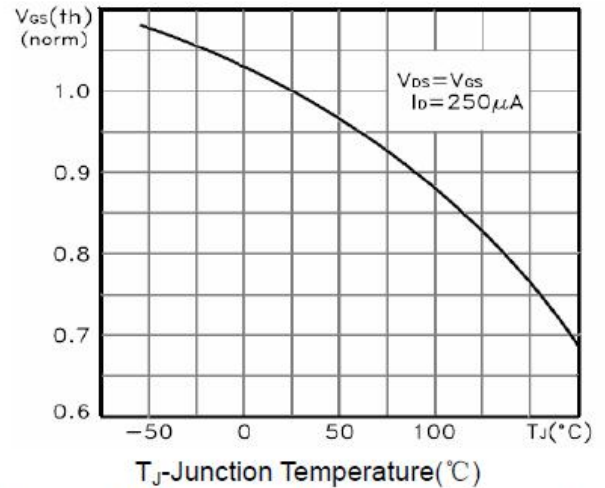


Figure 10  $V_{GS(th)}$  vs Junction Temperature

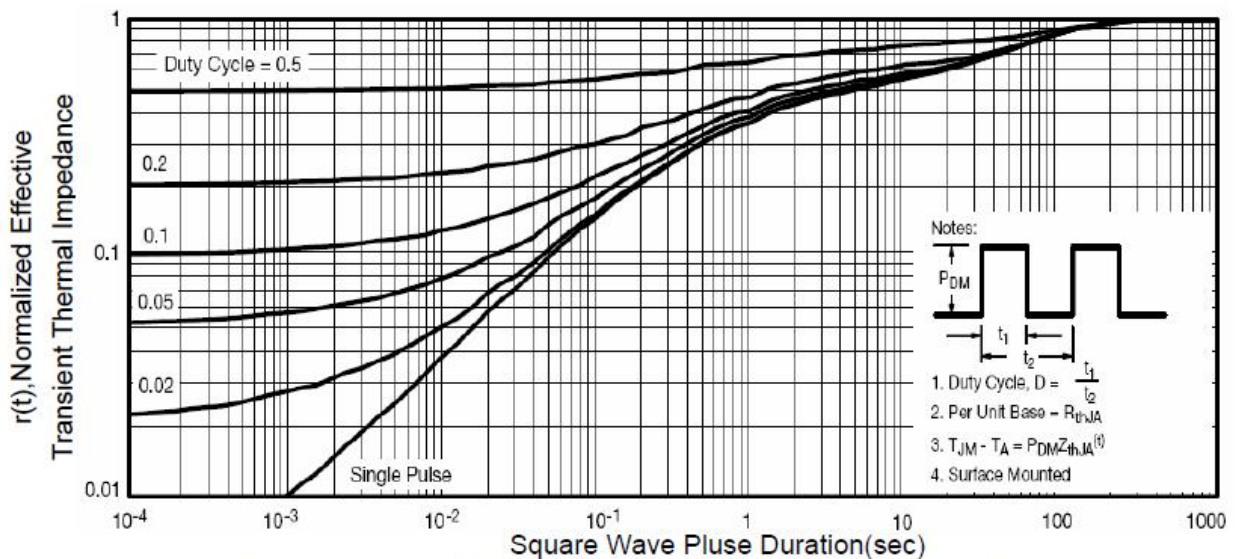


Figure 11 Normalized Maximum Transient Thermal Impedance

## Typical Electrical and Thermal Characteristics (Curves):N MOS

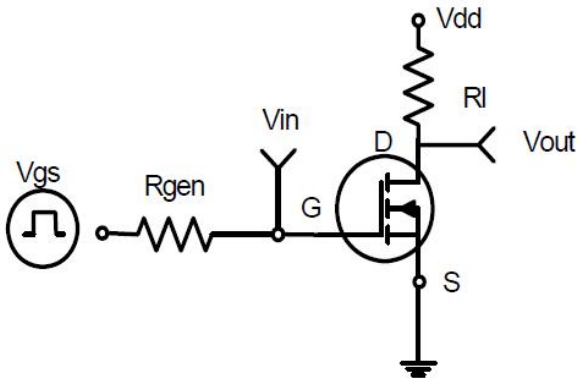


Figure 1: Switching Test Circuit

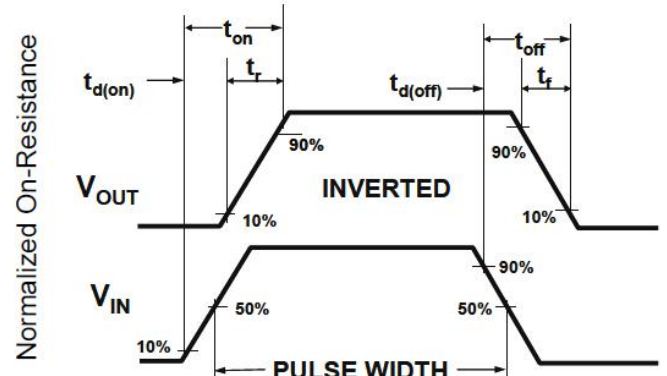


Figure 2: Switching Waveforms

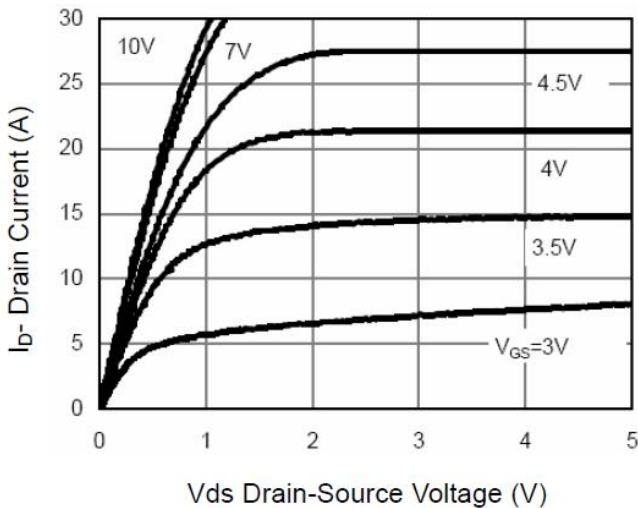


Figure 3 Output Characteristics

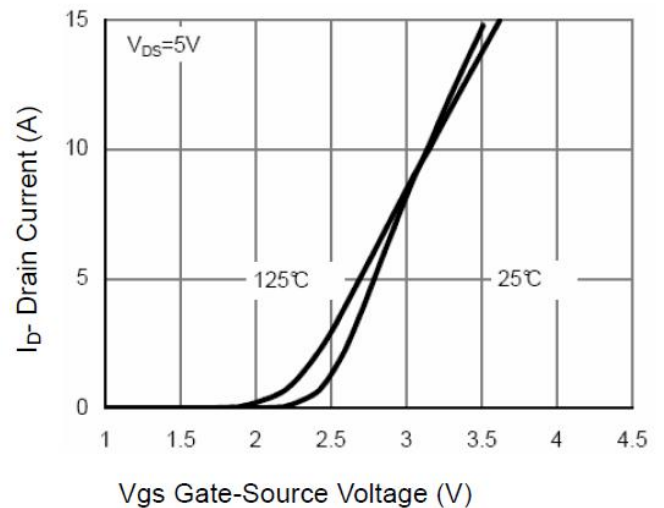


Figure 4 Transfer Characteristics

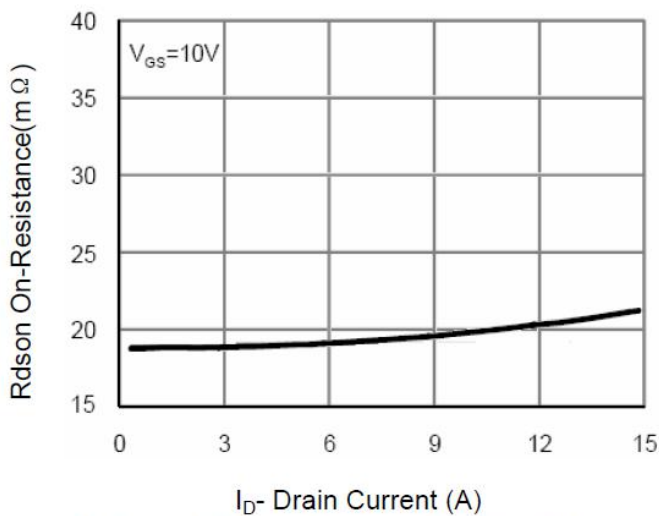


Figure 5 Drain-Source On-Resistance

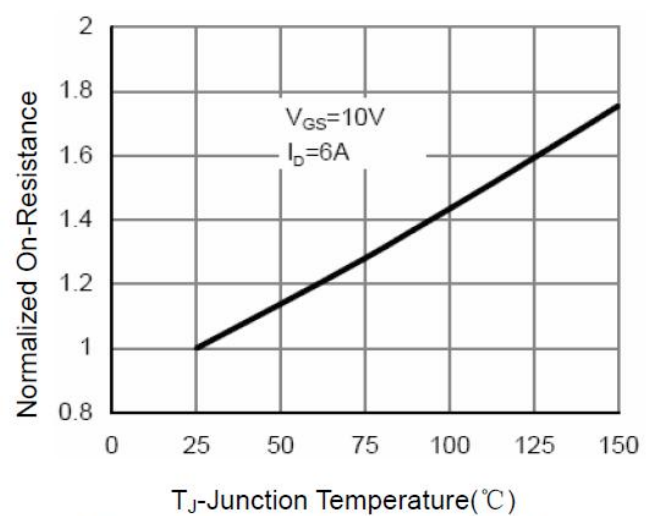


Figure 6 Drain-Source On-Resistance

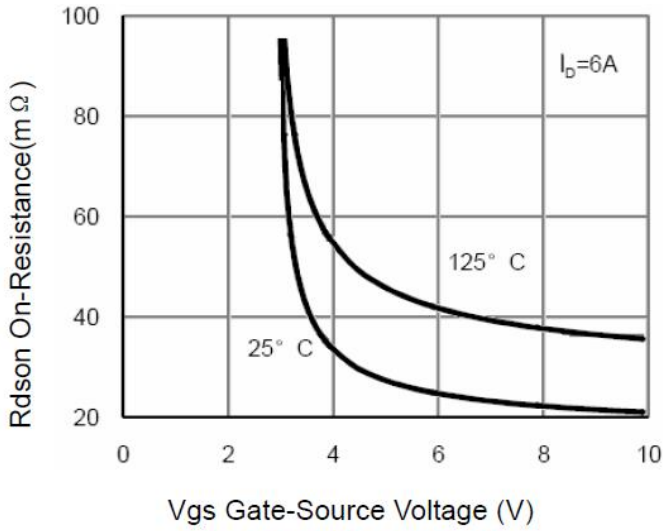


Figure 7 Rdson vs Vgs

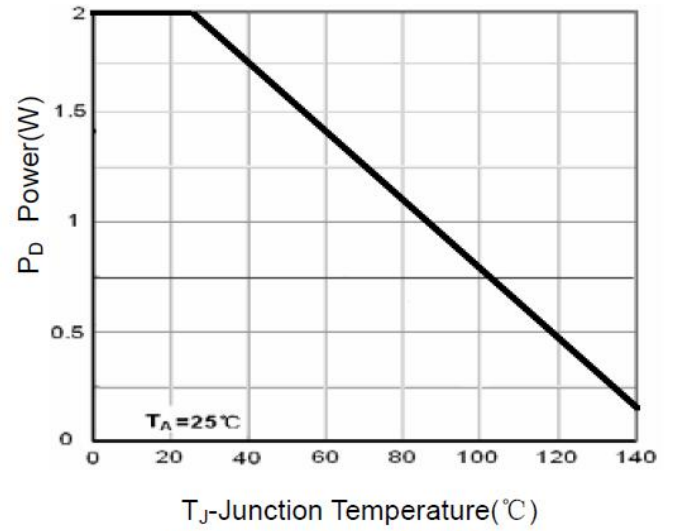


Figure 8 Power Dissipation

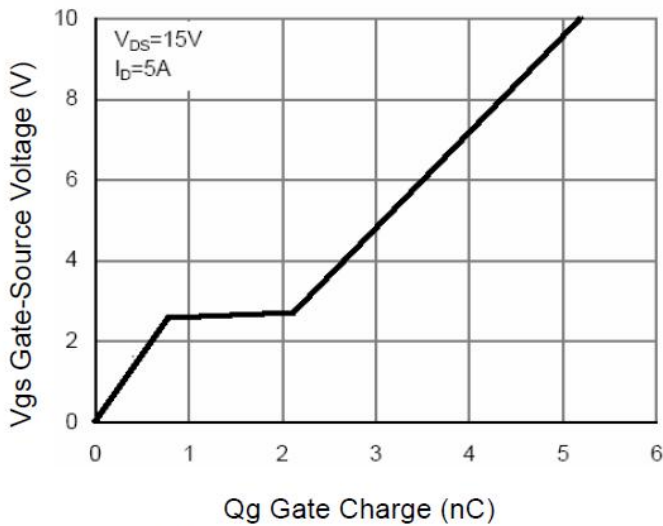


Figure 9 Gate Charge

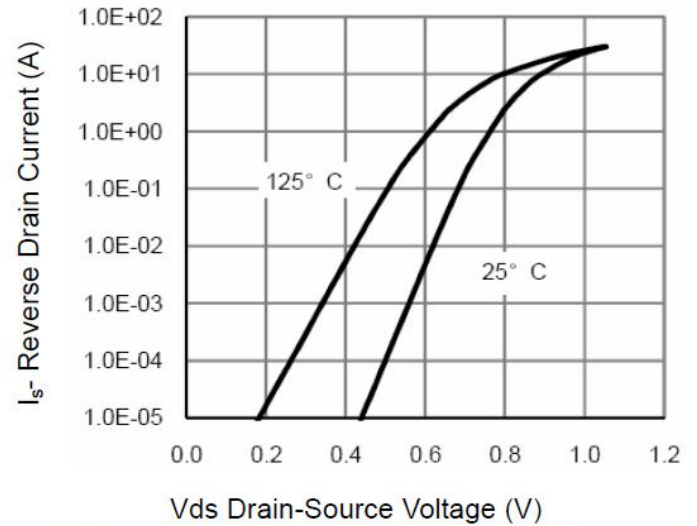


Figure 10 Source- Drain Diode Forward

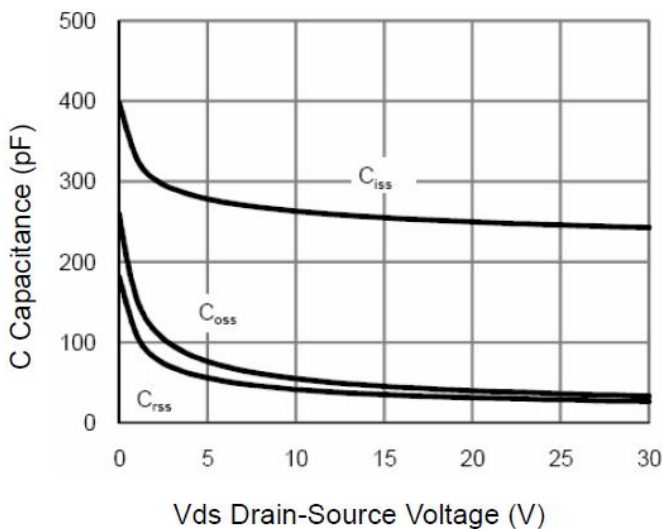


Figure 11 Capacitance vs Vds

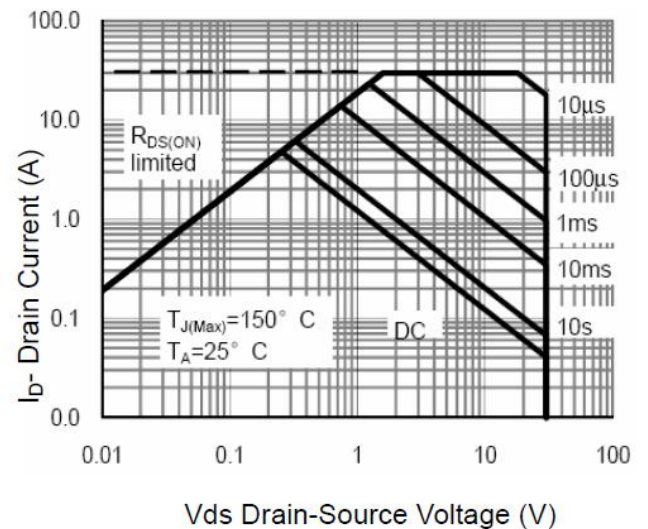
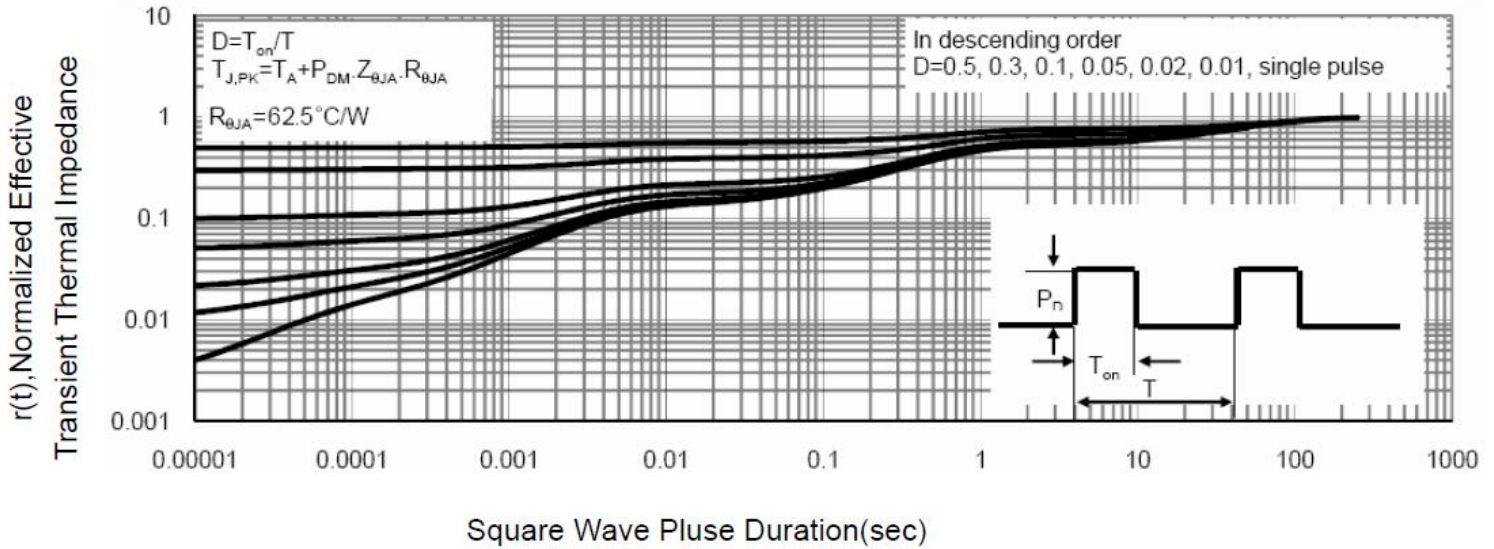


Figure 12 Safe Operation Area



**Figure 13 Normalized Maximum Transient Thermal Impedance**

**Order information:**

Order information							
	Y	2	N/	6	55	S	()
公司商标代号 Company symbol							
1: NIL ,2:2 MOS							
P: PMOS, N:N MOS							
BVDSS: 6—60V;10—100V;20—200V; 35—350V; 40—400V							
RDS(on) : 55—55m Ω ;38—38m Ω ; 16—16m Ω							
D:DIP;S:SOP							
Special code							



**Dimension and PCB layout :**

