

N-Channel 20V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)			
20	0.012 at V _{GS} = 10 V	12	6.1 nC			
20	0.015 at V _{GS} = 4.5 V	11	0.1110			

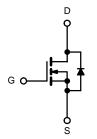
SO-8

FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

- Notebook CPU Core
 - High-Side Switch



N-Channel MOSFET

S	3	6 D
G	4	5 D
	Top View	
ABSOLUTE M	AXIMUM RA	TINGS $T_A = 25 ^{\circ}C$,
Parameter		

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	20		
Gate-Source Voltage	V _{GS}	± 16	V		
	T _C = 25 °C		12		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	11		
Continuous Diain Current (1) = 130 C)	T _A = 25 °C	'D	10 ^{b, c}		
	$T_A = 70 ^{\circ}C$		8 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	47		
Continuous Source-Drain Diode Current	T _C = 25 °C	I.	3.7		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.0 ^{b, c}		
Single Pulse Avalanche Current L = 0.1 mH		I _{AS}	20		
Avalanche Energy		E _{AS}	21	mJ	
	T _C = 25 °C		4.1		
Maximum Dawar Dissipation	T _C = 70 °C	P _D	2.5	W	
Maximum Power Dissipation	T _A = 25 °C	' D	2.2 ^{b, c}	VV	
	T _A = 70 °C		1.3 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	39	55	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	25	29	C/VV	

Notes:

- a. Base on T_C = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.

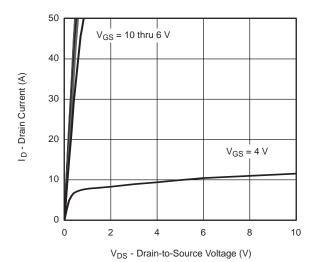


Static V _{DS} V _{DS} = 0 V. I _D = 250 μA 20 V V _{DS} Temperature Coefficient Λ/V _{DS} /T _J I _D = 250 μA 26 mV/* V _{GS(m)} Temperature Coefficient Λ/V _{DS} /T _J I _D = 250 μA 1.0 3.0 V Gate-Source Threshold Voltage V _{GS(m)} Temperature Coefficient Λ/V _{DS} /T _J V _{DS} = 250 μA 1.0 3.0 V Gate-Source Leakage I _{GSS} V _{DS} = 0 V. V _{QS} = 20 V ± 100 nA Zero Gate Voltage Drain Current I _{DSS} V _{DS} = 0 V. V _{QS} = 0 V ± 100 nA Zero Gate Voltage Drain Current I _{DSS} V _{DS} = 20 V. V _{QS} = 0 V ± 100 nA On-State Drain Current I _{D(m)} V _{DS} = 20 V. V _{QS} = 0 V. T _J = 55 °C 10 A On-State Drain Current I _{D(m)} V _{DS} = 20 V. V _{QS} = 0 V. T _J = 50 °C 10 A On-State Drain Current I _{D(m)} V _{DS} = 50 V. V _{QS} = 10 V. D _D = 0 A 0.015 A On-State Drain Current 9tb V _{DS} = 10 V. I _D = 10 A 50 S Dynamic* Dynamic*	SPECIFICATIONS $T_J = 25 ^{\circ}\text{C}$ Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Drain-Source Breakdown Voltage V _{OS} V _{OS} = 0 V, I _D = 250 μA 20 V V _{DS} Temperature Coefficient AV_{DS}/T_J I _D = 250 μA 26 mV/V ^S Sate-Source Threshold Voltage V _{SS(th)} Ty I _D = 250 μA 1.0 3.0 V Gate-Source Leakage V _{SS} (th) V _{DS} = V _{SS} (th) 1.0 3.0 V Zero Gate Voltage Drain Current I _{DSS} V _{DS} = 0 V, V _{CS} = 0 V 1 μA Anni-Source Con-State Resistance ⁸ I _{D(en)} V _{DS} = 20 V, V _{CS} = 0 V 2 1 On-State Drain Current ^a I _{D(en)} V _{DS} = 20 V, V _{CS} = 0 V 1 μA On-State Drain Current ^a I _{D(en)} V _{DS} = 5 V, V _{CS} = 0 V 2 A On-State Resistance ^a R _{DS(en)} V _{DS} = 10 V, I _D = 10 A 0.012 Ω Forward Transconductance ^a 9ts V _{DS} = 10 V, I _D = 10 A 50 S Dypamic ^b 1 1 4 4 4 4 4 4 4 4 5 5 S 5 <th></th> <th>Cymbol</th> <th>rest conditions</th> <th>141111.</th> <th>l ihb.</th> <th>IVIGA.</th> <th>Oint</th>		Cymbol	rest conditions	141111.	l ihb.	IVIGA.	Oint	
V _{DS} Temperature Coefficient Δ/V _{DS} (T _J) I _D = 250 μA 26 m/V** V _{CS(M)} V _{CS(M)} (Pemperature Coefficient Δ/V _{DS} (M) 1.0 -6 m/V** Gate-Source Threshold Voltage V _{CS(M)} V _{DS} = V _{CS} , I _D = 250 μA 1.0 3.0 V Zero Gate Voltage Drain Current I _{DSS} V _{DS} = 0 V, V _{CS} = 20 V ± 100 nA Zero Gate Voltage Drain Current* I _{DS} V _{DS} = 20 V, V _{CS} = 0 V ± 100 nA On-State Drain Current* I _{D(On)} V _{DS} = 20 V, V _{CS} = 0 V ± 10 µA On-State Drain Current* I _{D(On)} V _{DS} = 5 V, V _{CS} = 10 V 20 A On-State Resistance** R _{DS} (n) V _{DS} = 5 V, V _{DS} = 10 V 20 A Drain-Source On-State Resistance** 9fs V _{DS} = 10 V, V _{DS} = 10 A 0.012 0.015 Ω Dynamic** Dynamic** V _{DS} = 10 V, V _{DS} = 10 V, I _D = 10 A 50 S S Dynamic** Dynamic** V _{DS} = 10 V, V _{DS} = 10 V, I _D = 10 A 165 pF P Reverse Transfer Capacitance		V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20			V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				-	26		mV/°C	
Gate-Source Threshold Voltage $V_{GS(th)}$ $V_{DS} = V_{GS}, I_D = 250 \mu A$ 1.0 3.0 V Gate-Source Leakage I _{GSS} $V_{DS} = 0 V, V_{GS} = 20 V$ ± 100 nA Zero Gate Voltage Drain Current I _{DSS} $V_{DS} = 20 V, V_{GS} = 0 V$ ± 100 nA On-State Drain Current ^a I _{D(m)} $V_{DS} = 20 V, V_{GS} = 0 V$ ± 0 10 µA On-State Drain Current ^a I _{D(m)} $V_{DS} = 50 V, V_{GS} = 0 V, T_{J} = 55 °C$ 10 A On-State Drain Current ^a I _{D(m)} $V_{DS} = 50 V, V_{GS} = 0 V, T_{J} = 55 °C$ 10 A On-State Drain Current ^a I _{D(m)} $V_{DS} = 50 V, V_{GS} = 10 V$ 20 A A Drain-Source On-State Resistance ^a $R_{DS(m)}$ $V_{DS} = 10 V, I_{D} = 10 A$ 0.015 5 S Drain-Source On-State Resistance ^a G_{DS} $V_{DS} = 10 V, I_{D} = 10 A$ 0.015 S S S S 9 0.015 S S S 9 0.015 S S S 0.015 S <td></td> <td></td> <td>$I_D = 250 \mu\text{A}$</td> <td></td> <td></td> <td></td>			$I_D = 250 \mu\text{A}$					
Gate-Source Leakage IGSS $V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$ ± 100 nA Zero Gate Voltage Drain Current IDSS $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ 1 μA On-State Drain Current ^a ID(on) $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ 20 A A Drain-Source On-State Resistance ^a RDS(on) $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ 20 A A Drain-Source On-State Resistance ^a RDS(on) $V_{DS} = 10 \text{ V}, V_{DS} = 10 \text{ A}$ 0.012 0.015 Forward Transconductance ^a 9fs $V_{DS} = 10 \text{ V}, V_{DS} = 10 \text{ A}$ 0.015 0.015 S Dynamic ^b Nput Capacitance C_{SS} $V_{DS} = 10 \text{ V}, V_{DS} = 10 \text{ A}$ 0.015 0.015 0.015 Output Capacitance C_{SS} $V_{DS} = 10 \text{ V}, V_{DS} = 0 \text{ V}, I_{D} = 10 \text{ A}$ 0.015		1	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						1	nA	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		300				1		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Zero Gate Voltage Drain Current	I _{DSS}				10		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	On-State Drain Current ^a	I _{D(on)}		20			А	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			V _{GS} = 10 V, I _D = 10 A				+	
Forward Transconductance ^a g_{fs} $V_{DS} = 10 \text{ V}$, $I_{D} = 10 \text{ A}$ 50 S Dynamic ^b Input Capacitance C_{i88} $V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$ 165 pF Reverse Transfer Capacitance C_{rss} $V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$ 165 pF Total Gate Charge Q_g $V_{DS} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $V_{DS} = 10 \text{ A}$ 15 23 Gate-Source Charge Q_{gs} $V_{DS} = 10 \text{ V}$, $V_{GS} = 5 \text{ V}$, $I_{D} = 10 \text{ A}$ 2.5 nC Gate-Drain Charge Q_{gs} $V_{DS} = 10 \text{ V}$, $V_{GS} = 5 \text{ V}$, $I_{D} = 10 \text{ A}$ 2.5 nC Gate Resistance R_g $f = 1 \text{ MHz}$ 0.36 1.8 3.6 Ω Turn-On Delay Time $t_{d(cn)}$ $V_{DD} = 10 \text{ V}$, $R_L = 1.4 \Omega$ 12 16 23 Fall Time t_f $V_{DD} = 10 \text{ V}$, $R_L = 1.4 \Omega$ 10 20 16 22 16 10 16 22 16 10 16 22 16 10 16 22<	Drain-Source On-State Resistance ^a	R _{DS(on)}	25 2		0.015		Ω	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Forward Transconductance ^a	9 _{fs}			50		S	
Input Capacitance C Input Capacitance					<u> </u>			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Capacitance	C _{iss}			800			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Output Capacitance	+	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		165		pF	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Reverse Transfer Capacitance				73			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	T. 10 (0)		V _{DS} = 10 V, V _{GS} = 10 V, I _D = 10 A		15	23	nC	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	lotal Gate Charge				6.8	10.2		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 10 \text{ A}$		2.5			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate-Drain Charge	Q_{gd}			2.3			
$ \begin{array}{ c c c c c }\hline \text{Rise Time} & & & & & & & & & & & & & & & & & & &$	Gate Resistance	R _g	f = 1 MHz	0.36	1.8	3.6	Ω	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Delay Time	t _{d(on)}			16	23		
Fall Time t_f 10 18 Turn-On Delay Time $t_{d(on)}$ 8 16 Rise Time t_r $V_{DD} = 10 \text{ V}$, $R_L = 1.4 \Omega$ 10 20 Turn-Off Delay Time $t_{d(off)}$ 16 22 Fall Time t_f 8 15 Drain-Source Body Diode Characteristics Continuous Source-Drain Diode Current t_g t_g t_g 10 t_g Pulse Diode Forward Current ^a t_g	Rise Time	t _r	V_{DD} = 10 V, R_L = 1.4 Ω		12	16	1	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Delay Time	t _{d(off)}	$I_D \cong 9 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		16	22		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Fall Time	t _f			10	18	200	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Delay Time	t _{d(on)}			8	16	115	
Fall Time $t_{\rm f}$ t_{\rm	Rise Time	t _r	V_{DD} = 10 V, R_L = 1.4 Ω		10	20		
	Turn-Off Delay Time	t _{d(off)}	$I_D\cong 9$ A, V_{GEN} = 10 V, R_g = 1 Ω		16	22		
Continuous Source-Drain Diode Current I_S $T_C = 25 ^{\circ}\text{C}$ 10 A Pulse Diode Forward Current ^a I_{SM} 50 Body Diode Voltage V_{SD} $I_S = 9 ^{\circ}\text{A}$ 0.8 1.2 V Body Diode Reverse Recovery Time V_{rr} 15 30 ns Body Diode Reverse Recovery Charge V_{rr} V	Fall Time	t _f			8	15		
Pulse Diode Forward Current ^a I_{SM} 50 Body Diode Voltage V_{SD} $I_{S} = 9$ A 0.8 1.2 V Body Diode Reverse Recovery Time t_{rr} Body Diode Reverse Recovery Charge Q_{rr} Reverse Recovery Fall Time t_{a} $I_{F} = 9$ A, $dI/dt = 100$ A/ μ s, $T_{J} = 25$ °C A A A A A A A A	Drain-Source Body Diode Characterist	ics						
Pulse Diode Forward Currenta I_{SM} 50Body Diode Voltage V_{SD} $I_S = 9 A$ 0.81.2 V Body Diode Reverse Recovery Time t_{rr} 1530nsBody Diode Reverse Recovery Charge Q_{rr} $I_F = 9 A$, $dI/dt = 100 A/\mu s$, $T_J = 25 °C$ 612nCReverse Recovery Fall Time t_a t_a t_a t_a t_a	Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			10	^	
Body Diode Reverse Recovery Time t_{rr} Body Diode Reverse Recovery Charge Q_{rr} Reverse Recovery Fall Time t_a $I_F = 9 \text{ A, dI/dt} = 100 \text{ A/µs, T}_J = 25 \text{ °C}$ $0 \text{ Body Diode Reverse Recovery Charge } t_a$	Pulse Diode Forward Current ^a	I _{SM}				50	_ A	
Body Diode Reverse Recovery Charge Q_{rr} Reverse Recovery Fall Time t_a $I_F = 9 \text{ A, dI/dt} = 100 \text{ A/µs, T}_J = 25 \text{ °C}$ $6 \qquad 12 \qquad \text{nC}$ $8 \qquad \qquad \text{ns}$	Body Diode Voltage	V _{SD}	I _S = 9 A		0.8	1.2	V	
Reverse Recovery Fall Time t_a	Body Diode Reverse Recovery Time				15	30	ns	
Reverse Recovery Fall Time t_a	Body Diode Reverse Recovery Charge	Q _{rr}	L = 0 A dl/dt = 100 A/··· T = 25 °C		6	12	nC	
Reverse Recovery Rise Time t _b 7	Reverse Recovery Fall Time		$I_F = 9 \text{ A}$, $\text{di/dl} = 100 \text{ A/}\mu\text{s}$, $I_J = 25 \text{ °C}$		8		ns	
	Reverse Recovery Rise Time				7			

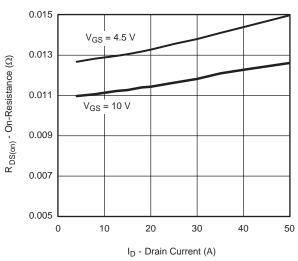
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$ b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

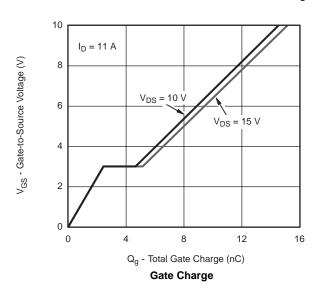




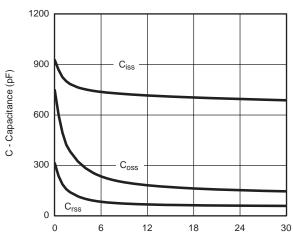
Output Characteristics



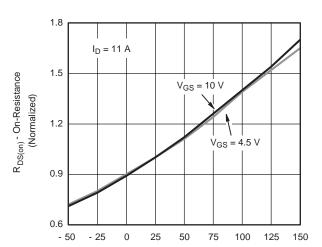
On-Resistance vs. Drain Current and Gate Voltage



V_{GS} - Gate-to-Source Voltage (V) **Transfer Characteristics**

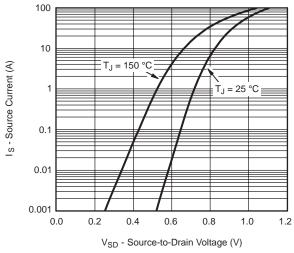


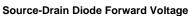
 V_{DS} - Drain-to-Source Voltage (V) $\label{eq:VDS} \mbox{\bf Capacitance}$

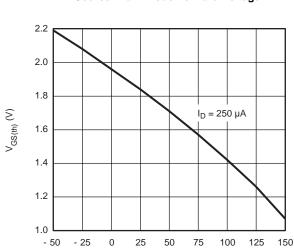


 $\label{eq:TJ-Junction} T_{J} \text{ - Junction Temperature (°C)}$ On-Resistance vs. Junction Temperature



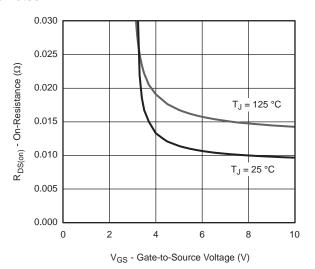




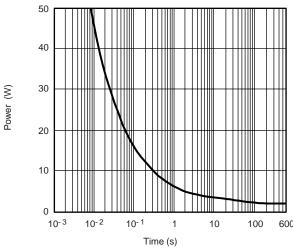


T_J - Temperature (°C)

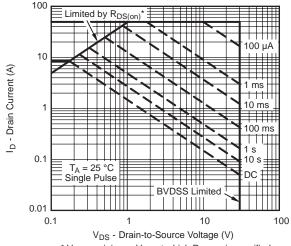
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



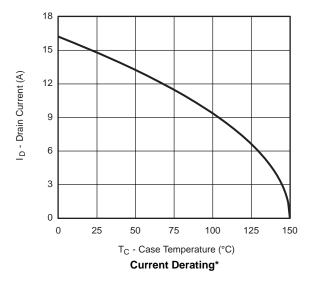
Single Pulse Power, Junction-to-Ambient

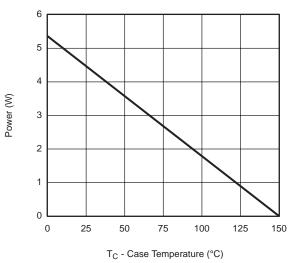


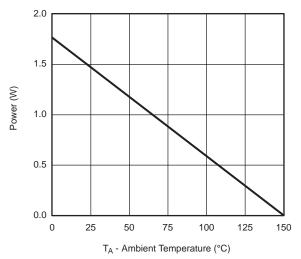
* $V_{\mbox{\footnotesize{GS}}} >$ minimum $V_{\mbox{\footnotesize{GS}}}$ at which $R_{\mbox{\footnotesize{DS(on)}}}$ is specified

Safe Operating Area, Junction-to-Ambient





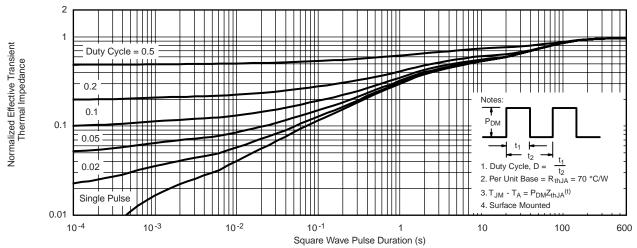




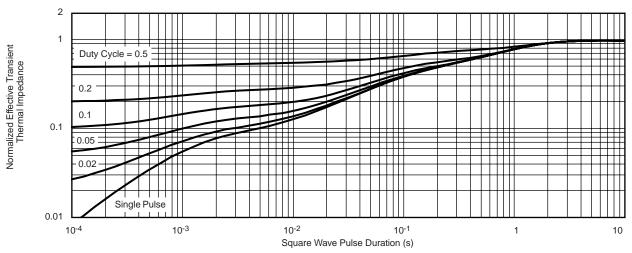
Power Derating, Junction-to-Foot Power Derating, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





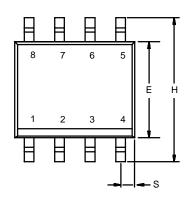
Normalized Thermal Transient Impedance, Junction-to-Ambient

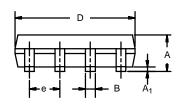


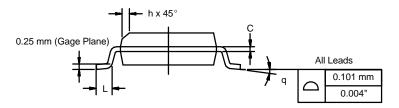
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD







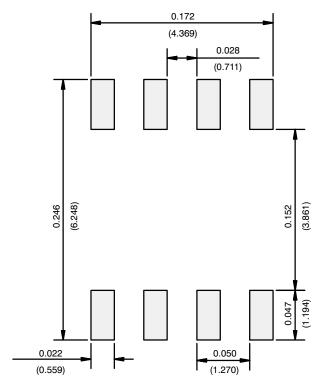
	MILLIMETERS		INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050) BSC	
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sep-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



Disclaimer

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Material Category Policy

Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be RoHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.tw)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.