5 Port 10/100 Ethernet Integrated Switch
(Loop Detection, Layer 2-4 MF Classifier, HW IGMP Snooping)

Features

- Wide operating temperature range
  - IP175LLF (0°C to 70°C)
  - IP175LLFI (-40°C to 85°C)
- Built in 5 MAC and 4 PHY
- Each port can be configured to be 10Based-T, 100Base-TX
- Up to 2K MAC addresses
- Support auto-polarity for 10Mbps
- Broadcast storm protection
- Auto MDI-MDIX
- Support one MII/RMII port
- Layer2-4 Multi-Field classifier
  - Support 8-MultiField entry
  - Support traffic policy
  - Support Multi-Filed filter
  - Support copy to mirror port
  - Support trap to CPU port
- Class of Service
  - Port based, MAC address, VID, VLAN priority, IPv4 ToS, IPv6 DSCP,TCP/UDP logical port and Multi-Field
- QoS
  - Support policy-based QoS
  - Support 4-level priority queues per port
  - WRR/WFQ/SP
- Support hardware IGMP v1,v2 snooping
- Support Port mirror
- Support 16 VLAN (IEEE Std 802.1q)
  - Port-based/tagged-based VLAN
  - Shared/Independent VLAN Learning
  - Support insert, remove tag
  - Support VLAN priority remarking
- Support STP, RSTP and MSTP
- Support port-based access control
- Supports rate control(WFQ)
  - In/Out port rate control
  - Traffic Policy
- Interrupt Pin
- Support special tag and QinQ header
- Support Link quality LED for 100Mbps
- Support direct LED
- Built in Linear regulator control register
- **Support auto power saving mode**
- 0.16um, 68-pin QFN Lead Free package

General Description

IP175LLF integrates a 5-port switch controller, SSRAM, and 4 10/100 Ethernet transceivers. Each of the transceivers compliers with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The DSP approach is utilized for designing transceivers with 0.16um technology; they have high noise immunity and robust performance.

IP175LLF operates in store and forward mode. IP175LLF have a lot of rich feature for different application, include router application, firewall, IEEE 802.1Q, IGMP snooping, policy-based QoS. It provides powerful QoS function, include traffic policy, traffic meter, and flexible queue scheduling (WRR/WFQ/SP). In virtual LAN, IP175LLF support port-based VLAN and IEEE 802.1Q tag-tagged VLAN (up to 16 VLAN groups).

IP175LLF support up to 2K MAC addresses, up to 16 VLANs and up to 8 Multi-Field entries. These tables are accessible through MII register. The address table can configure either “2K unicast addresses” or “1K unicast addresses and 1K multicast addresses“. The Multi-Field classification is powerful classifier (layer2 to layer 4 packet headers) in packet classification. The classifier divides incoming packets into multiple classes based on prescribed rules. Each traffic class from classifier can drop out-of-profile packets, monitor traffic, specify forwarding behavior, and specify output queue.

Beside a 5-port switch application, IP175LLF supports one MII/RMII ports for router application. The external MAC can monitor or configure IP175LLF by accessing MII registers through SMI0.

MII/RMII port also can be configured to be MAC mode. It is used to interface an external PHY to work as 4+1 switch.

Table of Contents

Revision History

Revision #	Change Description
IP175LLF-DS-R01	Initial release
IP175LLF-DS-R01.1	1) Modify band gap resister from 6.19k ohm to 5.9k ohm on page 16. 2) Change the package type from 68-PIN PQFP to 68-PIN QFN.
IP175LLF-DS-R01.2	Modify Absolute Maximum Rating on page 104
IP175LLF-DS-R01.3	1) Add CRS0 description on page 18. 2) Remove P4EXT.
IP175LLF-DS-R01.4	Remove serial and dual colcor LED mode on page 1 and 34.
IP175LLF-DS-R01.5	1) Modify the RMII circuit diagram on page 23. 2) Modify the application of SMI on page 36. 3) Modify LED control register on page 66. 4) Modify the default value of MII0_RMII_EN on page 69. 5) Modify the default value of IGMP on page 61 and 71.
IP175LLF-DS-R01.6	Modify the package dimension (D2/E2) on page 111 and 112.
IP175LLF-DS-R01.7	Modify IP175L to IP175LLF.
IP175LLF-DS-R01.8	Add PHY5 description on page 37 to 48.
IP175LLF-DS-R02	1) Modify the router application diagram on page 8. 2) Modify MII description on page 1 and 23.
IP175LLF-DS-R03	Add IP175LLFI information on page 1, 107, 108 and 114.
IP175LLF-DS-R04	1) Modify phy 25.12[15:0] register (default value 16'd22 → 16'h0016) 2) Modify phy 25.13[15:0] register (default value 16'd443 → 16'h01BB) 3) Modify phy 25.14[15:0] register (default value 16'd3389 → 16'h0D3D) 4) Modify phy 25.15[15:0] register (default value 16'd6000 → 16'h1770) 5) Modify phy 25.16[15:0] register (default value 16'd23 → 16'h0017) 6) Modify phy 25.17[15:0] register (default value 16'd23 → 16'h0017) 7) Modify phy 25.18[15:0] register (default value 16'd5800 → 16'h16A8) 8) Modify phy 25.19[15:0] register (default value 16'd5800 → 16'h16A8) 9) Remove "This bit does not affect MII1 port".

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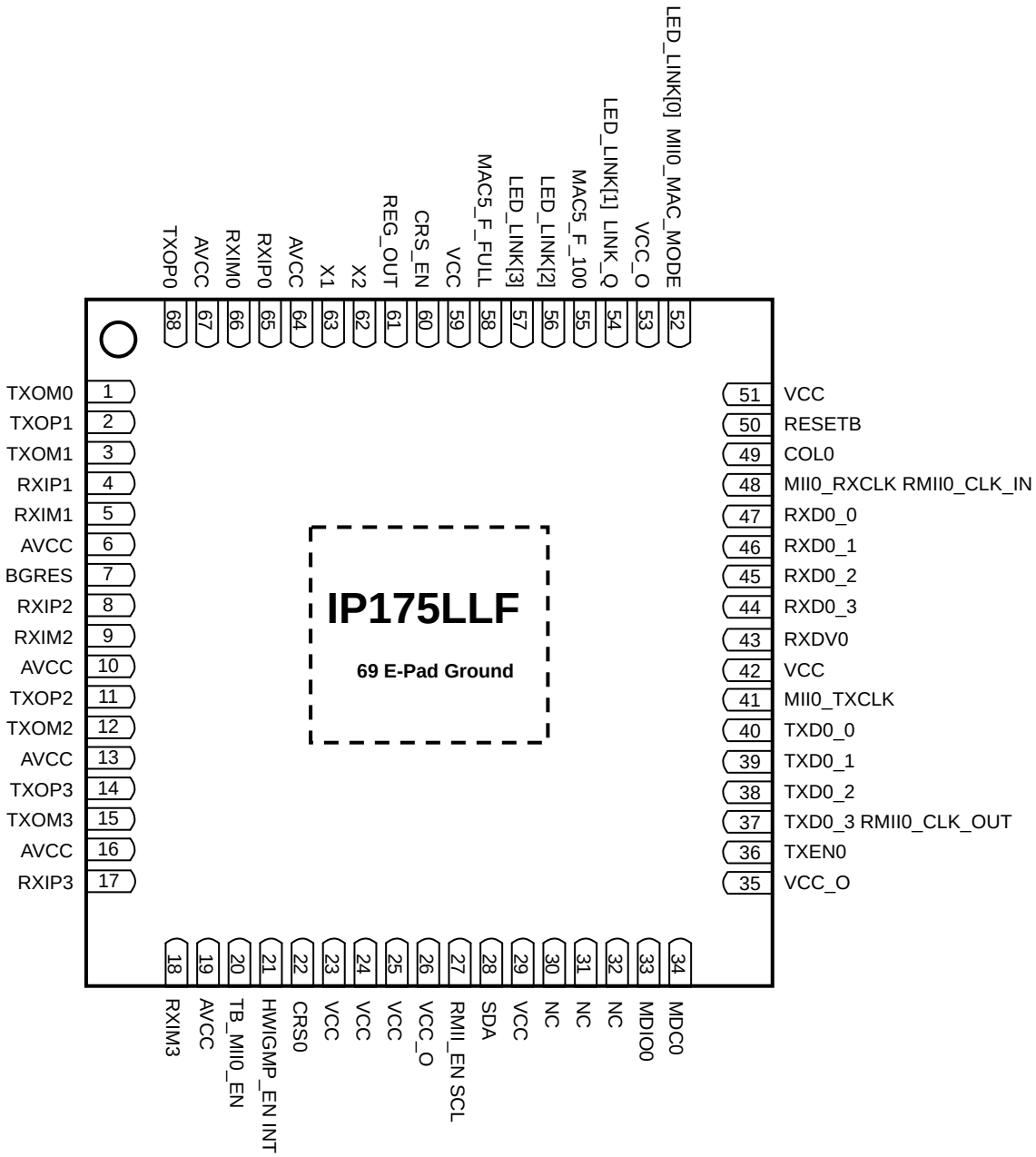
Comparison Table between IP175D and IP175LLF

Product Name	IP175D	IP175LLF
Package Type	128pin PQFP	68pin QFN
Major Block	MAC/6ports+PHY/5ports	MAC/5ports+PHY/4ports
Features	Same as IP175LLF	Same as IP175D

1 Pin Diagram

1.1 IP175LLF Pin diagram (QFN68)

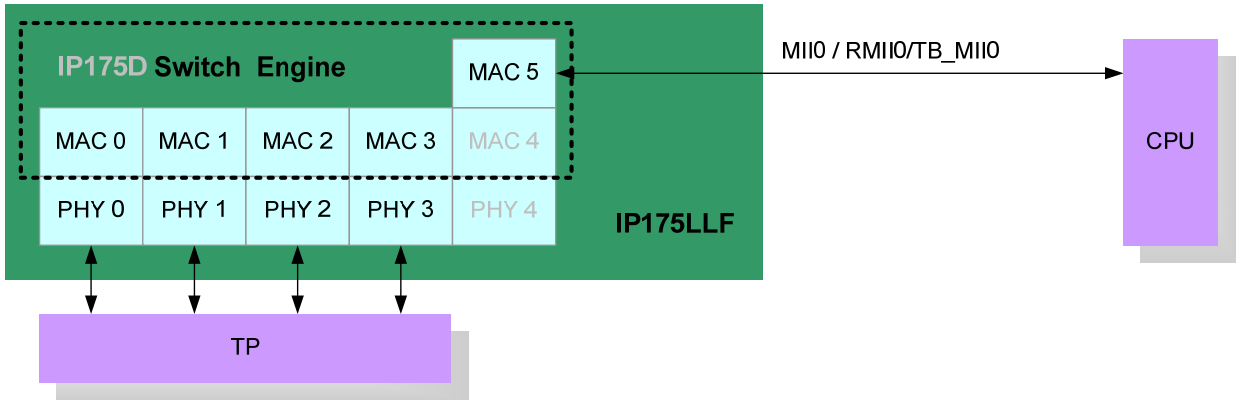
(8mm X 8mm Top view)



Exposed pad (pad 69) is system GND, must be soldered to PCB ground plane

Figure 1 Pin Diagram (IP175LLF)

Router application using one MII/RMII port
(can be configured to 3LAN+1WAN, 2LAN+2WAN, 1LAN+3WAN)



2 Pin Description

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with internal pull low 140k ohm
IPH	Input pin with internal pull high 222k ohm

Type	Description
IPL1	Input pin with internal pull low 31.6k ohm
IPH1	Input pin with internal pull high 31.6k ohm
IPL2	Input pin with internal pull low 140k ohm
IPH2	Input pin with internal pull high 222k ohm

Pin No.	Label	Type	Description
Analog			
61	REG_OUT	O	Regulator output. The internal linear regulator uses this pin to control external transistor to generates a voltage source between 1.85v ~ 2.05v. IP175LLF uses the DVCC/AVCC as feedback voltage.

Pin description **(continued)**

Pin No.	Label	Type	Description
LED pins used as initial setting (the setting is latched at the end of reset)			
54	LINK_Q	IPH1	Link quality 1: enable (default) 0: disable When the function is enabled, besides link on/off status, activity status, link LED shows link quality. The link LED will be flash (on: 2sec / off: 2sec) when the SNR of received signal is lower than the desired value for normal operation.

Pin description (continued)

Pin No.	Label	Type	Description
Initial setting			
20	TB_MII0_EN	IPL	Turbo MII0 mode enable (pin setting only) When Turbo MII0 mode enable, MII0CLK speed can be changed by programming MII register 21.22[2]. (50MHz or 31.25MHz) 1:enable 0:disable (default)
21	HWIGMP_EN	IPL2	Hardware IGMP enable 1:enable 0:disable (default)
60	CRS_EN	IPL	CRS pin enable for external MII mode 1:enable 0:disable (default)

Pin description (continued)

Pin No.	Label	Type	Description
External MII port setting (the setting is latched at the end of reset)			
27	RMII_EN	IPL2	RMII enable for all MII ports. 1: All MII/RMII interfaces work in RMII mode 0: All MII/RMII interfaces work in MII mode (default).
52	MII0_MAC_MOD	IPL1	External MII0 port MAC mode MII0 is connected to MAC5 of IP175LLF. 1: MII0 works as a MAC and should be connected to an external PHY. 0: MII0 works as a PHY and should be connected to an external MAC device (default).

Pin description (continued)

Pin No.	Label	Type	Description
External MII0 interface (PHY mode, MII0_MAC_MOD=0)			
48	MII0_RXCLK	O	MII receive clock MII0_RXCLK and MII0_TXCLK are the same clock source and in phase.
41	MII0_TXCLK	O	MII transmit clock
40, 39, 38, 37	TXD0_0, TXD0_1, TXD0_2, TXD0_3	I	MII transmit data It is sampled at the rising edge of MII0_TXCLK.
36	TXEN0	I	MII transmit enable It is used to frame TXD0[3:0]. It is sampled at the rising edge of MII0_TXCLK.
49	COL0	O	MII collision It is active when MII0 is half duplex and a collision event happens.
43	RXDV0	O	MII receive data valid It is used to frame RXD0[3:0]. It is sent out at the falling edge of MII0_RXCLK.
47, 46, 45, 44	RXD0_0, RXD0_1, RXD0_2, RXD0_3	O	MII receive data It is sent out at the falling edge of MII0_RXCLK.

Pin description (continued)

Pin No.	Label	Type	Description
External MII0 interface (MAC mode, MII0_MAC_MOD=1)			
41	MII0_TXCLK	I	MII transmit clock It is an input clock and it is connected to MII_TXCLK of external PHY.
40, 39, 38, 37	TXD0_0, TXD0_1, TXD0_2, TXD0_3	O	MII transmit data It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII0_TXCLK.
36	TXEN0	O	MII transmit enable It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII0_TXCLK.
49	COL0	I	MII collision It is an input signal and is connected to the MII_COL of external PHY.
43	RXDV0	I	MII receive data valid It is an input signal and is connected to the MII_RXDV of external PHY. RXDV0 is used to frame RXD0[3:0].
47, 46, 45, 44	RXD0_0, RXD0_1, RXD0_2, RXD0_3	I	Receive data It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII0_RXCLK.
48	MII0_RXCLK	I	MII receive clock

Pin description (continued)

Pin No.	Label	Type	Description
External RMII0 interface (RMII_EN=1)			
47, 46	RXD0_0, RXD0_1	I	RMII receive data It is connected RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC.
43	RXDV0	I	RMII receive data valid It is connected RMII_RXDV of external PHY or RMII_TXEN of external MAC.
40, 39	TXD0_0, TXD0_1	O	RMII transmit data It is connected RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY.
36	TXEN0	O	RMII transmit enable It is connected RMII_RXDV of external MAC or RMII_TXEN of external PHY.
37	RMII0_CLK_OUT	O	A 50Mhz reference clock output for other RMII devices
48	RMII0_CLK_IN	I	50Mhz RMII reference clock input

Pin description (continued)

Pin No.	Label	Type	Description
Force mode (the setting is latched at the end of reset)			
55	MAC5_F_100	IPL1	Force MAC5 work at 100M or 10M. 1: force 100M 0: force 10M (default)

Pin description (continued)

Pin No.	Label	Type	Description
Force mode (the setting is latched at the end of reset)			
58	MAC5_F_FULL	IPL1	Force MAC5 at full duplex or half duplex 1: force full duplex 0: force half duplex (default)

Pin description (continued)

Pin No.	Label	Type	Description
Transceiver			
65, 66, 4, 5, 8, 9, 17, 18	RXIP0, RXIM0, RXIP1, RXIM1, RXIP2, RXIM2, RXIP3, RXIM3	I	TP receive
68, 1, 2, 3, 11, 12, 14, 15,	TXOP0, TXOM0, TXOP1, TXOM1, TXOP2, TXOM2, TXOP3, TXOM3	O	TP transmit
7	BGRES	O	Band gap resister. It is connected to GND through a 5.9 k ohm resistor. Please refer to application circuit for more information.

Pin description (continued)

Pin No.	Label	Type	Description
Misc.			
63	X1	I	System clock input or crystal input It is recommended to connect X1 and X2 to a crystal. If the clock source is from another chip, the clock should be active at least for 1ms before pin 50 RESETB de-asserted.
62	X2	O	Crystal output
50	RESETB	I	Reset, low active
22	CRS0	IPL	Carrier sense of MII0 (home plug application) It is valid only if CRS_EN is pull high It is an input signal and is connected to MII_CRS of external PHY.
21	INT	IPL2/ O	Interrupt output It can be either active low or high by writing MII register 21.20[15]
EEPROM (only 24C02, 24C04, 24C08 & 24C16 supported)			
27	SCL	IPL2/ O	After reset, it is used as clock pin SCL of EEPROM. Its period is longer than 10us. IP175LLF stops reading EEPROM if it finds there is no 55AA pattern in address 0. After reading EEPROM, this pin becomes an input pin.
28	SDA	IPH2/ O	After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin. It is pulled up in EEPROM application circuit.
SMI			
34, 33	MDC0, MDIO0	IPL, IPL2	SMI0 The external MAC device uses the interface to access IP175LLF's MII registers.

Pin description **(continued)**

Pin No.	Label	Type	Description
LED			
57, 56, 54, 52	LED_LINK[3:0]	O	Link, Activity (output after reset) LED mode0: 100M Link + Activity (same as mode 2) LED mode1: LED mode2, 100M Link + Activity (1: 100M Link fail, 0: 100M Link ok and no activity, flash: 100M Link ok and TX/RX activity) LED mode3: Link + Activity (1: link fail, 0: link ok, flash: Link ok and TX/ RX activity)

Pin description **(continued)**

Pin No.	Label	Type	Description
Power			
26, 35, 53	VCC_O		3.3V PAD power
6, 10, 13, 16,19,64, 67	AVCC		1.9v Analog power
23,24,25, 29,42,51 59	VCC		1.9v Core power

3 Function Description

3.1 Flow Control

IP175LLF supports the standard 802.3X flow control frames on both transmit and receive sides. On the receive side, if IP175LLF receives a pause control frame, the IP175LLF will defer transmitting next normal frame; on the transmit side, IP175LLF issues pause control frame to remote station when the output of the destination port is overflowed. The source address (SA) of pause control frame will be {IP175LLF OUI (0090C3), port number}. For example, the SA of port 1 pause control frame will be " 00 90 C3 00 00 01".

When CoS is enabled, IP175LLF may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives the highest priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

IP175LLF's PHY 0~4 MII register 4.10 can not use to set flow control ability for each port. The flow control function can be only enabled by programming MII register 20.5[1].

3.2 Broadcast Storm Protection

A port of IP175LLF begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 20.17~20.19 bq_stm_thr_sel [1:0] in 10ms (100Mbps) or 100ms (10Mbps).
The function can be enabled by programming MII register 20.16[13:8].

3.3 Rate Control

The rate control is provided by applying to port rate control, Multi-Field traffic policy and WFQ scheduling. IP175LLF use token bucket to measure the traffic to against the traffic profile. The traffic profile is a predefine traffic rate which contain three parameters: timing interval[1], credit size and burst size. User can configure desired rate from MII register 21.8-12, except for Multi-Field traffic policy. Configuring rate parameter of Multi-Field traffic policy is from MII register 26.16-17. When the rate has been configured, the meter measure the traffic and then against its predefined traffic profile. Switch passes in-of-profile packets and drop (or shape) out-of-profile packets in ingress (or egress).

[1] In ingress port rate control and Multi-Field traffic policy, timing interval parameter is fixed to 1ms.

The rate control equation that used in IP175LLF is illustrated below:

$$\text{TX or TX output queue number bandwidth (Byte per second)} = \frac{\text{credit\_size (byte)}}{\text{ti x 1ms}}$$

$$\text{RX or Multi-Field table ingress QoS bandwidth (Byte per second)} = \frac{\text{credit\_size (byte)}}{\text{1ms}}$$

MBS: max burst size is use as a compensation buffer during idle period.

TX or TX output queue: bw_mbs must be greater than bw_credit_size and max_packet_length
(bw_mbs > bw_credit_size and bw_mbs > max_packet_length)

RX or Multi-Field table ingress QoS : bw_mbs equal to bw_credit_size
(bw_mbs = bw_credit_size)

CREDIT_SIZE: credit size that will add into bucket per time interval

TI: time interval (unit 1ms)

Example: TX Bandwidth 256kbps (max_packet_length = 1518 byte = 16'h05EE)

$$256\text{kbps} = 32\text{kBps} = \frac{32}{1\text{x}1\text{ms}}$$

1. bw_credit_size[15:0] = 16'h0020
2. bw_mbs[15:0] = 16'h0020
3. bw_ti[6:0] = 7'h01

Example: RX Bandwidth 512kbps (max_packet_length = 1518 byte = 16'h05EE)

$$512\text{kbps} = 64\text{kBps} = \frac{64}{1\text{ms}}$$

1. bw_credit_size[15:0] = 16'h0040
2. bw_mbs[15:0] = 16'h0040

3.4 External MII

IP175LLF provides the ability of the connection to an external MAC or PHY. MII0 interface can be configured MAC mode or PHY mode without modify layout. In addition to be compatible with IEEE 802.3 MII interface, the interface also can configure RMII.

3.4.1 To define the speed, duplex and pause of MII port

MII interface can be configured as either MAC mode or PHY mode. In MAC mode and PHY mode, the MII port's speed, duplex and pause ability can set through pin, EEPROM or MII register.

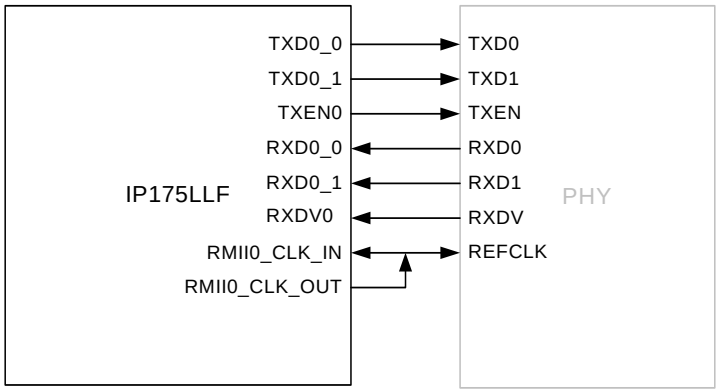
	Pin	EEPROM		MII register		
		Name	Reg	Name	Phy	Reg
MII0 speed	MAC5_F_100	MAC5_FORCE_100	2.7	MAC5_FORCE_100	20	4.15
MII0 duplex	MAC5_F_FULL	MAC5_FORCE_FULL	2.5	MAC5_FORCE_FULL	20	4.13
MII0 pause	--	MAC_X_EN	3.0	MAC_X_EN	20	5.0

3.4.2 The Application Circuit of RMII

(RMII_EN=1)

When RMII mode is enabled, IP175LLF supports reference clock RMII_CLK_OUT for each RMII port. The clock is used by the external PHY (or MAC) and IP175LLF itself.

The following circuit diagram is the RMII circuit of MII0.



3.5 Virtual LAN (VLAN)

IP175LLF is a VLAN aware-switch and support two classification rule: port-based VLAN and tag-based VLAN. Each port can configure its classification rule respectively. In tag-based VLAN the switch supports up to 16 VLAN groups. Two ingress VLAN rule and egress VLAN rule are provided. The ingress VLAN rule is used to discard packet that violate this rule. The egress rule checks VLAN member set and performs the determination of tagging or un-tagging. In learning process the switch supports shared and independent VLAN learning.

The VLAN table contains a set of match condition and their actions. Entry 0-5 firstly reserved for port-based VLAN if the corresponding port is set to port-based VLAN. For instance port 0 is set to port-based VLAN classification and then entry 0 is reserved for port 0. In port-based VLAN the match condition does not care and it is only used for tag-based VLAN. The context of VLAN table is placed in MII register 22.11-29 and 23.0-31.

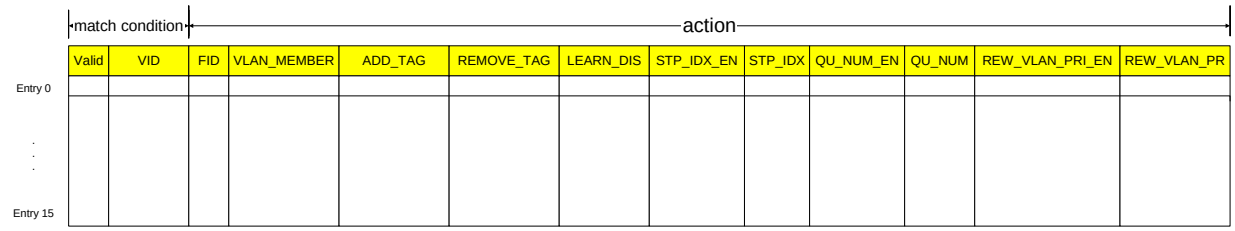


Figure 3-1 VLAN table

3.5.1 Port-based VLAN

If any packet is received by a given port, the switch will perform VLAN table searching. User can use the VLAN Classification Register to set VLAN classification rule on each port. In port-based VLAN classification, frame is classified based on the port which it arrive. Once a port configures port-based VLAN, it will occupy the corresponding VLAN entry.

3.5.2 Tag-based VLAN

In tag-based VLAN classification two modes are provided for applying VLAN classification: using VID to classify VLAN and using PVID to classify VLAN. Using VID to classify VLAN, VID searching is performed according to frame's VID. If any packets carrier no VID information, the VID searching is performed using PVID. In using PVID to classify VLAN the PVID for a given port is used for VID searching, whether VLAN tagged or untagged frames are received on this port.

3.5.3 VLAN Ingress Filtering

IP175LLF specify a VLAN ingress rule in MII register 22.1. Any frames received on a port are discarded if it violates this rule.

3.5.4 Shared and Independent VLAN Learning

The learning process supports shared and independent VLAN learning. In shared VLAN learning rule the learning information from a VLAN can make used by the others VLANs. In independent VLAN learning rule the learning information from a VLAN makes use only itself. This standard was specified in IEEE 802.1Q.

3.5.5 The determination of the requirement to insert or remove tag

IP175LLF supports the ability of insertion and removal tag header. User can configure the set of ports that add or remove tag header for each VLAN through MII register 23.8-23. Table 1 is a combination of frame type and transmission port type.

Frame type of the received packet	The operation of a port which forwards the packet	
	Forward to a untagged filed	Forward to a tagged field
Untagged	Forward the packet without modification	Insert a tag using the default VLAN tag value of the source port
Priority-tagged (VLAN ID=0)	Strip tag	Only Replace the VID with PVID of the source port
VLAN-tagged	Strip tag	Forward the packet without modification

Table 1 Determination of insertion and removal tag

3.6 Quality of Service (QoS)

IP175LLF uses a combination of traffic policy, priority classification and output queue scheduling to achieve policy-based QoS. Since current internet carrier different type services, such as file transfer, email, video, voice and Web. Because the switch offers a limited resource, it can not assure any resource guarantees to applications or users. Traffic policy can aggregate traffic flow and police against its traffic profile. This way can restrain the traffics from entering the switch effectively. Finally, packets will place into appropriate output queue based on priority classification.

3.6.1 Traffic Policy

In IP175LLF traffic policy is a consisting of classifier, meter and dropper. The classifier separate received packets into different traffic stream based on matched condition. IP175LLF provides 8 Multi-Field entries, each entry is a combination of one or more layer 2-4 header. Multi-Field classification can classify packets into traffic classes and traffic flows. For instance an end-to-end flow is recognized using five-tuple. Each Multi-Field contains a meter for measuring the traffic. The meter passes the in-of-profile packets for forwarding and put out-of-profile packets into dropper for dropping. User can configure the parameters of traffic policy from MII register 26.0-23.

Each entry associated with Multi-Field counter is in order to monitor traffic rate by user (or CPU). The counter value is represented in byte units. The user (or CPU) can monitor the traffic rate to periodically read the value of multi-field counter through MII register.

3.6.2 Priority Classification

Priority classification is used to separate packets into four priority levels. In IP175LLF packet classification can categorize packets based on port-based classification and frame-based classification. Port-based classification, packets coming from the same port have a fixed priority level. Frame-based classification, frame categorization is based on one header filed or a combination of more header fields. In frame-based classification has a flexible packet classification to classify priority level and the following header fields are provided by determining the priority.

- Special tag
- Source MAC address
- Destination MAC address
- VID
- VLAN priority
- IPv4 ToS/IPv6 DSCP
- TCP/UDP logical port
- Layer 2-4 Multi-Field

Figure 3-2 illustrates the priority classification flow chart.

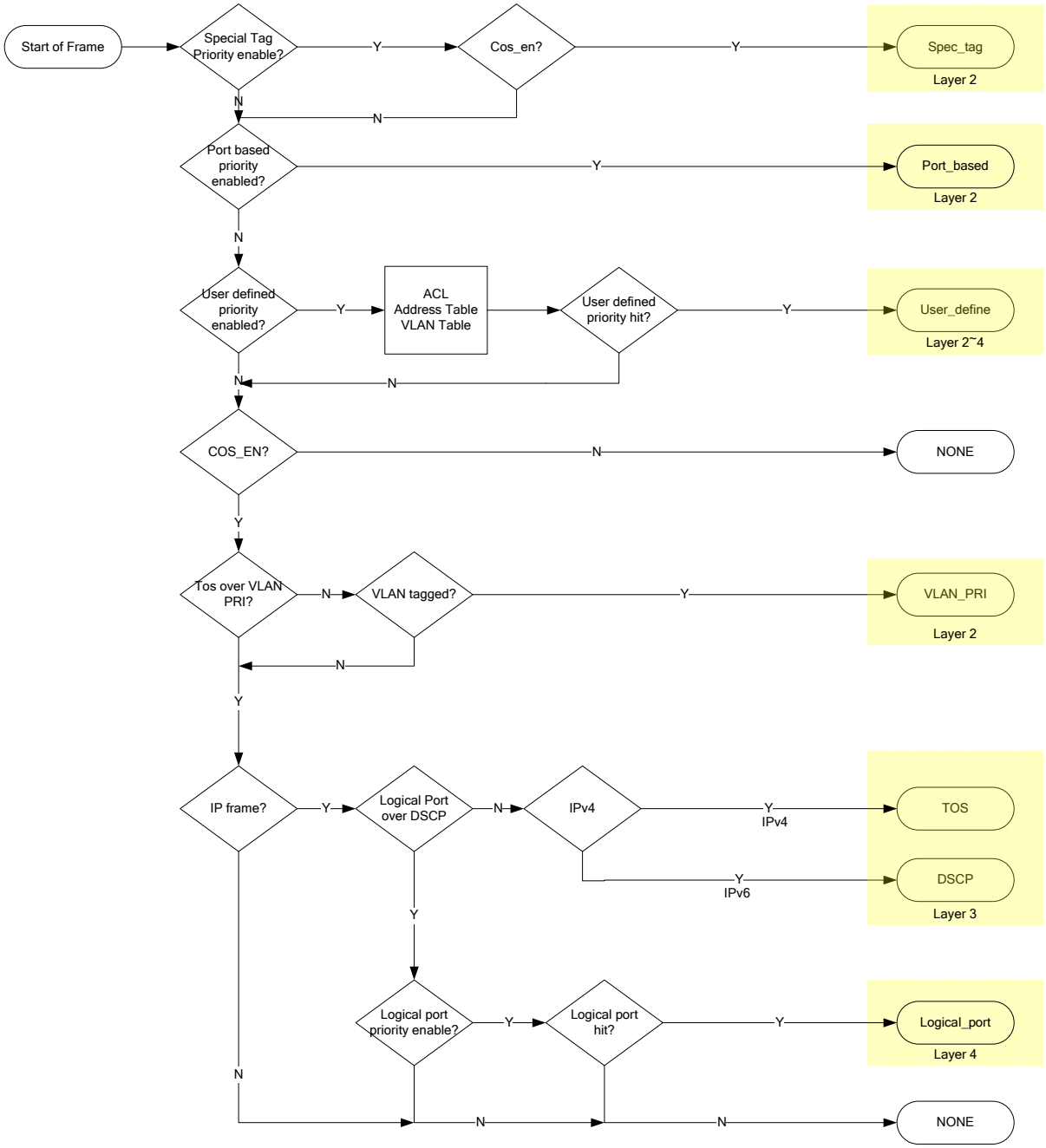


Figure 3-2 Priority classification flow chart

3.6.3 Output Queue Scheduling

IP175LLF support four scheduling modes and list in Table 2.

Mode #	Q3	Q2	Q1	Q0
Mode 0	WRR	WRR	WRR	WRR
Mode 1	WFQ	WFQ	WFQ	WFQ(BE)
Mode 2	SP	WFQ	WFQ	BE
Mode 3	SP	SP	SP	SP

SP: Strictly Priority; WRR: Weight Round Robin; WFQ: Weight Fair Queuing; BE: Best Effort

Table 2 Queue scheduling

SP:
In strictly priority, the packets in a queue will go first till its queue is empty.
WRR:
User can control the number of packet transmission on an output queue by setting its weight.
WFQ:
User can allocate a bandwidth on an output queue by setting its rate. Configuring WFQ bandwidth can be through MII register 21.8-12.

3.7 Port mirror

There are some circumstances that the network administrator requires to monitor the network status. The port mirroring function can help the network administrator diagnose the network.

A port mirroring function can be accomplished by assigning a monitored port and a snooping port. The IP175LLF supports four kinds of monitoring methods: source port, destination port, one port of source and destination, source-destination pair. This function can be enabled by programming the corresponding bit in MII registers 20.20~20.21.

In addition to monitor a physical port, it can monitor traffic based on layer 2-4 Multi-Field packet header or MAC address

3.8 Layer 2-4 Multi-Field Classification

IP175LLF support 8 Multi-Field entries. The Multi-Field table consists of a set of classification rules and actions. This Multi-Field classification is a combination of one or more layer 2-4 packet header. The classifier can classify incoming traffic to traffic class and traffic flow. The traffic class is a collection with the same conditions. For example the classifier aggregates a collection of packet with the same DSCP. Traffic flow can identify end-to-end traffic flow by using five-tuple (source IP, destination IP, protocol, source port and destination port).

When packets are received by a port, the switch will search Multi-Field table. If incoming packets match a predefined Multi-Field entry, the corresponding action is performed. The action consists of six parameters: drop packet, limits incoming traffic bandwidth, monitor traffic bandwidth, forward to CPU, copy to mirror port and queue number assignment. It is possible to match multiple entries for an incoming packet and then the first matching entry is effective.

Each entry includes a counter called Multi-Field counter. This counter is useful for monitoring propose. A counter keeps track of the number of bytes match predefined Multi-Filed condition. User also can periodically read a Multi-Field to monitor a specific traffic rate.

3.9 MAC Address Table

IP175LLF support 2K MAC addresses. The address table can configure either 2K unicast address or 1K unicast address/1K multicast address. The multicast table occupies the MAC table from 0x400 to 0x7FF if the AT_STR bit (reg 20.13.3) set to high. The MAC table is organized as hash table which consist of 512

buckets with four entries in each bucket. Each bucket is located through its respective hash key, calculated from MAC and FID by using XOR algorithm. It is possible that multiple MAC addresses index to the same bucket, term as collision. IP175LLF provides four entries within each buck for reducing collision rate. Finally, the 11-bit hash index mapping to MAC table consist of three parameters: multicast address bit, hash key and entry number. The MSB of hash index distinguishes multicast address from MAC addresses. The least two significant bit in hash index indicates entry number. The other bit is hash key which calculated from MAC and FID using XOR algorithm. In IP175LLF the formula of hash index is computed based on table structure. The user can set AT_STR bit to configure table structure. The 11-bit hash index is computed as following:

AT_STR=0 (2K unicast table)
Hash Index = { XOR({2'b00,FID,MAC[47:45]}, MAC[44:36], MAC[35:27], MAC[26:18], MAC[17:9], MAC[8:0]), Entry Number }
AT_STR=1 (1K unicast table and 1K multicast table)
Hash Index = {Multicast Address Bit, XOR({4'h0,FID}, MAC[47:40], MAC[39:32], MAC[31:24], MAC[23:16], MAC[15:8], MAC[7:0]), Entry Number }

3.9.1 Entry Content

Entry content in MAC table contains the forwarding information for a specific MAC address. This table content is automatically updated by learning process and can directly access from the CPU through Address Table Access register (see MII register 21.14-19).

The contents are described in Table 3, Table 4 and Table 5.

MII Register	Name	Description
21.15	MAC_ADDR[15:0]	MAC address[15:0]
21.16	MAC_ADDR[31:16]	MAC address[31:16]
21.17	MAC_ADDR[47:32]	MAC address[47:32]
21.18[15:14]	FILTER_INFO	Filter information: - 2'b00: reserved - 2'b01: discard frame if frame's SMAC match MAC address - 2'b10: ignore VLAN member set - 2'b11: copy frame to mirror port if frame's DMAC match MAC address
21.18[13:10]	PRI_INFO	Priority information: To assign queue number for frames with match MAC table entry. The information is divided two parts: match condition and its action. **Match Condition (21.18[13:12]):** - 2'b00: reserved - 2'b01: match DMAC (Destination MAC Address) - 2'b10: match SMAC (Source MAC Address) - 2'b11: match DMAC or SMAC **Action (21.18[11:10]):** - Assign to Queue 0 - Assign to Queue 1 - Assign to Queue 2 - Assign to Queue 3
21.18[9:6]	FID	4-bit FID
21.18[5:3]	PORT_ID	Port ID: - 3'b000: discard frame if frame's DMAC match MAC address - 3'b001- 3'b110: port ID - 3'b111: reserved
21.18[2:0]	AGE	Age time: If this field is set all zero, it indicates the corresponding

		entry is aged out. It means entry is invalid.
21.19.0	Reserved	Reserved
21.19.1	STATIC	Static entry: this entry is not aged out by aging process or overwritten by learning process

Table 3 Entry content for unicast MAC address

MII Register	Name	Description
21.15	MAC_ADDR[15:0]	MAC address[15:0]
21.16	MAC_ADDR[31:16]	MAC address[31:16]
21.17	MAC_ADDR[47:32]	MAC address[47:32]
21.18[15:14]	FILTER_INFO	Filter information: - 2'b00: reserved - 2'b01: discard frame if frame's SMAC match MAC address - 2'b10: ignore VLAN member set - 2'b11: copy frame to mirror port if frame's DMAC match MAC address
21.18[13:10]	PRI_INFO	Priority information: To assign queue number for frames with match MAC table entry. The information is divided two parts: match condition and its action. **Match Condition (21.18[13:12]):** - 2'b00: reserved - 2'b01: match DMAC (Destination MAC Address) - 2'b10: match SMAC (Source MAC Address) - 2'b11: match DMAC or SMAC **Action (21.18[11:10]):** - Assign to Queue 0 - Assign to Queue 1 - Assign to Queue 2 - Assign to Queue 3
21.18[9:6]	FID	4-bit FID
21.18[5:0]	PORT_MAP	Port Map: - 0x00: discard frame if frame's DMAC match MAC address - 0x01 to 0x3F: destination port map
21.19.0	IGMP	IGMP entry indicator: This bit shall set to zero
21.19.1	Valid	Entry is valid

Table 4 Entry content for multicast MAC address

MII Register	Name	Description
21.15	MAC_ADDR[15:0]	MAC address[15:0]
21.16[6:0]	MAC_ADDR[22:16]	MAC address[22:16]
21.16.7	MAC_ADDR[23]	This bit shall be set to zero
21.16[10:8]	TIMEOUT_P0	Port 0 timeout: If this field is set all zero, it indicates the corresponding port is timeout.
21.16[13:11]	TIMEOUT_P1	Port 1 timeout
{21.17.0, 21.16[15:14]}	TIMEOUT_P2	Port 2 timeout
21.17[3:1]	TIMEOUT_P3	Port 3 timeout
21.17[6:4]	Reserved	Reserved
21.17[9:7]	TIMEOUT_P5	Port 5 timeout
21.17[15:0]	Reserved	Reserved
21.18[15:14]	FILTER_INFO	Filter information:

		- 2'b00: reserved - 2'b01: discard frame if frame's SMAC match MAC address - 2'b10: ignore VLAN member set - 2'b11: copy frame to mirror port if frame's DMAC match MAC address
21.18[13:10]	PRI_INFO	Priority information: To assign queue number for frames with match MAC table entry. The information is divided two parts: match condition and its action. **Match Condition (21.18[13:12]):** - 2'b00: reserved - 2'b01: match DMAC (Destination MAC Address) - 2'b10: match SMAC (Source MAC Address) - 2'b11: match DMAC or SMAC **Action (21.18[11:10]):** - Assign to Queue 0 - Assign to Queue 1 - Assign to Queue 2 - Assign to Queue 3
21.18[9:6]	FID	4-bit FID
21.18[5:0]	PORT_MAP	Port Map: - 0x00: discard frame if frame's DMAC match MAC address - 0x01 to 0x3F: destination port map
21.19.0	IGMP	IGMP entry indicator: This bit shall set to one
21.19.1	Valid	Entry is valid

Table 5 Entry content for IP multicast address

3.9.2 Accessing MAC Table

The MAC table can be accessed by through MII register 21.14-19. IP175LLF provides two access commands: single read and single write. A single read or write transfer only executes a single I/O operation and user only can access a particular memory address. When a given MAC+FID read from (or write to) MAC table, the MAC+FID is used to compute hash index for mapping to MAC table.

Single Read

The single read process is described as following steps:

Step 1 – Set hash index in reg 21.14[10:0]
Step 2 – Set single read command in reg 21.14[12:11]
Step 3 – Set START bit in reg 21.14.15 to initiate read command
Step 4 – check DATA_VALID bit in reg 21.14.13 to determine if data is valid. If this bit is set to high, enter to step 5
Step 5 – read data from data buffer register (reg 21.15-19). User must read data buffer register from reg 21.15 to reg 21.19 in regular order.

Single Write

The single write process is described as following steps:

Step 1 – Write desired data to data buffer register (reg 21.15-19)
Step 2 – Set hash index in reg 21.14[10:0]
Step 3 – Set single write command in reg 21.14[12:11]
Step 4 – Set START bit in reg 21.14.15 to initiate read command

3.10 CPU Interrupt Control for loop detection

IP175LLF uses interrupt to notify CPU of loop detection status. User can decide interrupt signal is active high or low. This function can be enabled by programming the corresponding bit in MII registers 21.20[15] and 21.20[3].

3.11 IGMP Snooping

IP175LLF support IGMP v1 and v2 snooping specified in RFC 1112 and RFC 2236 respectively. Because IGMP is used between hosts and neighboring multicast routers, IP175LLF listen the IGMP message communication between router and host to establish multicast group membership. Based on the group membership information, IP175LLF forwards IP multicast data to its membership which registered in group table. For hardware IGMP snooping timeout mechanism is provided by applying the hosts silently leave a specific multicast group. “Silently Leave” means that a host does not respond to query message when it want to leaves group. Except for hardware IGMP snooping, IP175LLF also support software IGMP snooping and IGMP snooping with CPU assistance. Software IGMP snooping imply that software must handle IP multicast traffic which include IGMP packet, IP multicast control packet and IP multicast data packet and then forward it to proper output port after processing done. For IGMP snooping with CPU assistance, it separate two parts: hardware supporting and software supporting. In hardware supporting, the switch directly forward IGMP packets and IP multicast control packets to CPU for further processing. Then software must process these packets and forward to proper output port. The external CPU also must maintain the table of multicast group. When IP multicast data packet is received by a port, the switch forward it according to this table.

IP175LLF supports not only IGMP snooping but also MLD snooping. MLD snooping does not support hardware MLD snooping. It only supports software MLD and MLD snooping with CPU assistance. For MLD snooping with CPU assistance, IP175LLF trap MLD packets to CPU for further processing and then forward these packets to proper ports. CPU shall update the table of multicast group according to MLD message. When IPv6 multicast packet is coming, it will be forwarded based on this table. For software MLD snooping IP175LLF traps MLD and IPv6 multicast packet to CPU. CPU shall process these packets and forward to proper ports.

3.12 Security Filtering

IP175LLF provides flexible security configuration to protect against attacks and filter suspicious traffics. These packets can be programmed to drop or forward to CPU for further processing. The IP175LLF provides packet filtering based on physical port, MAC address, logical port and layer 2-4 Multi-Field packet headers.

3.12.1 Physical Port Filtering

A port can be disabled the forwarding and learning ability respectively. For instance a host connects to a physical port directly. The security rule is that everyone shall be authenticated by an authenticating server or administrator if he wants to access network. Administrator (or CPU) can disable forwarding and learning ability on a given port, if a host is in unauthorized state.

3.12.2 MAC Address Filtering

The feature of MAC address filtering can be configured by two ways: specific MAC address filtering and unknown MAC address filtering. Specific MAC address filtering allows to drop packets with specific either source MAC address or destination. Specific MAC address filtering can also drop packet on per VLAN group. Configuring contexts of the specific MAC address filtering is through “Address Table Access Register”. Unknown MAC address filtering only allows that packets with registered SMAC (source MAC address) can access network.

3.12.3 Logical Port Filtering

IP175LLF support discard packets based on logical port. The logical port can define a particular port

number or a range port number. If the source's logical port or the destination's logical port in the incoming packet match any of the pre-defined logical ports, the incoming frame will be discarded.

3.12.4 Layer 2-4 Multi-Field Filtering

IP175LLF support discard packets based on a combination of layer 2-4 Multi-Field packet headers.

3.13 IEEE 802.1x

IP175LLF support IEEE 802.1x security. The EAPOL is used by authentication process. EAPOL is detected by checking destination MAC address defined in 01:80:C2:00:00:03 and then trap to CPU for further processing. Eventually, CPU determines whether the port configures in authorized state or not. CPU can also determine whether the requestor is qualified or not based on source MAC address. When the switch is a VLAN-aware switch, CPU can determine whether the port (or SMAC) is placed in the authorized state per VLAN.

3.14 Spanning Tree

In IP175LLF spanning tree operation separate into software implement and hardware implement. In software implement CPU must process BPDU packet and configure the sate of each port. In hardware implement the switch trap BPDU to CPU. The following table describes how to configure the state of each port in IP175LLF.

State	Fwd BPDU packet to CPU	Fwd BPDU packet from CPU	Address learning	Fwd all packet normally	(Forward enable, Learning enable)[2]
Disable	X (note 2)	X (note 2)	X	X	(0,0)
Blocking	O	X (note 3)	X	X	(0,0)
Listening	O	O	X	X	(0,0)
Learning	O	O	O	X	(0,1)
Forwarding	O	O	O	O	(1,1)

Note1: O: enabled, X: disabled
Note2: CPU should not send packets to IP175LLF and should discard packets from IP175LLF.
Note3: CPU should not send packets to IP175LLF.

Table 6 Configuring port state

IP175LLF Support fast aging function for RSTP, User can configure the parameter from MII register 20.14[6:5] and 20.14[4:0].

IP175LLF support 4 multiple spanning tree VLAN table which contains the VLAN-dependent port state. MSTP allows users to map many VLANs to a spanning tree group, each with its own topology.

3.15 Special Tag

The purpose of special tag is:

- To allow a frame (IP175LLF to CPU) to carrier ingress port number and violation event.
- To allow a frame (CPU to switch) to indicate the output port mask and output queue number carrier in special tag header

The VLAN TPID is represented in two octets, the hexadecimal value 8100. The octets display from left to right, the left octet is 0x80 and the right octet is 0x00. Special tag information appears in the right octet whose value is not a zero.

[2] The forwarding and learning ability of each port are configured in MII register 20.6. For MSTP the forwarding and learning ability of each port are configured in MII register 24.0-3.

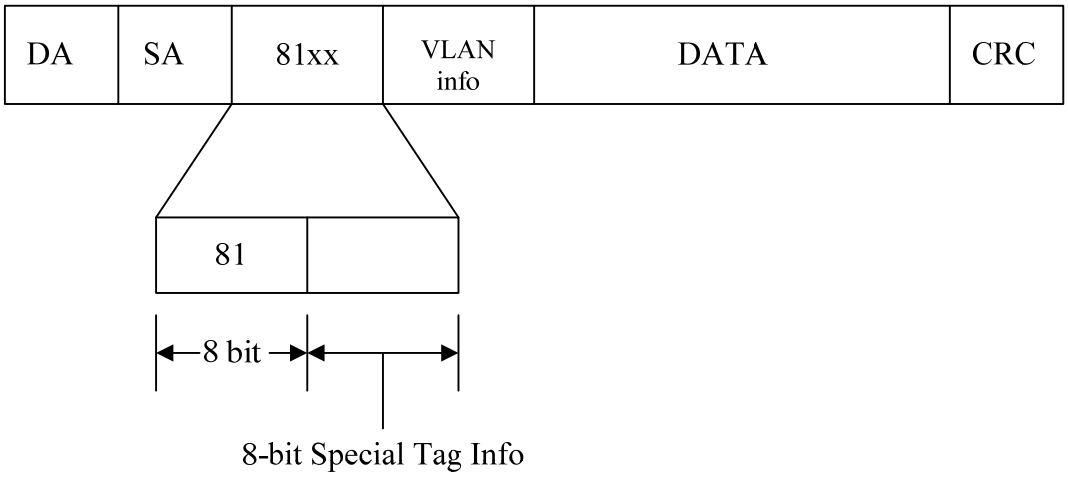


Figure 3-3 Special tag format

There are two formats of special tag, depending on the frame direction. The special tag format is defined as following.

1. Special Tag for RX (switch to CPU)

Frame direction is from switch to CPU. The special tag information consists of ingress port number and violation event. Ingress port number is where did the frame come from? Violation event is an event vector consisting of security violation, VLAN violation and miss address table.

Security violation: IP175LLF support unknown SMAC filtering and user can enable it from MII register 20.12. Unknown SMAC means source MAC address of the received frame is not found in address table. When this function is enabled, the received frames with unknown SMAC is marked “illegal SMAC”. IP175LLF discard the frame with illegal SMAC. A register bit is provided to allow this frame forward to CPU. Except to trap illegal frame to CPU, the IP175LLF also can mark this frame as security violation frame. Therefore CPU receive a frame whose security violation bit is marked, it will know source MAC address of this frame is not registered in address table.

VLAN violation: If a VLAN table searching results in a miss, this bit is set.

Miss address table: If an address table searching results in a miss, this bit is set.

Special Tagged Information	Description
Bit 7-3	Packet Information - bit 4: Reserved - bit 3: Reserved - bit 2: Miss address table - bit 1: Security violation - bit 0: VLAN violation
Bit 2-0	Ingress Port number - 3’b000: Disabled - 3’b001: Port 0 - 3’b010: Port 1 - 3’b011: Port 2 - 3’b100: Port 3 - Other: Reserved

2. Special Tag for TX (From CPU to switch)

Frame direction is from CPU to switch. This function provides for forwarding decision, priority assign and learning disable. These parameter embedded in special tag header can be set by CPU.

If the CPU transmits packet without Special Tag, the packet will be forwarded according to the mac address table.

Special Tagged Information	Description
Bit 7	0: Learn Enable 1: Learn Disable
Bit 6-5	Priority Assignment - 2'b00: Disabled - 2'b01: Queue 1 - 2'b10: Queue 2 - 2'b11: Queue 3
Bit 3-0	Output Port Mask - bit 3: port 3 - bit 2: port 2 - bit 1: port 1 - bit 0: port 0

3.16 Loop Detection

A loop detection apparatus and method for IP175LLF having a loop detection module is configured to detect a particular port receiving a loop frame indicative of a loop condition occurrence at the port. IP175LLF support auto blocking/recover rx/tx traffic of mii0 and loop port.

This function can be enabled by programming the corresponding bit in MII registers 21.20~20.21 and 27.9~27.11.

In detail, please refer to the loop detection application note.

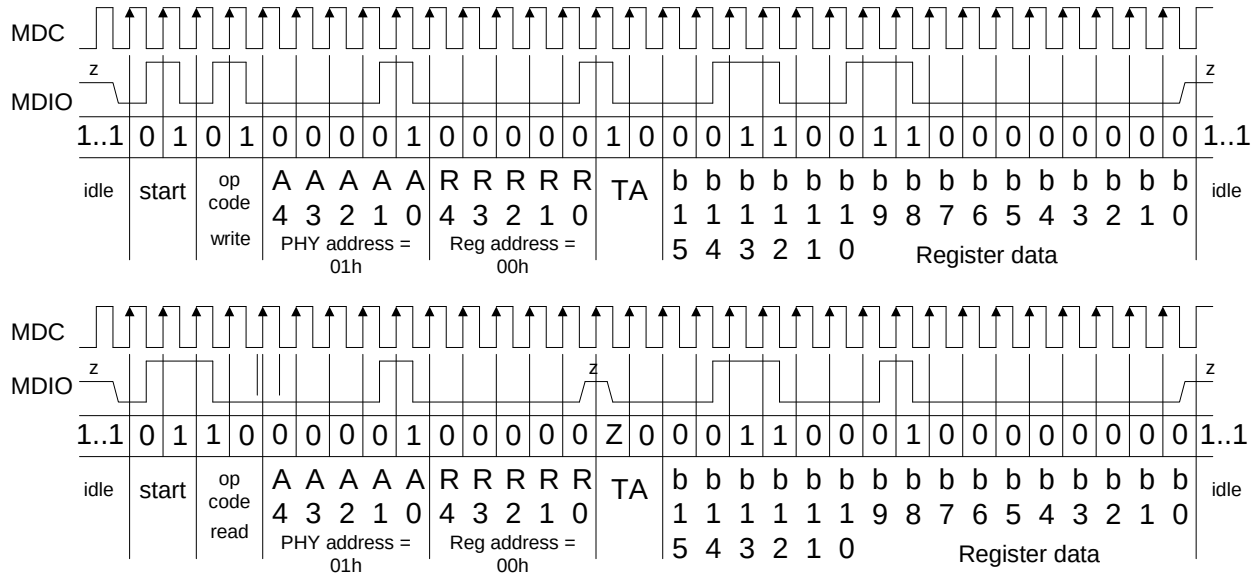
3.17 LED Blink Timing

LED mode	Blinking speed
Active led blink	On -> Off 44ms -> On 176ms -> Off 44ms …
Collision led blink	Off -> On 176ms -> Off 44ms ->On 176ms …
Link quality fail blink	On 2s -> Off 2s -> On 2s -> Off 2s …
Neon like LED(initial setup LED)	On 286ms -> Off 2s -> On 286ms -> Off 2s …

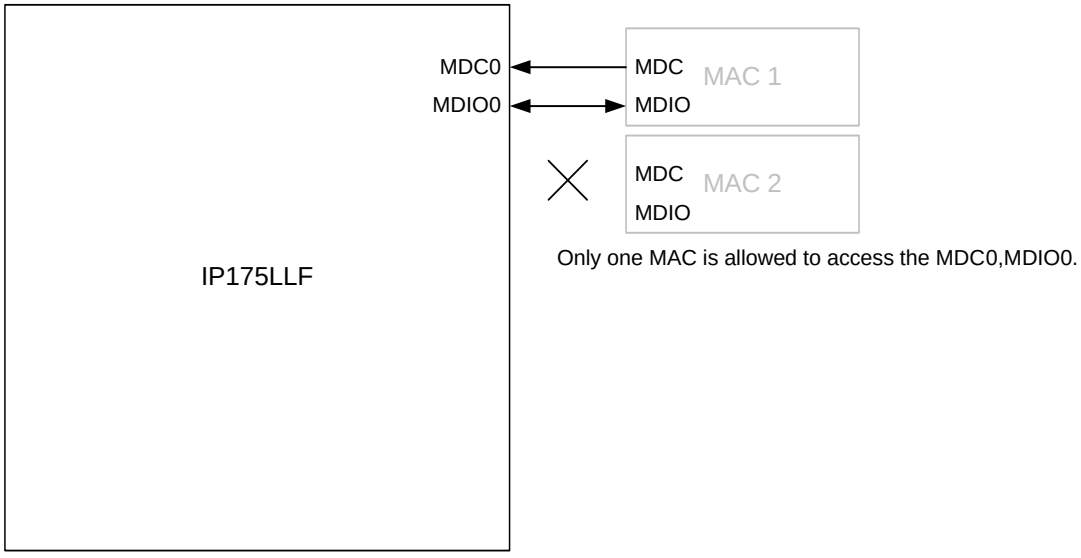
3.18 Serial Management Interface

IP175LLF supports one serial management interfaces (SMI). User can access IP175LLF's MII registers through MDC0 and MDIO0. Its format is shown in the following table. To access MII register in IP175LLF, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

Frame format	<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>



The application of SMI



3.19 Reset

The IP175LLF supports three kinds of reset function.
1. Hardware Reset: Pin 50 RESETB should be asserted LOW at least for 5ms to reset IP175LLF. The IP175LLF gets initial values from pins and EEPROM after reset.
2. Software Reset: After Hardware Reset, user can write 16'h175D to PHY 20 Register 2 via SMI to reset IP175LLF.The IP175LLF resets all of PHY's and switch Engine, but IP175LLF does not load initial values form pins and EEPROM.
3. PHY Reset: Please write "1" to bit 15 of MII register 0 to reset the PHY. The PHY address is from 0 to 3 for port 0~3 respectively.

3.20 Built in regulator

IP175LLF is built in one linear regulator. It use pin 61 REG_OUT to control an external transistor to generator a stable voltage source. IP175LLF generates a voltage source between 1.85v ~ 2.05v.

4 PHY Register

4.1 PHY ID Map

PHY ID	Description	Default	Note
0	Port 0 PHY		
1	Port 1 PHY		
2	Port 2 PHY		
3	Port 3 PHY		
5	TMII0/MII0/RMII0		
20~27	Switch Registers		

4.2 PHY 0~3 and 5 Register Map

PHY ID	Register	Description	Default	Note
0~3 and 5	0	Control Register		X5
0~3 and 5	1	Status Register		X5
0~3	2	PHY Identifier 1 Register		X1
0~3	3	PHY Identifier 2 Register		X1
0~3 and 5	4	Auto-Negotiation Advertisement Register		X5
0~3 and 5	5	Auto-Negotiation Link Partner Ability Register		X5
0~3	6	Auto-Negotiation Expansion Registers		X4
0~3	16	Special Control Register (APS)		X1
0~3	18	Special Status Register		X4
0~3	22	MDI-MDIX Control Register		X1

X1: 4 ports share the register
X4 & X5: Each port has its individual register

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High.

4.3 MII Register 0

4.3.1 MII Register 0 of PHY0~3

(Each PHY has its own MII register 0 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
Control register					
3~0	0.15	--	RW/ SC	Reset The PHY is reset if user write “1” to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP175LLF.	0
3~0	0.14	--	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, IP175LLF will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN. Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test.	0
3~0	0.13	--	RW	Speed Selection 1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	1
3~0	0.12	--	RW	Auto-Negotiation Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable MII register 3~0.22 Auto MDI-MDIX should be disabled if Auto-Negotiation is disabled.	1
3~0	0.11	--	R/W	Power Down 1: power down mode 0: normal operation	0
3~0	0.10	--		Isolate IP175LLF doesn’t support this function.	0
3~0	0.9	--	RW SC	Restart Auto- Negotiation 1 = re-starting Auto-Negotiation 0 = normal operation	0
3~0	0.8	--	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	0
3~0	0.7	--	R/W	Collision test	0
3~0	0[6:0]	--	RO	Reserved	0

4.3.2 MII Register 0 of PHY5

PHY	MII	ROM	R/W	Description	Default
Control register					
5	0.15	--	RO	Reserved	0
5	0.14	--	RO	Reserved	0
5	0.13	--	RO	Speed Selection 1 = 100Mbps 0 = 10Mbps	Set by Pin55
5	0.12	--	RO	Auto-Negotiation Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
5	0.11	--	RO	Reserved	0
5	0.10	--	RO	Reserved	0
5	0.9	--	RO	Reserved	0
5	0.8	--	RO	Duplex mode 1 = full duplex 0 = half duplex	Set by Pin58
5	0.7	--	RO	Reserved	0
5	0[6:0]	--	RO	Reserved	0

4.4 MII Register 1

4.4.1 MII Register 1 of PHY0~3

(Each PHY has its own MII register 1 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
Status register					
3~0	1.15	--	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP175LLF does not support 100Base-T4. This bit is fixed to be 0.	0
3~0	1.14	--	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
3~0	1.13	--	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
3~0	1.12	--	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
3~0	1.11	--	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
3~0	1[10:7]	--	RO	Reserved	0
3~0	1.6	--	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
3~0	1.5	--	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0
3~0	1.4	--	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP175LLF has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP175LLF reset.	0
3~0	1.3	--	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP175LLF has the ability to perform Auto-Negotiation.	1

PHY	MII	ROM	R/W	Description	Default
Status register					
3~0	1.2	--	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP175LLF has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
3~0	1.1	--		Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP175LLF has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP175LLF reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled.	0
3~0	1.0	--	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities IP175LLF has extended register capabilities.	1

4.4.2 MII Register 1 of PHY5

PHY	MII	ROM	R/W	Description	Default
Status register					
5	1.15	--	RO	Reserved	0
5	1.14	--	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
5	1.13	--	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
5	1.12	--	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
5	1.11	--	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
5	1[10:7]	--	RO	Reserved	0
5	1.6	--	RO	Reserved	0
5	1.5	--	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress	1
5	1.4	--	RO	Reserved	0
5	1.3	--	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable	1
5	1.2	--	RO	Link Status 1 = Link Pass 0 = Link Fail	1
5	1.1	--	RO	Reserved	0
5	1.0	--	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities	1

4.5 MII Register 2 of PHY0~3 (4 PHYs share the MII register)

PHY	MII	ROM	R/W	Description	Default
PHY Identifier 1 register					
3~0	2	--	RO	IP175LLF OUI (Organizationally Unique Identifier) ID, the msb is 3rd bit of IP175LLF OUI ID, and the lsb is 18th bit of IP175LLF OUI ID. IP175LLF OUI is 0090C3.	16'h0243

4.6 MII Register 3 of PHY0~3 (4 PHYs share the MII register)

PHY	MII	ROM	R/W	Description	Default
PHY Identifier 2 register					
3~0	3[15:10]	--	RO	PHY identifier IP175LLF OUI ID, the msb is 19th bit of IP175LLF OUI ID, and lsb is 24th bit of IP175LLF OUI ID.	6'h03
3~0	3[9:4]	--	RO	Manufacture's Model Number IP175LLF model number	6'h18
3~0	3[3:0]	--	RO	Revision Number IP175LLF revision number	0

4.7 MII Register 4

4.7.1 MII Register 4 of PHY0~3

(Each PHY has its own MII register 4 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
Auto-Negotiation Advertisement register					
3~0	4.15	--	RO	Next Page Not supported. This bit is fixed to be 0.	0
3~0	4.14	--	RO	Reserved by IEEE, write as 0, ignore on read	0
3~0	4.13	--	R/W	Remote Fault 1: Advertises that this port has detected a remote fault. 0: There is no remote fault.	0
3~0	4[12:11]	--	RO	Reserved for future IEEE use, write as 0, ignore on read	0
3~0	4.10	--	RW	Pause 1 = Advertises that this port has implemented pause function 0 = No pause function supported	1
3~0	4.9	--	RO	100BASE-T4 Not supported	0
3~0	4.8	--	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	*

FORCE	FORCE100	FORCE_FULL	Default
0	Don't care	Don't care	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3~0	4.7	--	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	*

FORCE	FORCE100	FORCE_FULL	Default
0	Don't care	Don't care	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

3~0	4.6	--	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	*

FORCE	FORCE100	FORCE_FULL	Default
0	Don't care	Don't care	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

3~0	4.5	--	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1

PHY	MII	ROM	R/W	Description	Default
3~0	4[4:0]	--	RO	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	5'b00001

4.7.2 MII Register 4 of PHY5

PHY	MII	ROM	R/W	Description	Default
Auto-Negotiation Advertisement register					
5	4.15	--	RO	Reserved	0
5	4.14	--	RO	Reserved	0
5	4.13	--	RO	Reserved	0
5	4[12:11]	--	RO	Reserved	0
5	4.10	--	RO	Pause 1 = Advertises that this port has implemented pause function 0 = No pause function supported	1
5	4.9	--	RO	Reserved	0
5	4.8	--	RO	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
5	4.7	--	RO	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
5	4.6	--	RO	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
5	4.5	--	RO	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
5	4[4:0]	--	RO	Reserved	5'b00001

4.8 MII Register 5

4.8.1 MII Register 5 of PHY0~3

(Each PHY has its own MII register 5 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
Auto-Negotiation Link Partner Ability register					
3~0	5.15		RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
3~0	5.14		RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
3~0	5.13		RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
3~0	5[12:11]	--	RO	Reserved by IEEE for future use, write as 0, read as 0.	0
3~0	5.10	--	RW	Pause 1 = Link partner support IEEE802.3x 0 = Link partner does not support IEEE802.3x When Nway enabled, this bit reflects link partner ability. (read only) When Nway disabled, this bit can be set by SMI. (read/write) When in 100FX, this bit is set by SMI.	0
3~0	5.9	--	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
3~0	5.8	--	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
3~0	5.7	--	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX For 100FX mode, this bit is set. When Nway is disabled, this bit is set if register 0.13=1.	0
3~0	5.6	--	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
3~0	5.5	--	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T When Nway is disabled, this bit is set if register 0.13=0	0
3~0	5[4:0]	--	RO	Selector Field Protocol selector of the link partner	5'b00000

4.8.2 MII Register 5 of PHY5

PHY	MII	ROM	R/W	Description	Default
Auto-Negotiation Link Partner Ability register					
5	5.15		RO	Reserved	0
5	5.14		RO	Reserved	1
5	5.13		RO	Reserved	0
5	5[12:11]	--	RO	Reserved	0
5	5.10	--	RO	Pause 1 = Link partner support IEEE802.3x 0 = Link partner does not support IEEE802.3x	1
5	5.9	--	RO	Reserved	0
5	5.8	--	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	Set by Pin55, Pin58
5	5.7	--	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	Set by Pin55, Pin58
5	5.6	--	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	Set by Pin55, Pin58
5	5.5	--	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T	Set by Pin55, Pin58
5	5[4:0]	--	RO	Reserved	5'b00001

4.9 MII Register 6 of PHY0~3

(Each PHY has its own MII register 6 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
Auto-Negotiation Expansion register					
3~0	6[15:5]	--	RO	Reserved	0
3~0	6.4	--	RO	1: a fault has been detected via parallel detection function. 0: a fault has not been detected via parallel detection function.	0
3~0	6.3	--	RO	1= Link partner is next page able. 0= Link partner is not next page able.	0
3~0	6.2	--	RO	1: IP175LLF next page able. 0: IP175LLF is not next page able. This bit is fixed to be “0” in IP175LLF	0
3~0	6.1	--	RO/ LH	1: A new page has been received. 0: A new page has not been received.	0
3~0	6.0	--	RO	If Nway is enabled, this bit means: 1: Link partner is Auto-Negotiation able. 0: Link partner is not Auto-Negotiation able. In 100FX or Nway disabled, this bit always =0.	0 (Nway) (100FX)

4.10 MII Register 16 of PHY0~3 (4 PHYs share the MII register)

PHY	MII	ROM	R/W	Description	Default
Special Control register					
3~0	16.7	--	RW	Auto power saving mode 1 = Enable APS mode 0 = Disable APS mode	1

4.11 MII Register 18 of PHY0~3

(Each PHY has its own MII register 18 with different PHY address)

PHY	MII	ROM	R/W	Description	Default
Special Status register					
3~0	18.11	--	RO	Speed Mode 1 = 100 Mbps 0 = 10 Mbps	1
3~0	18.10	--	RO	Duplex Mode 1 = Full Duplex 0 = Half Duplex	0

4.12 MII Register 22 of PHY0~3 (4 PHYs share the MII register)

PHY	MII	ROM	R/W	Description	Default
MDI-MDIX Control register					
3~0	22.8		RW	PHY3 Auto MDI-MDIX Enable 1 = Enable Auto MDI-MDIX 0 = Disable Auto MDI-MDIX It should be disabled if MII register 3.0.12 Auto-Negotiation is disabled.	1
3~0	22.7		RW	PHY2 Auto MDI-MDIX Enable 1 = Enable Auto MDI-MDIX 0 = Disable Auto MDI-MDIX It should be disabled if MII register 2.0.12 Auto-Negotiation is disabled.	1
3~0	22.6		RW	PHY1 Auto MDI-MDIX Enable 1 = Enable Auto MDI-MDIX 0 = Disable Auto MDI-MDIX It should be disabled if MII register 1.0.12 Auto-Negotiation is disabled.	1
3~0	22.5		RW	PHY0 Auto MDI-MDIX Enable 1 = Enable Auto MDI-MDIX 0 = Disable Auto MDI-MDIX It should be disabled if MII register 0.0.12 Auto-Negotiation is disabled.	1
3~0	22.3		RW	PHY3 MDI-MDIX Selection (only available when 22.8 = 0) 1 = MDIX mode 0 = MDI mode	0
3~0	22.2		RW	PHY2 MDI-MDIX Selection (only available when 22.7 = 0) 1 = MDIX mode 0 = MDI mode	0
3~0	22.1		RW	PHY1 MDI-MDIX Selection (only available when 22.6 = 0) 1 = MDIX mode 0 = MDI mode	0
3~0	22.0		RW	PHY0 MDI-MDIX Selection (only available when 22.5 = 0) 1 = MDIX mode 0 = MDI mode	0

5 Switch Register

The IP175LLF can be configured via external EEPROM interface at boot time. During operation, IP175LLF registers are accessible via MDC0/MDIO0 interface.

5.1 Switch Register Map

PHY 20

REG NUM	Description
0	Chip identification
1	Reserved
2	System Reset
3	
4	Force Mode
5	Congestion Control
6	Port State
7	Illegal Frame Filter
8	Packet Identification
9	
10	
11	
12	Network Security
13	Learning Control Register
14	Ageing Time Parameter
15	
16	Broadcast Storm Protection
17	
18	
19	
20	Port Mirror
21	
22	Source Block Protection
23	Reserved
24	LED Control Register
25	Reserved
26	
27	
28	Reserved
29	
30	
31	

PHY 21

REG NUM	Description
0	External MII Configuration
1	
2	
3	
4	
5	IGMP Control Register
6	
7	
8	Rate Control
9	
10	
11	Reserved
12	Rate Control
13	Reserved
14	Address Table Access Register
15	
16	
17	
18	
19	
20	Loop Detection Register
21	
22	Miscellaneous Control Register
23	
24	
25	CRC Counter
26	Reserved
27	
28	
29	
30	
31	

PHY 22

REG NUM	Description
0	VLAN Control Register
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	VLAN Table
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	Reserved
31	

PHY 23

REG NUM	Description
0	VLAN Table
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	

PHY 24

REG NUM	Description
0	VLAN Table
1	
2	
3	
4	Reserved
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	

PHY 25

REG NUM	Description
0	Priority Classification
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	Queue Scheduling
23	
24	Reserved
25	
26	
27	
28	
29	
30	
31	

	REG NUM	Description
PHY 26	0	MF
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	Reserved
	25	
	26	
	27	
	28	
	29	
	30	
	31	

5.2 Switch Register EEPROM Map

	7	6	5	4	3	2	1	0
0~1	Load eeprom (55AA)							
2	MII force mode							
3	Congestion control							
4~5	Port state							
6	Illegal frame filter							
7~9	Reserved address							
10~12	Miscellaneous special packet identification							
13~14	Network security							
15~16	Learning control							
17~19	Aging time parameter							
20~27	Broadcast storm protection							
28~30	Port mirror							
31	Source block protection							
32	Reserved							
33	LED control							
34~39	Reserved							
40~45	External MII setting							
46	IGMP control							
47~48	Router port timeout							
49	IGMP group timeout							
50~51	Miscellaneous control							
52~53	Reserved							

	7	6	5	4	3	2	1	0
54	Miscellaneous control							
55~56	VLAN classification							
57~58	VLAN ingress rule							
59~60	VLAN egress rule							
61~74	Default VLAN information							
75~82	VLAN control							
83~114	VLAN identifier							
115~130	VLAN member							
131~146	Add tag control							
147~162	Remove tag control							
163~178	VLAN miscellaneous							
179~186	Spanning tree table							
187~188	Priority base control							
189~190	Port priority map							
191~192	VLAN priority							
193~208	TOS/DSCP priority map							
209~228	TCP/UDP port priority							
229~232	Queue scheduling control							

5.3 Switch Control Register

R/W = Read/Write, SC = Self-Clearing, RO = Read Only

5.3.1 Chip Identification

PHY	MII	ROM	R/W	Description	Default
20	0[15:0]	--	RO	PART_NUM Part ID number	16'h 175D

5.3.2 Software Reset Register

PHY	MII	ROM	R/W	Description	Default
20	2[15:0]	--	R/W	SOFT_RESET[15:0] Software reset register IP175LLF is reset if uses write "175D" to this register. It is self-cleared. The reset period is around 2ms. User has to wait for at least 2 ms to access IP175LLF. When read this register, it shows the internal status of IP175LLF.	16'h00
	3[1:0]	--	R/W	TABLE_LOCK[1:0] Lock content of table. Bit[1]: Multi-Field table Bit[0]: Address table	2'b00

5.3.3 MII Force Mode

PHY	MII	ROM	R/W	Description	Default
20	4.15	2[7]	R/W	MAC5_FORCE_100 1: force MAC5 to be 100M 0: force MAC5 to be 10M	*
20	4.14	2[6]	R/W	Reserved	0
20	4.13	2[5]	R/W	MAC5_FORCE_FULL 1: force MAC5 to be full duplex 0: force MAC5 to be half duplex	*
20	4.12	2[4]		Reserved	0

5.3.4 Congestion Control Register

PHY	MII	ROM	R/W	Description	Default
20	5[15:9]			RESERVED	
	5[8]	2[0]	R/W	CONT_PAUSE To continuously send pause packet 1:enable 0:disable	1'b0
	5[7]	3[7]	R/W	MOD_CARRIER_ALGORITHM Modified carrier based collision algorithm 1:enable 0:disable	1'b0
	5[6]	3[6]	R/W	INPUT_FILTER 1: enable 0: disable	1'b0
	5[5]	3[5]	R/W	DROP16 Drop input packet after 16 times collision in succession.	1'b0
	5[4]	3[4]	R/W	MODBCK Modified backoff collision algorithm	1'b1
	5[3]	3[3]	R/W	BP_KIND Backpressure Kind 0: carrier based 1: collision based	1'b0
	5[2]	3[2]	R/W	BK_EN Backpressure enable 1: enable (default), 0: disable	*
	5[1]	3[1]	R/W	X_EN IEEE 802.3x flow control enable (5 ports share the register) 1: enable (default), 0:disable If modify this register, a software reset (MII register 20.2) must be generated to notify PHY for flow control status change.	*
	5[0]	3[0]	R/W	MAC_X_EN Flow control enable of MII0-2 1: enable (default) 0: disable	*

5.3.5 Port State

PHY	MII	ROM	R/W	Description		Default
20	6[13:8]	4[5:0]	R/W	FORWARD_EN[5:0] Frame forwarding capability enable for each port		6'h3F
				bit 5	1: enable frame forwarding capability of port 5 0: disable frame forwarding capability of port 5	
				bit 4	1: enable frame forwarding capability of port 4 0: disable frame forwarding capability of port 4	
				bit 3	1: enable frame forwarding capability of port 3 0: disable frame forwarding capability of port 3	
				bit 2	1: enable frame forwarding capability of port 2 0: disable frame forwarding capability of port 2	
				bit 1	1: enable frame forwarding capability of port 1 0: disable frame forwarding capability of port 1	
				bit 0	1: enable frame forwarding capability of port 0 0: disable frame forwarding capability of port 0	
	6[5:0]	5[5:0]	R/W	LEARNING_EN[5:0] MAC address Learning capability enable for each port		6'h3F
				bit 5	1: enable address learning capability of port 5 0: disable address learning capability of port 5	
				bit 4	1: enable address learning capability of port 4 0: disable address learning capability of port 4	
				bit 3	1: enable address learning capability of port 3 0: disable address learning capability of port 3	
				bit 2	1: enable address learning capability of port 2 0: disable address learning capability of port 2	
				bit 1	1: enable address learning capability of port 1 0: disable address learning capability of port 1	
				bit 0	1: enable address learning capability of port 0 0: disable address learning capability of port 0	

5.3.6 Illegal Frame Filter

PHY	MII	ROM	R/W	Description	Default
20	7[15:5]			RESERVED	
	7[4:3]	6[4:3]	R/W	LONG_FRM[1:0] Max forwarded packet length 00: 1536 bytes (default) 01: 1552 bytes 10: 1792 bytes 11: reserved	*
	7[2]	6[2]	R/W	MC_SMC Filter Frame with multicast source MAC address	1'b0
	7[1]	6[1]	R/W	NULL_MAC Filter Frame with null source or destination MAC address	1'b0
	7[0]	6[0]	R/W	CRC_ERROR Filter CRC Frame	1'b1

5.3.7 Special Packet Identification

5.3.7.1 Reserved Address 01-80-C2-00-00-00 to 01-80-C2-00-00-1F

PHY	MII	ROM	R/W	Description	Default
20	8[15:14]	7[7:6]	R/W	TRAP_RSVD_ADDR1[1:0] Reserved address range 1 Reserved MAC address is from 01:80:C2:00:00:11 to 01:80:C2:00:00:1F 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	8[13:12]	7[5:4]	R/W	TRAP_ABM[1:0] All Bridges Multicast address defined by IEEE 802.1D Reserved MAC address is 01:80:C2:00:00:10 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	8[11:10]	7[3:2]	R/W	TRAP_RSVD_ADDR0[1:0] Reserved address range 0 Reserved MAC address is from 01:80:C2:00:00:04 to 01:80:C2:00:00:0D, 01:80:C2:00:00:0F 00: forward (default) 01: forward to CPU 10: discard 11: reserved	*
	8[9:8]	7[1:0]	R/W	TRAP_LLDP[1:0] Link Layer Discovery Protocol Reserved MAC address is 01:80:C2:00:00:0E LLDP Data Units (LLDPDUs) encoded with an Ethertype value of 0x88CC. 00: forward (default) 01: forward to CPU 10: discard 11: reserved	*
20	8[7:6]	8[7:6]	R/W	TRAP_802P1X[1:0] IEEE 802.1X Port-Based Network Access Control Reserved MAC address is 01:80:C2:00:00:03 00: forward (default) 01: forward to CPU 10: discard 11: reserved	*

PHY	MII	ROM	R/W	Description	Default
	8[5:4]	8[5:4]	R/W	TRAP_SP[1:0] IEEE 802 standard protocol – Slow Protocols Reserved MAC address is 01:80:C2:00:00:02 00: forward (default) 01: forward to CPU 10: discard 11: reserved	*
	8[3]			RESERVED	
	8[2]	8[2]	R/W	TRAP_PAUSE Point-to-Point Pause function Reserved MAC address is 01:80:C2:00:00:01 1: forward 0: discard (default)	1'b0
	8[1:0]	8[1:0]	R/W	TRAP_BPDU[1:0] Standard Spanning Tree Protocol Reserved MAC address is 01:80:C2:00:00:00 00: forward (default) 01: forward to CPU 10: discard 11: reserved	*

5.3.7.2 Reserved Address 01-80-C2-00-00-20 to 01-80-C2-00-00-FF

PHY	MII	ROM	R/W	Description	Default
20	9[15:8]			RESERVED	
	9[7:6]	9[7:6]	R/W	TRAP_RSVD_ADDR3[1:0] Reserved address range 3 Reserved MAC address is from 01:80:C2:00:00:30 to 01:80:C2:00:00:FF 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	9[5:4]	9[5:4]	R/W	TRAP_RSVD_ADDR2[1:0] Reserved address range 2 Reserved MAC address is from 01:80:C2:00:00:22 to 01:80:C2:00:00:2F 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	9[3:2]	9[3:2]	R/W	TRAP_GVRP[1:0] GVRP Address: 01-80-C2-00-00-21 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	9[1:0]	9[1:0]	R/W	TRAP_GMRP[1:0] GMRP Address: 01-80-C2-00-00-20 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

5.3.7.3 Miscellaneous Special Packet Identification

PHY	MII	ROM	R/W	Description	Default
20	10[15:14]	10[7:6]	R/W	TRAP_ICMP Internet Control Message Protocol ICMPv4: TYPE=0x0800 and Protocol=1 ICMPv6: TYPE=0x86DD and Protocol=58 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

PHY	MII	ROM	R/W	Description	Default
	10[13:12]	10[5:4]	R/W	TRAP_MLD_CTRL MLD Control Packet DMAC=33-33-XX-XX-XX-XX EtherType=0x86DD Version=6 Next Header=58 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[11:10]	10[3:2]	R/W	TRAP_MLD Multicast Listener Discovery DMAC=33-33-XX-XX-XX-XX EtherType=0x86DD Version=6 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[9:8]	10[1:0]	R/W	TRAP_IPM_DATA IP Multicast Data Packet DMAC=01-00-5E-XX-XX-XX EtherType=0x0800 Version=4 DIP=224.0.1.0~239.225.225.225 Protocol is not IGMP 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[7:6]	11[7:6]	R/W	TRAP_IPM_CTRL IP Multicast Control Packet DMAC=01-00-5E-XX-XX-XX EtherType=0x0800 Version=4 DIP=224.0.0.x Protocol is not IGMP 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

PHY	MII	ROM	R/W	Description	Default
	10[5:4]	11[5:4]	R/W	TRAP_IGMP Internet Group Management Protocol DMAC=01-00-5E-XX-XX-XX EtherType=0x0800 Version=4 Protocol=2(IGMP) 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[3:2]	11[3:2]	R/W	TRAP_RARP[1:0] Reverse Address Resolution Protocol The destination MAC address is FF: FF: FF: FF: FF: FF and Ether-Type field is 0x8035 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[1:0]	11[1:0]	R/W	TRAP_ARP[1:0] Address Resolution Protocol The destination MAC address is FF: FF: FF: FF: FF: FF and Ether-Type field is 0x0806 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

PHY	MII	ROM	R/W	Description	Default
20	11[15:4]			RESERVED	
	11[3:2]	12[3:2]	R/W	TRAP_BOOTP Bootstrap Protocol Port Number=16'd67 or 16'd68 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	11[1:0]	12[1:0]	R/W	TRAP_PPPoE Point-to-Point Protocol over Ethernet Ether-Type=0x8863 or 0x8864 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

5.3.8 Network Security

PHY	MII	ROM	R/W	Description	Default
20	12[14]	13[6]	R/W	ILL_SMAC_2CPU Illegal SMAC to CPU 0: If frame with illegal SMAC, discard it. 1: If frame with illegal SMAC, forward it to CPU.	1'b0
	12[13:8]	13[5:0]	R/W	ILL_SMAC_PROT[5:0] Illegal source MAC address protection 0: disable 1: enable. Bit[0]: port 0 Bit[1]: port 1 Bit[2]: port 2 Bit[3]: port 3 Bit[4]: port 4 Bit[5]: port 5	6'h00
	12[7:6]			RESERVED	
	12[5:0]	14[5:0]	R/W	CHK_PORT[5:0] The frame is examined based on the combination of SMAC and ingress port number in address table. Bit[0]: port 0 Bit[1]: port 1 Bit[2]: port 2 Bit[3]: port 3 Bit[4]: port 4 Bit[5]: port 5 It is valid only if the corresponding ILL_SMAC_PROT bit is enabled	6'b111111

5.3.9 Learning Control Register

PHY	MII	ROM	R/W	Description	Default
20	13[15:10]			RESERVED	
	13[9:8]	15[7:6]	R/W	FILTER_MDMAC Filter unknown multicast DMAC 2'b00 : Flooding 2'b01 : Forward to CPU 2'b10 : Discard 2'b11 : Reserved Note : Multicast DMAC does not include broadcast DMAC	2'b00
	13[7:6]	15[5:4]	R/W	FILTER_UDMAC Filter unknown unicast DMAC 2'b00 : Flooding 2'b01 : Forward to CPU 2'b10 : Discard 2'b11 : Reserved	2'b00
	13[5]	16[5]	R/W	LEARN_DIS_PAUSE Learning disable because of PAUSE frame	1'b1

PHY	MII	ROM	R/W	Description	Default
	13[4]	16[4]	R/W	RESERVED	
	13[3]	16[3]	R/W	AT_STR Address Table Structure 0: 2K Address Table for unicast frame (default) 1: 1K Address Table for unicast frame and 1K Address Table for multicast frame Note – We recommend clear address table once this bit is modified.	pin_21 (0)
	13[2]			RESERVED	
	13[1]	16[1]	R/W	IGMP_OVER_VLAN 0 : Disable 1 : Enable It is valid only for LEARN_CONSTRAIN is enabled	pin_21 (0)
	13[0]	16[0]	R/W	LEARN_CONSTRAIN Learning Constraint 0 : VLAN information(FID) is not used to create a hash key 1 : VLAN information(FID) is used to create a hash key Note – We recommend clear address table once this bit is modified.	1'b0

5.3.10 Aging Time Parameter

PHY	MII	ROM	R/W	Description	Default
20	14[15:7]			RESERVED	
	14[6:5]	17[6:5]	R/W	AGE_TIME_UNIT 2'b00 : 1 minutes 2'b01 : 1 second 2'b10 : 10 ms 2'b11 : fast mode. This mode will age out whole table in 1~2 ms. For some special application (ex. RSTP) need to clear table ASAP. Independent with AGE_TIME_VLE.	2'b00
	14[4:0]	17[4:0]	R/W	AGE_TIME_VLE Age Time Value. 5'h00: no aging AGE_TIME= AGE_TIME_UNIT * AGE_TIME_VLE	*
	15[15:9]			RESERVED	
	15[8]	18[3]	R/W	PID_EN If set, the aging module ages entries whose Port ID matches PID_VAL	1'b0
	15[7:5]	18[2:0]	R/W	PID_VAL[2:0] Port ID Value 3'b000 : reserved (default) 3'b001 : port 0 3'b010 : port 1 3'b011 : port 2 3'b100 : port 3 3'b101 : port 4 3'b110 : port 5 (cpu port) other : reserved	3'b000
	15[4]	19[4]	R/W	FID_EN If set, the aging module ages entries whose FID matches FID_VAL 0: Disable 1: Enable	1'b0
	15[3:0]	19[3:0]	R/W	FID_VAL[3:0] FID Value	4'h0

5.3.11 Broadcast Storm Protection

PHY	MII	ROM	R/W	Description	Default
20	16[15:14]			RESERVED	
	16[13:8]	20[5:0]	R/W	BF_STM_EN[5:0] Broadcast storm enable 1: enable Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in MII register 20.17~20.19 0: disable (default)	*
	16[7:6]			RESERVED	
	16[5:0]	21[5:0]	R/W	BF_FFFF_ONLY[5:0] Multicast broadcast storm protection disable 1: "Broadcast storm protection" does not include multicast packets. IP175LLF drops the packets with DA equals to 0xFFFFFFFF only when the broadcast threshold is reached (default), 0: "Broadcast storm protection" includes multicast packets. IP175LLF drops the packets with DA equals to 0xFFFFFFFFF, or multi-cast address when the broadcast threshold is reached. "Broadcast storm protection" does not drop packets due to not learned address.	6'h3f
	17[15:8]	23[7:0]	R/W	BF_STM_THR_1[7:0] Broadcast storm threshold setting for port 1	8'h08
	17[7:0]	22[7:0]	R/W	BF_STM_THR_0[7:0] Broadcast storm threshold setting for port 0 Threshold setting range is from 1 to 255 packets/10ms for 100Mbps connection or 1 to 255 packets/100ms for 10Mbps connection	8'h08
	18[15:8]	25[7:0]	R/W	BF_STM_THR_3[7:0] Broadcast storm threshold setting for port 3	8'h08
	18[7:0]	24[7:0]	R/W	BF_STM_THR_2[7:0] Broadcast storm threshold setting for port 2	8'h08
	19[15:8]	27[7:0]	R/W	BF_STM_THR_5[7:0] Broadcast storm threshold setting for port 5	8'h08
	19[7:0]	26[7:0]	R/W	BF_STM_THR_4[7:0] Broadcast storm threshold setting for port 4	8'h08

5.3.12 Port Mirror

PHY	MII	ROM	R/W	Description	Default
20	20[15]	28[7]	R/W	PORT_MIRROR_EN	1'b0
	20[14:13]	28[6:5]	R/W	PORT_MIRROR_MODE[1:0] Select a mirror mode to monitor 2'b00: mirror one port of RX (default) 2'b01: mirror one port of TX 2'b10: mirror source-destination pair (port of TX and RX must be the different) 2'b11: mirror one port of TX and RX (port of TX and RX must be the same)	2'b00
	20[12:6]			RESERVED	
	20[5:0]	29[5:0]	R/W	SEL_RX_PORT_MIRROR[5:0] Select the source (receive) port to be mirrored 6'b00_0000: reserved (default) 6'b00_0001: port 0 6'b00_0010: port 1 6'b00_0100: port 2 6'b00_1000: port 3 6'b01_0000: port 4 6'b10_0000: port 5 (MII0) other: reserved	6'h00
	21[15]			RESERVED	
	21[14:12]	28[4:2]	R/W	SEL_MIRROR_PORT[2:0] Select a mirror port to monitor any other port 3'b000: port 0 3'b001: port 1 3'b010: port 2 3'b011: port 3 3'b100: port 4 3'b101: port 5 (MII0)(default) other: reserved	3'b101
	21[11:6]			RESERVED	
	21[5:0]	30[5:0]	R/W	SEL_TX_PORT_MIRROR[5:0] Select the destination (transmit) port to be mirrored 6'b00_0000: reserved (default) 6'b00_0001: port 0 6'b00_0010: port 1 6'b00_0100: port 2 6'b00_1000: port 3 6'b01_0000: port 4 6'b10_0000: port 5 (MII0) other: reserved	6'h00

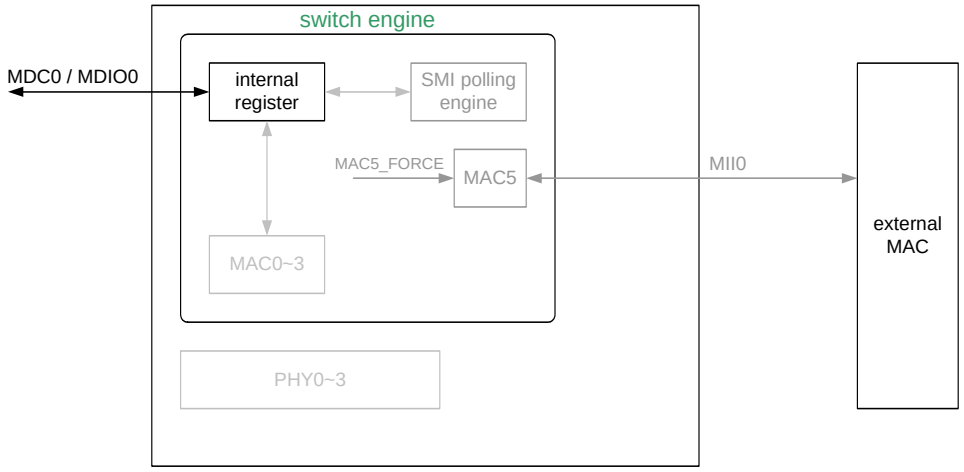
5.3.13 Source Block Protection

PHY	MII	ROM	R/W	Description	Default
20	22[15:7]			RESERVED	
	22[6]	31[6]	R/W	SBP_EN Source Block Protection Enable	1'b0
	22[5:0]		R (SC)	SBP_STATUS[5:0] Source Block Protection Status Bit[0]: port 0 Bit[1]: port 1 Bit[2]: port 2 Bit[3]: port 3 Bit[4]: port 4 Bit[5]: port 5 Self-clear after read	6'h00

5.3.14 LED Control Register

PHY	MII	ROM	R/W	Description	Default
20	24[1:0]	33[1:0]	R/W	LED_SEL[1:0] LED output mode selection. LED_SEL[1:0]=2'b00: LED mode 0, LED_SEL[1:0]=2'b01: LED mode 1, LED_SEL[1:0]=2'b10: LED mode 2, LED_SEL[1:0]=2'b11: LED mode 3 (default)	2'b11

5.4 External MII Control Register



5.4.1 External MII Status Report Register

PHY	MII	ROM	R/W	Description	Default
21	0[7]	--	RO	MII0_FULL 1: full, 0: half	1'b1
	0[6]	--	RO	MII0_SPEED10 1: 10M, 0: 100M	1'b0
	0[5]	--	RO	MII0_FLOW MII0 flow control ability 1: enable, 0: disable	1'b1

5.4.2 MII0 MAC Mode Register

PHY	MII	ROM	R/W	Description	Default
21	1[15]	--	RO	MAC_XCTRLEN[0] Flow control capability of the link partner of external PHY on MII0 1: link partner supports flow control, 0: link partner does not support flow control	1'b1
	1[14]	--	RO	MAC_FORCE[0] 1: MII0's speed and duplex are forced because IP175LLF finds external PHY doesn't support SMI 0: MII0 polls external PHY through SMI to decide its speed and duplex.	1'b0
	1[13]	--	RO	MII0_link 1: link ok, 0: un-link	1'b1
	1[12:8]	40[4:0]	R/W	Capability of external PHY on MII0 bit12: flow control ability, bit11: 100M full duplex, bit10 : 100M half duplex, bit9 : 10M full duplex, bit8: 10M half duplex	5'b 11111
	1[7]	--	RO	Speed of external PHY on MII0 1: 10M, 0: 100M	1'b0
	1[6]	--	RO	Duplex of external PHY on MII0 1: full duplex, 0: half duplex	1'b1
	1[5]	--	RO	Link status of external PHY on MII0 1: link on, 0: link off	1'b1
	1[4:0]	41[4:0]	R/W	MII0_MAC_PHY_ADDR[4:0]	5'b 00000

5.4.3 MII0 Control Register 1

PHY	MII	ROM	R/W	Description	Default
21	3[14]	--	RO	SMI0_POLLING 1: MII0 MAC mode 0: MII0 PHY mode	1'b0
	3[11]	44[5]	R/W	MII0_MAC_MODE_EN External MII0 port MAC mode 1: MII0 works as a MAC and should be connected to an external PHY. 0: MII0 works as a PHY and should be connected to an external MAC device (default).	*
	3[10]	44[4]	R/W	MII0_RMII_EN (RMII_EN) 1: MII0 RMII interface enabled 0: MII0 RMII interface disabled (default).	pin 27 (0)
	3[6]	44[0]	R/W	MII0_MAC_REPEATER 1: external PHY 's TXEN does not loop back to CRS (default) 0: external PHY 's TXEN loop back to CRS	1'b1
	3[4]	45[6]	R/W	MII0_PHY_COL_DELAY 0: no delay, 1: collision delay 24 clocks (default) It is valid only if MII0 is enabled and it works at PHY mode.	1'b1
	3[2]	45[5]	R/W	RESERVED	0
	3[0]	45[4]	R/W	RESERVED	0

5.4.4 MII0 Control Register 2

PHY	MII	ROM	R/W	Description	Default
21	4[1]	45[2]	R/W	MII0_CHK_CRC Examine CRC filed of every incoming frame of MII 0 port.	1'b1

5.5 IGMP Control Register

5.5.1 Base Control Register

PHY	MII	ROM	R/W	Description	Default
21	5[15:11]			RESERVED	
	5[10]	50[6]	R/W	FAST_LEAVE	1'b1
	5[9]	45[1]	R/W	MG_INCLUDE_RP Multicast group include router port 0:Disabled 1:Enabled	1'b0
	5[8]	45[0]	R/W	FLOOD_UNIGMP Flood Unknown IGMP Unknown IGMP is not one of following: 1. General Query 2. Group-Specific Query 3. IGMP Report 4. IGMP Leave	1'b0
	5[7]	46[7]	R/W	FLOOD_IPM_CTRL Flood IP Multicast Control Packet 0:Disabled 1:Enabled Note – IP multicast control packet: DMAC=01-00-5e-xx-xx-xx, DIP= 224.0.0.x and non-IGMP	1'b0
	5[6:5]	46[6:5]	R/W	UNIPM_MODE[1:0] Unknown IP Multicast Data Mode 2'b00 : discard 2'b01 : forward to CPU 2'b10 : flood packet 2'b11 : forward to router port Note – IP multicast data packet: DMAC=01-00-5e-xx-xx-xx and DIP=outside 224.0.0.x	2'b11
	5[4]	46[4]	R/W	DISCARD_LEAVE Discard IGMP leave message 0:Disabled 1:Enabled	1'b0
	5[3]	46[3]	R/W	FLOOD_RPT Flood report message to other ports 0:Disabled 1:Enabled	1'b0
	5[2]	46[2]	R/W	LRP_NULL_SIP Learn router port even if source IP address is 0.0.0.0 0:Disable 1:Enable It is valid only if LEARN_RP is enabled	1'b0

PHY	MII	ROM	R/W	Description	Default
	5[1]	46[1]	R/W	LEARN_RP Learn Router Port 0: Disable (default) 1: Enable	pin_21 (0)
	5[0]	46[0]	R/W	HW_IGMP_EN Hardware IGMP Enable 0:Disable (default) 1:Enable	pin_21 (0)

5.5.2 Router Port Timeout

PHY	MII	ROM	R/W	Description	Default
21	6[15:8]	47[7:0]	R/W	ROUTER_TIMEOUT_VLE[7:0] Router Timeout Value Router Timeout = ROUTER_TIMEOUT_UNIT * ROUTER_TIMEOUT_VLE	*
	6[7:6]	48[7:6]	R/W	ROUTER_TIMEOUT_UNIT[1:0] 2'b00: 1 second 2'b01: 2 second 2'b10: 4 second 2'b11: 8 second	*
	6[5:0]	48[5:0]	R/W	DEFAULT_ROUTER_PORT[5:0] bit0: port 0 bit1: port 1 bit2: port 2 bit3: port 3 bit4: port 4 bit5: port 5	6'b000000

5.5.3 IGMP Group Timeout

PHY	MII	ROM	R/W	Description	Default
21	7[15:8]	49[7:0]	R/W	IGMP_TIMEOUT_VLE[7:0] IGMP Timeout Value IGMP Timeout = IGMP_TIMEOUT_UNIT * IGMP_TIMEOUT_VLE	*
	7[1:0]	50[1:0]	R/W	IGMP_TIMEOUT_UNIT[1:0] IGMP Timeout Unit 2'b00: 1 second 2'b01: 2 second 2'b10: 4 second 2'b11: 8 second	*

5.6 Rate Control

5.6.1 Basic Rate Setting Register

PHY	MII	ROM	R/W	Description	Default
21	8[7]	--		RESERVED	1'b0
	8[6:0]	--	R/W	BW_TI[6:0] Rate control time interval. Only used by egress port and output queue unit : millisecond	7'h01
	9[15:0]	--	R/W	BW_MBS[15:0] Rate control Maximum Burst Size Expressed in byte.	16'h 0000
	10[15:0]	--	R/W	BW_CREDIT_SIZE[15:0] Credit size to accumulate the bucket in per time interval. Expressed in byte.	16'h 0000

5.6.2 Rate Setting Access Control Register

PHY	MII	ROM	R/W	Description	Default
21	12[2:0]	--	R/W	BW_PORT[2:0] Port number for setting bandwidth rate.	3'h0
	12[3]	--	R/W	BW_IOE Bandwidth rate setting is on ingress or egress port 0: ingress port (default) 1: egress port	1'b0
	12[5:4]	--	R/W	BW_QUEUE[1:0] Assign the egress output queue number for setting rate control value 2'b00:egress port (default) 2'b01:queue 1 2'b10:queue 2 2'b11:queue 3	2'b00
	12[8]	--	R/W	BW_RW Rate control data read/write signal 0: read rate control data (default) 1: write rate control data	1'b0
	12[9]	--	R/W (SC)	BW_RW_START Indicates start read/write rate control data of a port, when write a logical "1" to this register. A self cleared register after read/write data done.	1'b0

5.7 Address Table Access Register

5.7.1 Command Register

PHY	MII	ROM	R/W	Description	Default
21	14[15]	--	R/W (SC)	START/DONE To initiate a read or write command when set as 1. Self-cleared after read or write command is finished 1: start access the address table 0: access operation is completed	1'b0
	14[14]	--		RESERVED	1'b0
	14[13]	--	RO	DATA_VALID Data Valid IP175LLF will set this bit to1 to indicate the data is available in "Data Buffer Register" for read operation	1'b0
	14[12:11]	--	R/W	COMMAND[1:0] Address Table Command 2'b00: reserved 2'b01: single write 2'b10: single read 2'b11: reserved	2'b00
	14[10:0]	--	R/W	INDEX The index selects one of address table entries.	11'h000

5.7.2 Data Buffer Register (For Unicast MAC Address)

PHY	MII	ROM	R/W	Description	Default
21	15[15:0]	--	R/W	MAC_ADDR[15:0]	16'h0000
	16[15:0]	--	R/W	MAC_ADDR[31:16]	16'h0000
	17[15:0]	--	R/W	MAC_ADDR[47:32]	16'h0000
	18[15:14]	--	R/W	FILTER_INFO	2'b00
	18[13:10]	--	R/W	PRI_INFO	4'h0
	18[9:6]	--	R/W	FID	4'h0
	18[5:3]	--	R/W	PORT_ID Note – If PORT_ID set to all zero, frame's DMAC matched this entry is discarded.	3'b000
	18[2:0]	--	R/W	AGE Note – Entry is aged out or invalid if this field is all zero.	3'b000
	19[15:2]			RESERVED	
	19[1]	--	R/W	STATIC Entry is static and can not overwrite or aged out.	1'b0
	19[0]	--	R/W	RESERVED	

5.7.3 Data Buffer Register (For Multicast MAC Address)

PHY	MII	ROM	R/W	Description	Default
21	15[15:0]	--	R/W	MAC_ADDR[15:0]	16'h0000
	16[15:0]	--	R/W	MAC_ADDR[31:16]	16'h0000
	17[15:0]	--	R/W	MAC_ADDR[47:32]	16'h0000

PHY	MII	ROM	R/W	Description	Default
	18[15:14]	--	R/W	FILTER_INFO	2'b00
	18[13:10]	--	R/W	PRI_INFO	4'h0
	18[9:6]	--	R/W	FID	4'h0
	18[5:0]	--	R/W	PORT_MAP Note –If PORT_MAP set to all zero, frame's DMAC matched this entry is discarded.	6'h0
	19[15:2]			RESERVED	
	19[1]	--	R/W	VALID Entry is valid.	1'b0
	19[0]	--	R/W	IGMP This bit shall set to 0.	1'b0

5.7.4 Data Buffer Register (For IP Multicast Address)

PHY	MII	ROM	R/W	Description	Default
21	15[15:0]	--	R/W	MAC_ADDR[15:0]	16'h0000
	16[15:14]	--	R/W	TIMEOUT_P2[1:0]	2'b00
	16[13:11]	--	R/W	TIMEOUT_P1[2:0]	3'b000
	16[10:8]	--	R/W	TIMEOUT_P0[2:0]	3'b000
	16[7]	--	R/W	MAC_ADDR[23] This bit shall be set to 0.	1'b0
	16[6:0]	--	R/W	MAC_ADDR[22:16]	7'h0
	17[15:10]			RESERVED	
	17[9:7]	--	R/W	TIMEOUT_P5[2:0]	3'b000
	17[6:4]	--	R/W	TIMEOUT_P4[2:0]	3'b000
	17[3:1]	--	R/W	TIMEOUT_P3[2:0]	3'b000
	17[0]	--	R/W	TIMEOUT_P2[2]	1'b0
	18[15:14]	--	R/W	FILTER_INFO	2'b00
	18[13:10]	--	R/W	PRI_INFO	4'h0
	18[9:6]	--	R/W	FID	4'h0
	18[5:0]	--	R/W	PORT_MAP Note – If PORT_MAP set to all zero, frame's DMAC matched this entry is discarded.	6'h0
	19[15:2]			RESERVED	
	19[1]	--	R/W	VALID Entry is valid.	1'b0
	19[0]	--	R/W	IGMP This bit shall set to 1.	1'b1

5.8 CPU Interrupt Register

5.8.1 CPU Interrupt Control Register

PHY	MII	ROM	R/W	Description	Default
21	20[15]	--	R/W	INIT_HIGH Interrupt signal is active high. 1: active high 0: active low	1'b0

5.8.2 Loop detection enable Register

PHY	MII	ROM	R/W	Description	Default
21	20[7:4]	--		Reserved	
	20[3]	--	R/W	Loop Detection Enable 1: enable 0: disable(default)	1'b0
	20[2:0]	--		Reserved	

5.8.3 Loop port indicator Register

PHY	MII	ROM	R/W	Description	Default
21	21[7:4]	--	RO (SC)	Loop port indicator When the cpu read loop port indicator register, IP175LLF will enable the rx/tx ability of all port and clear loop port indicator status. [7] indcates port 3 [6] indcates port 2 [5] indcates port 1 [4] indicates port 0	4'h0
	21[3]	--	RO (SC)	It indicates any of port 0~4 is loop	1'b0
	21[2]	--	RO (SC)	It indcates port 4 is loop	1'b0
	21[1:0]	--		Reserved	1'b0

5.9 Miscellaneous Control Register

PHY	MII	ROM	R/W	Description	Default
21	22[15]			RESERVED	
	22[14]	51[6]	R/W	REDUCE_IPG This function reduce the IPG by random from 0~20 PPM 1: enable 0: disable	*
	22[13]	51[5]	R/W	TWOPARTD Reset the inter-frame-gap counter to zero, if the CRS signal asserted during the two third of IPG period. 1: enable 0 disable	1'b1
	22[12]	51[4]	R/W	HP_DIS_FLOW_EN High priority packet to disable flow control 1: a port will disable its flow control function for 2 sec if it receives a high priority packet. 0: the function is disabled	1'b0
	22[11:10]	51[3:2]	R/W	DRIVE[1:0] Pad driving capability selection 00: 4 mA 01: 8 mA 10: 12 mA 11: 16 mA	2'b01
	22[9:8]			RESERVED	
	22[3]	50[5]	R/W	LINK_Q_EN,LINK quality enable 1:enable (default) 0:disable	pin_101 (1)
	22[2]	50[4]	R/W	TB31_EN Turbo MII0 31.25MHZ output enable 1: Turbo MII mode (MII0) output 31.25MHZ MIICLK 0: Turbo MII mode (MII0) output 50MHZ MIICLK	1'b0
	22[1]	50[3]	R/W	STAG_TX_EN Special tagging for TX enable 1: enable 0: disable	1'b0
	22[0]	50[2]	R/W	STAG_RX_EN Special tagging for RX enable 1: enable 0: disable	1'b0

PHY	MII	ROM	R/W	Description		Default
Reserved register (It is for testing only and is not released to users)						
21	23[12]	52[7]	R/W	PHY_TEST_PIN_SETTING_5		*
	23[11]	52[6]	R/W	PHY_TEST_PIN_SETTING_2		*
				Default Value		
				TEST2=0	TEST2=1	
				0	Pin 79 (0)	
	23[10]	52[5]	R/W	PHY_TEST_PIN_SETTING_3		*
	23[9]	52[4]	R/W	PHY_TEST_PIN_SETTING_4		*
	23[8]	52[3]	R/W	PHY_TEST_PIN_SETTING_0		*
	23[7]	52[2]	R/W	PHY_TEST_PIN_SETTING_6		*
	23[6]	52[1]	R/W	PHY_TEST_PIN_SETTING_1		*
	23[5:0]	53[5:0]	R/W	TMOD_SEL[5:0]		*

PHY	MII	ROM	R/W	Description	Default
21	24[7:2]	54[7:2]	R/W	FLOOD_FRM[5:0] Flood frame for each port	6'h00
	24[1]	--	RO	FAST Fast mode for simulation, 1: Fast mode, 0: normal mode	*
	24[0]	54[0]	R/W	ALLPASS Receive all incoming frame with error.	1'b0

5.10 CRC Counter

PHY	MII	ROM	R/W	Description	Default
21	25[15:8]			RESERVED	
	25 [7:0]	--	RO (SC)	CRC_COUNTER[7:0] CRC counter which accumulates the CRC number of all ports. Any port received a frame with CRC error will increase this counter by 1. Self-clear after read.	8'h00

5.11 VLAN Group Control Register

5.11.1 VLAN Classification

PHY	MII	ROM	R/W	Description	Default
22	0[15]	--	R/W (SC)	VLAN_TABLE_CLR Clear the contents of VLAN TABLE register 1: clear register 0: do nothing (default) Self-clear after set and register cleared	1'b0
	0[14]			RESERVED	
	0[13:12]	55[7:6]	R/W	UNVID_MODE[1:0] Unknown-VID Mode 2'b00 : discard 2'b01 : forward to CPU 2'b10 : flood packet 2'b11 : reserved	2'b00
	0[11:6]	55[5:0]	R/W	VLAN_CLS[5:0] VLAN Classification associated with each port Only active at tagged-based VLAN 0 : use VID to classify VLAN -use VID to search VLAN table if tag packet -use PVID to search VLAN table if untag packet 1 : use PVID to classify VLAN -always use PVID to search VLAN table	6'h00
	0[5:0]	56[5:0]	R/W	VLAN_MODE[5:0] VLAN Mode setting associated with each port 0 : Port-based VLAN (default) 1 : Tagged-based VLAN	6'h00

5.11.2 VLAN Ingress Rule

PHY	MII	ROM	R/W	Description	Default
22	1[15:12]			RESERVED	
	1[11]	57[3]	R/W	VLAN_DROP_CFI Drop incoming frame, if the CFI field is not equal to zero.	1'b0
	1[10:8]	57[2:0]	R/W	RSVD_VID[2:0] Reserved VID	3'b100
				Bit 0: The null VID. If set, frames with null VID (priority-tagged frame) treat as untagged frames. 0: disable (default) 1: enable	
				Bit 1: VID=1 (default VID) Replace default VID with PVID 0: disable (default) 1: enable	
				Bit 2: VID=FFF Discard frame if the VID is the value FFF 0: disable 1: enable (default)	
	1[7:6]	58[7:6]	R/W	ACCEPTABLE_FRM_TYPE[1:0] Acceptable Frame Type 2'b00 Admit all frames (default) 2'b01 Admit VLAN-tagged frames 2'b10 Admit Untagged frames 2'b11 Reserved	2'b00
	1[5:0]	58[5:0]	R/W	VLAN_INGRESS_FILTER[5:0] VLAN Ingress Filter associated with each port If ingress filter for a given port is set, frame shall discard on that port whose VLAN classification does not include that port in it member set.	6'h3F

5.11.3 VLAN Egress Rule

PHY	MII	ROM	R/W	Description	Default
22	2[15:12]			RESERVED	
	2[11:6]	59[5:0]	R/W	IGMP_IGNORE_MEMBER[5:0] IGMP Ignore member set Ignore member set for frame with DMAC inside 01-00-5e-xx-xx-xx	*
	2[5:0]	60[5:0]	R/W	KEEP_TAG[5:0] (QinQ register) Keep VLAN Tag Header 0: Disabled 1: Keep VLAN tag header from frame. If frames transmission on a egress port tags frame, the frame may contain two tag headers	6'h00

5.11.4 Default VLAN Information

PHY	MII	ROM	R/W	Description	Default

PHY	MII	ROM	R/W	Description	Default
22	3[15:0]	62[7:0] 61[7:0]	R/W	TPID_VALUE[15:0] 802.1Q Tag Protocol Type	16'h8100

PHY	MII	ROM	R/W	Description	Default
22	4[15:0]	64[7:0] 63[7:0]	R/W	VLAN_INFO_0. Port 0 default VLAN information value (PVID_0)	16'h0001
	5[15:0]	66[7:0] 65[7:0]	R/W	VLAN_INFO_1. Port 1 default VLAN information value (PVID_1)	16'h0001
	6[15:0]	68[7:0] 67[7:0]	R/W	VLAN_INFO_2. Port 2 default VLAN information value (PVID_2)	16'h0001
	7[15:0]	70[7:0] 69[7:0]	R/W	VLAN_INFO_3. Port 3 default VLAN information value (PVID_3)	16'h0001
	8[15:0]	72[7:0] 71[7:0]	R/W	VLAN_INFO_4. Port 4 default VALN information value (PVID_4)	16'h0001
	9[15:0]	74[7:0] 73[7:0]	R/W	VLAN_INFO_5. Port 5 default VALN information value (PVID_5)	16'h0001

5.11.5 VLAN Table

5.11.5.1 VLAN Control Register

PHY	MII	ROM	R/W	Description	Default
22	10[15:0]	76[7:0] 75[7:0]	R/W	VLAN_VALID[15:0] VALN filter is valid. The VALN filter entry X is valid associated with the VID_X.	16'h 0000
	11[15:0]	78[7:0] 77[7:0]	R/W	QU_NUM_EN[15:0] Assign new queue number enable Assign a new queue number which defined in PRI_NUM_X register associated with the VID_X.	16'h00 00
	12[15:0]	80[7:0] 79[7:0]	R/W	STP_IDX_EN[15:0] Spanning Tree Protocol Index Enable	16'h00 00
	13[15:0]	82[7:0] 81[7:0]	R/W	REW_VLAN_PRI_EN[15:0] Re-write VLAN priority field Enable	16'h00 00

5.11.5.2 VLAN Identifier Register

PHY	MII	ROM	R/W	Description	Default
22	14[15:12]	84[7:4]	R/W	FID_0[3:0] VLAN field identifier associated with VALN 0.	4'h0
	14[11:0]	84[3:0] 83[7:0]	R/W	VID_0[11:0] VLAN identifier associated with VALN 0.	12'h001
	15[15:12]	86[7:4]	R/W	FID_1[3:0] VLAN field identifier associated with VALN 1.	4'h0
	15[11:0]	86[3:0] 85[7:4]	R/W	VID_1[11:0] VLAN identifier associated with VALN 1.	12'h002
	16[15:12]	88[7:4]	R/W	FID_2[3:0] VLAN field identifier associated with VALN 2.	4'h0
	16[11:0]	88[3:0] 87[7:0]	R/W	VID_2[11:0] VLAN identifier associated with VALN 2.	12'h003
	17[15:12]	90[7:4]	R/W	FID_3[3:0] VLAN field identifier associated with VALN 3.	4'h0
	17[11:0]	90[3:0] 89[7:0]	R/W	VID_3[11:0] VLAN identifier associated with VALN 3.	12'h004
	18[15:12]	92[7:4]	R/W	FID_4[3:0] VLAN field identifier associated with VALN 4.	4'h0
	18[11:0]	92[3:0] 91[7:0]	R/W	VID_4[11:0] VLAN identifier associated with VALN 4.	12'h005
	19[15:12]	94[7:4]	R/W	FID_5[3:0] VLAN field identifier associated with VALN 5.	4'h0
	19[11:0]	94[3:0] 93[7:0]	R/W	VID_5[11:0] VLAN identifier associated with VALN 5.	12'h006
	20[15:12]	96[7:4]	R/W	FID_6[3:0] VLAN field identifier associated with VALN 6.	4'h0
	20[11:0]	96[3:0[95[7:0]	R/W	VID_6[11:0] VLAN identifier associated with VALN 6.	12'h007
	21[15:12]	98[7:4]	R/W	FID_7[3:0] VLAN field identifier associated with VALN 7.	4'h0

PHY	MII	ROM	R/W	Description	Default
	21[11:0]	98[3:0] 97[7:0]	R/W	VID_7[11:0] VLAN identifier associated with VALN 7.	12'h008
	22[15:12]	100[7:4]	R/W	FID_8[3:0] VLAN field identifier associated with VALN 8.	4'h0
	22[11:0]	100[3:0] 99[7:0]	R/W	VID_8[11:0] VLAN identifier associated with VALN 8.	12'h009
	23[15:12]	102[7:4]	R/W	FID_9[3:0] VLAN field identifier associated with VALN 9.	4'h0
	2311:0]	102[3:0] 101[7:0]	R/W	VID_9[11:0] VLAN identifier associated with VALN 9.	12'h00A
22	24[15:12]	104[7:4]	R/W	FID_A[3:0] VLAN field identifier associated with VALN A.	4'h0
	24[11:0]	104[3:0] 103[7:0]	R/W	VID_A[11:0] VLAN identifier associated with VALN A.	12'h00B
	25[15:12]	106[7:4]	R/W	FID_B[3:0] VLAN field identifier associated with VALN B.	4'h0
	25[11:0]	105[3:0] 105[7:0]	R/W	VID_B[11:0] VLAN identifier associated with VALN B.	12'h00C
	26[15:12]	108[7:4]	R/W	FID_C[3:0] VLAN field identifier associated with VALN C.	4'h0
	26[11:0]	108[3:0] 107[7:0]	R/W	VID_C[11:0] VLAN identifier associated with VALN C.	12'h00D
	27[15:12]	110[7:4]	R/W	FID_D[3:0] VLAN field identifier associated with VALN D.	4'h0
	27[11:0]	110[3:0] 109[7:0]	R/W	VID_D[11:0] VLAN identifier associated with VALN D.	12'h00E
	28[15:12]	112[7:4]	R/W	FID_E[3:0] VLAN field identifier associated with VALN E.	4'h0
	28[11:0]	112[3:0] 111[7:0]	R/W	VID_E[11:0] VLAN identifier associated with VALN E.	12'h00F
	29[15:12]	114[7:4]	R/W	FID_F[3:0] VLAN field identifier associated with VALN F.	4'h0
	29[11:0]	114[3:0] 113[7:0]	R/W	VID_F[11:0] VLAN identifier associated with VALN F.	12'h010

5.11.5.3 VLAN Member Register

PHY	MII	ROM	R/W	Description	Default
23	0[5:0]	115[5:0]	R/W	VLAN_MEMBER_0[5:0] VLAN member port VLAN member port associated with the VID_0.	6'h3F
	0[13:8]	116[5:0]	R/W	VLAN_MEMBER_1[5:0] VLAN member port VLAN member port associated with the VID_1.	6'h3F
	1[5:0]	117[5:0]	R/W	VLAN_MEMBER_2[5:0] VLAN member port VLAN member port associated with the VID_2.	6'h3F

PHY	MII	ROM	R/W	Description	Default
	1[13:8]	118[5:0]	R/W	VLAN_MEMBER_3[5:0] VLAN member port VLAN member port associated with the VID_3.	6'h3F
	2[5:0]	119[5:0]	R/W	VLAN_MEMBER_4[5:0] VLAN member port VLAN member port associated with the VID_4.	6'h3F
	2[13:8]	120[5:0]	R/W	VLAN_MEMBER_5[5:0] VLAN member port VLAN member port associated with the VID_5.	6'h3F
23	3[5:0]	121[5:0]	R/W	VLAN_MEMBER_6[5:0] VLAN member port VLAN member port associated with the VID_6.	6'h00
	3[13:8]	122[5:0]	R/W	VLAN_MEMBER_7[5:0] VLAN member port VLAN member port associated with the VID_7.	6'h00
	4[5:0]	123[5:0]	R/W	VLAN_MEMBER_8[5:0] VLAN member port VLAN member port associated with the VID_8.	6'h00
	4[13:8]	124[5:0]	R/W	VLAN_MEMBER_9[5:0] VLAN member port VLAN member port associated with the VID_9.	6'h00
	5[5:0]	125[5:0]	R/W	VLAN_MEMBER_A[5:0] VLAN member port VLAN member port associated with the VID_A.	6'h00
	5[13:8]	126[5:0]	R/W	VLAN_MEMBER_B[5:0] VLAN member port VLAN member port associated with the VID_B.	6'h00
	6[5:0]	127[5:0]	R/W	VLAN_MEMBER_C[5:0] VLAN member port VLAN member port associated with the VID_C.	6'h00
	6[13:8]	128[5:0]	R/W	VLAN_MEMBER_D[5:0] VLAN member port VLAN member port associated with the VID_D.	6'h00
	7[5:0]	129[5:0]	R/W	VLAN_MEMBER_E[5:0] VLAN member port VLAN member port associated with the VID_E.	6'h00
	7[13:8]	130[5:0]	R/W	VLAN_MEMBER_F[5:0] VLAN member port VLAN member port associated with the VID_F.	6'h00

5.11.5.4 Add Tag Control Register

PHY	MII	ROM	R/W	Description		Default
23	8[5:0]	131[5:0]	R/W	ADD_TAG_0[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_0.		6'b 000000
				Bit 0	1: port 0 adds a VLAN tag to each outgoing packet. 0: port 0 doesn't add a VLAN tag.	
				Bit 1	1: port 1 adds a VLAN tag to each outgoing packet. 0: port 1 doesn't add a VLAN tag.	
				Bit 2	1: port 2 adds a VLAN tag to each outgoing packet. 0: port 2 doesn't add a VLAN tag.	
				Bit 3	1: port 3 adds a VLAN tag to each outgoing packet. 0: port 3 doesn't add a VLAN tag.	
				Bit 4	1: port 4 adds a VLAN tag to each outgoing packet. 0: port 4 doesn't add a VLAN tag.	
				Bit 5	1: port 5 adds a VLAN tag to each outgoing packet. 0: port 5 doesn't add a VLAN tag.	
23	8[13:8]	132[5:0]	R/W	ADD_TAG_1[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_1.		6'b 000000
	9[5:0]	133[5:0]	R/W	ADD_TAG_2[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_2.		6'b 000000
	9[13:8]	134[5:0]	R/W	ADD_TAG_3[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_3.		6'b 000000
	10[5:0]	135[5:0]	R/W	ADD_TAG_4[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_4.		6'b 000000
	10[13:8]	136[5:0]	R/W	ADD_TAG_5[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_5.		6'b 000000
	11[5:0]	137[5:0]	R/W	ADD_TAG_6[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_6.		6'b 000000
	11[13:8]	138[5:0]	R/W	ADD_TAG_7[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_7.		6'b 000000

PHY	MII	ROM	R/W	Description	Default
	12[5:0]	139[5:0]	R/W	ADD_TAG_8[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_8.	6'b 000000
	12[13:8]	140[5:0]	R/W	ADD_TAG_9[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_9.	6'b 000000
	13[5:0]	141[5:0]	R/W	ADD_TAG_A[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_A.	6'b 000000
	13[13:8]	142[5:0]	R/W	ADD_TAG_B[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_B.	6'b 000000
23	14[5:0]	143[5:0]	R/W	ADD_TAG_C[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_C.	6'b 000000
	14[13:8]	144[5:0]	R/W	ADD_TAG_D[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_D.	6'b 000000
	15[5:0]	145[5:0]	R/W	ADD_TAG_E[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_E.	6'b 000000
	15[13:8]	146[5:0]	R/W	ADD_TAG_F[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_F.	6'b 000000

5.11.5.5 Remove Tag Control Register

PHY	MII	ROM	R/W	Description		Default
23	16[5:0]	147[5:0]	R/W	REMOVE_TAG_0[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_0.		6'b 000000
				Bit 0	1: port 0 removes the VLAN tag of each outgoing packet. 0: port 0 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 1	1: port 1 removes the VLAN tag of each outgoing packet. 0: port 1 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 2	1: port 2 removes the VLAN tag of each outgoing packet. 0: port 2 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 3	1: port 3 removes the VLAN tag of each outgoing packet. 0: port 3 doesn't remove the VLAN tag of each outgoing packet.	
				Bit 4	1: port 4 removes the VLAN tag of each outgoing packet. 0: port 4 doesn't remove the VLAN tag of each outgoing packet.	

PHY	MII	ROM	R/W	Description	Default
				Bit 5 1: port 5 removes the VLAN tag of each outgoing packet. 0: port 5 doesn't remove the VLAN tag of each outgoing packet.	
	16[13:8]	148[5:0]	R/W	REMOVE_TAG_1[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_1.	6'b 000000
	17[5:0]	149[5:0]	R/W	REMOVE_TAG_2[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_2.	6'b 000000
	17[13:8]	150[5:0]	R/W	REMOVE_TAG_3[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_3.	6'b 000000
	18[5:0]	151[5:0]	R/W	REMOVE_TAG_4[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_4.	6'b 000000
	18[13:8]	152[5:0]	R/W	REMOVE_TAG_5[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_5.	6'b 000000
	19[5:0]	153[5:0]	R/W	REMOVE_TAG_6[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_6.	6'b 000000
	19[13:8]	154[5:0]	R/W	REMOVE_TAG_7[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_7.	6'b 000000
	20[5:0]	155[5:0]	R/W	REMOVE_TAG_8[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_8.	6'b 000000
	20[13:8]	156[5:0]	R/W	REMOVE_TAG_9[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_9.	6'b 000000
	21[5:0]	1575:0]	R/W	REMOVE_TAG_A[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_A.	6'b 000000
	21[13:8]	158[5:0]	R/W	REMOVE_TAG_B[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_B.	6'b 000000

PHY	MII	ROM	R/W	Description	Default
	22[5:0]	159[5:0]	R/W	REMOVE_TAG_C[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_C.	6'b 000000
	22[13:8]	160[5:0]	R/W	REMOVE_TAG_D[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_D.	6'b 000000
	23[5:0]	161[5:0]	R/W	REMOVE_TAG_E[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_E.	6'b 000000
	23[13:8]	162[5:0]	R/W	REMOVE_TAG_F[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_F.	6'b 000000

5.11.5.6 VLAN Miscellaneous Register

PHY	MII	ROM	R/W	Description		Default
23	24[7:0]	163[7:0]	R/W	VLAN_MISC_0[7:0] VLAN Miscellaneous Registers 0		8'h00
				Bit 1-0	STP_IDX[1:0] Spanning Tree Index This registers is effective only STP_IDX_EN[0] is enabled	
				Bit 3-2	QU_NUM[1:0] Priority Queue Number This registers is effective only QU_NUM_EN[0] is enabled	
				Bit 4	LEARN_DIS Learning Disable	
				Bit 7-5	REW_VLAN_PRI[2:0] Rewrite VLAN priority value This registers is effective only REW_VLAN_PRI_EN[0] is enabled	
	24[15:8]	164[7:0]	R/W	VLAN_MISC_1[7:0] VLAN Miscellaneous Registers 1		8'h00
	25[7:0]	165[7:0]	R/W	VLAN_MISC_2[7:0] VLAN Miscellaneous Registers 2		8'h00
	25[15:8]	166[7:0]	R/W	VLAN_MISC_3[7:0] VLAN Miscellaneous Registers 3		8'h00
	26[7:0]	167[7:0]	R/W	VLAN_MISC_4[7:0] VLAN Miscellaneous Registers 4		8'h00
	26[15:8]	168[7:0]	R/W	VLAN_MISC_5[7:0] VLAN Miscellaneous Registers 5		8'h00
	27[7:0]	169[7:0]	R/W	VLAN_MISC_6[7:0] VLAN Miscellaneous Registers 6		8'h00
	27[15:8]	170[7:0]	R/W	VLAN_MISC_7[7:0] VLAN Miscellaneous Registers 7		8'h00

PHY	MII	ROM	R/W	Description	Default
	28[7:0]	171[7:0]	R/W	VLAN_MISC_8[7:0] VLAN Miscellaneous Registers 8	8'h00
	28[15:8]	172[7:0]	R/W	VLAN_MISC_9[7:0] VLAN Miscellaneous Registers 9	8'h00
	29[7:0]	173[7:0]	R/W	VLAN_MISC_A[7:0] VLAN Miscellaneous Registers A	8'h00
	29[15:8]	174[7:0]	R/W	VLAN_MISC_B[7:0] VLAN Miscellaneous Registers B	8'h00
	30[7:0]	175[7:0]	R/W	VLAN_MISC_C[7:0] VLAN Miscellaneous Registers C	8'h00
23	30[15:8]	176[7:0]	R/W	VLAN_MISC_D[7:0] VLAN Miscellaneous Registers D	8'h00
	31[7:0]	177[7:0]	R/W	VLAN_MISC_E[7:0] VLAN Miscellaneous Registers E	8'h00
	31[15:8]	178[7:0]	R/W	VLAN_MISC_F[7:0] VLAN Miscellaneous Registers F	8'h00

5.11.5.7 Spanning Tree Table

PHY	MII	ROM	R/W	Description	Default
24	0[13:8]	179[5:0]	R/W	STP_FORWARD_EN_0[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	0[5:0]	180[5:0]	R/W	STP_LEARNING_EN_0[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
	1[13:8]	181[5:0]	R/W	STP_FORWARD_EN_1[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	1[5:0]	182[5:0]	R/W	STP_LEARNING_EN_1[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
	2[13:8]	183[5:0]	R/W	STP_FORWARD_EN_2[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	2[5:0]	184[5:0]	R/W	STP_LEARNING_EN_2[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
	3[13:8]	185[5:0]	R/W	STP_FORWARD_EN_3[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	3[5:0]	186[5:0]	R/W	STP_LEARNING_EN_3[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111

5.12 Quality of Service (QOS)

5.12.1 Priority Classification

5.12.1.1 Base Control Register

PHY	MII	ROM	R/W	Description	Default
25	0[15]	187[7]	R/W	LP_OVER_DSCP Logical port takes a high precedence than DSCP priority.	1'b0
	0[14]	187[6]	R/W	TOS_OVER_VLAN_PRI IP frame take a higher precedence than VLAN priority. That is the IP frame's priority is over the frame with VLAN tagged.	1'b0
	0[13:8]	187[5:0]	R/W	COS_EN[5:0] Class of service enable for each port 1: enable 0: disabled (default)	*
	0[7]	188[7]	R/W	USER_DEF_PRI User Define Priority	1'b0
	0[6]			RESERVED	
	0[5:0]	188[5:0]	R/W	PORT_PRI_EN[5:0] Port based priority function enable control registers for each port.	*

5.12.1.2 Port Priority Map

PHY	MII	ROM	R/W	Description	Default
25	1[1:0]	189[1:0]	R/W	P0_PRI[1:0] Port 0 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[3:2]	189[3:2]	R/W	P1_PRI[1:0] Port 1 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[5:4]	189[5:4]	R/W	P2_PRI[1:0] Port 2 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[7:6]	189[7:6]	R/W	P3_PRI[1:0] Port 3 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11

25	1[9:8]	190[1:0]	R/W	P4_PRI[1:0] Port 4 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[11:10]	190[3:2]	R/W	P5_PRI[1:0] Port 0 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11

5.12.1.3 VLAN Priority Map

PHY	MII	ROM	R/W	Description	Default
25	2[15:14]	191[7:6]	R/W	VLAN_PRI7 Priority map when the VLAN priority is 7	2'b00
	2[13:12]	191[5:4]	R/W	VLAN_PRI6 Priority map when the VLAN priority is 6	2'b00
	2[11:10]	191[3:2]	R/W	VLAN_PRI5 Priority map when the VLAN priority is 5	2'b00
	2[9:8]	191[1:0]	R/W	VLAN_PRI4 Priority map when the VLAN priority is 4	2'b00
	2[7:6]	192[7:6]	R/W	VLAN_PRI3 Priority map when the VLAN priority is 3	2'b00
	2[5:4]	192[5:4]	R/W	VLAN_PRI2 Priority map when the VLAN priority is 2	2'b00
	2[3:2]	192[3:2]	R/W	VLAN_PRI1 Priority map when the VLAN priority is 1	2'b00
	2[1:0]	192[1:0]	R/W	VLAN_PRI0 Priority map when the VLAN priority is 0	2'b00

5.12.1.4 TOS/DSCP Priority Map

PHY	MII	ROM	R/W	Description	Default
25	3[15:14]	193[7:6]	R/W	DSCP_7 Priority map when the DSCP field is 7	2'b00
	3[13:12]	193[5:4]	R/W	DSCP_6 Priority map when the DSCP field is 6	2'b00
	3[11:10]	193[3:2]	R/W	DSCP_5 Priority map when the DSCP field is 5	2'b00
	3[9:8]	193[1:0]	R/W	DSCP_4 Priority map when the DSCP field is 4	2'b00
	3[7:6]	194[7:6]	R/W	DSCP_3 Priority map when the DSCP field is 3	2'b00
	3[5:4]	194[5:4]	R/W	DSCP_2 Priority map when the DSCP field is 2	2'b00
	3[3:2]	194[3:2]	R/W	DSCP_1 Priority map when the DSCP field is 1	2'b00

	3[1:0]	194[1:0]	R/W	DSCP_0 (Best Effort) Priority map when the DSCP field is 0	2'b00
	4[15:14]	195[7:6]	R/W	DSCP_F Priority map when the DSCP field is F	2'b00
	4[13:12]	195[5:4]	R/W	DSCP_E (AF13) Priority map when the DSCP field is E	2'b00
	4[11:10]	195[3:2]	R/W	DSCP_D Priority map when the DSCP field is D	2'b00
	4[9:8]	195[1:0]	R/W	DSCP_C (AF12) Priority map when the DSCP field is C	2'b00
25	4[7:6]	196[7:6]	R/W	DSCP_B Priority map when the DSCP field is B	2'b00
	4[5:4]	196[5:4]	R/W	DSCP_A (AF11) Priority map when the DSCP field is A	2'b11
	4[3:2]	196[3:2]	R/W	DSCP_9 Priority map when the DSCP field is 9	2'b00
	4[1:0]	196[1:0]	R/W	DSCP_8 (CS1) Priority map when the DSCP field is 8	2'b00
	5[15:14]	197[7:6]	R/W	DSCP_17 Priority map when the DSCP field is 17	2'b00
	5[13:12]	197[5:4]	R/W	DSCP_16 (AF23) Priority map when the DSCP field is 16	2'b00
	5[11:10]	197[3:2]	R/W	DSCP_15 Priority map when the DSCP field is 15	2'b00
	5[9:8]	197[1:0]	R/W	DSCP_14 (AF22) Priority map when the DSCP field is 14	2'b00
	5[7:6]	198[7:6]	R/W	DSCP_13 Priority map when the DSCP field is 13	2'b00
	5[5:4]	198[5:4]	R/W	DSCP_12 (AF21) Priority map when the DSCP field is 12	2'b11
	5[3:2]	198[3:2]	R/W	DSCP_11 Priority map when the DSCP field is 11	2'b00
	5[1:0]	198[1:0]	R/W	DSCP_10 (CS2) Priority map when the DSCP field is 10	2'b00
	6[15:14]	199[7:6]	R/W	DSCP_1F Priority map when the DSCP field is 1F	2'b00
	6[13:12]	199[5:4]	R/W	DSCP_1E (AF33) Priority map when the DSCP field is 1E	2'b00
	6[11:10]	199[3:2]	R/W	DSCP_1D Priority map when the DSCP field is 1D	2'b00
	6[9:8]	199[1:0]	R/W	DSCP_1C (AF32) Priority map when the DSCP field is 1C	2'b00
	6[7:6]	200[7:6]	R/W	DSCP_1B Priority map when the DSCP field is 1B	2'b00
	6[5:4]	200[5:4]	R/W	DSCP_1A (AF31) Priority map when the DSCP field is 1A	2'b11

	6[3:2]	200[3:2]	R/W	DSCP_19 Priority map when the DSCP field is 19	2'b00
	6[1:0]	200[1:0]	R/W	DSCP_18 (CS3) Priority map when the DSCP field is 18	2'b00
	7[15:14]	201[7:6]	R/W	DSCP_27 Priority map when the DSCP field is 27	2'b00
	7[13:12]	201[5:4]	R/W	DSCP_26 (AF43) Priority map when the DSCP field is 26	2'b00
	7[11:10]	201[3:2]	R/W	DSCP_25 Priority map when the DSCP field is 25	2'b00
	7[9:8]	201[1:0]	R/W	DSCP_24 (AF42) Priority map when the DSCP field is 24	2'b00
25	7[7:6]	202[7:6]	R/W	DSCP_23 Priority map when the DSCP field is 23	2'b00
	7[5:4]	202[5:4]	R/W	DSCP_22 (AF41) Priority map when the DSCP field is 22	2'b11
	7[3:2]	202[3:2]	R/W	DSCP_21 Priority map when the DSCP field is 21	2'b00
	7[1:0]	202[1:0]	R/W	DSCP_20 (CS4) Priority map when the DSCP field is 20	2'b00
	8[15:14]	203[7:6]	R/W	DSCP_2F Priority map when the DSCP field is 2F	2'b00
	8[13:12]	203[5:4]	R/W	DSCP_2E (EF) Priority map when the DSCP field is 2E	2'b11
	8[11:10]	203[3:2]	R/W	DSCP_2D Priority map when the DSCP field is 2D	2'b00
	8[9:8]	203[1:0]	R/W	DSCP_2C Priority map when the DSCP field is 2C	2'b00
	8[7:6]	204[7:6]	R/W	DSCP_2B Priority map when the DSCP field is 2B	2'b00
	8[5:4]	204[5:4]	R/W	DSCP_2A Priority map when the DSCP field is 2A	2'b00
	8[3:2]	204[3:2]	R/W	DSCP_29 Priority map when the DSCP field is 29	2'b00
	8[1:0]	204[1:0]	R/W	DSCP_28 (CS5) Priority map when the DSCP field is 28	2'b00
	9[15:14]	205[7:6]	R/W	DSCP_37 Priority map when the DSCP field is 37	2'b00
	9[13:12]	205[5:4]	R/W	DSCP_36 Priority map when the DSCP field is 36	2'b00
	9[11:10]	205[3:2]	R/W	DSCP_35 Priority map when the DSCP field is 35	2'b00
	9[9:8]	205[1:0]	R/W	DSCP_34 Priority map when the DSCP field is 34	2'b00
	9[7:6]	206[7:6]	R/W	DSCP_33 Priority map when the DSCP field is 33	2'b00

	9[5:4]	206[5:4]	R/W	DSCP_32 Priority map when the DSCP field is 32	2'b00
	9[3:2]	206[3:2]	R/W	DSCP_31 Priority map when the DSCP field is 31	2'b00
	9[1:0]	206[1:0]	R/W	DSCP_30 (CS6) Priority map when the DSCP field is 30	2'b11
	10[15:14]	207[7:6]	R/W	DSCP_3F Priority map when the DSCP field is 3F	2'b00
	10[13:12]	207[5:4]	R/W	DSCP_3E Priority map when the DSCP field is 3E	2'b00
	10[11:10]	207[3:2]	R/W	DSCP_3D Priority map when the DSCP field is 3D	2'b00
25	10[9:8]	207[1:0]	R/W	DSCP_3C Priority map when the DSCP field is 3C	2'b00
	10[7:6]	208[7:6]	R/W	DSCP_3B Priority map when the DSCP field is 3B	2'b00
	10[5:4]	208[5:4]	R/W	DSCP_3A Priority map when the DSCP field is 3A	2'b00
	10[3:2]	208[3:2]	R/W	DSCP_39 Priority map when the DSCP field is 39	2'b00
	10[1:0]	208[1:0]	R/W	DSCP_38 (CS7) Priority map when the DSCP field is 38	2'b11

5.12.1.5 TCP/UDP Port Priority

PHY	MII	ROM	R/W	Description	Default
25	11[15:8]			RESERVED	
	11[7:6]	209[7:6]	R/W	LP_TYPE Logical Port Type 2'b00 – Logic port priority disable 2'b01 – Source logic port priority enable 2'b10 – Destination logic port priority enable 2'b11 – Source or destination logic port priority enable	2'b11
	11[5:4]	209[5:4]	R/W	USERDEF_RANGE_EN[1:0] User defined logic port range enable. bit[1]: user define range 1 register enable bit[0]: user define range 0 register enable	2'b11
	11[3:0]	209[3:0]	R/W	PREDEF_PORT_EN[3:0] Pre-defined logic port number enable. bit[3]: logic port 3 enable, port 6000 bit[2]: logic port 2 enable, port 3389 bit[1]: logic port 1 enable, port 443 bit[0]: logic port 0 enable, port 22	4'hF
	12[15:0]	211[7:0] 210[7:0]	R/W	PREDEF_PORT_0[15:0] Pre-defined logical port 0. The default value is SSH protocol.	16'h00 16
	13[15:0]	213[7:0] 212[7:0]	R/W	PREDEF_PORT_1[15:0] Pre-defined logical port 1. The default value is HTTPs protocol.	16'h01 BB
	14[15:0]	215[7:0] 214[7:0]	R/W	PREDEF_PORT_2[15:0] Pre-defined logical port 2. The default value is RDP (Windows Remote Desktop Protocol) protocol.	16'h0D 3D
	15[15:0]	217[7:0] 216[7:0]	R/W	PREDEF_PORT_3[15:0] Pre-defined logical port 3. The default value is XWIN protocol.	16'h17 70
	16[15:0]	219[7:0] 218[7:0]	R/W	USERDEF_RANGE0_LOW User defined logic port range 0 low limit	16'h00 17
	17[15:0]	221[7:0] 220[7:0]	R/W	USERDEF_RANGE0_HIGH User defined logic port range 0 high limit The default value is TELNET protocol.	16'h00 17
	18[15:0]	223[7:0] 222[7:0]	R/W	USERDEF_RANGE1_LOW User defined logic port range 1 low limit	16'h16 A8
25	19[15:0]	225[7:0] 224[7:0]	R/W	USERDEF_RANGE1_HIGH User defined logic port range 1 high limit The default value is VNC protocol.	16'h16 A8
	20[15:12]			RESERVED	
	20[11:10]	226[3:2]	R/W	USERDEF_RANGE_1Q[1:0] User defined logic port range 1 transmit priority queue mapping.	2'b10
	20[9:8]	226[1:0]	R/W	USERDEF_RANGE_0Q[1:0] User defined logic port range 0 transmit priority queue mapping.	2'b10

	20[7:6]	227[7:6]	R/W	PREDEF_PORT_3Q[1:0] Pre-defined port 3 transmit priority queue mapping.	2'b10
	20[5:4]	227[5:4]	R/W	PREDEF_PORT_2Q[1:0] Pre-defined port 2 transmit priority queue mapping.	2'b10
	20[3:2]	227[3:2]	R/W	PREDEF_PORT_1Q[1:0] Pre-defined port 1 transmit priority queue mapping.	2'b10
	20[1:0]	227[1:0]	R/W	PREDEF_PORT_0Q[1:0] Pre-defined port 0 transmit priority queue mapping.	2'b10
	21[15:6]			RESERVED	
	21[5:2]	228[5:2]	R/W	PREDEF_PORT_DROP[3:0] Pre-defined logic port drop packet. Drop the incoming packets that match the TCP/UDP port number defined in PREDEF_PORT_0[15:0] to PREDEF_PORT_3[15:0]. Drop ability has the precedence over the frame classify priority. [0] drop packet port number matches PREDEF_PORT_0[15:0] [1] drop packet port number matches PREDEF_PORT_1[15:0] [2] drop packet port number matches PREDEF_PORT_2[15:0] [3] drop packet port number matches PREDEF_PORT_3[15:0]	4'h0
	21[1:0]	228[1:0]	R/W	USERDEF_RANGE_DROP[1:0] User defined logic port drop packet. Drop the incoming packets that match the TCP/UDP port number defined in port range register. [0] USERDEF_RANGE0_LOW~ USERDEF_RANGE0_HIGH [1] USERDEF_RANGE1_LOW~ USERDEF_RANGE1_HIGH Drop ability has the precedence over the frame classify priority.	2'b00

5.12.2 Queue Scheduling Configuration Register

PHY	MII	ROM	R/W	Description	Default
25	22[13]	229[5]	R/W	QOS_OVER_FC QoS over Flow Control	1'b0
	22[12]			RESERVED	
	22[11:10]	229[3:2]	R/W	SCH_TYPE_5[1:0] Queue scheduling configuration of port 5. Q3 Q2 Q1 Q0 2'b00: WRR WRR WRR WRR 2'b01: WFQ WFQ WFQ WFQ(BE) 2'b10: SP WFQ WFQ BE 2'b11: SP SP SP SP WRR: Weight Round Robin WFQ: Weight Far Queuing BE: Best Effort SP: Strictly Priority	2'b00
	22[9:8]	229[1:0]	R/W	SCH_TYPE_4[1:0] Queue scheduling configuration of port 4.	2'b00

	22[7:6]	230[7:6]	R/W	SCH_TYPE_3[1:0] Queue scheduling configuration of port 3.	2'b00
	22[5:4]	230[5:4]	R/W	SCH_TYPE_2[1:0] Queue scheduling configuration of port 2.	2'b00
	22[3:2]	230[3:2]	R/W	SCH_TYPE_1[1:0] Queue scheduling configuration of port 1.	2'b00
	22[1:0]	230[1:0]	R/W	SCH_TYPE_0[1:0] Queue scheduling configuration of port 0.	2'b00

PHY	MII	ROM	R/W	Description	Default
25	23[15:12]	231[7:4]	R/W	Q3_WEIGHT Output queue 3 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets . , 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b1000
	23[11:8]	231[3:0]	R/W	Q2_WEIGHT Output queue 2 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets . , 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b0100
25	23[7:4]	232[7:4]	R/W	Q1_WEIGHT Output queue 1 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets . , 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b0010
	23[3:0]	232[3:0]	R/W	Q0_WEIGHT Output queue 0 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets . , 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b0001

5.13 QoS Multi-Field Classification

5.13.1 Multi-Field Classification Table Control Register

PHY	MII	ROM	R/W	Description	Default
26	0[15]	--	R/W	MF_QOS_EN Multi-Field QoS access control function enabled. When this bit is enabled, switch engine will use Multi-Field registers to classify the incoming frame.	1'b0
	0[10]	--	R/W (SC)	MF_REG_CLR Clear the contents of Multi-Field classification register and Multi-Filed table QOS rate control register. This bit is for programming convenience consideration. When set it will clear all the multi-field registers to zero, excepts the IP mask registers – MF_IP_SA_MASK[3:0] & MF_IP_DA_MASK[3:0]. 1: clear registers 0: do nothing (default) A self-cleared register after set and registers cleared.	1'b0
	0[9]	--	R/W (SC)	MF_CNT_RESET Multi-Field counter reset. When reset, it will reference the setting of MF_RESET_EN register. 1: enable 0: disable	1'b0
	0[8]	--	R/W (SC)	MF_ENTRY_RESET Multi-Field entry reset. When reset, it will reference the setting of MF_RESET_EN register. 1: enable 0: disable	1'b0
	0[7:0]	--	R/W	MF_RESET_EN[7:0] Multi-Filed reset enable for each entry or counter. 1: enable 0: disable	8'h00

5.13.2 Multi-Field Classification Register

PHY	MII	ROM	R/W	Description	Default
26	1[15:14]	--	R/W	MF_CTRL[1:0] Multi-Field entry control registers bit[1]: Filtering/Forwarding - 0: Forward - 1: Filter bit[0]: Traffic Conditioning (QoS Rate control)	2'b00
	1[12]	--	R/W	MF_IP_RANGE Enable the IP address range monitoring function. When enabled, the source and destination IP address register is used as an IP address range monitor register. MF_IM_SA will be a IP address monitor start number MF_IM_DA will be a IP address monitor stop number { MF_IM_DIP, MF_IM_SIP } Monitor type 00 reserved 01 source address 10 destination address 11 source or dest. addr	1'b0
	1[11]	--	R/W	MF_IM_SA_EN IP/MAC source address field enable.	1'b0
	1[10]	--	R/W	MF_IM_SIP IP/MAC source address field is used as an IP address.	1'b0
	1[9:6]	--	R/W	MF_IP_SA_MASK[3:0] IP source address subnet mask. The IP address can be grouped into four groups, each group contains eight bits and represented in decimal format (known as dotted decimal notation). This register is used as a mask to extract the IP address.	4'hF
	1[5]	--	R/W	MF_IM_DA_EN IP/MAC destination address field enable.	1'b0
	1[4]	--	R/W	MF_IM_DIP IP/MAC destination address field is used as an IP address.	1'b0
	1[3:0]	--	R/W	MF_IP_DA_MASK[3:0] IP destination address subnet mask.	4'hF
	2[15:0] 3[15:0] 4[15:0]	--	R/W	MF_IM_SA[47:0] IP/MAC source address. When IP address is in using, only the 32-bits of LSB part will be referenced and ignore the rest. phy26.2= MF_IM_SA[15:0] phy26.3= MF_IM_SA[31:16] phy26.4= MF_IM_SA[47:32]	48'h0
	5[15:0] 6[15:0] 7[15:0]	--	R/W	MF_IM_DA[47:0] IP/MAC destination address. When IP address is in using, only the 32-bits of LSB part will be referenced and ignore the rest. phy26.5= MF_IM_DA[15:0] phy26.6= MF_IM_DA[31:16] phy26.7= MF_IM_DA[47:32]	48'h0

	8[15:0]	--	R/W	MF_ET_VALUE[15:0] EtherType value	16'h0000
	9[15]	--	R/W	MF_ET_EN EtherType field enable	1'b0
	9[14]			RESERVED	
	9[13:12]	--	R/W	MF_FW_CTRL[1:0] Forward or copy packet to specific port when Multi_Field entry hit 2'b00: Disable 2'b01: Forward to CPU 2'b10: Copy to mirror port 2'b11: Reserved It is valid only if the corresponding MF_CTRL[1] bit is disable (Forwarding enable)	2'b00
	9[11:9]	--	R/W	MF_PRI_CTRL[2:0] Forward packet to specific queue when Multi_Field entry hit 3'b000: Disable 3'b100: Forward to queue 0 3'b101: Forward to queue 1 3'b110: Forward to queue 2 3'b111: Forward to queue 3 Other: Reserved	3'b000
	9[8]	--	R/W	MF_PTL_EN IP protocol number field enable.	1'b0
	9[7:0]	--	R/W	MF_PTL_NUM[7:0] IP protocol number field.	8'h00
	10[15:5]			RESERVED	
	10[4]	--	R/W	MF_LG_RANGE Enable the TCP/UDP port range monitoring function. When enabled, the source and destination port register is used as a port range monitor register. MF_LG_SP_NUM will be a port monitor start number MF_LG_DP_NUM will be a port monitor stop number {MF_LG_DP_TYPE, MF_LG_SP_TYPE} Monitor type 00 reserved 01 TCP 10 UDP 11 TCP or UDP {MF_LG_DP_EN, MF_LG_SP_EN} Monitor type 00 reserved 01 source port 10 destination port 11 source or dest. port	1'b0
26	10 [3]	--	R/W	MF_LG_SP_EN TCP/UDP source port field enable.	1'b0
	10[2]	--	R/W	MF_LG_SP_TYPE Indicates the MF_LG_SP_NUM field is a TCP or UDP port. 0: TCP port 1: UDP port	1'b0

	10[1]	--	R/W	MF_LG_DP_EN TCP/UDP destination port field enable.	1'b0
	10[0]	--	R/W	MF_LG_DP_TYPE Indicates the MF_LG_DP_NUM field is a TCP or UDP port. 0: TCP port 1: UDP port	1'b0
	11[15:0]	--	R/W	MF_LG_SP_NUM[15:0] TCP/UDP source port number to be monitored.	16'h0
	12[15:0]	--	R/W	MF_LG_DP_NUM[15:0] TCP/UDP destination port number to be monitored.	16'h0
	13[15]		R/W	MF_SP_EN Physical source port field enable	1'b0
	13[14:10]	--	R/W	MF_SP_NUM[4:0] Physical source port number (port 0 ~ 4) bit[4]: port 4 bit[3]: port 3 bit[2]: port 2 bit[1]: port 1 bit[0]: port 0	5'h00
	13[9:0]			RESERVED	
	14[7]	--	R/W	MF_BA_EN Behavior Aggregate function enable	1'b0
	14[6]	--	R/W	MF_BA_TYPE Behavior Aggregate function type 0: DSCP (ipv4 TOS or ipv6 DSCP) 1: VLAN priority	1'b0
	14[5:0]	--	R/W	MF_BA_VALUE[5:0] Behavior Aggregate value For DSCP, using whole 6-bits, but the upper 3-bit for VLAN priority reference.	6'h00

5.13.3 Multi-Field Table QoS Rate Control Register

PHY	MII	ROM	R/W	Description	Default
26	16[15:0]	--	R/W	MF_MBS[15:0] Maximum Burst Size Expressed in byte. It is valid only if the corresponding MF_CTRL[0] bit is enable.	16'h 0000
	17[15:0]	--	R/W	MF_CREDIT_SIZE[15:0] Credit size to accumulate the bucket in per time interval. Expressed in byte. It is valid only if the corresponding MF_CTRL[0] bit is enable.	16'h 0000

5.13.4 Multi-Field Access Control Register

PHY	MII	ROM	R/W	Description	Default
26	19[7:0]	--	R/W	MF_VALID[7:0] Multi-Field function valid for each entry.	8'h00

	20[2:0]	--	R/W	MF_ENTRY[2:0] Multi-Field entry number. 8-entry is used MF QoS function,	3'h0
	20[3]	--	R/W	MF_RW Multi-field data read/write signal 0: read Multi-Field data 1: write Multi-Field data	1'b0
	20[4]	--	R/W (SC)	MF_RW_START Indicates start read/write Multi-Field of an entry, when write a logical "1" to this register. A self cleared register after read/write data done.	1'b0
	20[5]	--	R/W	MF_OVERFLOW_THR MF counter overflow threshold index 1: 32'hFFFF_0000 0: 32'hFF00_0000	1'b0
	20[6]	--	R/W (SC)	MF_CNT_READ Indicates start read Multi-Field counter content of an entry, when write a logical "1" to this register. A self cleared register after read counter done.	1'b0
	21[15:0]	--	RO (SC)	MF_CNT_LSB[15:0] Multi-Field counter content after data read, LSB part.	16'h0000
	22[15:0]	--	RO (SC)	MF_CNT_MSB[31:16] Multi-Field counter content after data read, MSB part.	16'h0000

5.13.5 Multi-Field Status Register

PHY	MII	ROM	R/W	Description	Default
26	23[7:0]	--	RO (SC)	MF_OVERFLOW[7:0] Multi-Field counter overflow for each entry	8'h00

5.14 Auto Blocking/Recovery loop port

PHY	MII	ROM	R/W	Description	Default
27	9[15:14]	--	R/W	Auto blocking loop port [15]: blocking RX/TX of MII0 [14]: blocking RX/TX of Loop port	2'b00
	11[15:14]		R/W	Auto recovery loop port [15]: Auto Recover RX/TX of MII0 After any port 0 ~ 4 have no loop, the blocking RX/TX of MII0 will be enabled again. [14]: Auto Recover RX/TX of Loop port Only when the loop port is link off, IP175LLF will enable the blocking RX/TX of loop port.	2'b00

6 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25℃	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10℃ ~ +70℃ (for IP175LLF) -40℃ ~ +85℃ (for IP175LLFI)
6	Equivalent Series Resistance	40 ohm Max.
7	Drive Level	100 μW
8	Load Capacitance	20 pF
9	Shunt Capacitance	7 pF Max
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Aging Rate A Year	+/- 5 ppm/year

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	-0.3V to 3.63V
Input Voltage	-0.3V to 3.63V
Output Voltage	-0.3V to 3.63V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta) (IP175LLF)	0°C to 70°C
IC Junction Temperature (Tj) (IP175LLF)	0°C to 125°C
Ambient Operating Temperature (Ta) (IP175LLFI)	-40°C to 85°C
IC Junction Temperature (Tj) (IP175LLFI)	-40°C to 125°C

7.2 DC Characteristic

Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	1.85	1.90	2.05	V	
Supply Voltage	VCC_O	3.135	3.3	3.465	V	
Regout Voltage	REG_OUT	1.85	1.90	2.05	V	All ports link at 10Mbps mode
Power Consumption			1		W	VCC=1.9v, 100Mbps full duplex

Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

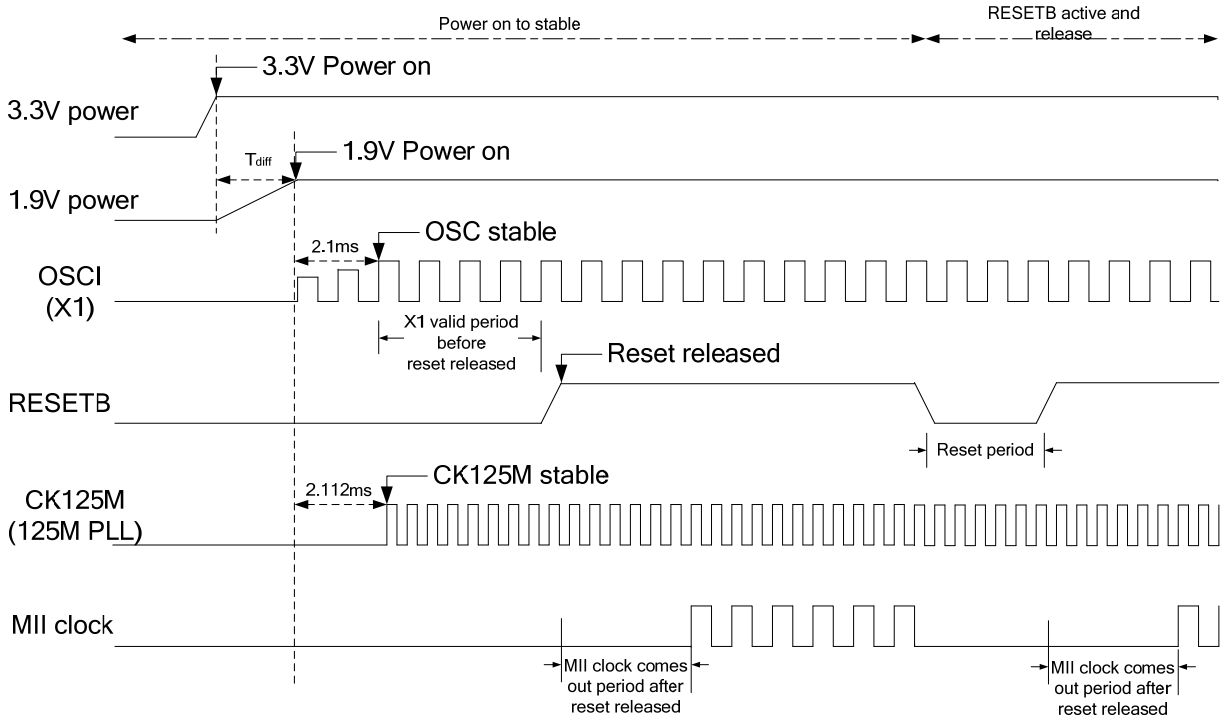
I/O Electrical Characteristics

Parameter	Sym	Min.	Max.	Unit	Conditions
Input Low Voltage -LED PAD direct mode -LED PAD bicolor mode -NOT LED PAD	VIL		 0.39*VCC_O 0.36*VCC_O 0.4*VCC_O	V	
Input High Voltage -LED PAD direct mode -LED PAD bicolor mode -NOT LED PAD	VIH	 0.58*VCC_O 0.58*VCC_O 0.6*VCC_O		V	
X1 Input Low Voltage	VIL		0.6	V	VCC = 1.9V
X1 Input High Voltage	VIH	1.5		V	VCC = 1.9V
Output Low Voltage	VOL		0.4	V	IOH=4mA, VCC_O_x=3.3V
Output High Voltage	VOH	2.4		V	IOL=4mA, VCC_O_x=3.3V
RESETB Threshold Voltage	Vrst	0.4*VCC_O	0.6*VCC_O	V	

7.3 AC Timing

7.3.1 Power On Sequence and Reset Timing

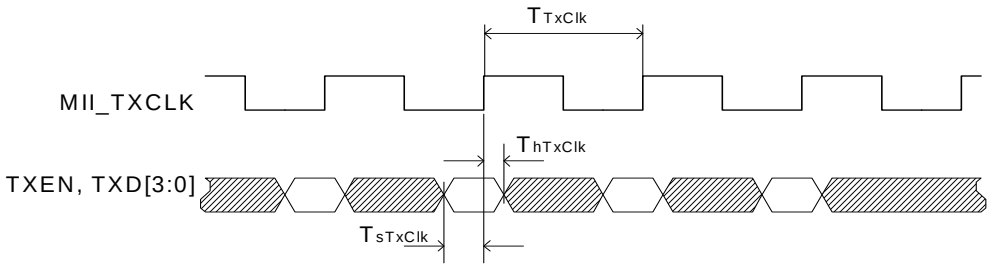
Description	Min.	Typ.	Max.	Unit
X1 valid period before reset released	10	-	-	ms
Reset period	10	-	-	ms
All power source ready before reset released	10			ms
Time difference between VCC3.3 and VCC1.9 (T_{diff})	-2			ms
MII clock comes out period after reset released	-	1	-	µs



7.3.2 PHY Mode MII (Turbo MII) Timing

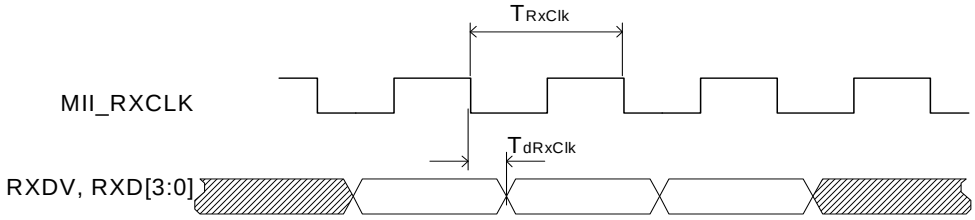
a. Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{TxClk}	Transmit clock period for TMII (50MHz)		20		ns
T_{TxClk}	Transmit clock period for TMII (31.25MHz)		32		ns
T_{sTxClk}	TXEN, TXD to MII_TXCLK setup time	10	-	-	ns
T_{hTxClk}	TXEN, TXD to MII_TXCLK hold time	5	-	-	ns



b. Receive Timing

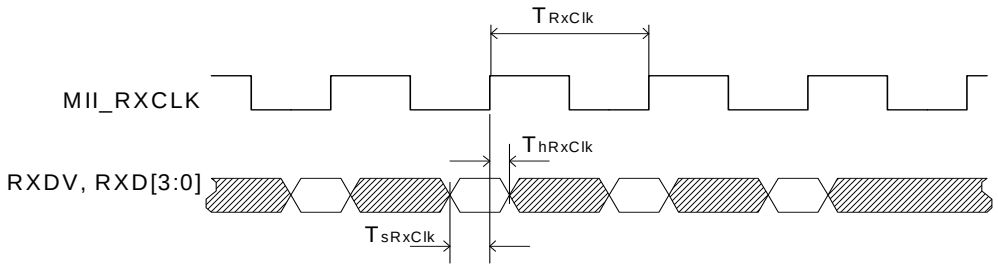
Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{RxClk}	Receive clock period for TMII (50MHz)		20		ns
T_{RxClk}	Receive clock period for TMII (31.25MHz)		32		ns
T_{dRxClk}	MII_RXCLK falling edge to RXDV, RXD	2	-	8	ns



7.3.3 MAC Mode MII (Turbo MII) Timing

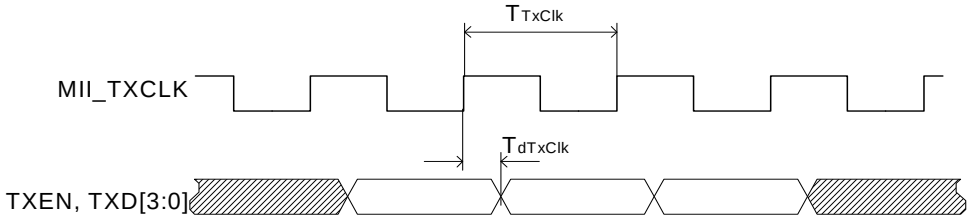
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{RxClk}	Receive clock period for TMII (50MHz)		20		ns
T_{RxClk}	Receive clock period for TMII (31.25MHz)		32		ns
T_{sRxClk}	RXDV, RXD to MII_RXCLK setup time	10	-	-	ns
T_{hRxClk}	RXDV, RXD to MII_RXCLK hold time	5	-	-	ns
$T_{sRxClk\ (TMII)}$	RXDV, RXD to MII_RXCLK setup time	4	-	-	ns
$T_{hRxClk\ (TMII)}$	RXDV, RXD to MII_RXCLK hold time	1	-	-	ns



b. Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{TxClk}	Transmit clock period for TMII (50MHz)		20		ns
T_{TxClk}	Transmit clock period for TMII (31.25MHz)		32		ns
T_{dTxClk}	MII_TXCLK rising edge to TXEN, TXD	6	-	22	ns
$T_{dTxClk\ (TMII)}$	MII_TXCLK rising edge to TXEN, TXD (note)	6	-	16.5	ns

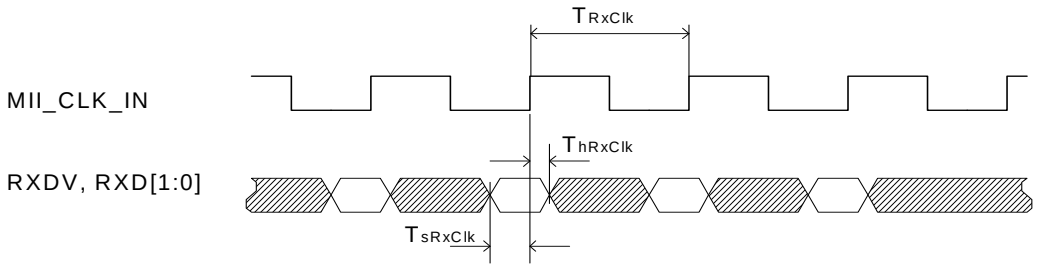


Note:
TMII Max. Condition: Voltage: 1.7V, Temperature: 125°C, Pad Load : 12 pF, Pad Drive : 8 mA

7.3.4 RMII Timing

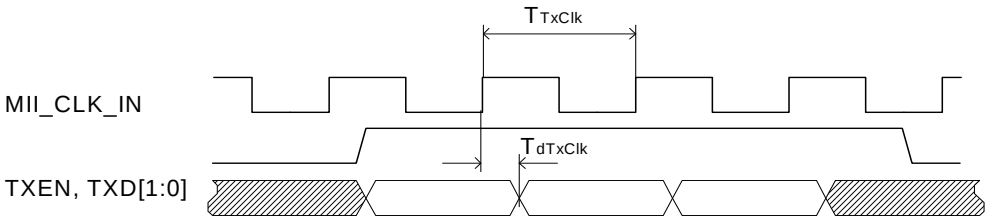
a. Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period	-	20	-	ns
T_{sRxClk}	RXDV, RXD to MII_CLK_IN setup time	4	-	-	ns
T_{hRxClk}	RXDV, RXD to MII_CLK_IN hold time	2	-	-	ns



b. Transmit Timing

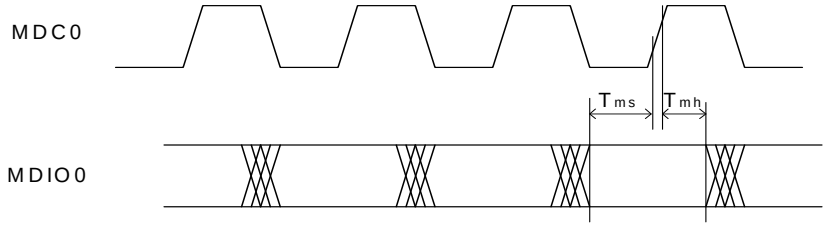
Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period	-	20	-	ns
T_{dTxClk}	MII_CLK_IN rising edge to TXEN, TXD	5	-	14	ns



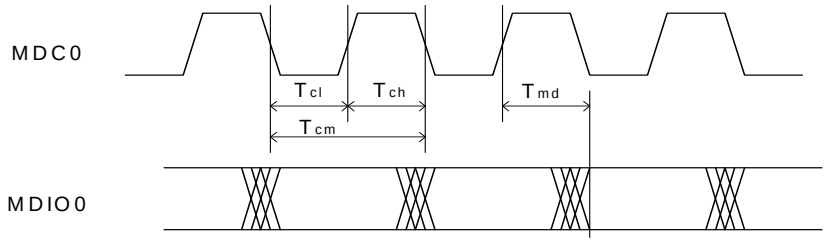
7.3.5 SMI Timing

a. MDC0/MDIO0 Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC0 High Time	40	-	-	ns
T_{cl}	MDC0 Low Time	40	-	-	ns
T_{cm}	MDC0 period	100	-	-	ns
T_{md}	MDIO0 output delay	5	-	15	ns
T_{ms}	MDIO0 setup time	10	-	-	ns
T_{mh}	MDIO0 hold time	5	-	-	ns



Write Cycle

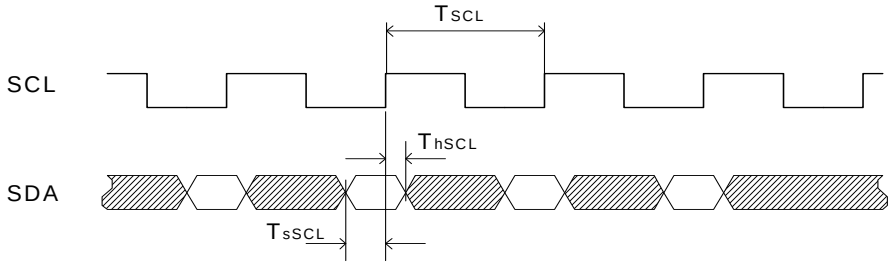


Read Cycle

7.3.6 EEPROM Timing

a.

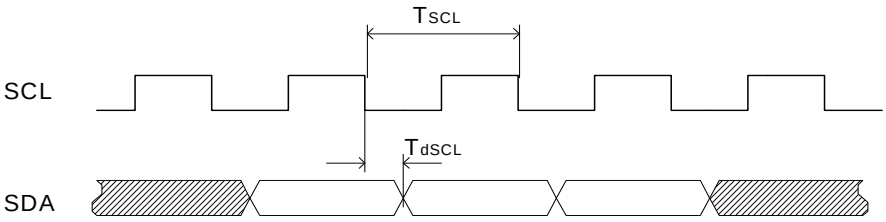
Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	20	-	-	ns
T_{hSCL}	SDA to SCL hold time	20	-	-	ns



Read data cycle

b.

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns



Comand cycle

7.4 Thermal Data

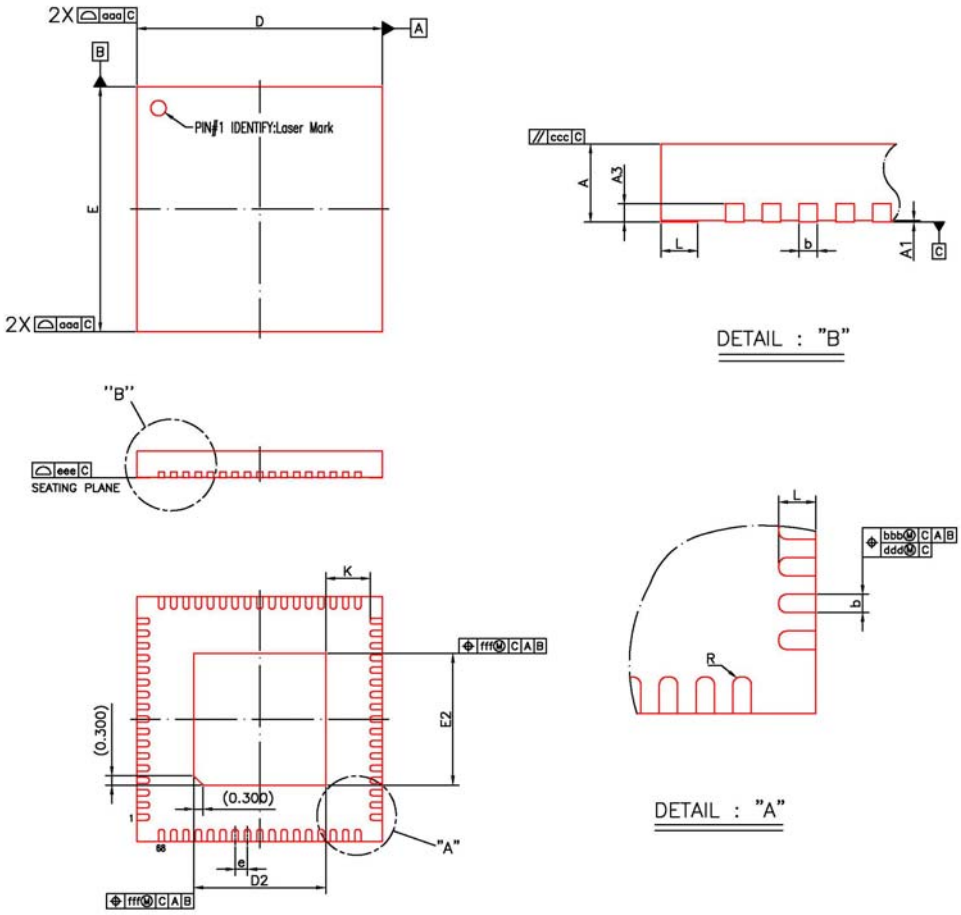
Theta Ja	Theta Jc	Conditions	Units
38.2	--	2 Layer PCB	^{o}C/W

8 Order Information

Part No.	Package	Notice
IP175LLF	68-PIN QFN	-
IP175LLFI	68-PIN QFN	-40°C to 85°C

9 Package Detail

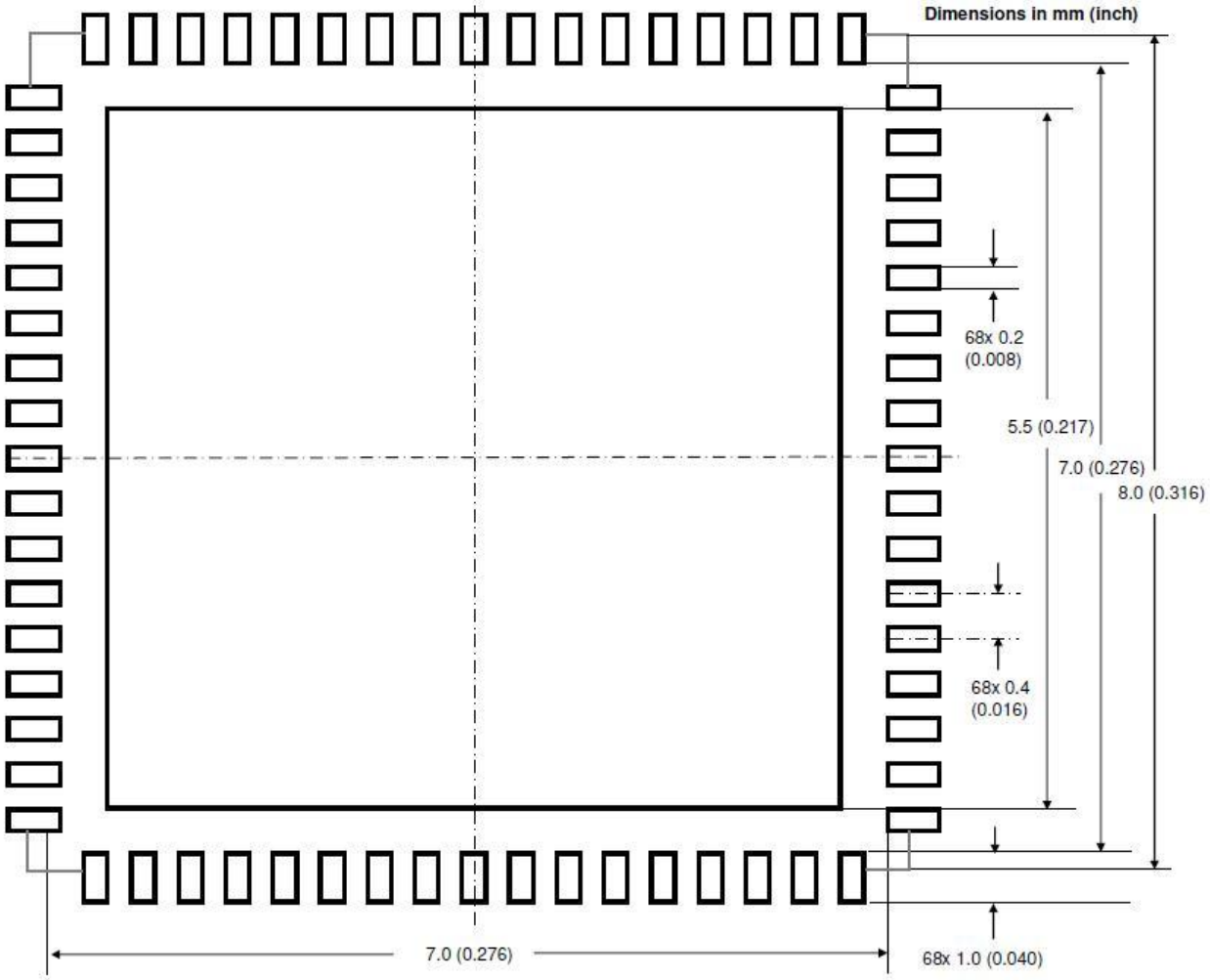
9.1 68 QFN Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.90	8.00	8.10	0.311	0.315	0.319
D2/E2	5.40	5.50	5.60	0.213	0.217	0.220
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLMETER
2. REFERENCE DOCUMENT : JEDEC MO-220

9.2 68 QFN PCB footprint



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