Boost/SEPIC/Flyback DC/DC Controller with I²C Bus

General Description

The VP3482 is a versatile controller designed for use in Boost, SEPIC and Flyback power converter and topologies that needs an external low-side N-MOSFET acting as primary switch. Besides cycle-by-cycle current limiting, current mode control scheme also makes it wide bandwidth and good transient response. The current limit can be programmed simply with an external resistor.

The switching frequency can be set in any value between 100kHz and 1MHz with a resistor or any external clock source. The VP3482 can be operated at high switching frequency to save the solution board size. It has built-in protection circuits such as thermal shutdown, under-voltage lockout, short circuit protection, and overvoltage protection. Internal soft-start circuitry reduces the in-rush current at start-up.

VP3482 is available in small QFN32L 5x5 green package.

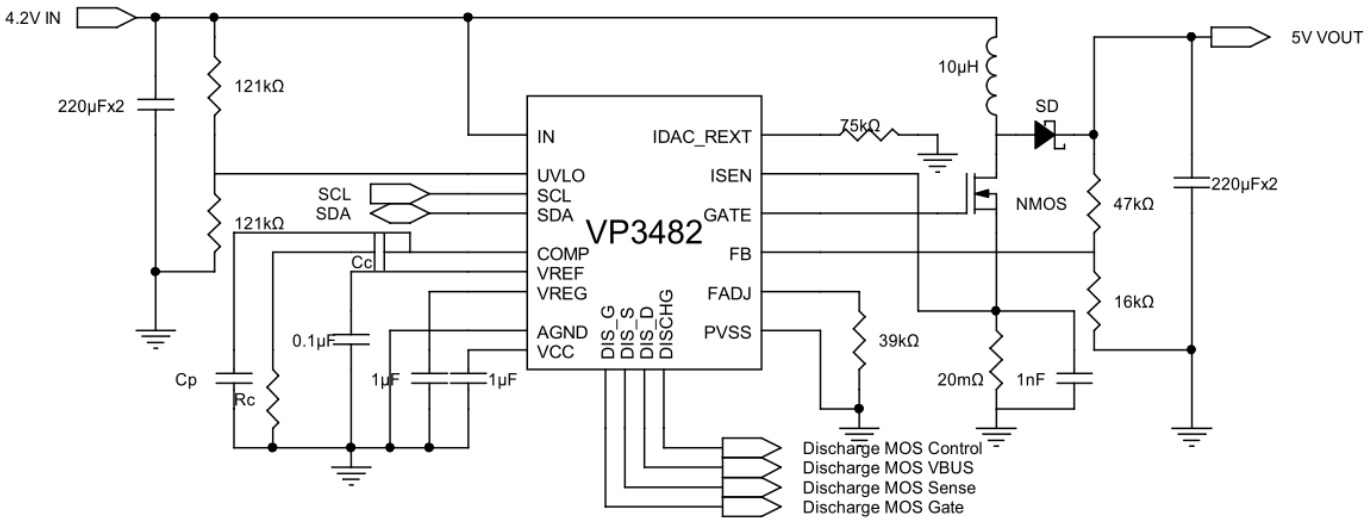
Features

- Wide Input Voltage from 2.97V to 40V
- Internal 1.275V Reference with ±1.5% Accuracy
- Adjustable 100kHz~1MHz Clock Frequency
- I²C Control Interface
- Built-in V_{BUS} Discharging MOSFET
- 1A Peak Current Limit Using Internal Driver
- Current Mode Operation
- Internal 4/2Ω MOSFET Switch
- External RC Compensation
- Internal Soft-Start
- High Efficiency at Light Loads
- Current Limit and Over Temperature Protection
- Adjustable Input UVLO Threshold Voltage
- QFN32 5x5 Green Package with RoHS Compliant

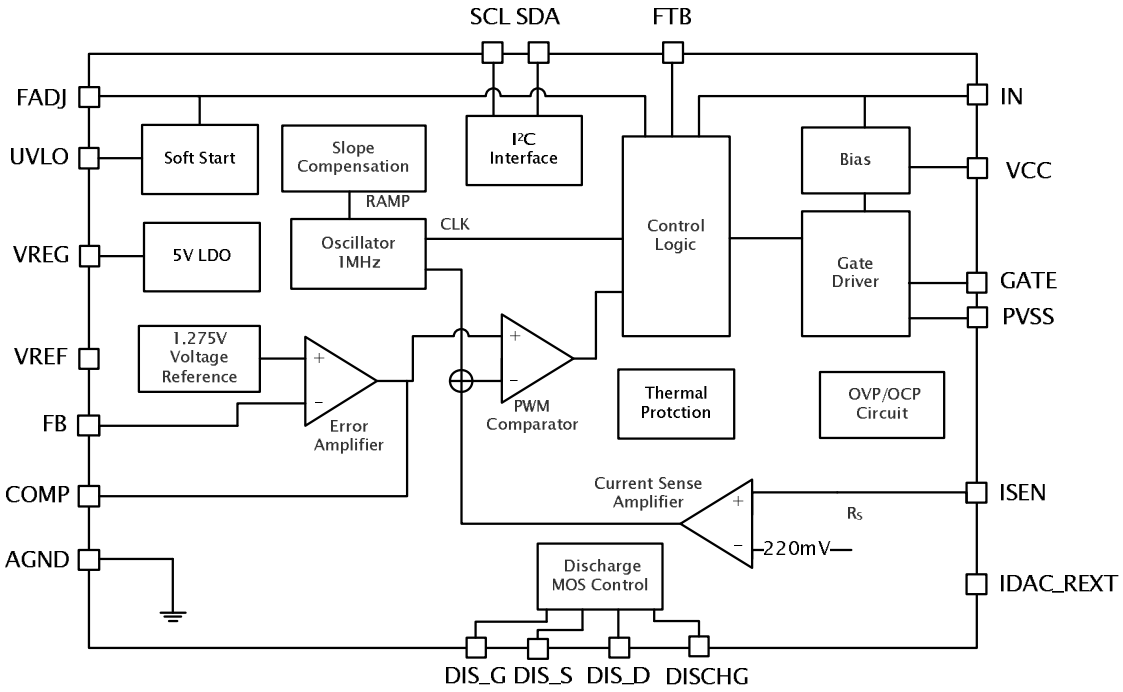
Applications

- USB PD Power Controller
- Battery Powered Device
- Offline Power Supply

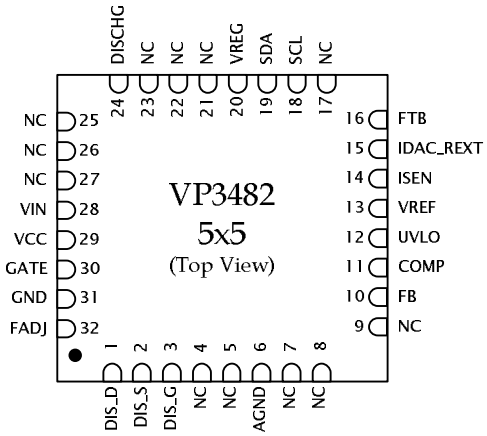
Typical Application



Functional Block Diagram



Pin Assignments



Pin Descriptions

Pin No.	Pin	I/O/P	Function Description
1	DIS_D	I	The drain terminal of the discharge MOSFET.
2	DIS_S	I	The source terminal of the discharge MOSFET.
3	DIS_G	I	The gate terminal of the discharge MOSFET.
4	NC	–	No connection.
5	NC	–	No connection.
6	AGND	P	Ground.
7	NC	–	No connection.
8	NC	–	No connection.
9	NC	–	No connection.
10	FB	I	Output Feedback. Connect the external resistor divider network from output to this pin to sense output voltage. The FB pin voltage is regulated to internal 1.275V reference voltage.
11	COMP	O	Compensation. Use a RC/C network to do proper loop compensation.
12	UVLO	I	Under Voltage Lockout. Use a proper ratio resistor divider network to determine the voltage input to allow switching and the hysteresis to disable switching.
13	VREF	–	Internal reference voltage, shall connect to a capacitor.
14	ISEN	I	Current Sense. Use an external resistor in series with ground to measure the voltage drop.
15	IDAC_REXT	–	The reference resistor connector of digital to analog converter current.
16	FTB	O	The fault output. (Open Drain)
17	NC	–	No connection.
18	SCL	I	I²C Serial Clock.
19	SDA	I/O	I²C Serial Data Input/Output.
20	VREG	O	5V LDO Output. Current driving capability should not exceed 20mA.
21	NC	–	No connection.
22	NC	–	No connection.
23	NC	–	No connection.
24	DISCHG	O	The gate control of the discharge NMOSFET.
25	NC	–	No connection.
26	NC	–	No connection.
27	NC	–	No connection.
28	VIN	I	Power Supply Input.
29	VCC	O	Internal regulator output.
30	GATE	O	Gate Drive. Connect this terminal to the gate pin of the external MOSFET.
31	GND	P	Ground
32	FADJ	I	Frequency Adjust/Synchronization/Shutdown. A resistor connected from this pin to ground simply sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the clock. Pull this pin for a time will shut the chip down.

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{IN}	Supply voltage range	-0.3 to 42	V
V_{LV} (COMP/UVLO/FB/FADJ/ GATE/ISEN/DISCHG/SCL/SDA)	Low voltage range	-0.3 to 6	V
V_{CC}(VREG)	Regulator output pin range	-0.3 to 5	V
V_{ISEN}	Current sense pin range	-0.4 to 0.6	V
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
Electrostatic discharge	Human body model	2	kV
Electrostatic discharge	Machine model	200	V
θ_{JC}	Thermal resistance (Junction to Case)	TBD	°C/W
θ_{JA}	Thermal resistance (Junction to Air)	TBD	°C/W

(*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

Recommended Operating Conditions

Symbol	Parameter	Specification		Unit
		Min	Max	
V_{IN}	Supply voltage	2.95	40	V
f_{OSC}	Switching voltage range	0.1	1	MHz
T_A	Operating free-air temperature range	-40	85	°C
T_J	Operating Junction range	-40	125	°C

Electrical Characteristics

V_{IN}=12V, R_{FADJ}=40kΩ, T_J=25℃, unless otherwise specified (* 1)

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ	Max	
V_{FB}	Feedback voltage	V_{COMP}=1.4V, 3V<V_{IN}<40V			1.275		V
		V_{COMP}=1.4V, 3V<V_{IN}<40V, -40℃<T_J<125℃		1.256		1.294	V
I_Q	Quiescent current in shutdown mode	V_{FADJ}=3V	V_{IN}=12V			900	μA
			V_{IN}=12V, -40℃<T_J<125℃			950	
			V_{IN}=5V			800	
			V_{IN}=5V, -40℃<T_J<125℃			850	
V_{UVLO}	Under voltage lockout	V_{UVLO} Ramp down		1.345		1.517	V
I_{UVLO}	UVLO source current	V_{EN} = 3V			4.5		μA
V_{UVLOSD}	UVLO Shutdown voltage			0.55	0.7	0.82	V
V_{COMP}	COMP pin voltage	V_{FB}=1.275V			1		V
I_{COMP}	COMP pin current sink	V_{FB}=0V			630		μA
$R_{DS(ON)}$	High-side switch $R_{DS(ON)}$ (*1)	V_{IN}=5V, I_{GATE}=0.2A			4		Ω
	Low-side switch $R_{DS(ON)}$ (*1)	V_{IN}=5V, I_{GATE}=0.2A			2		
A_{VOL}	Error amplifier voltage gain	V_{COMP}=1.4V, I_{EAO}=100μA			60		V/V
g_M	Error amplifier trans-conductance	V_{COMP}=1.4V			430		μ℧
V_{GATE}	Maximum GATE driving swing	V_{IN}<5.8V			V_{IN}		V
		V_{IN}≥5.8V			5.2		
f_{OSC}	Oscillation frequency	R_{FADJ}=40kΩ		0.4	0.475	0.555	MHz
D_{MAX}	Maximum duty cycle	R_{FADJ}=40kΩ			85		%
ΔV_{LINE}	Voltage line regulation	3V<V_{EN}<40V			0.02		%/V
ΔV_{LOAD}	Voltage load regulation	I_{EAO} Source/Sink			±0.5		%/A
$t_{MIN(ON)}$	Minimum on-time					571	nS
I_{SUPPLY}	Supply Current	R_{FADJ}=40kΩ			3.8		mA
V_{SENSE}	Current sense threshold voltage			100		190	mV
V_{SC}	Overload current limit sense voltage			157		280	mV
V_{SL}	Internal compensation ramp				90		mV
V_{OVP}	Output overvoltage protection	V_{COMP}=1.4V		26	85	135	mV
$V_{OVP(HYS)}$	Output overvoltage protection hysteresis	V_{COMP}=1.4V		28	70	106	mV

Electrical Characteristics (cont.)

V_{IN}=12V, R_{FADJ}=40kΩ, T_J=25℃, unless otherwise specified (* 1)

Symbol	Parameter	Test Condition	Specification			Unit
			Min	Typ	Max	
I_{EAO}	Error amplifier output current (Source/Sink)	Source,V_{COMP} = 1.4V, V_{FB} = 1.1V		630		μA
		Source, V_{COMP} = 1.4V, V_{FB} = 1.1V -40℃<T_J<125℃	470		840	
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V		75		
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V -40℃<T_J<125℃	30		105	
V_{EAO}	Error amplifier output voltage	V_{FB}=0V, COMP pin floating		2.65		V
		V_{FB}=0V, COMP pin floating -40℃<T_J<125℃	2.45		2.95	
		V_{FB}=1.4V		0.66		
		V_{FB}=1.4V -40℃<T_J<125℃	0.32		0.9	
V_{SD}	Shutdown signal threshold on FADJ pin	Chip Enable		1.26		V
		Chip Enable, -40℃<T_J<125℃			1.4	
		Chip Disable		0.63		
		Chip Disable, -40℃<T_J<125℃	0.4			
t_{SS}	Soft start delay	V_{FB} = 1.2V, COMP pin floating	8.7	15	21.3	mS
t_R	GATE pin rising time	Cgs = 3000pF, V_{GATE} = 0V to 3V		18		nS
t_F	GATE pin falling time	Cgs = 3000pF, V_{GATE} = 3V to 0V		12		nS
I_{SD}	Shutdown pin current FADJ pin	V_{SD}=0V		20		μA
T_{SD}	Thermal shutdown			175		℃
$T_{SD(HYS)}$	Thermal shutdown hysteresis			10		℃

(*1): Stress beyond those listed at “absolute maximum rating” table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up “recommended operation conditions” table.

Functional Descriptions

The VP3482 employs the current-mode, adjustable frequency pulse-width modulation (PWM) architecture. It operates at adjustable switching frequency under medium to high load current conditions.

Overvoltage and UVLO Protection

The VP3482 uses FB pin to detect overvoltage occurrence. The overvoltage protection should be triggered at the voltage rises to $V_{FB}+V_{OVP}$. When OVP occurs only the MOSFET will be turned off, the output voltage will drop. VP3482 will switch when the voltage on FB pin is less then ($V_{OVP}+V_{FB}-V_{OVP(HYS)}$).

The VP3482 provides UVLO pin to program enable and disable thresholds. The voltage on UVLO pin would be compared with internal reference 1.43V. Figure 1 shows how the UVLO detection works.

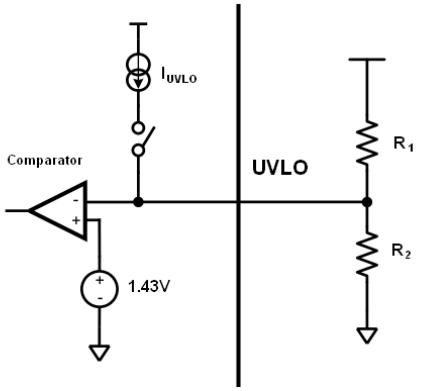


Figure 1. UVLO Pin Configuration

The R1/R2 network programs the enable threshold voltage V_{EN}. When the VP3482 is enabled the I_{UVLO} will source 5μA current flows the R_2 which causes a hysteresis. Hence the disable threshold, V_{SH}, is lower then the enable threshold V_{EN}.

$$R_2 = \frac{1.43V}{I_{UVLO}} \times \left(1 + \frac{1.43V - V_{SH}}{V_{EN} - 1.43V}\right)$$

$$R_1 = R_2 \times \left(\frac{V_{EN}}{1.43V} - 1\right)$$

Select appropriate value of V_{EN}, V_{SH} and use above two equations to determine the value of R_1 and R_2.

Bias Voltage

VP3482 generates the internal bias voltage from IN input voltage if it does not exceeds 6V. When VIN is higher then 6V the VP3482 will use internal regulation to bias the chip. To improve the stability of the bias, an external capacitor of 0.47μF~4.7μF is strongly recommended to add on VREG terminal.

In any case, do not add external voltage on VCC pin or the chip would be damaged.

Frequency Adjust

The switching frequency can be adjusted from 100kHz to 1MHz by a external resistor in series with FADJ terminal and ground. The following equation is used to calculate resistor value.

$$R_{FADJ} = \frac{22 \times 10^3}{f_S} - 5.74$$

Where f_S is in kHz and R_{FADJ} is in kΩ.

Clock Synchronization

VP3482 is able to be synchronized to an external clock by connecting to the FADJ terminal with R_{FADJ} in series with ground as shown in figure 2.

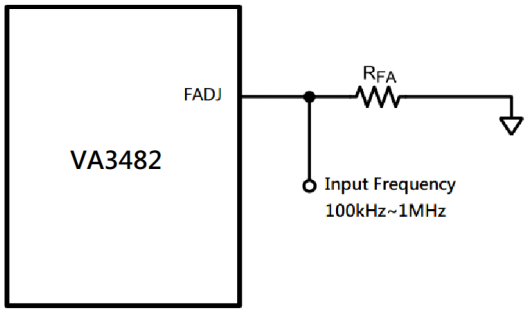


Figure 2. Clock Synchronization

Shutdown

The FADJ pin can be used as a shutdown pin. If the

Functional Descriptions (cont.)

high signal pulls up this pin, VP3482 will stop the switching and then enter the shutdown state. In this state, VP3482 consumes about 250μA typically.

The use of shutdown control in frequency adjustment mode is quite simple. Connects the FADJ pin to ground will force the VP3482 runs at specified frequency and pulls this pin high will shutdown the IC. In both frequency and synchronization mode, pulls FADJ pin high lasting then 30μs will also force the VP3482 enter the shutdown state.

Slope Compensation

VP3482 employs current mode control scheme. It has many advantages such as cycle-by-cycle current limit for the switch and easier to parallel power stages because automatic current sharing. The compensation ramp is already added in VP3482 and the slope of the default compensation ramp could satisfy most applications.

Overvoltage Protection

The VP3482 has overvoltage protection for the output. OVP occurrence is detected by sensing feedback (FB) pin. When the voltage at FB pin is over $V_{FB}+V_{OVP}$, overvoltage protection is triggered and the drive pin and the GATE pin will be tied-low.

Once the voltage at FB pin is lower then $V_{FB}+(V_{OVP}-V_{OVP(HYS)})$, the VP3482 will begin to switch again. Be aware that the error amplifier is still in operation during OVP event.

Short Circuit Protection

The ISEN pin is used to sense the over-current occurrence. If the difference between ISEN pin and ground is greater then 220mV, the current limit will be activated. The comparator will decrease the switching frequency by the factor of 8 and maintains this condition until the over-current (short) event is removed.

Programming Output Voltage

Since the output voltage of VP3482 could be configured with external resistors and I²C bus. It is needed to following the two steps described as below.

1. Setting Default Output Voltage:

While enabling the VP3482, the voltage divider taped to FB pin programs the default output voltage with the equation:

$$V_{OUT} = 1.43V \times \frac{R_1 + R_2}{R_1}$$

In real application, keep R_1 around 10~20kΩ and select R_2 according to the required output voltage. Place the voltage divider near the FB pin and keep the connecting trance away from the noisy nodes like GATE.

2. Programming Output Voltage Through I²C Bus

In many applications the output voltage could be adjusted depends on the power supply. VP3482 has an I²C DAC to provide the flexibility to change the output voltage with an MCU or other digital chips.

I²C is a easy way to adjust output voltage by the following equation:

$$V_{LSB} = R_1 \times \frac{1.43V}{8 \times R_{IDAC\_EXT}}$$

where V_{LSB} is the minimal offset voltage of one bit on FB pin and R_{IDAC_EXT} is the external resistor of the IDAC_REXT pin connected to ground.

Functional Descriptions (cont.)

See I²C Configuration section for detail I²C register definitions and descriptions.

I²C Configuration

The 7-bit I²C slave address of VP3482 is 0x7A. VP3482 supports only I²C single byte read and I²C single byte write. Table 1 lists the definition of registers and their functional descriptions.

REG_0

DIN[7]	DIN[6]	DIN[5]	DIN[4]	DIN[3]	DIN[2]	DIN[1]	DIN[0]
b7							b0

REG_1

PD_DA CBIAS	SEL	SHUT_ DOWN				DIN[9]	DIN[8]
b7							b0

Table 1. I²C Register Definition

Register 1: BIT[5] = 1: SHUTDOWN, 0:NORMAL
BIT[6] = 1: STEPDOWN, 0: STEPUP
BIT[7] = 1: IDAC OFF, 0:IDAC ON

Once the default voltage is determined by external resistors, the output voltage could be adjusted by writing 10-bit value in register #0 bit 7~bit 0 and register #1 bit 1~ bit 0.

Register #1 bit 5 is the shutdown mode control bit. Set to 1 will shut the VP3482 down and set to 0 will enable it.

Register #1 bit 6 is to determine whether the IDAC sinks the current or sources the current. Set to 0 will increasing the output from the default output voltage, set to 1 will decrease.

Set register #1 bit 7 to 1 will disable the I²C voltage control scheme, set to 0 will be back to normal.

Default Value: Register 0 = 0x01
Register 1 = 0x00

Using of Discharging NMOSFET

VP3482 has built in an NMOSFET for the purpose of discharging output voltage. Figure 3 shows the equivalent discharging MOSFET circuit inside the VP3482.

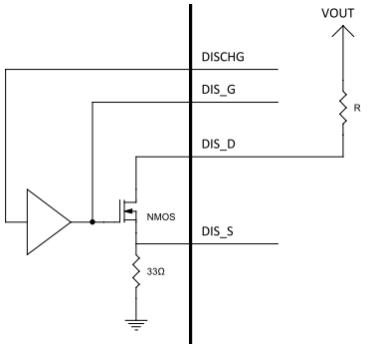


Figure 3. Discharging MOSFET

When the discharge MOS is used to discharge the output voltage, a current limiting resistor R shall be connected in series with DIS_D pin and VOUT. DIS_S is used to sense the remaining output voltage and should be connected to MCU voltage sensing pin. DISCHG is connected to the gate of discharging MOS with buffer and controlled by MCU. Since the DIS_G pin is the gate of the discharging MOS and could be replaced by DISCHG pin, DIS_G pin should be left floating and do not connect to any net.

LDO Output

VP3482 provides 5V/20mA internal LDO output at VREG pin. Once the VP3482 is powered on, the LDO output is enabled immediately and can not be turned off. VREG pin is a good power source for the MCU and can save the system cost and reduce design complexity. However, it will consume more standby current in shutdown mode.

Application Information

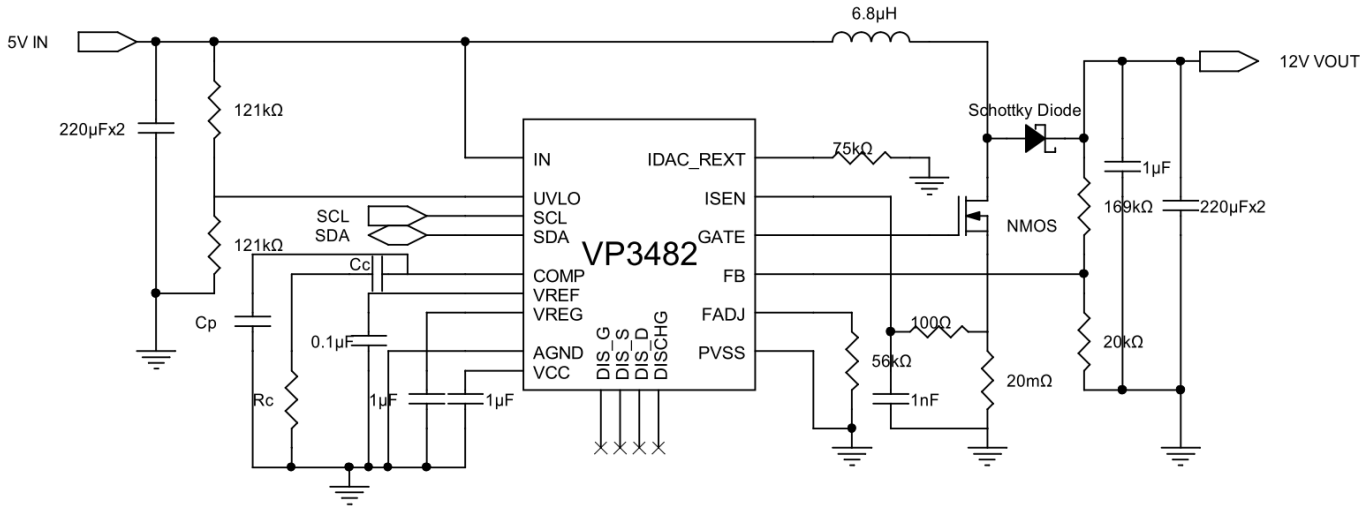


Figure 4. VP3482 Typical Boost Application

Application Information (cont.)

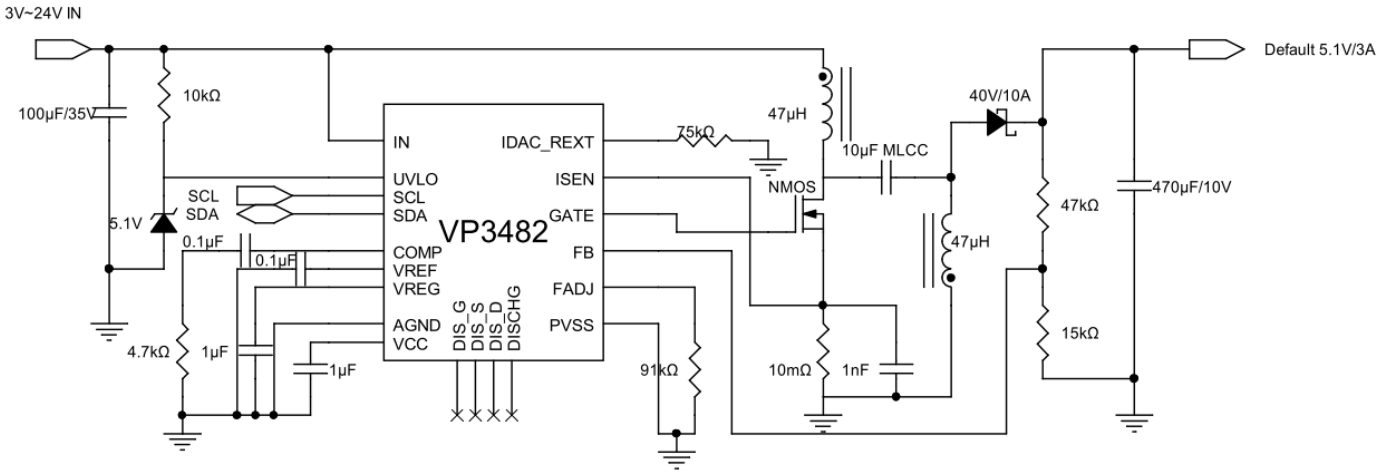
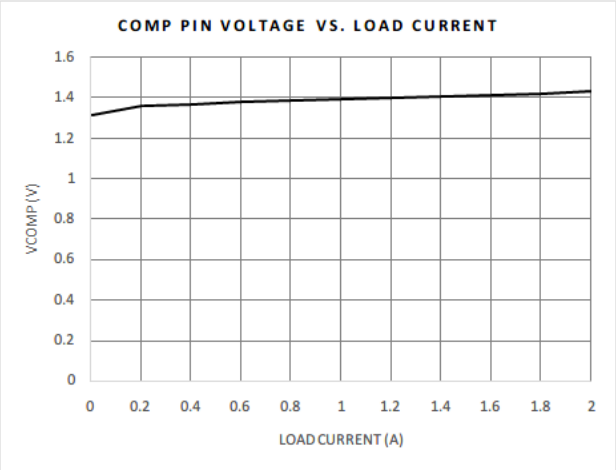
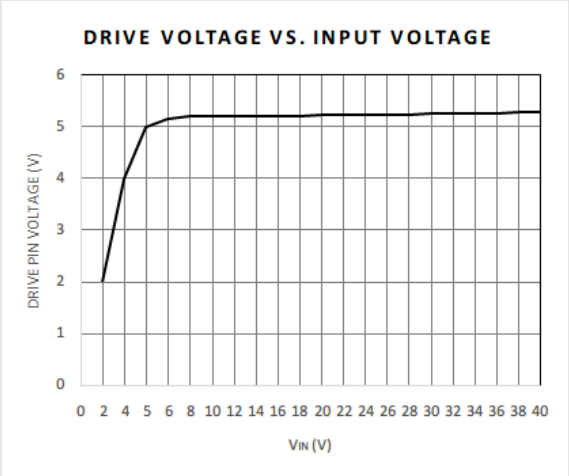
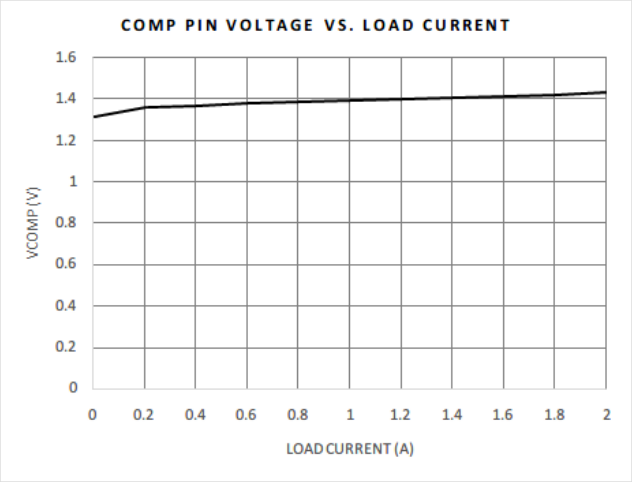


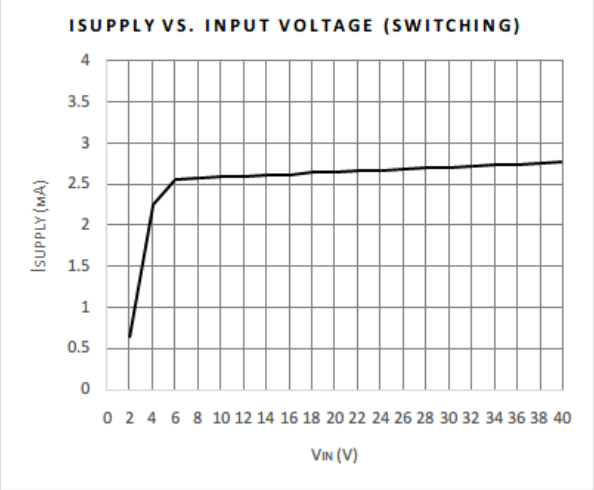
Figure 5. VP3482 Typical SEPIC Application

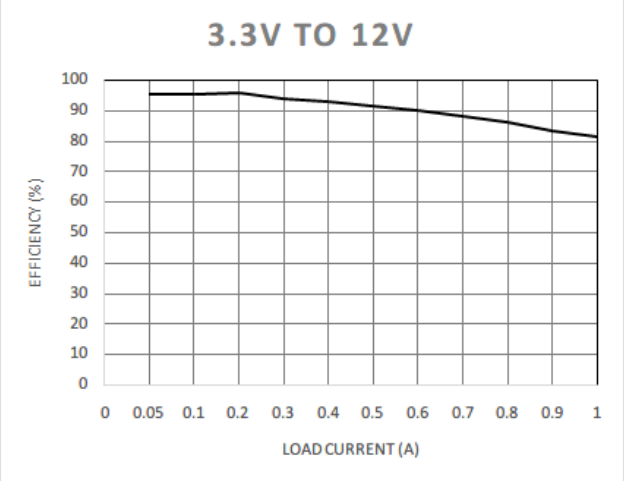
Typical Characteristic

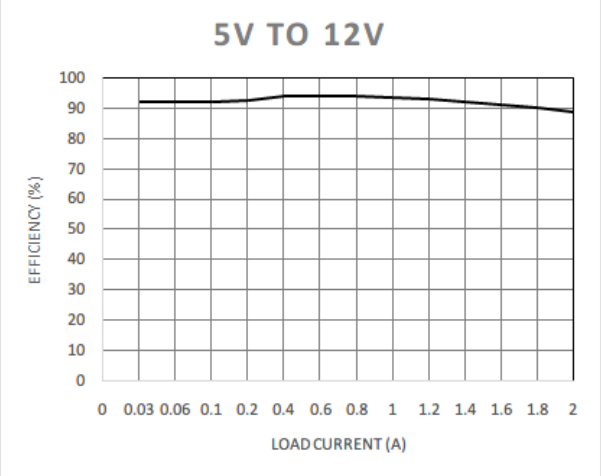




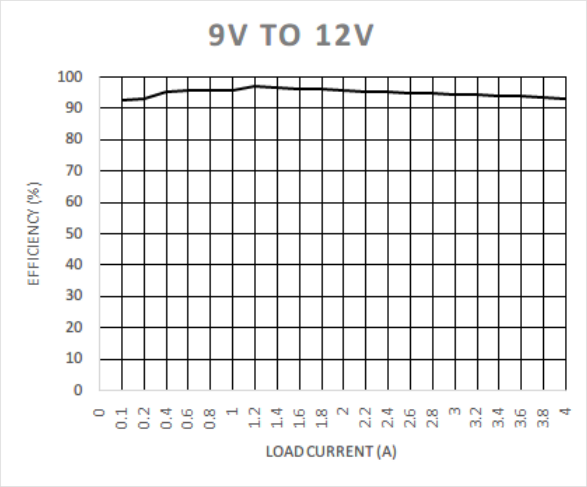


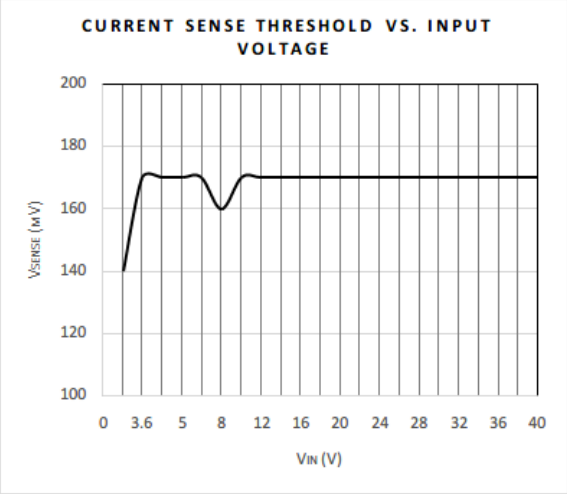


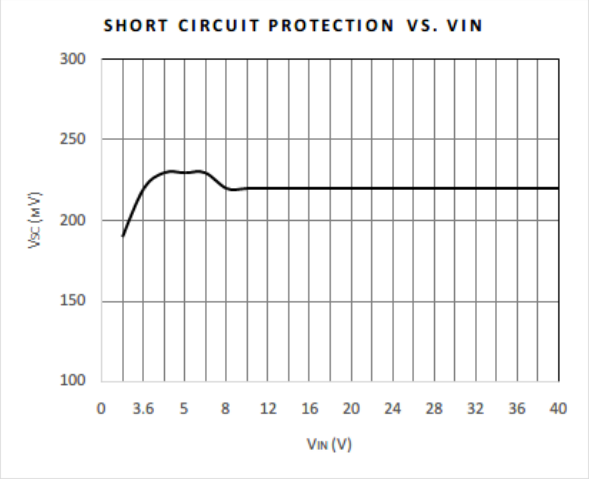


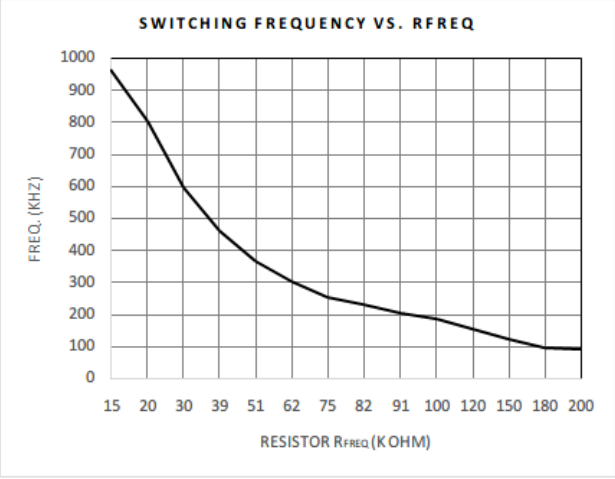


Typical Characteristic (cont.)



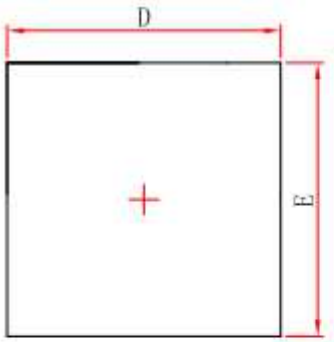




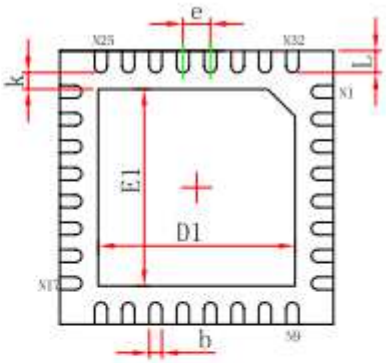


Package Information

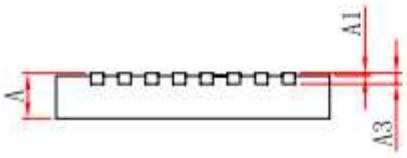
WQFN32L 5x5



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

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