

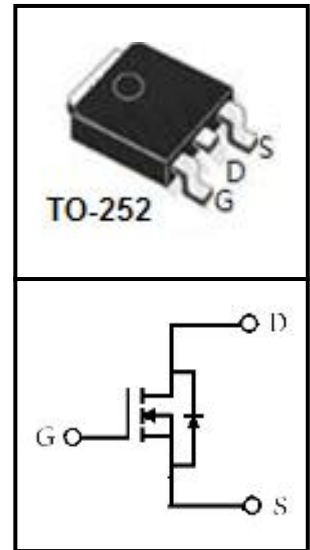
80V N-Channel Split Gate MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



| Device Marking and Package Information | | |
|--|---------|-----------|
| Device | Package | Marking |
| CSD08N6P5 | TO-252 | CSD08N6P5 |

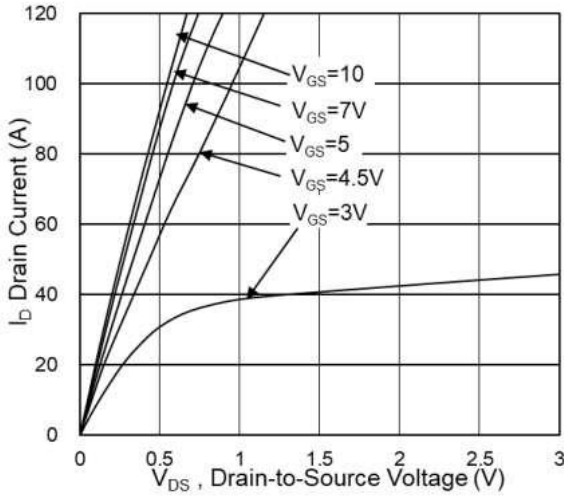
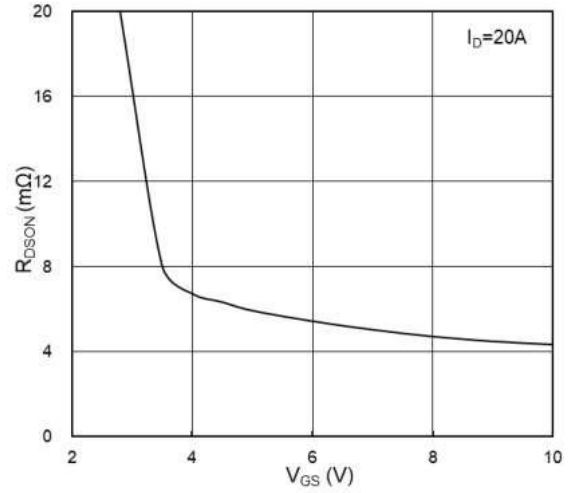
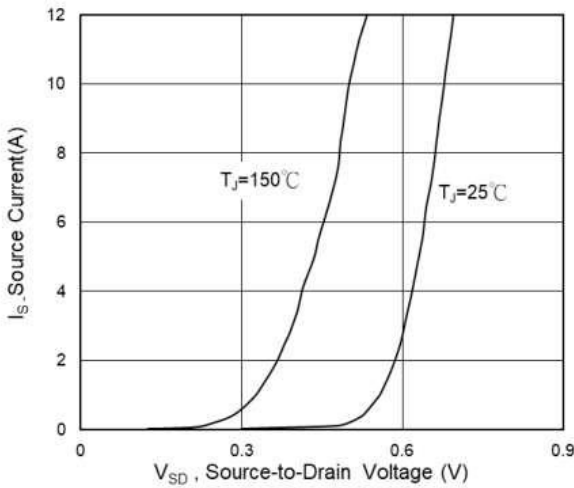
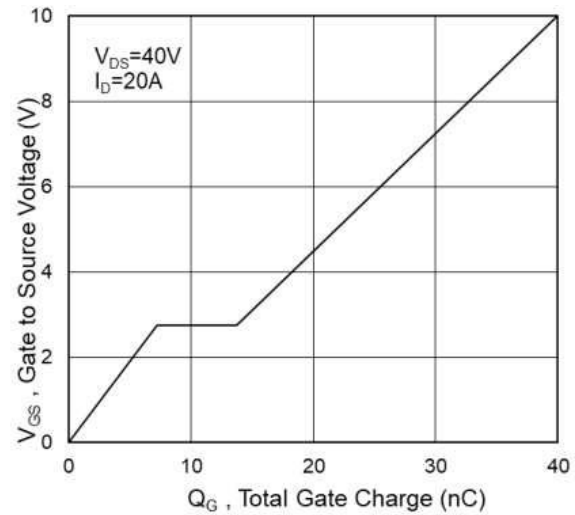
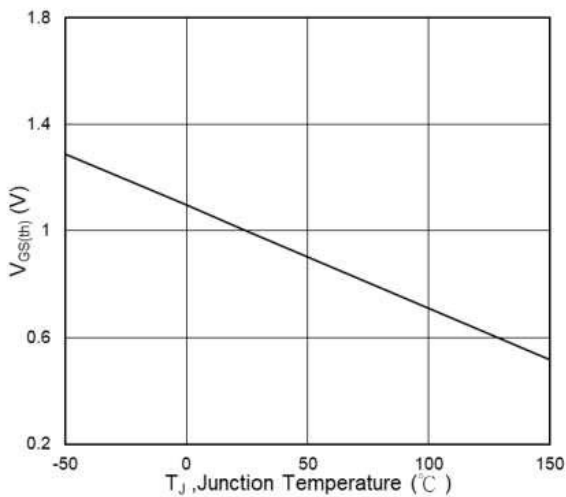
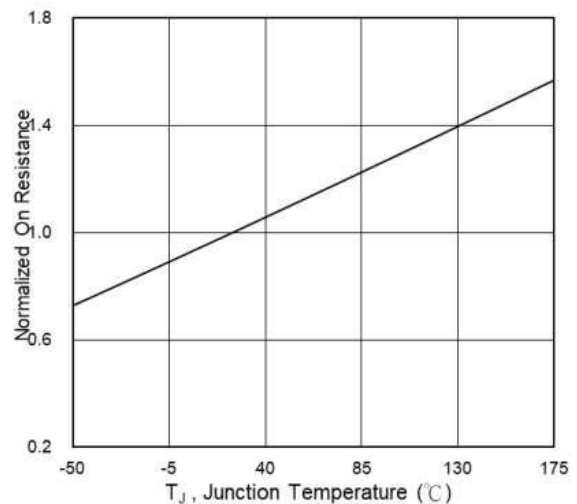
| Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted | | | |
|---|----------------|----------|------------------|
| Parameter | Symbol | Value | Unit |
| Drain-Source Voltage ($V_{GS} = 0\text{V}$) | V_{DSS} | 80 | V |
| Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1) | I_D | 98 | A |
| Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1) | | 65 | A |
| Pulsed Drain Current (note2) | I_{DM} | 270 | A |
| Gate Source Voltage | V_{GSS} | ± 20 | V |
| Single Pulse Avalanche Energy (note3) | E_{AS} | 75.6 | mJ |
| Power Dissipation $T_C = 25^\circ\text{C}$ (note4) | P_D | 60 | W |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55~+175 | $^\circ\text{C}$ |

| Thermal Characteristics | | | |
|---|-----------------|-------|--------------------|
| Parameter | Symbol | Value | Unit |
| Thermal Resistance, Junction-to-Ambient (note1) | $R_{\theta JA}$ | 62 | $^\circ\text{C/W}$ |
| Thermal Resistance Junction-Case (note1) | $R_{\theta JC}$ | 2.2 | $^\circ\text{C/W}$ |

| Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified | | | | | | |
|--|---------------|--|-------|------|-----------|-----------|
| Parameter | Symbol | Test Conditions | Value | | | Unit |
| | | | Min. | Typ. | Max. | |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0V, I_D = 250\mu A$ | 80 | -- | -- | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 64V, V_{GS} = 0V, T_J = 25^\circ\text{C}$ | -- | -- | 1 | μA |
| | | $V_{DS} = 64V, V_{GS} = 0V, T_J = 55^\circ\text{C}$ | -- | -- | 5 | μA |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20V$ | -- | -- | ± 100 | nA |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\mu A$ | 1.2 | -- | 2.5 | V |
| Drain-Source On-Resistance (note2) | $R_{DS(on)}$ | $V_{GS} = 10V, I_D = 20A$ | -- | 4.5 | 6.5 | $m\Omega$ |
| | | $V_{GS} = 4.5V, I_D = 20A$ | -- | 6.5 | 8.5 | $m\Omega$ |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0V,$ $V_{DS} = 40V,$ $f = 1.0MHz$ | -- | 2860 | -- | pF |
| Output Capacitance | C_{oss} | | -- | 410 | -- | |
| Reverse Transfer Capacitance | C_{rss} | | -- | 38 | -- | |
| Total Gate Charge (-4.5V) | Q_g | $V_{DD} = 40V, I_D = 20A,$ $V_{GS} = 10V$ | -- | 40 | -- | nC |
| Gate-Source Charge | Q_{gs} | | -- | 7.2 | -- | |
| Gate-Drain Charge | Q_{gd} | | -- | 6.5 | -- | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DS} = 40V, V_{GS} = 10V,$ $R_G = 3\Omega, I_D = 20A$ | -- | 8.3 | -- | ns |
| Turn-on Rise Time | t_r | | -- | 4.2 | -- | |
| Turn-off Delay Time | $t_{d(off)}$ | | -- | 36 | -- | |
| Turn-off Fall Time | t_f | | -- | 6.9 | -- | |
| Body Diode Characteristics | | | | | | |
| Continuous Body Diode Current | I_S | $T_C = 25^\circ\text{C}$ | -- | -- | 98 | A |
| Pulsed Diode Forward Current | I_{SM} | | -- | -- | 270 | |
| Body Diode Voltage | V_{SD} | $T_J = 25^\circ\text{C}, I_{SD} = 40A, V_{GS} = 0V$ | -- | 0.77 | 1.2 | V |
| Reverse Recovery Charge | t_{rr} | $T_J = 25^\circ\text{C}, I_F = 20A,$ $di/dt = 100A/\mu s$ | -- | 27 | -- | nS |
| Forward Turn-on Time | Q_{rr} | | -- | 89 | -- | nC |

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH$
4. The power dissipation is limited by 175°C junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage

Fig.3 Forward Characteristics of Reverse Diode

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized VGS(th) vs. TJ

Fig.6 Normalized RDSON vs. TJ

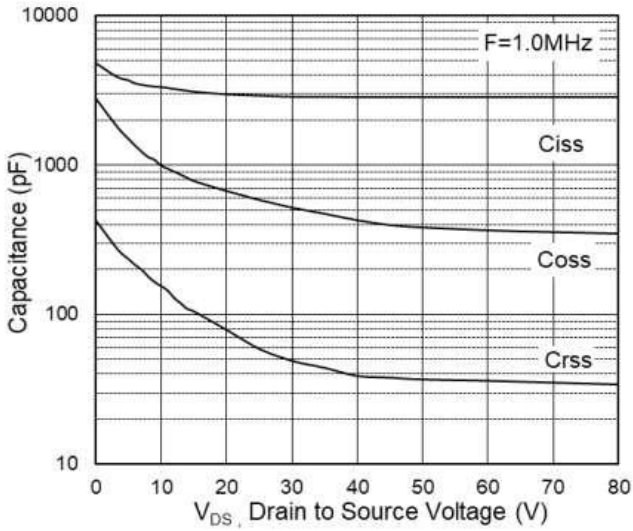
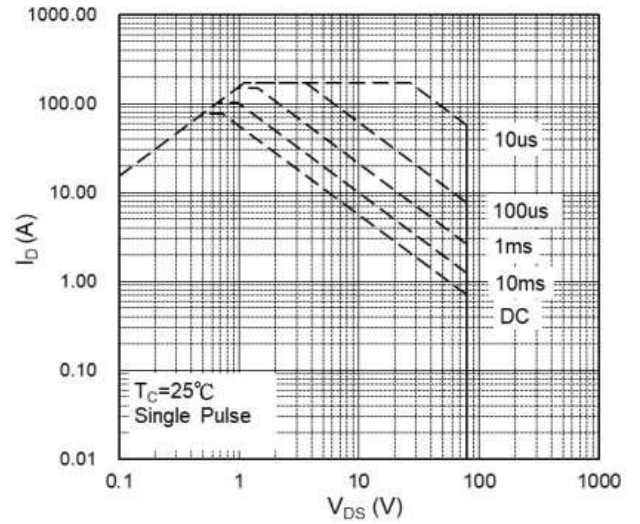
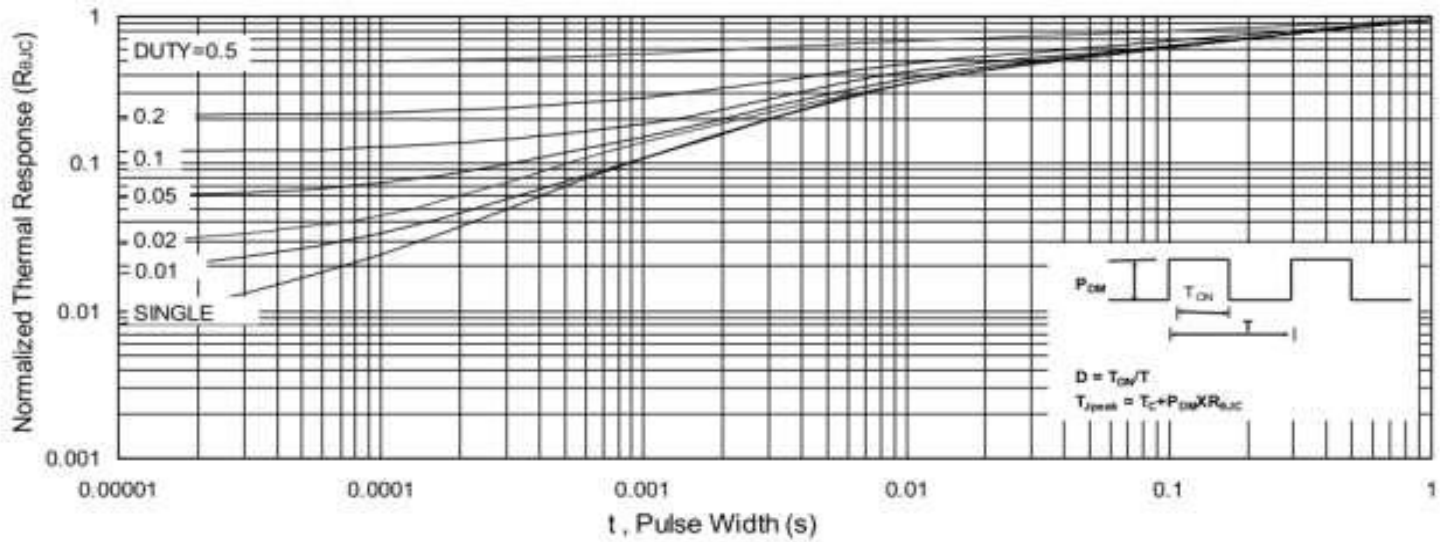
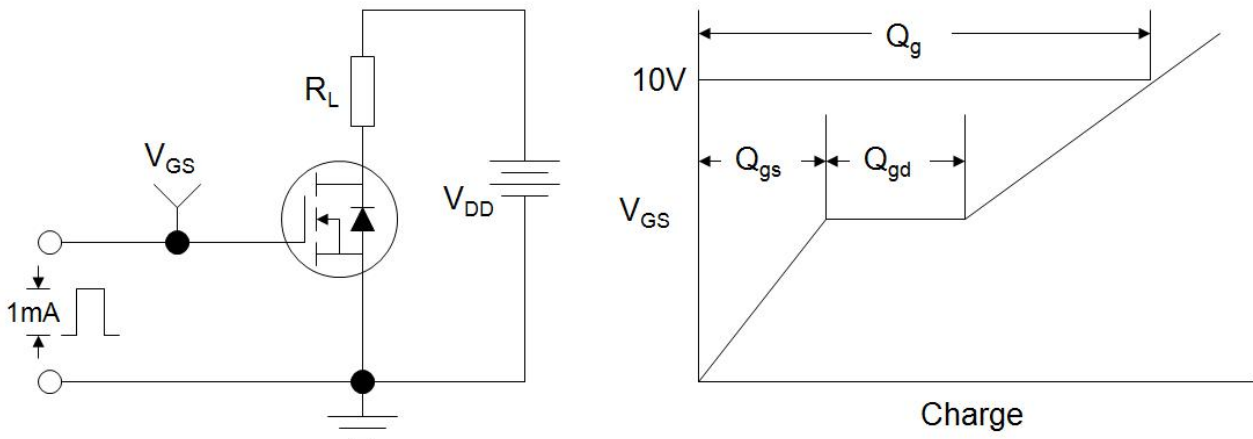
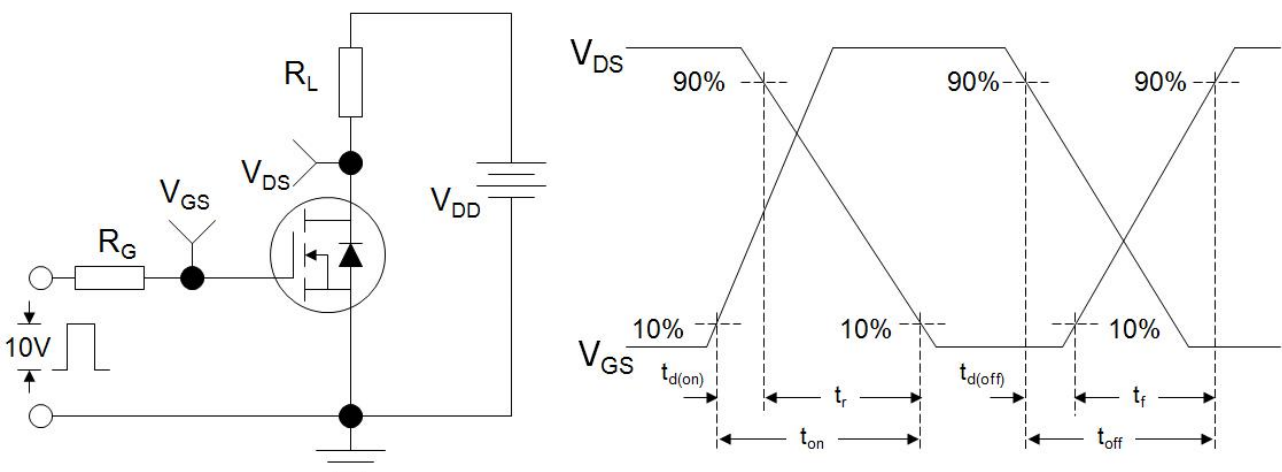
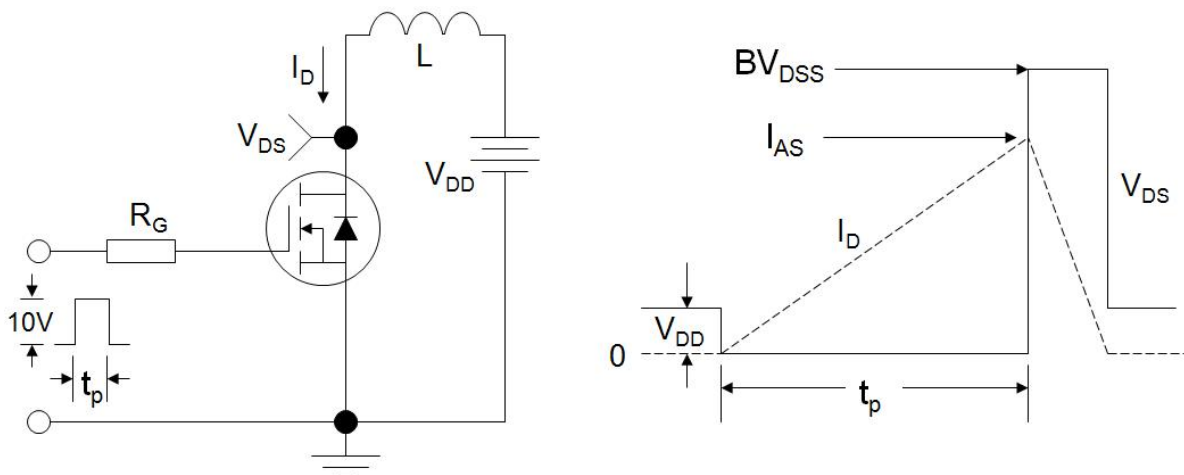
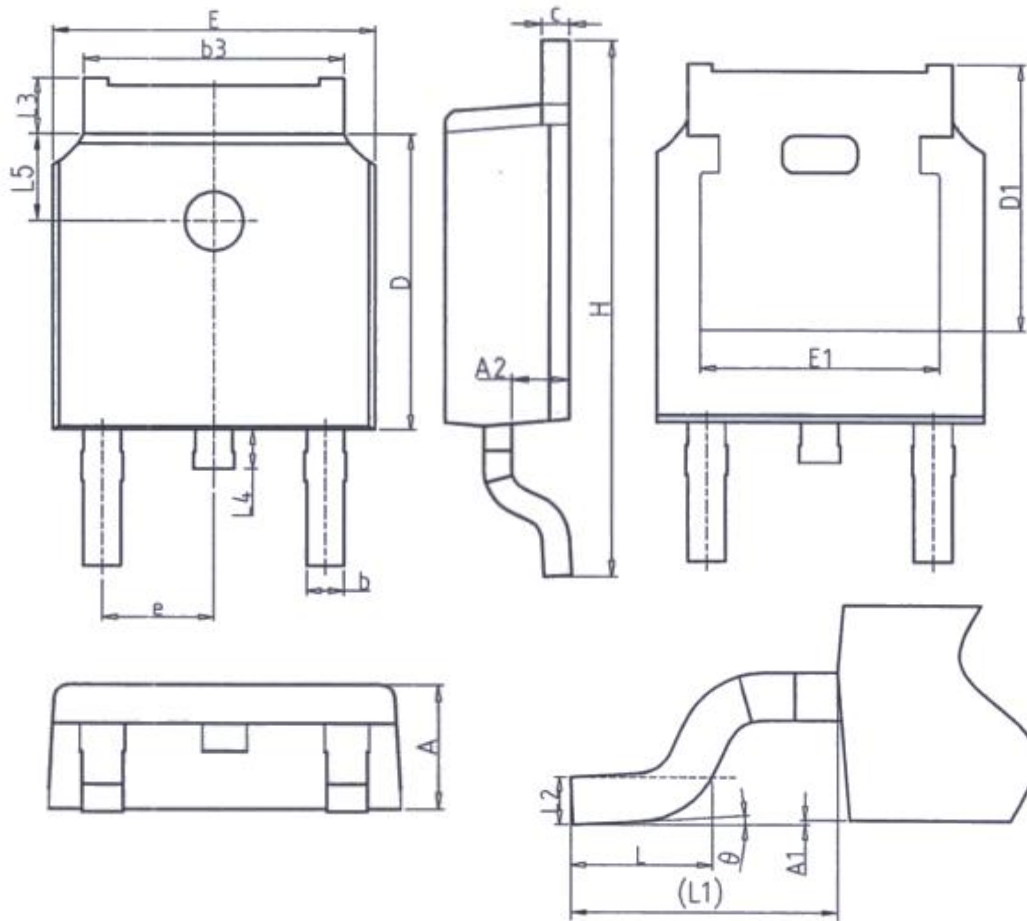
Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


TO-252


| Unit: mm | | |
|----------|---------|------|
| Symbol | Min. | Max. |
| A | 2.20 | 2.40 |
| A1 | 0.00 | 0.20 |
| A2 | 0.97 | 1.17 |
| b | 0.68 | 0.90 |
| b3 | 5.20 | 5.50 |
| c | 0.43 | 0.63 |
| D | 5.98 | 6.22 |
| D1 | 5.30REF | |
| E | 6.40 | 6.80 |
| E1 | 4.63 | - |

| Unit: mm | | |
|----------|----------|-------|
| Symbol | Min. | Max. |
| e | 2.286BSC | |
| H | 9.40 | 10.50 |
| L | 1.38 | 1.75 |
| L1 | 2.90REF | |
| L2 | 0.51BSC | |
| L3 | 0.88 | 1.28 |
| L4 | - | 1.00 |
| L5 | 1.65 | 1.95 |
| theta | 0° | 8° |

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