

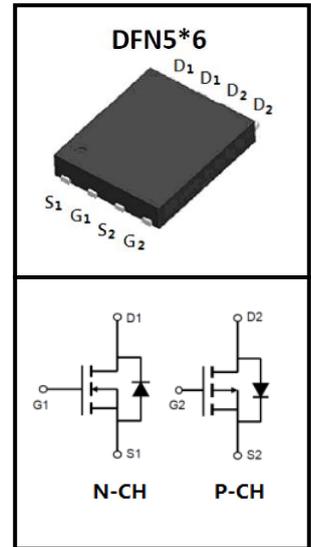
N+P-Channel Logic Level Enhancement Mode Power MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- H-bridge
- Inverters



Device Marking and Package Information

Device	Package	Marking
CTN04PN035	DFN5*6	CTN04PN035

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value		Unit
Drain-Source Voltage ($V_{GS} = 0V$)	V_{DSS}	40	-40	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	I_D	18	-18	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		10	-9.5	
Pulsed Drain Current (note2)	I_{DM}	32	-26	A
Gate Source Voltage	V_{GSS}	± 20	± 20	V
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	P_D	10	20	W
Single Pulse Avalanche Energy (note3)	E_{AS}	12	25	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+175		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	40	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	65	$^\circ\text{C/W}$

Electrical Characteristics $T_j = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = 32V, V_{GS} = 0V, T_J = 100^\circ\text{C}$	--	--	5	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	--	2.5	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 15A$	--	15	20	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	--	17	23	$m\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$	--	415	--	pF
Output Capacitance	C_{oss}		--	112	--	
Reverse Transfer Capacitance	C_{rss}		--	11	--	
Total Gate Charge (4.5V)	Q_g	$V_{DS} = 30V, I_D = 4A, V_{GS} = 10V$	--	6.5	--	nC
Gate-Source Charge	Q_{gs}		--	1.2	--	
Gate-Drain Charge	Q_{gd}		--	1.1	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 15V, I_D = 4A, V_{GS} = 10V, R_G = 3.3\Omega$	--	4	--	ns
Turn-on Rise Time	t_r		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	15	--	
Turn-off Fall Time	t_f		--	2	--	
Body Diode Characteristics						
Continuous Body Diode Current	I_S		--	--	18	A
Pulsed Diode Forward Current	I_{SM}		--	--	32	A
Body Diode Voltage	V_{SD}	$I_{SD} = 1A, V_{GS} = 0V$	--	--	1.2	V

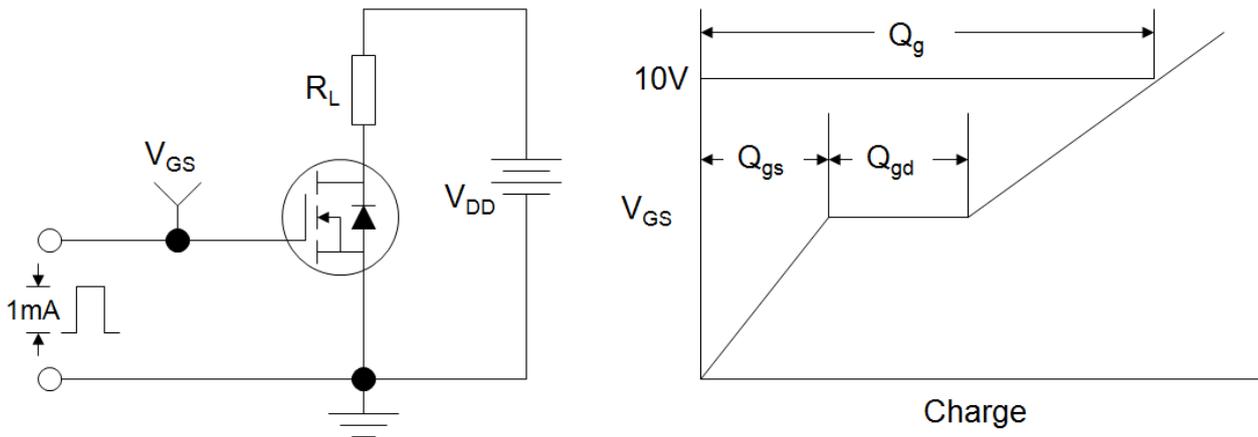
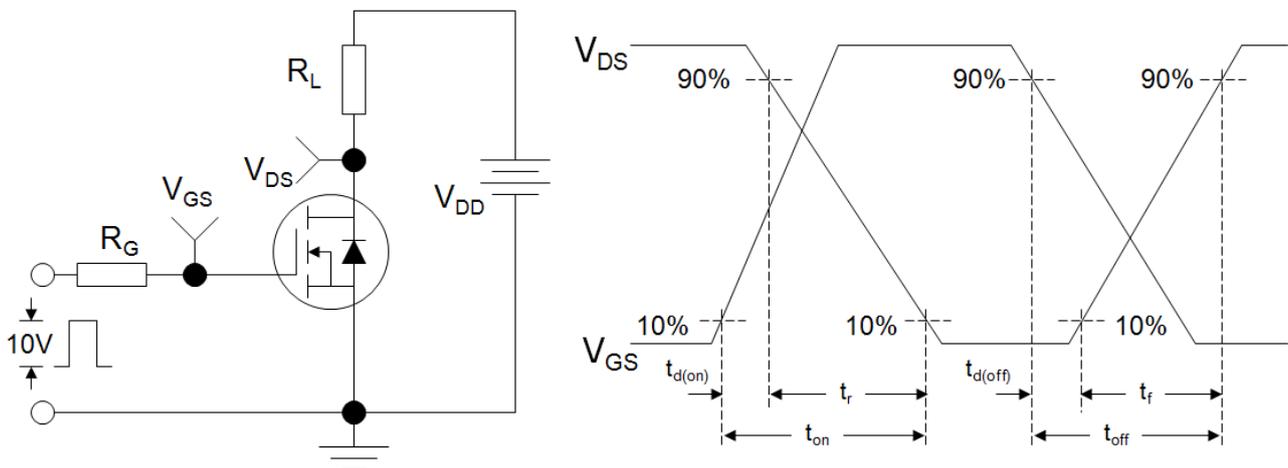
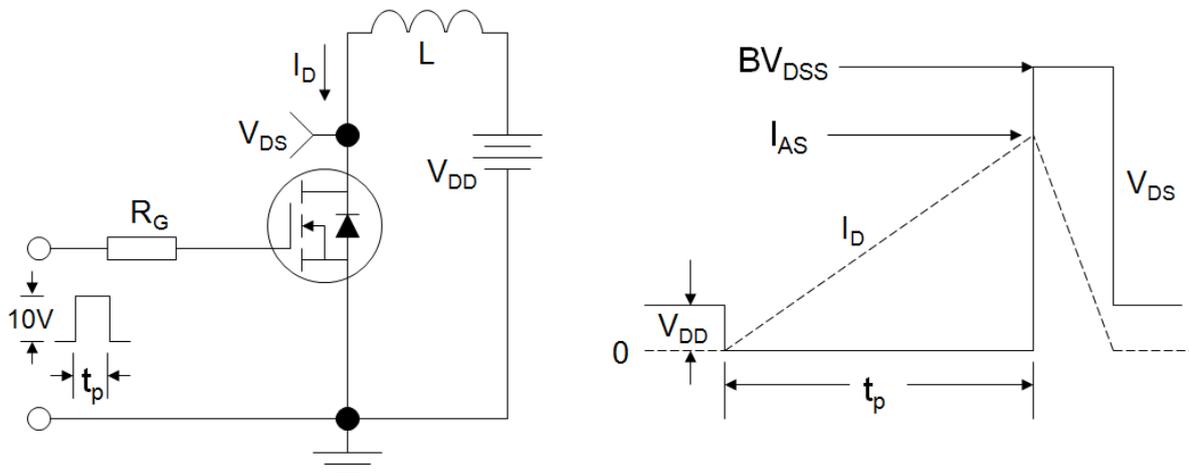
Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH$
4. The power dissipation is limited by 175°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

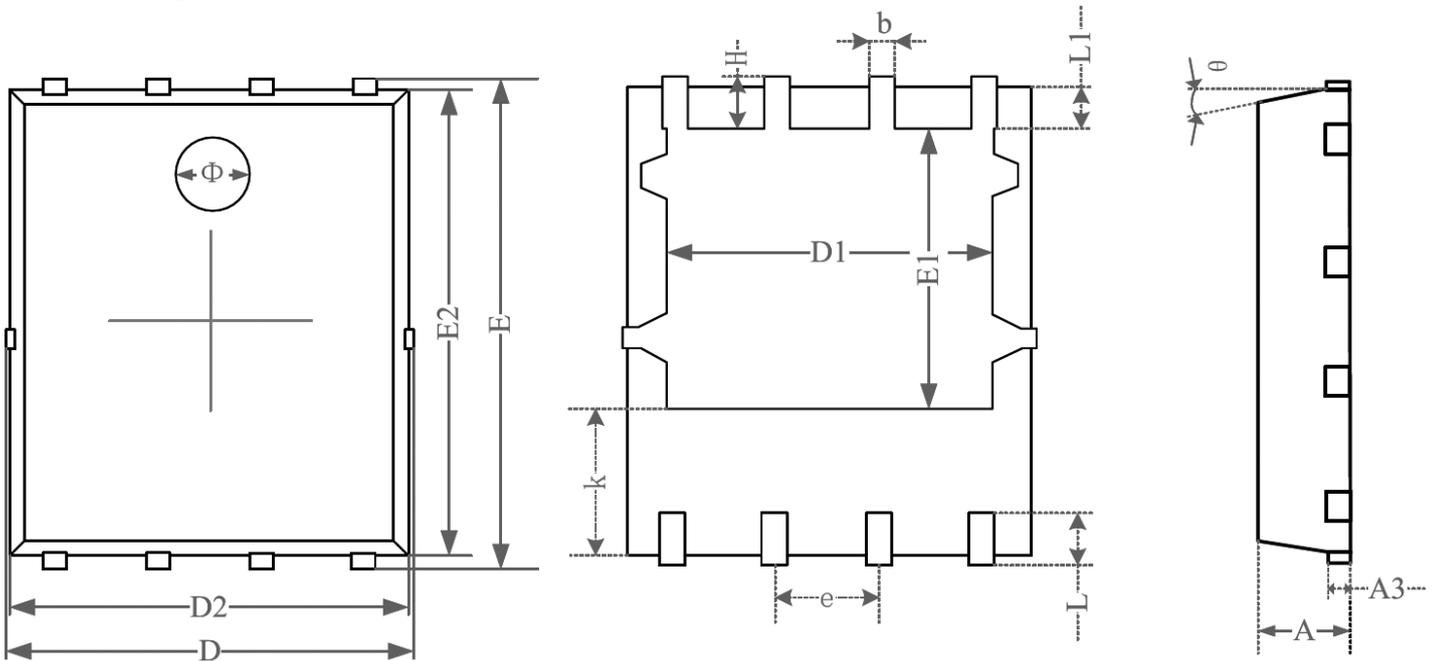
Electrical Characteristics $T_j = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	-40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = -32V, V_{GS} = 0V, T_J = 100^\circ\text{C}$	--	--	5	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.2	--	-2.5	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -15A$	--	29	35	$m\Omega$
		$V_{GS} = -4.5V, I_D = -10A$	--	38.5	46	$m\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz$	--	1040	--	pF
Output Capacitance	C_{oss}		--	180	--	
Reverse Transfer Capacitance	C_{rss}		--	125	--	
Total Gate Charge (4.5V)	Q_g	$V_{DS} = -30V, I_D = -4A, V_{GS} = -10V$	--	19	--	nC
Gate-Source Charge	Q_{gs}		--	3.6	--	
Gate-Drain Charge	Q_{gd}		--	4.6	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = -15V, I_D = -4A, V_{GS} = -10V, R_G = 3.3\Omega$	--	10	--	ns
Turn-on Rise Time	t_r		--	5.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	3.6	--	
Turn-off Fall Time	t_f		--	4.6	--	
Body Diode Characteristics						
Continuous Body Diode Current	I_S		--	--	-18	A
Pulsed Diode Forward Current	I_{SM}		--	--	-26	A
Body Diode Voltage	V_{SD}	$I_{SD} = -1A, V_{GS} = 0V$	--	--	-1.2	V

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH$
4. The power dissipation is limited by 175°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


DFN5*6



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.870	0.900	0.930	0.034	0.035	0.036
A3	0.152REF.			0.006REF.		
D	4.944	5.020	5.096	0.195	0.198	0.201
E	5.974	6.050	6.126	0.235	0.238	0.241
D1	3.910	4.010	4.110	0.154	0.158	0.162
E1	3.375	3.475	3.575	0.133	0.137	0.141
D2	4.870	4.900	4.930	0.192	0.193	0.194
E2	5.720	5.750	5.780	0.226	0.227	0.228
k	1.190	1.290	1.390	0.047	0.051	0.055
b	0.350	0.380	0.410	0.014	0.015	0.016
e	1.270TYP.			0.050TYP.		
L	0.559	0.635	0.711	0.022	0.025	0.028
L1	0.424	0.500	0.576	0.017	0.020	0.023
H	0.574	0.650	0.726	0.023	0.026	0.029
θ	10°	11°	12°	10°	11°	12°
Φ	1.150	1.200	1.250	0.045	0.047	0.049

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