PolyPhase Synchronous Boost Controller with PMBus Interface

FEATURES

- **Wide V_{IN} Range: 4.5V to 60V**
- **1% Total Output Voltage Accuracy Over Temperature at V_{IN} = 12V**
- **PMBus Compliant Serial Interface:**
  - **Programmable V_{OUT}: Up to 60V with 0.2% Resolution**
  - **Read Back of Average and Peak Temperature, Current, and Voltage (25Hz Refresh Rate)**
  - **Fault Status**
- Phase-Lockable Frequency: 75kHz to 850kHz
- Less than 1ms Power-Up Time
- Power Good Output Voltage Monitor
- Internal LDO Powers Gate Driver from VBIAS or $EXTV_{CC}$
- Low Shutdown Current: I_Q < 10µA
- Clock Out for 4-Phase Operation (40A Output Current)
- Available in a Thermally-Enhanced 5mm x 6mm QFN

APPLICATIONS

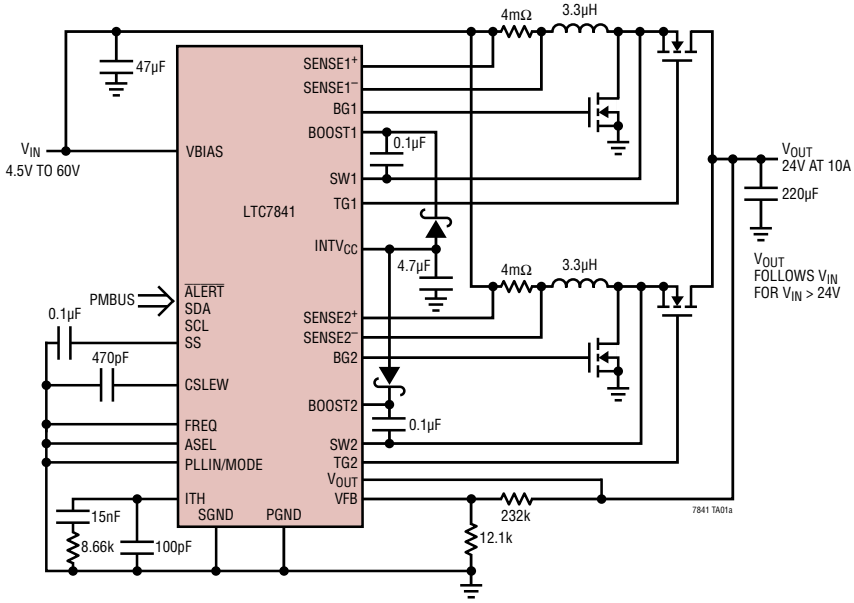
- Automotive Systems, Medical, Industrial

DESCRIPTION

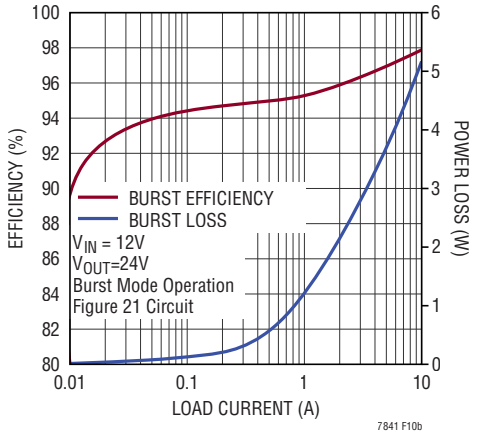
The LTC®7841 is a high performance PolyPhase® single output synchronous boost converter controller that drives two N-channel power MOSFET stages out-of-phase. Multiphase operation reduces input and output capacitor requirements and allows the use of smaller inductors than the single-phase equivalent. Synchronous rectification increases efficiency, reduces power loss and eases thermal requirements, enabling high power boost applications. The output voltage can be adjusted up to 60V with 0.2% resolution via a PMBus-compliant serial interface. The serial interface can also be used to read back fault status, input/output current, input/output voltage and temperature. System configuration and monitoring is supported by the LTpowerPlay® development system.

PolyPhase operation allows the LTC7841 to be configured for 2-, 3-, 4-, 6-, and 12-phase operation.

TYPICAL APPLICATION



Efficiency and Power Loss vs Output Current



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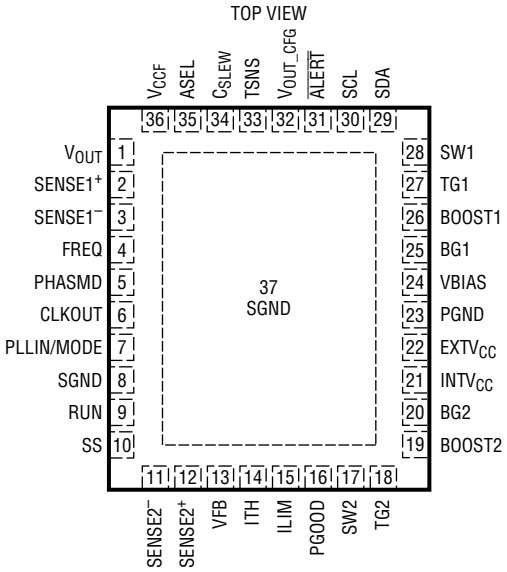
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

VBIAS, V_{OUT} ..... 65V to –0.3V
BOOST1, BOOST2 ..... 71V to –0.3V
SW1, SW2 ..... 65V to –5V
$INTV_{CC}$, (BOOST1 – SW1), (BOOST2 – SW2) . 6V to -0.3V
PGOOD, SDA, SCL, PLLIN/MODE ..... 6V to –0.3V
ALERT ..... 5V to –0.3V
RUN ..... 8V to –0.3V
$EXTV_{CC}$ ..... 14V to –0.3V
$SENSE1^+$, $SENSE1^-$, $SENSE2^+$, $SENSE2^-$ .... 65V to –0.3V
($SENSE1^+$ – $SENSE1^-$), ($SENSE2^+$ – $SENSE2^-$),
(V_{BIAS} – $SENSE1^+$), (V_{BIAS} – $SENSE2^+$),
(V_{BIAS} – $SENSE1^-$), (V_{BIAS} – $SENSE2^+$) .... 0.3V to –0.3V
ILIM, SS, ITH, FREQ, PHASMD, VFB ..... $INTV_{CC}$ to –0.3V
ASEL, CSLEW, TSNS, V_{OUT_CFG} ..... V_{CCF} to –0.3V
Operating Junction Temperature Range ... –40°C to 150°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

θ_{JA} = 43°C/W
EXPOSED PAD (PIN 37) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7841EUHE#PBF	LTC7841EUHE#TRPBF	7841	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LTC7841IUHE#PBF	LTC7841IUHE#TRPBF	7841	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{RUN} = 5V, $EXTV_{CC}$ = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VBIAS	Input Supply Operating Voltage Range	VBIAS Rising		4.5		60	V
V_{FB}	Regulated Feedback Voltage	VOUT_COMMAND = 50% VOUT_COMMAND = 25% VOUT_COMMAND = 99.8%	● ● ●	1.188 0.590 2.371	1.2 0.6 2.395	1.212 0.610 2.419	V V V
	Feedback Current	(Note 4)			±5	±50	nA
V_{OUTSNS}	V_{OUTSNS} Leakage Pin Current	V_{OUT} = 36V			30		uA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Note 4); VBIAS = 6V to 60V			0.002	0.01	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 1.6V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
g_m	Transconductance Amplifier g_m	(Note 4); I_{TH} = 1.2V; Sink/Source 5µA			2		mmho
I_Q	Input DC Supply Current	(Note 5)					
	Pulse Skip or Forced Continuous Mode	RUN = 5V, V_{FB} = 1.25V (No Load)			2.5	4	mA
	Sleep Mode	RUN = 5V, V_{FB} = 1.25V (No Load)			0.800	1.5	mA
	Shutdown	RUN = 0V			8		µA
UVLO	$INTV_{CC}$ Undervoltage Lockout Thresholds	$INTV_{CC}$ Ramping Up $INTV_{CC}$ Ramping Down	● ●	 3.5	4.1 3.8	4.4	V V
	$SENSE^+$ Pin Current	V_{FB} = 1.1V, I_{LIM} = Float			200	300	µA
	$SENSE^-$ Pin Current	V_{FB} = 1.1V, I_{LIM} = Float				±1	µA
I_{SS}	Soft-Start Charge Current	V_{SS} = 0V		7	10	13	µA
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	●	1.18	1.28	1.38	V
	RUN Pin Hysteresis				100		mV
	RUN Pin Hysteresis Current	V_{RUN} > 1.28V			4.5		µA
	RUN Pin Current	V_{RUN} < 1.28V			0.5		µA
$\Delta V_{REF,ADJ}$	Maximum Reference Adjust Range Set Point Accuracy Resolution LSB Step Size	MFR_VOUT_COMMAND = 0% to 99.8% MFR_VOUT_COMMAND = 37.5% to 99.8%		0 –1	 9 4.69	2.395 1	V % Bits mV
NL_ V_{OUT}	DAC Nonlinearity				±1		LSB
I_{ASEL}	ASEL Programming Current				10		µA
I_{CSLEW}	C_{SLEW} Pull-Up Current				–10		µA
T_{INIT}	Initialization Time	(Note 9)			1		ms
SR_{MARGIN}	Reference Slew Rate During Margin Change	(see Note 8) C_{SLEW} = 470pF, Nominal SR mode C_{SLEW} = 470pF, Fast SR mode C_{SLEW} = 470pF, Slow SR mode C_{SLEW} = OPEN C_{SLEW} = INTVcc	 	 	 0.8 1.6 0.1 80 10	 	 %/ms %/ms %/ms %/ms %/µs
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 1.1V, ILIM = 0 V_{FB} = 1.1V, ILIM = FLOAT V_{FB} = 1.1V, ILIM = $INTV_{CC}$	● ● ●	42 68 88	50 75 100	58 82 110	mV mV mV
	Matching Between $V_{SENSE1(MAX)}$ and $V_{SENSE2(MAX)}$	V_{FB} = 1.1V, I_{LIM} = $INTV_{CC}$ V_{FB} = 1.1V, I_{LIM} = Float V_{FB} = 1.1V, I_{LIM} = GND	● ● ●	–12 –10 –9	0 0 0	12 10 9	mV mV mV

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver							
	Top Gate Rise Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Top Gate Fall Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Bottom Gate Rise Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Bottom Gate Fall Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Top Gate Pull-Up Resistance				1.2		Ω
	Top Gate Pull-Down Resistance				1.2		Ω
	Bottom Gate Pull-Up Resistance				1.2		Ω
	Bottom Gate Pull-Down Resistance				1.2		Ω
	Top Gate Off to Bottom Gate On Switch-On Delay Time	C_{LOAD} = 3300pF (Each Driver)			30		ns
	Bottom Gate Off to Top Gate On Switch-On Delay Time	C_{LOAD} = 3300pF (Each Driver)			30		ns
	Maximum BG Duty Factor				96		%
$t_{ON(MIN)}$	Minimum BG On-Time	(Note 7)			110		ns
$INTV_{CC}$ Linear Regulator							
	Internal V_{CC} Voltage	6V < V_{BIAS} < 60V, V_{EXTVCC} = 0V		5.2	5.4	5.6	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
	Internal V_{CC} Voltage	6V < V_{EXTVCC} < 13V		5.2	5.4	5.6	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 40mA, V_{EXTVCC} = 8.5V			0.5	2	%
	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.8	5	V
	$EXTV_{CC}$ Hysteresis				250		mV
Oscillator and Phase-Locked Loop							
	Programmable Frequency	R_{FREQ} = 25k R_{FREQ} = 60k R_{FREQ} = 100k		 335	105 400 760	 465	kHz kHz kHz
f_{LOW}	Lowest Fixed Frequency	V_{FREQ} = 0V		320	350	380	kHz
	Highest Fixed Frequency	V_{FREQ} = $INTV_{CC}$		488	535	585	kHz
	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		850	kHz
PGOOD Output							
	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.4	V
	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative Hysteresis		 –12	 –10 2.5	 –8	 % %
		V_{FB} Ramping Positive Hysteresis		8	10 2.5	12	% %
	PGOOD Delay	PGOOD Going High to Low			45		µs
	OV Protection Threshold	V_{FB} Ramping Positive		1.296	1.32	1.344	V
Output Voltage Readback							
N	Resolution LSB Step Size				13 10		Bits mV
	Readback Voltage Range	Diode connected between $INTV_{CC}$ and V_{CCF} pins No diode	● ●			60 55	V V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT_TUE}	Total Unadjusted Error		●			±1.2	%
$T_{CONVERT}$	Conversion Time				40		ms
Input Voltage Readback (VBIAS)							
N	Resolution LSB Step Size				13 10		Bits mV
	Readback Voltage Range	Diode connected between $INTV_{CC}$ and V_{CCF} pins No diode	● ●			60 55	V V
V_{IN_TUE}	Total Unadjusted Error		●			±1.6	%
$T_{CONVERT}$	Conversion Time				40		ms
Output Current Readback							
N	Resolution LSB Step Size	$V_{SENSE}+ – V_{SENSE}–$			13 50		Bits µV
$V_{F/S}$	Full Scale Sense Voltage				±1.638		V
I_{OUT_TUE}	Total Unadjusted Error	$V_{SENSE}+ – V_{SENSE}– > 25mV$			±2		%
$T_{CONVERT}$	Conversion Time				40		ms
Input Current Readback							
N	Resolution LSB Step Size	$V_{SENSE}+ – V_{SENSE}–$			13 50		Bits µV
$V_{F/S}$	Full Scale Sense Voltage				±1.638		V
I_{IN_TUE}	Total Unadjusted Error	$V_{SENSE}+ – V_{SENSE}– > 25mV$ $\|V_{SENSE}+ – V_{SENSE}–\| < 25mV$	● ●			±2 ±0.5	% mV
$T_{CONVERT}$	Conversion Time				40		ms
Internal Temperature Readback							
N	Resolution LSB Step Size				9 1		Bits °C
$V_{F/S}$	Full Scale Temperature				±256		°C
T_{IN_TUE}	Internal Temperature Total Unadjusted Error				±3		°C
$T_{CONVERT}$	Conversion Time				40		ms
External Temperature Sense (TSNS pin) Readback							
N	Resolution LSB Step Size				10 4		Bits mV
$V_{F/S}$	Full Scale Voltage				4.096		V
T_{EXT_TUE}	TSNS Voltage Total Unadjusted Error	R_{TSNS} = 50kΩ			±5		%
$T_{CONVERT}$	Conversion Time				40		ms
I_{TSNS}	TSNS Pin Source Current				20		µA
PMBus Interface Parameters							
V_{IH}, SDA, SCL	Input High Voltage			2.1			V
V_{IL}, SDA, SCL	Input Low Voltage					0.8	V
I_{IH}, SDA, SCL	Input Leakage Current			5		5	µA
V_{OL}, SDA	Output Low Voltage (SDA)	Sinking 3mA				0.4	V
V_{OL}, $\overline{ALERT}$	Output Low Voltage (ALERT)	Sinking 1mA				0.4	V
f_{SCL}	Serial Bus Operating Frequency			10		400	kHz

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
T_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
T_{HD_SDA}	Hold Time After (Repeated) Start Condition			0.6			µs
T_{SU_SDA}	Repeated Start Condition Setup Time			0.6			µs
T_{SU_STO}	Stop Condition Setup Time			0.6			µs
$T_{HD\_DAT(OUT)}$	Data Hold Time			300		900	ns
$T_{HD\_DAT(IN)}$	Input Data Hold Time			0			ns
T_{SU_DAT}	Data Set-Up Time			100			ns
T_{LOW}	Clock Low Period			1.3		10000	µs
T_{HIGH}	Clock High Period			0.6			µs
$T_{TIMEOUT\_SMB}$	Stuck PMBus Timer	Measured from Last PMBus Start Event			30		ms
Boost1 and Boost2 Charge Pump							
	BOOST Charge Pump Available Output Current	$V_{SW1,2}$ = 12V, $V_{BOOST1,2} - V_{SW1,2}$ = 4.5V; FREQ = 0V Forced Continuous or Pulse-Skipping Mode			55		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC7841 is tested under pulsed load conditions such that $T_J = T_A$. The LTC7841E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7841I is guaranteed over the full –40°C to 125°C temperature range

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet 43°C/W)$$

Note 4: The LTC7841 is tested in a feedback loop that servos V_{ITH} to the output of the error amplifier while maintaining I_{TH} at the midpoint of the current limit range.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels

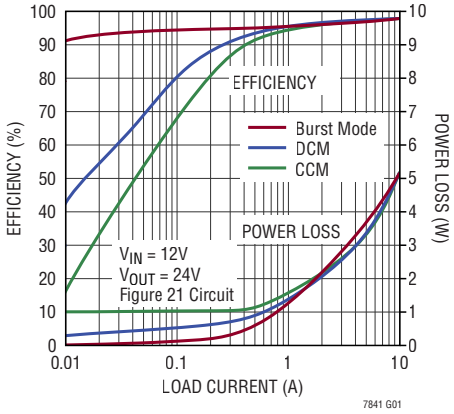
Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥ of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

Note 8: Nominal, Fast, or Slow Slew Rate mode is set by MFR_CONFIG PMBus Command.

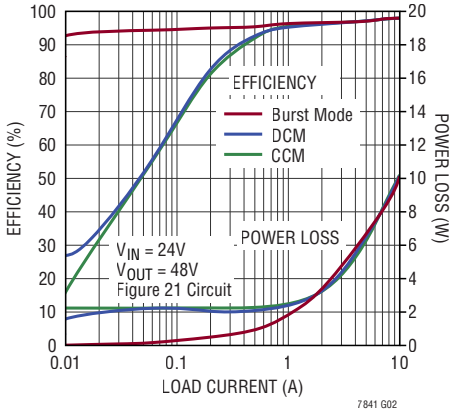
Note 9: Initialization time begins when $INTV_{CC}$ > 4.3V and RUN > 1.38V and ends when TG/BG switching begins.

TYPICAL PERFORMANCE CHARACTERISTICS

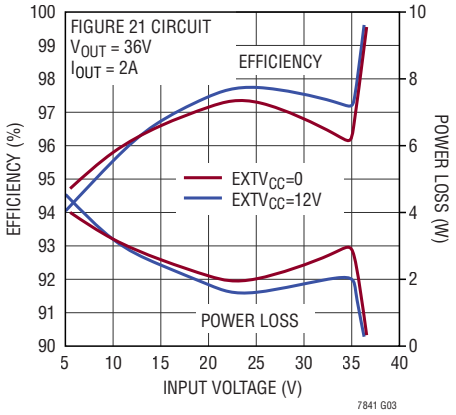
Efficiency and Power Loss vs Output Current



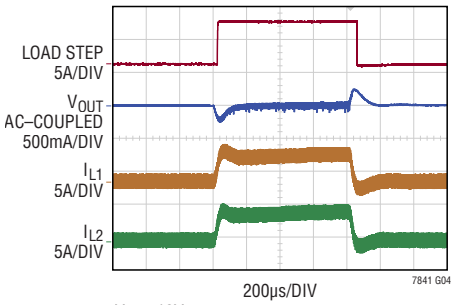
Efficiency and Power Loss vs Output Current



Efficiency and Power Loss vs V_{IN} with and Without $EXTV_{CC}$

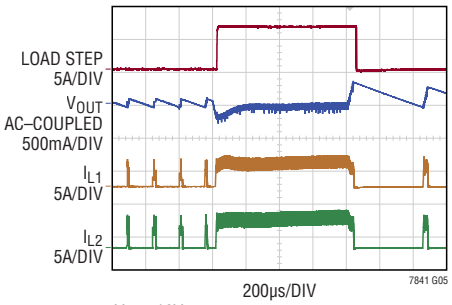


Load Step Forced Continuous Mode



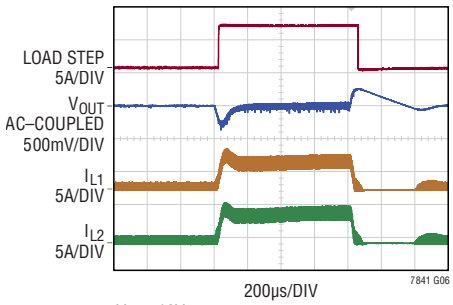
VIN = 12V
VOUT = 24V
LOAD STEP FROM 500mA TO 7A
FIGURE 21 CIRCUIT

Load Step Burst Mode Operation



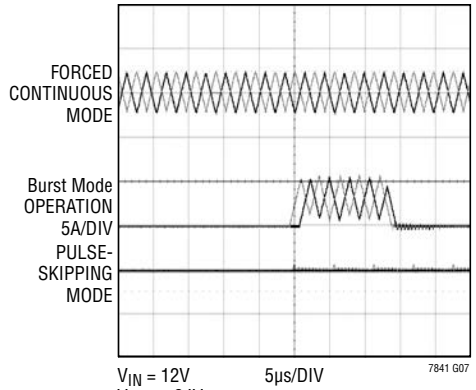
VIN = 12V
VOUT = 24V
LOAD STEP FROM 500mA TO 7A
FIGURE 21 CIRCUIT

Load Step Pulse-Skipping Mode



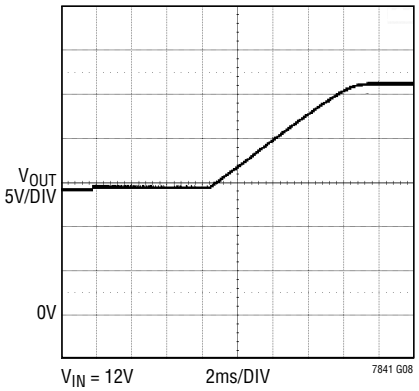
VIN = 12V
VOUT = 24V
LOAD STEP FROM 500mA TO 7A
FIGURE 21 CIRCUIT

Inductor Currents at Light Load



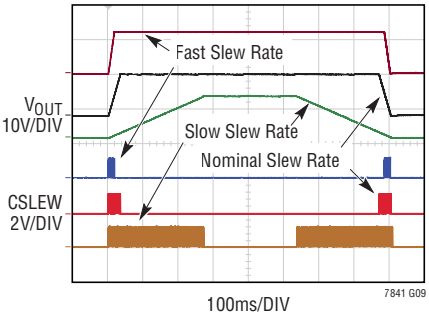
VIN = 12V
VOUT = 24V
ILOAD = 200µA
FIGURE 21 CIRCUIT

Soft Start-Up



VIN = 12V
VOUT = 24V
FIGURE 21 CIRCUIT

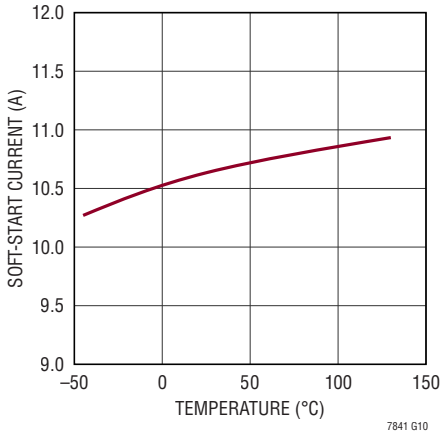
Output Voltage Changes with MFR_VOUT_COMMAND



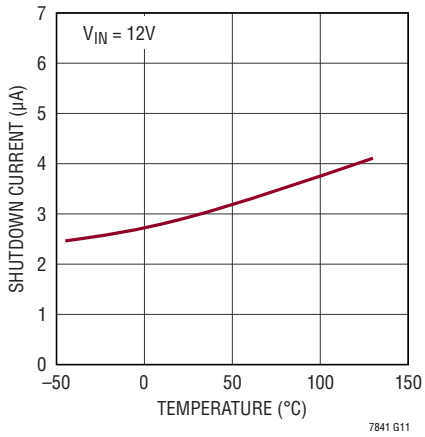
VIN = 12V
VOUT = 24V to 36V to 24V
FIGURE 21 CIRCUIT
CSLEW = 470pF

TYPICAL PERFORMANCE CHARACTERISTICS

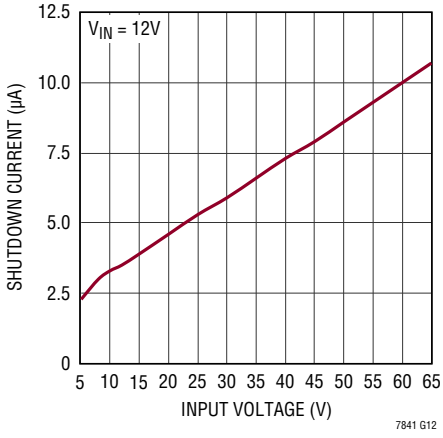
Soft-Start Pull-Up Current vs Temperature



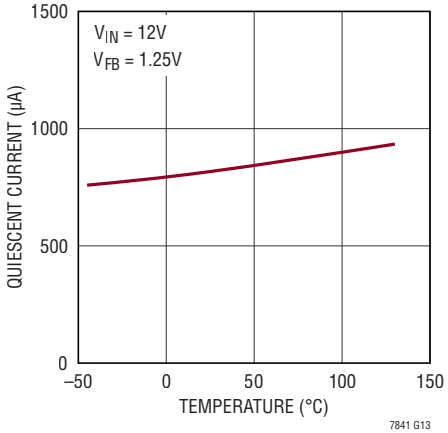
Shutdown Current vs Temperature



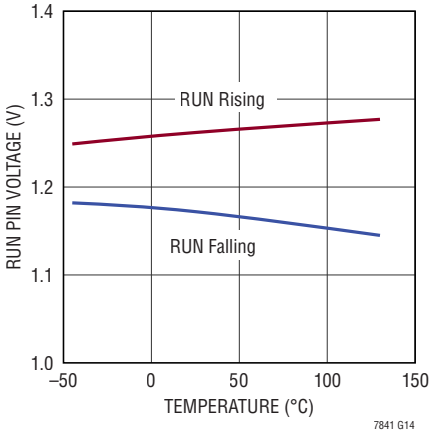
Shutdown Current vs Input Voltage



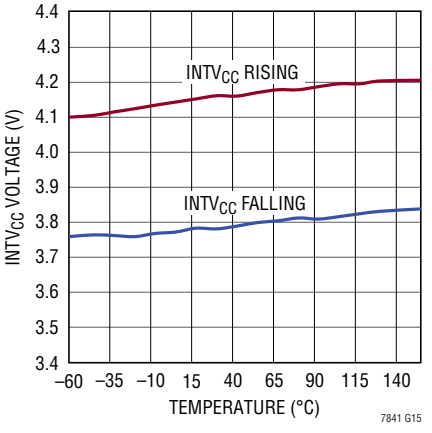
Quiescent Current vs Temperature



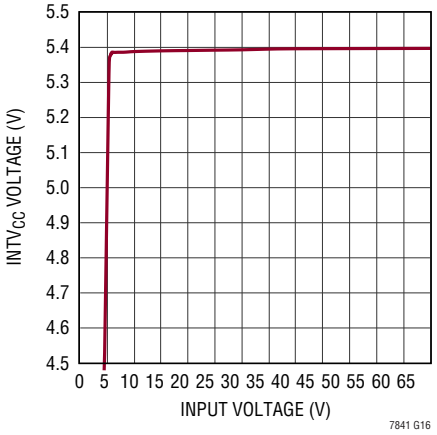
Shutdown (RUN) Threshold vs Temperature



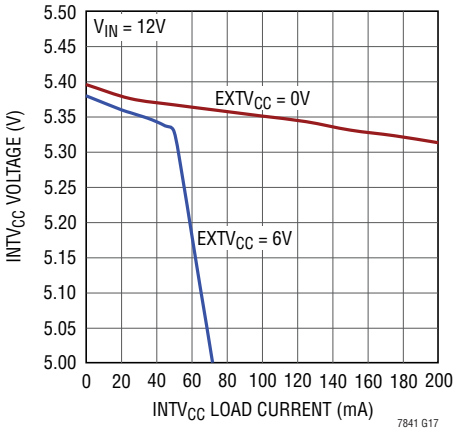
Undervoltage Lockout Threshold vs Temperature



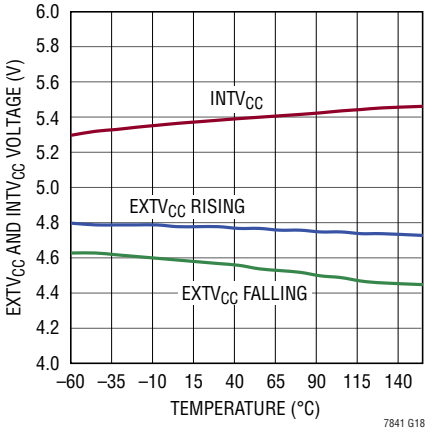
$INTV_{CC}$ Line Regulation



$INTV_{CC}$ vs $INTV_{CC}$ Load Current

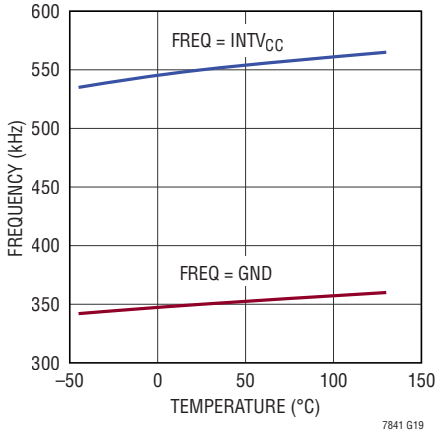


$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltages vs Temperature

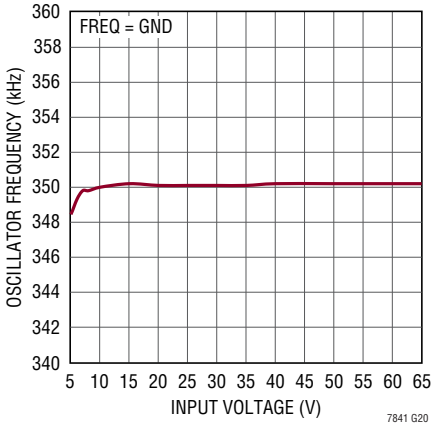


TYPICAL PERFORMANCE CHARACTERISTICS

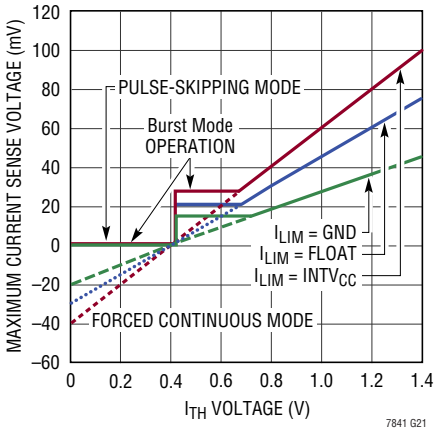
Oscillator Frequency vs Temperature



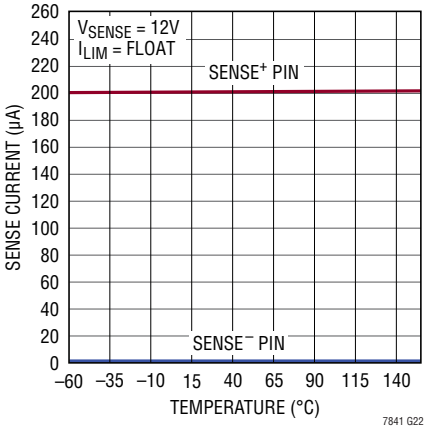
Oscillator Frequency vs Input Voltage



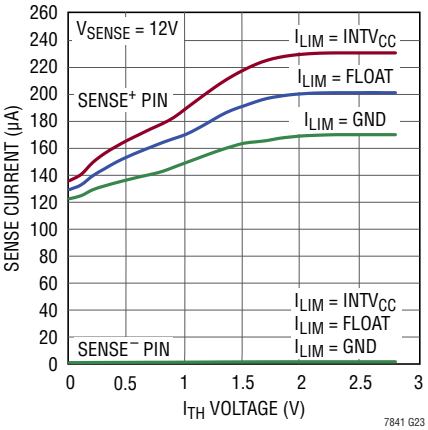
Maximum Current Sense Threshold vs ITH Voltage



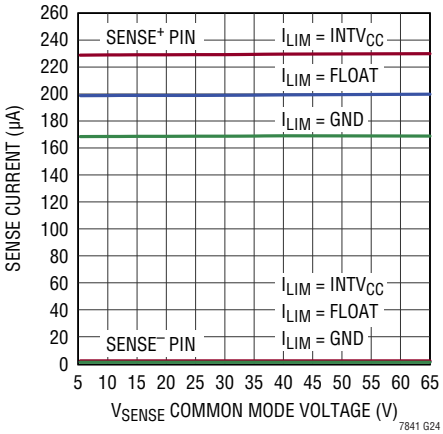
SENSE Pin Input Current vs Temperature



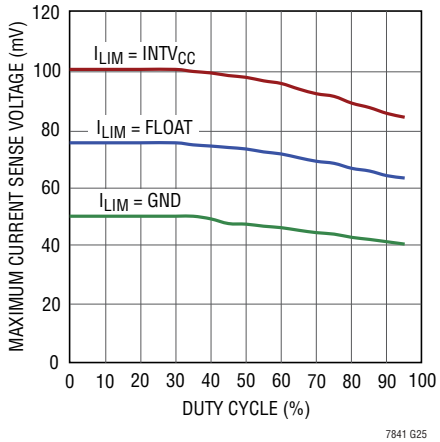
SENSE Pin Input Current vs I_{TH} Voltage



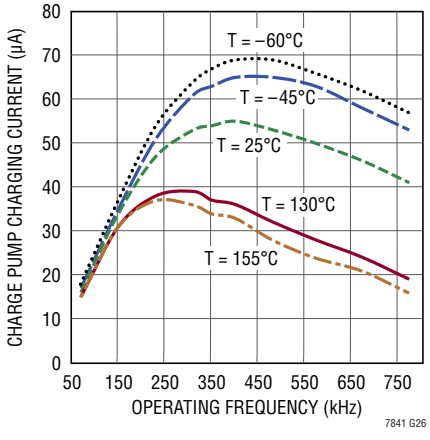
SENSE Pin Input Current vs V_{SENSE} Voltage



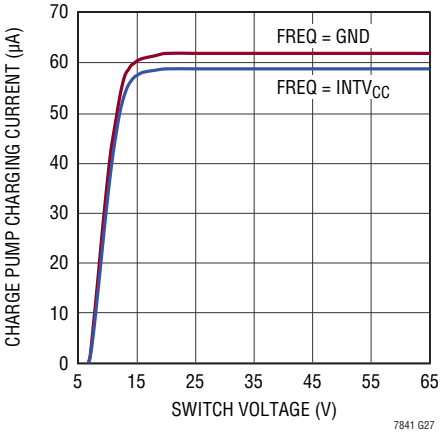
Maximum Current Sense Threshold vs Duty Cycle



Charge Pump Charging Current vs Operating Frequency

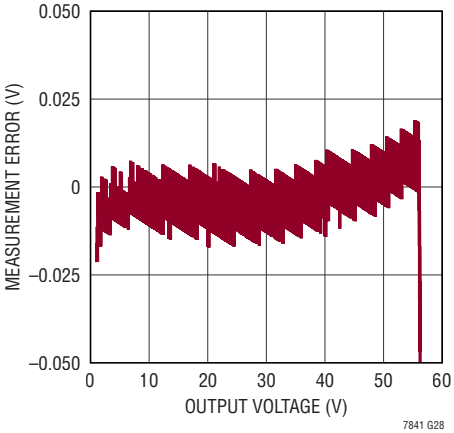


Charge Pump Charging Current vs Switch Voltage

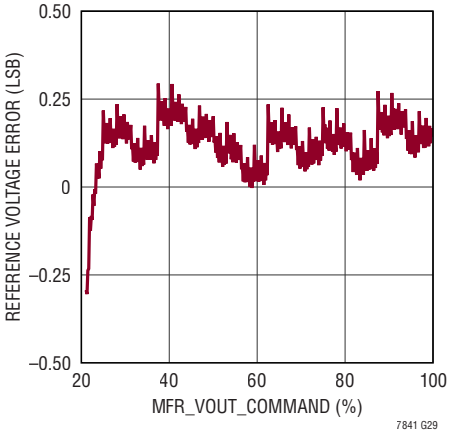


TYPICAL PERFORMANCE CHARACTERISTICS

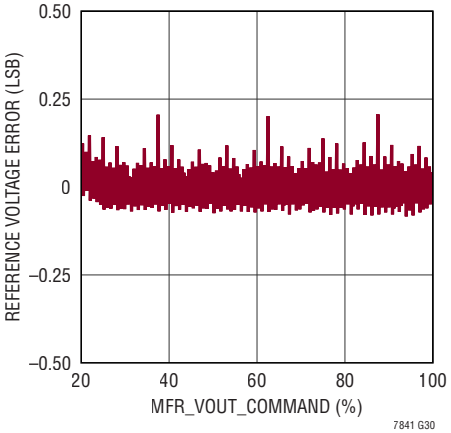
V_{OUT} Measurement Error vs V_{OUT}



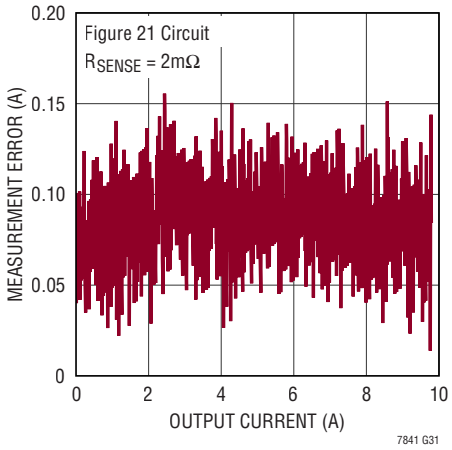
V_{OUT} Command INL



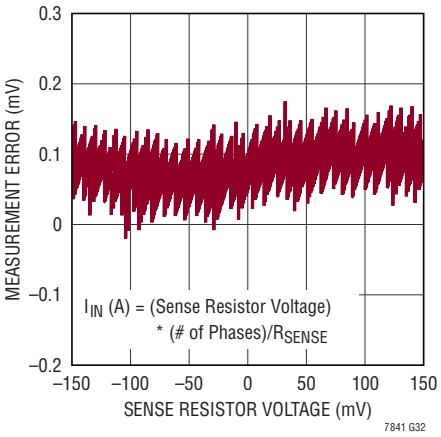
V_{OUT} Command DNL



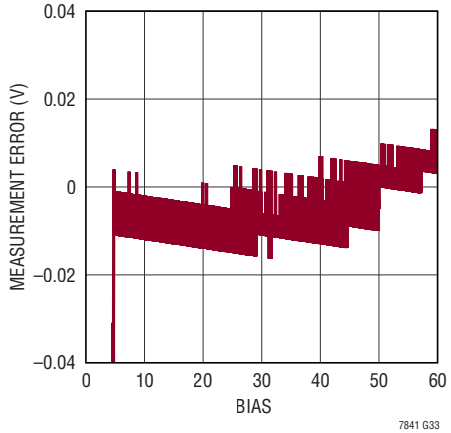
I_{OUT} Measurement Error vs I_{OUT}



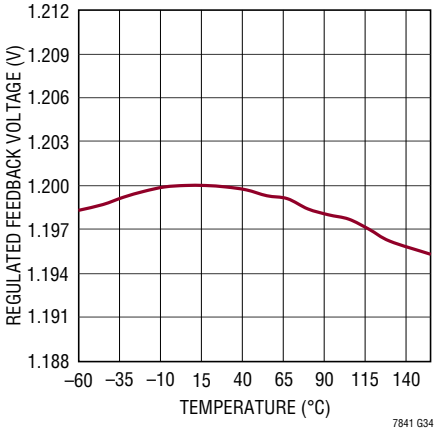
I_{IN} Measurement Error vs I_{IN}



V_{IN} Measurement Error vs V_{BIAS}



Regulated Feedback Voltage vs Temperature



PIN FUNCTIONS

SENSE1$^-$, SENSE2$^-$ (Pins 3, 11): The (–) Input to the Differential Current Comparators. When greater than $INTV_{CC}$, the SENSE – pin supplies current to the Current Comparator.

FREQ (Pin 4): The frequency control pin for the internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Connecting a resistor from the FREQ pin to GND can program the frequency. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

PHASMD (Pin 5): This pin can be floated, tied to SGND or tied to $INTV_{CC}$ to program the phase relationship between edges of BG1 and BG2, as well as the phase relationship between BG1 and CLKOUT.

CLKOUT (Pin 6): Output Clock Signal available to daisy chain multiple LTC7841 ICs in Multiphase Systems. The PHASMD pin voltage controls the relationship between BG1 and CLKOUT. The output levels swing from $INTV_{CC}$ to ground.

PLLIN/MODE (Pin 7): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising BG1 signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, determines how the LTC7841 operates at light loads. Pulling this pin to ground selects Burst Mode® operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V selects pulse skipping operation. Adding a 100k resistor between the PLLIN/MODE pin and $INTV_{CC}$ can accomplish this.

SGND (Pin 8, 37): Small Signal Ground and Paddle. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at a single point.

RUN (Pin 9): Run Control Input. Forcing this pin below 1.28V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC7841, reducing quiescent current to approximately 8µA. An external resistor divider connected to V_{IN} can set the threshold for converter operation. Once running, a 4.5µA current is sourced from the RUN pin allowing the user to program hysteresis using the resistor values.

ILIM (Pin 15): Current Comparator Sense Voltage Range Input. This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to SGND, open, and $INTV_{CC}$ to set the peak current sense voltage to 50mV, 75mV and 100mV, respectively.

$INTV_{CC}$ (Pin 21): Output of the Internal 5.4V Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to power ground with a minimum of 2.2µF ceramic or other low ESR capacitor. Do not use the $INTV_{CC}$ pin for any other purpose.

$EXTV_{CC}$ (Pin 22): External Power Input. When this pin is between 4.8V and 6V, an internal switch bypasses the internal regulator and supply power to $INTV_{CC}$ directly from $EXTV_{CC}$. Do not float this pin. It can be connected to ground when not used.

PGND (Pin 23): Driver Power Ground. Connects to the sources of bottom N-channel MOSFETs and the (–) terminal(s) of C_{IN}.

VBIAS (Pin 24): Main Supply Pin. It is normally tied to the input supply V_{IN} or to the output of the boost converter. A bypass capacitor should be tied between this pin and the signal ground pin. The operating voltage range on this pin is 4.5V to 60V.

BG1, BG2 (Pins 25, 20): Bottom Gate. Connect to the gate of the main N-channel MOSFET.

BOOST1, BOOST2 (Pins 26, 19): Floating power supply for the synchronous N-channel MOSFET. Bypass to SW with a capacitor and supply with a Schottky diode connected to $INTV_{CC}$.

PIN FUNCTIONS

SW1, SW2 (Pins 28, 17): Switch Node. Connect to the source of the synchronous N-channel MOSFET, the drain main N-channel MOSFET and the inductor.

TG1, TG2 (Pins 27, 18): Top Gate. Connect to the gate of the synchronous N-channel MOSFET.

PGOOD (Pin 16): Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is more than ±10 % away from the regulated output voltage. To avoid false trips the output voltage must be outside the range for 25µs before this output is activated.

SS (Pin 10): Output Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage during start-up.

ITH (Pins 14): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

V_{OUT} (Pin 1): Output Voltage Sense Input. This pin receives the remotely sensed output voltage and is input to the internal ADC. The converted value is readable by the READ_VOUT PMBus command.

SENSE1$^+$, SENSE2$^+$ (Pins 2, 12): Positive Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the positive terminal of a current sense resistor. The current sense resistor is normally placed at the input of the boost controller in series with the inductor. This pin also supplies power to the current comparator.

C_{SLEW} (Pin 34): Slew Rate Control. Add a capacitor to program V_{OUT} transition slew rate during changing the output voltage. The slew rate is equal to 1.7% per ms per nF of slew rate capacitance. With a 1nF capacitor, the slew rate is 1.7%/ms. Two default slew rates are also available when this pin is open or connected to $INTV_{CC}$. The slew rate can also be increased 2x or decreased 0.125x using the MFR_CONFIG command.

ASEL (Pin 35): Serial Bus Address Configuration Input. Connect a ±1% resistor from this pin to ground in order to select the 3 LSBs of the serial bus interface address. (see Table 4).

$\overline{\text{ALERT}}$ (Pin 31): Open Drain Digital Output. Connect the system SMBALERT interrupt signal to this pin. A pull-up resistor is required in the application.

SDA (Pin 29): Serial Bus Data Input and Output. A pull-up resistor is required in the application.

SCL (Pin 30): Serial Bus Clock Input. A pull-up resistor is required in the application.

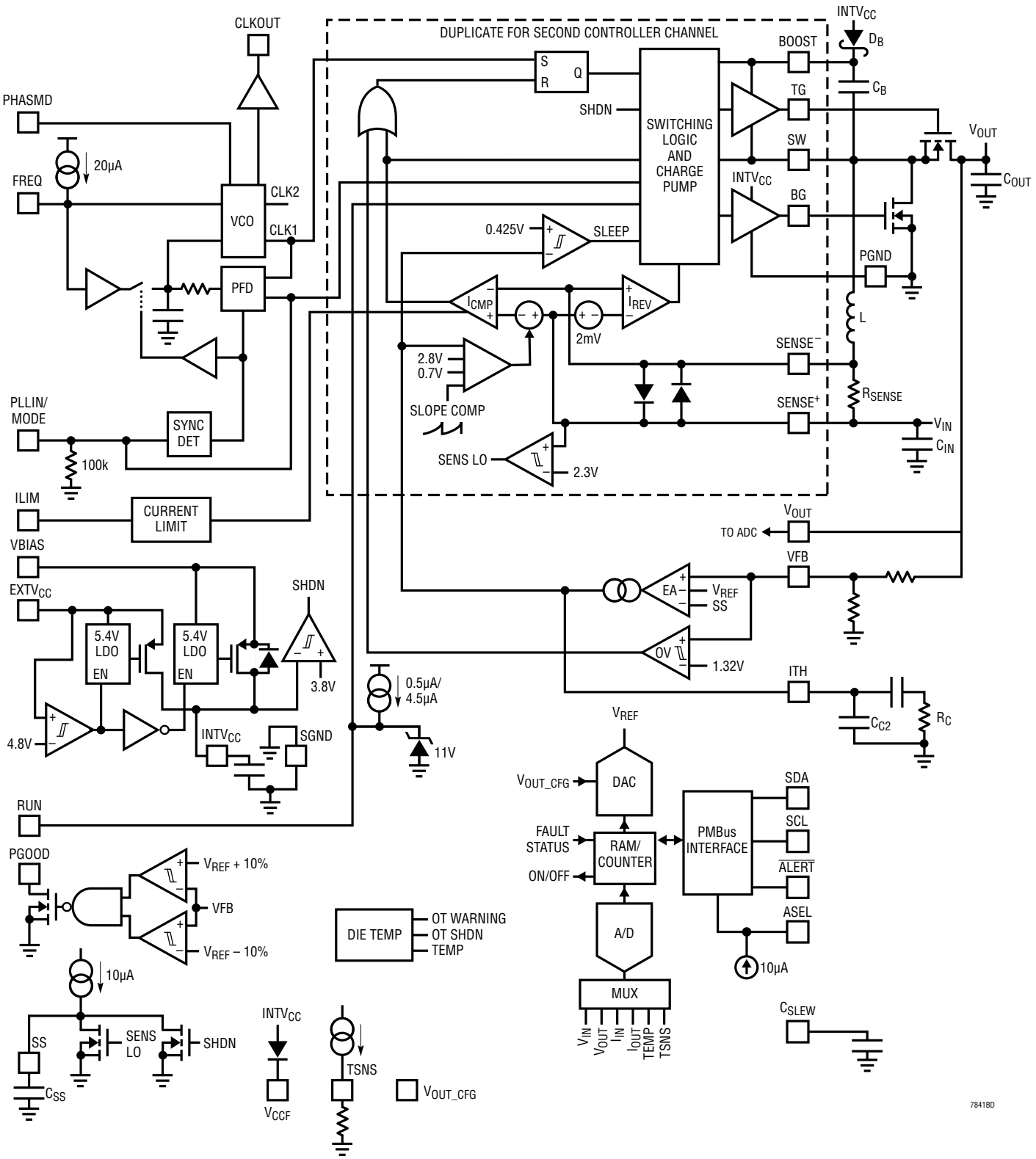
VFB (Pin 13): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider connected across the output.

V_{OUT_CFG} (Pin 32): Internal Reference Power-On Voltage. This pin function is disabled in the LTC7841.

TSNS (Pin 33): External Temperature Sensor Input. A NTC resistor from this pin to ground is used to monitor the external temperature. The temperature can be read via the PMBus.

V_{CCF} (Pin 36): Leave this pin unconnected or use 0.1µF capacitor for internal supply decoupling. For input or output voltages greater than 55V, connect a small signal Schottky diode from $INTV_{CC}$ to this pin to achieve best ADC readback accuracy.

BLOCK DIAGRAM



COMMAND TABLE

PMBus COMMAND CODE	COMMAND NAME	TYPE	SCALING	DATA BYTES	DESCRIPTION
0x01	OPERATION	R/W Byte		1	On/Off, Margin High/Low,Initialized to OFF at Start-Up
0x20	VOUT_MODE	Read Byte		1 or 2	Read Data Format for MFR_VOUT_COMMAND, Hard-Wired to 0x3F
0x79	STATUS_WORD	R/W Word		2	Read Fault Status (16-bit)
0x88	READ_VIN	R Word	10mV/Bit	2	Read Input Voltage Value
0x89	READ_IIN	R Word	50µV/ $R_{SENSE}(\Omega)$/Bit	2	Read Input Current Value(in Volts across R_{SENSE})
0x8B	READ_VOUT	R Word	10mV/Bit	2	Read Output Voltage Value
0x8C	READ_IOUT	R Word	50µV/ $R_{SENSE}(\Omega)$/Bit	2	Read Output Current Value (in Volts across R_{SENSE})
0x8D	READ_TEMPERATURE_1	R Word	Int: 1°C/Bit or Ext: 0.5mV/Bit	2	Read Temperature Value (MFR_CONFIG Sets Internal or External)
0x98	PMBUS_REVISION	Read Byte		1 or 2	Read PMBus Revision = 0x22 (Rev 2.2)
0xD7	MFR_IOUT_PEAK	R/W Word	50µV/ $R_{SENSE}(\Omega)$/Bit	2	Read Highest Output Current Value Since Last Reset
0xDD	MFR_VOUT_PEAK	R/W Word	10mV/Bit	2	Read Highest Output Voltage Value Since Last Reset
0xDE	MFR_VIN_PEAK	R/W Word	10mV/Bit	2	Read Highest Input Voltage Value Since Last Reset
0xDF	MFR_TEMPERATURE1_PEAK	R/W Word	1°C/Bit or 0.5mV/Bit	2	Read Highest Temperature Value Since Last Reset
0xE1	MFR_IIN_PEAK	R/W Word	50µV/ $R_{SENSE}(\Omega)$/Bit	2	Read Highest Input Current Value Since Last Reset
0xE3	MFR_CLEAR_PEAKS	W Byte		0, 1 or 2	Clear All Peak Values
0xE5	MFR_VOUT_MARGIN_HIGH	R/W Word	0.2%/Bit	2	V_{OUT} Margining Command
0xE7	MFR_SPECIAL_ID	Read Word		2	Read 16-bit GUI Value Unique to the LTC7841 (= 0x40D0)
0xE8	MFR_VOUT_COMMAND	R/W Word	0.2%/Bit	2	V_{OUT} Command (% of $V_{OUT,MAX}$), Set to 0% at Start-Up
0xE9	MFR_CONFIG	R/W Byte		1 or 2	Configuration Register: DAC Slew Rate/Step Control, Int/Ext Temperature Select
0xED	MFR_VOUT_MARGIN_LOW	R/W Word	0.2%/Bit	2	V_{OUT} Margining Command
0xFA	MFR_RAIL_ADDRESS	R/W Byte		1 or 2	Set Common PMBus Address, Defaults to Disabled
0xFD	MFR_RESET	W Byte		0, 1 or 2	Reset PMBus Interface to Power-On State

OPERATION

Main Control Loop

The LTC7841 uses a constant-frequency, current mode step-up architecture with the two controller channels operating out of phase. During normal operation, each external bottom MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the VFB pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground), to the internal reference voltage. In a boost converter, the required inductor current is determined by the load current, V_{IN} and V_{OUT}. When the load current increases, it causes a slight decrease in VFB relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current in each channel matches the new requirement based on the new load current.

After the bottom MOSFET is turned off each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator, IREV, or the beginning of the next clock cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is tied to a voltage less than 4.8V, the VBIAS LDO (low dropout linear regulator) supplies 5.4V from VBIAS to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.8V, the VBIAS LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies 5.4V from $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from an external source, thus removing the power dissipation of the VBIAS LDO.

Shutdown (RUN Pin)

The two internal controllers of the LTC7841 can be shut down using the RUN pin. Pulling this pin below 1.28V shuts down the main control loops for both phases and the serial interface. Pulling this pin below 0.7V disables both channels and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7841 draws only 8µA of quiescent current.

NOTE: Do not apply a heavy load for an extended time while the chip is in shutdown. The top MOSFETs are turned off during shutdown and the output load may cause excessive dissipation in the body diodes.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{IN}), as long as the maximum current into the RUN pin does not exceed 100µA. An external resistor divider connected to V_{IN} can set the threshold for converter operation. Once running, a 4.5µA current is sourced from the RUN pin allowing the user to program hysteresis using the resistor values.

Standby Mode

Standby mode is invoked by clearing the ON bit in the OPERATION command. Standby mode shuts down the main control loops for both phases like the RUN pin shutdown, however leaves the ADC and PMBus still active. In standby mode, the LTC7841 will still respond to the PMBus host but will only refresh the telemetry at a 1Hz rate instead of 25Hz. Exiting standby mode (setting ON bit back to 1) resets all faults and the ALERT pin. Data written to internal registers is not affected by standby mode.

Pulling RUN pin below 1.28V overrides the Standby mode and turns off the ADC and PMBus. When RUN returns above 1.28V, the ON bit is initialized to 0 and thus must be set to 1 to turn the control loop back on.

Table 1. Summary of Shutdown Modes

Input Conditions		ON/OFF States			
RUN Pin	**ON bit**	**V_{OUT}**	**PMBus**	**ADC**	**I_Q**
RUN < 0.7V	X	OFF	OFF	OFF	8µA
0.7V < RUN < 1.28V	X	OFF	OFF	OFF	350µA
RUN > 1.28V	0	OFF	ON	1Hz Refresh	1mA
RUN > 1.28V	1	ON	ON	25Hz Refresh	1mA to 2mA (Note 5)

OPERATION

Start-Up (SS Pin)

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal reference, the LTC7841 regulates the VFB voltage to the SS pin voltage instead of the reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to SGND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to the reference (and beyond up to $INTV_{CC}$), the output voltage rises smoothly to its final value.

Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction (PLLIN/MODE Pin)

The LTC7841 can be enabled to enter high efficiency Burst Mode operation, constant-frequency, pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground (e.g., SGND). To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the required current, the error amplifier EA will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode much of the internal circuitry is turned off and the LTC7841 draws only 800µA of quiescent current. In sleep mode the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IREV) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation.

In forced continuous operation or when clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC7841 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

OPERATION

The switching frequency of the LTC7841's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 10.

A phase-locked loop (PLL) is available on the LTC7841 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC7841's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of the first controller's external bottom MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of the second controller's external bottom MOSFET is 180 or 240 degrees out-of-phase to the rising edge of the external clock source. When synchronized, the LTC7841 will operate in forced continuous mode of operation.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of BG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC7841's PLL is from approximately 55kHz to 1MHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling). The recommended maximum amplitude for low level and minimum amplitude for high level of external clock are 0V and 2.5V, respectively.

PolyPhase Applications (CLKOUT and PHASMD Pins)

The LTC7841 features two pins, CLKOUT and PHASMD, that allow other controller ICs to be daisy-chained with the LTC7841 in PolyPhase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The PHASMD pin is used to adjust the phase of the CLKOUT signal as well as the relative phases between the two internal controllers, as summarized in Table 2. The phases are calculated relative to the zero degrees phase being defined as the rising edge of the bottom gate driver output of controller 1 (BG1). Depending on the phase selection, a PolyPhase application with multiple LTC7841s can be configured for 2-, 3-, 4- , 6- and 12-phase operation.

Table 2.

V_{PHASMD}	CONTROLLER 2 PHASE (°)	CLKOUT PHASE (°)
GND	180	60
Floating	180	90
$INTV_{CC}$	240	120

CLKOUT is disabled when the controller is in shutdown or in sleep mode.

Operation When V_{IN} > Regulated V_{OUT}

When V_{IN} rises above the regulated V_{OUT} voltage, the boost controller can behave differently depending on the mode, inductor current and V_{IN} voltage. In forced continuous mode, the control loop works to keep the top MOSFET on continuously once V_{IN} rises above V_{OUT}. The internal charge pump delivers current to the boost capacitor to maintain a sufficiently high TG voltage. The amount of current the charge pump can deliver is characterized by two curves in the Typical Performance Characteristics section.

OPERATION

In pulse-skipping mode, if V_{IN} is between 100% and 110% of the regulated V_{OUT} voltage, TG turns on if the inductor current rises above a certain threshold and turns off if the inductor current falls below this threshold. This threshold current is set to approximately 6%, 4% or 3% of the maximum ILIM current when the ILIM pin is grounded, floating or tied to $INTV_{CC}$, respectively. If the controller is programmed to Burst Mode operation under this same V_{IN} window, then TG remains off regardless of the inductor current.

If V_{IN} rises above 110% of the regulated V_{OUT} voltage in any mode, the controller turns on TG regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the chip is asleep. With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. To prevent excessive power dissipation across the body diode of the top MOSFET in this situation, the chip can be switched over to forced continuous mode to enable the charge pump; a Schottky diode can also be placed in parallel with the top MOSFET.

Power Good

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shut down). When the VFB pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (abs max).

Overvoltage Protection

An overvoltage event is defined as when the output feedback voltage (V_{FB}) is greater than 110% of its normal regulated point set by the DAC. During an overvoltage event, TG1/TG2 are turned on continuously until the overvoltage condition is cleared, regardless of whether Burst Mode operation, pulse-skipping mode, or forced continuous mode is selected by the PLLIN/MODE pin. This can cause large negative inductor currents to flow from the output to the input if the output voltage is higher than the input voltage.

Note however that in Burst Mode operation, the LTC7841 is in sleep during an overvoltage condition, which disables the internal oscillator and BOOST-SW charge pump. So the BOOST-SW voltage may discharge (due to leakage) if the overvoltage conditions persists indefinitely. If BOOST-SW discharges, then by definition TG would turn off.

BOOST Supply Refresh and Internal Charge Pump

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There are two considerations for keeping the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 200µs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough BOOST-SW voltage to allow the top MOSFET ready to be fully enhanced instead of waiting for the initial few cycles to charge up. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 55µA.

OPERATION

Internal Reference DAC

The LTC7841 has an internal 9-bit DAC that allows the internal reference voltage to be set to any value in the range of 0 to 2.4V with 0.2%/bit resolution. The digital value is changed with the MFR_VOUT_COMMAND command through the PMBus interface. When a change in the reference is detected, the reference is ramped (0.2%/step) from its current value to the new value at a rate set by the capacitor value connected to the C_{SLEW} pin. The slew rate can also be changed by the PMBus interface using the MFR_CONFIG command. Using this command, the slew rate can be set to one of three relative values: nominal (1x), fast (2x) and slow (0.125x). The LTC7841 can be pre-loaded with two additional reference values with the MFR_VOUT_MARGIN_HIGH and MFR_VOUT_MARGIN_LOW commands. Once loaded, the reference can then be switched between any of these three register values by setting the appropriate margin bit in the OPERATION register.

Whenever a power cycle, RUN pin turn-on, or MFR_RESET event occurs, the MFR_VOUT_COMMAND register will be re-initialized to zero. Margin high/low registers are also initialized to zero at this time.

During V_{OUT} changes, PLLIN/MODE pin setting is ignored and forced continuous mode is used to guarantee that V_{OUT} is changed at the programmed slew rate regardless of the load.

Telemetry Readback

The LTC7841 has an integrated 13-bit ADC that monitors and performs conversions on the input and output voltage, input and output current, and either die temperature or remote sense temperature. The values are refreshed at a 25Hz rate and are readable through the PMBus interface. A peak monitor is also available for each of these telemetry measurements to provide that highest value measured since the start of the monitor. The monitor is reset by the MFR_CLEAR_PEAKS command, writing to the individual peak register, or cycling the RUN pin.

Temperature Monitor and Thermal Warning/Shutdown

The LTC7841 has two internal die temperature monitors — one that is digitized by the ADC and reported with the READ_TEMPERATURE_1 command and a second that is used to shut down the LTC7841 IC when the die temperature exceeds 170°C. A third temperature monitor is also available for external temperature sensing by connecting an external temperature sense element to the TSNS pin. This is useful for monitoring temperature close to the power inductor or power MOSFETs where temperature is typically highest. The LTC7841 reports either internal die temperature or external temperature sense voltage with the READ_TEMPERATURE_1 command. The MFR_CONFIG register is used to set which one is active. When internal die temperature is selected and the internal die temperature exceeds 150°C, the overtemperature warning bit in the STATUS_WORD is set and the $\overline{\text{ALERT}}$ pin pulls low to alert the PMBus master. This overtemperature warning bit is latched and remains set until the host clears it. Both internal die temperature monitors have about 20°C of hysteresis before the overtemperature condition is cleared.

SERIAL INTERFACE

The LTC7841 serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using an external resistor. In addition the LTC7841 always responds to the global broadcast address of 0x5A or 0x5B (7 bit). The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte and 6) read word. The PMBus write operations are not acted upon until a complete valid message is received by the LTC7841 including the STOP bit.

Communication Failure

Attempts to access unsupported commands or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_WORD command and the $\overline{\text{ALERT}}$ pin is pulled low.

OPERATION

Device Addressing

The LTC7841 offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTC7841 devices on the bus. The LTC7841 global address is fixed 0x5A or 0x5B (7 bit) or 0xB4 or 0xB6 (8 bit) and cannot be disabled.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTC7841. The value of the device address is set by the ASEL configuration pin. Rail addressing provides a means of the PMBus master addressing a set of channels connected to the same output rail, simultaneously. This is similar to global addressing, however, the PMBus address can be dynamically assigned by using the MFR_RAIL_ADDRESS command. It is recommended that rail addressing should be limited to command write operations.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts.

Fault Status

The STATUS_WORD and $\overline{\text{ALERT}}$ pin provide fault status information of the LTC7841 to the host.

Bus Timeout Failure

The LTC7841 implements a timeout feature to avoid hanging the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 25ms or the LTC7841 will tri-state the bus and ignore the given data packet. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), and all data bytes.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTC7841 supports the full PMBus frequency range from 10kHz to 400kHz.

Similarity Between PMBus, SMBus and I^2C 2-Wire Interface

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I^2C byte commands because PMBus/SMBus provide time-outs to prevent bus hangs and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I^2C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I^2C controllers but is required for SMBus/PMBus reads. If a general purpose I^2C controller is used, check that repeat start is supported.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Paragraph 5: Transport.

For a description of the differences between SMBus and I^2C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I^2C.

PMBus Serial Interface

The LTC7841 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 1, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC7841 is a slave device. The master can communicate with the LTC7841 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word
- Alert Response Address

OPERATION

Figures 3 through 6 illustrate the aforementioned PMBus protocols. All transactions support GCP (group command protocol).

Figure 2 is a key to the protocol diagrams in this section.

A value shown below a field in the following figures is a mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

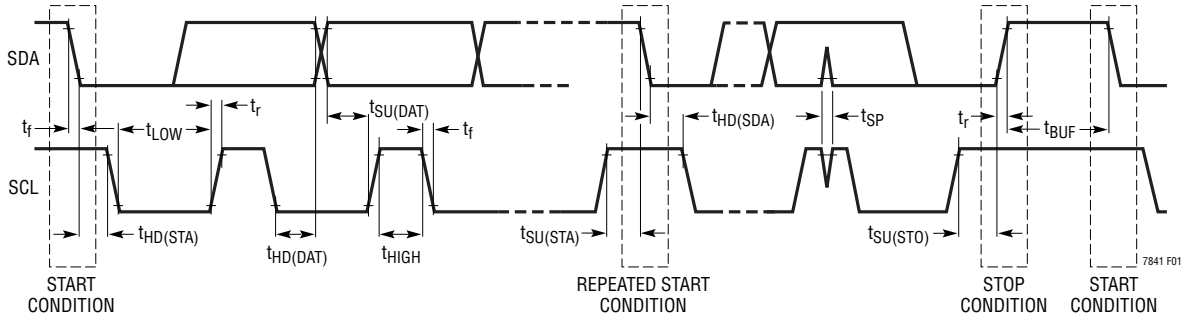


Figure 1. Timing Diagram

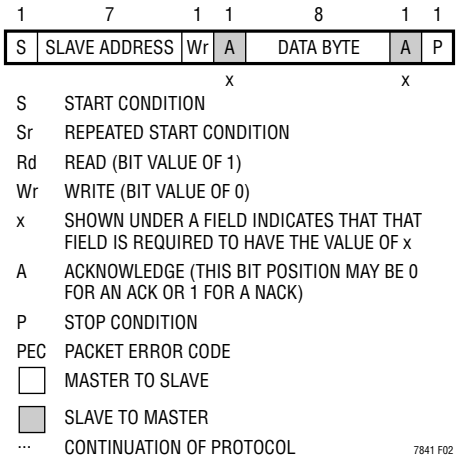


Figure 2. PMBus Packet Protocol Diagram Element Key

OPERATION

Examples of these formats are shown in Figures 3 through 7.

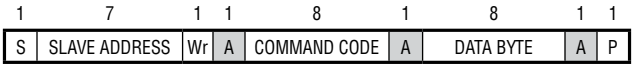


Figure 3. Write Byte Protocol

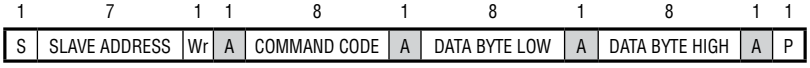


Figure 4. Write Word Protocol

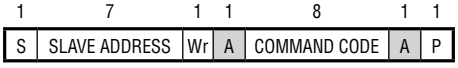


Figure 5. Send Byte Protocol

Figure 6. Read Word Protocol

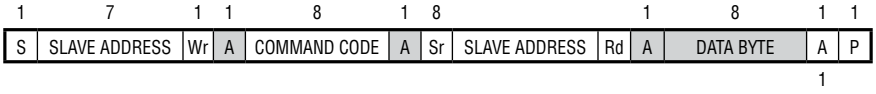


Figure 7. Read Byte Protocol

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7841 application circuit. The LTC7841 can be configured to use either inductor DCR (DC resistance) sensing or a discrete sense resistor (R_{SENSE}) for current sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power-efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits and current readback(ADC) for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected. Note that the two controller channels of the LTC7841 should be designed with the same components.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The current sense resistor is normally placed at the input of the boost controller in series with the inductor.

The SENSE+ pin also provides power to the current comparator. It draws ~200µA during normal operation. There is a small base current of less than 1µA that flows into the SENSE– pin. The high impedance SENSE– input to the current comparators allows accurate DCR sensing.

Filter components mutual to the sense lines should be placed close to the LTC7841, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 8). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 9b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

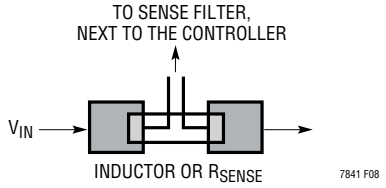
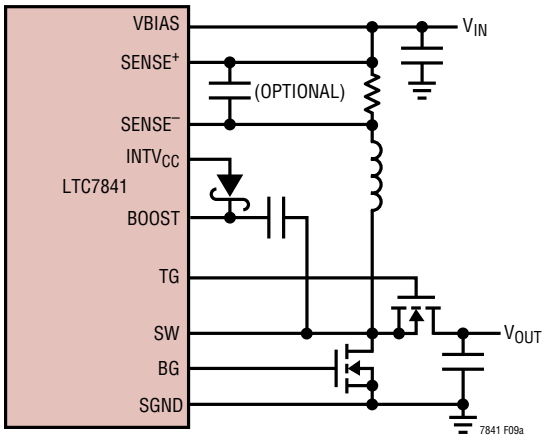
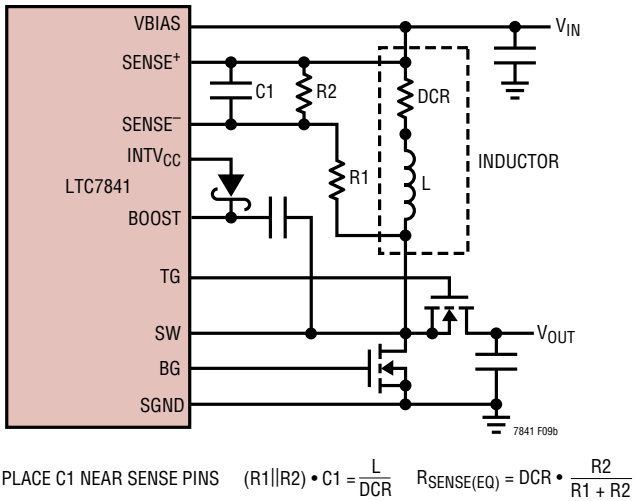


Figure 8. Sense Lines Placement with Inductor or Sense Resistor



(a) Using a Resistor to Sense Current



(b) Using the Inductor DCR to Sense Current

Figure 9. Two Different Methods of Sensing Current

APPLICATIONS INFORMATION

Sense Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 9a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$. When the ILIM pin is grounded, floating or tied to $INTV_{CC}$, the maximum threshold is set to 50mV, 75mV or 100mV, respectively. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

The actual value of I_{MAX} for each channel depends on the required output current $I_{OUT(MAX)}$ and can be calculated using:

$$I_{MAX} = \left(\frac{I_{OUT(MAX)}}{2}\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right)$$

When using the controller in low V_{IN} and very high voltage output applications, the maximum inductor current and correspondingly the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for boost regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current level depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7841 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 9b. The DCR of the inductor can be less than 1mΩ for high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor could reduce the efficiency by a few percent compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the maximum current sense threshold ($V_{SENSE(MAX)}$).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the $SENSE^-$ pin's ±1µA current.

The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

APPLICATIONS INFORMATION

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C)\bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1\bullet R_D}{1-R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at V_{IN} = 1/2V_{OUT}:

$$P_{LOSS\_R1} = \frac{(V_{OUT} - V_{IN})\bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{V_{IN}}{f\bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is ΔI_L = 0.3(I_{MAX}). The maximum ΔI_L occurs at V_{IN} = 1/2V_{OUT}.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease. Once the value of L is known, an inductor with low DCR and low core losses should be selected.

Power MOSFET Selection

Two external power MOSFETs must be selected for each controller in the LTC7841: one N-channel MOSFET for the bottom (main) switch, and one N-channel MOSFET for the top (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.4V during start-up (see $EXTV_{CC}$ pin connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturer's data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in VDS. This result is then multiplied by the ratio of the application applied

APPLICATIONS INFORMATION

VDS to the gate charge curve specified VDS. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

If the maximum output current is $I_{OUT(MAX)}$ and each channel takes one half of the total output current, the MOSFET power dissipations in each channel at maximum output current are given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V^2_{IN}} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)} + k \bullet V_{OUT}{}^3 \bullet \frac{I_{OUT(MAX)}}{2 \bullet V_{IN}} \bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ (approximately 1Ω). The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

Both MOSFETs have I^2R losses while the bottom N-channel equation includes an additional term for transition losses, which are highest at low input voltages. For high V_{IN} the high current efficiency generally improves with larger MOSFETs, while for low V_{IN} the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the bottom switch duty factor is low or during overvoltage when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

C_{IN} and C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple voltage due to charging and discharging the bulk capacitance in a single phase boost converter is given by:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

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The LTC7841 is configured as a 2-phase single output converter where the outputs of the two channels are connected together and both channels have the same duty cycle. With 2-phase operation, the two channels are operated 180 degrees out-of-phase. This effectively interleaves the output capacitor current pulses, greatly reducing the output capacitor ripple current. As a result, the ESR requirement of the capacitor can be relaxed. Because the ripple current in the output capacitor is a square wave, the ripple current requirements for the output capacitor depend on the duty cycle, the number of phases and the maximum output current. Figure 10 illustrates the normalized output capacitor ripple current as a function of duty cycle in a 2-phase configuration. To choose a ripple current rating for the output capacitor, first establish the duty cycle range based on the output voltage and range of input voltage. Referring to Figure 10, choose the worst-case high normalized ripple current as a percentage of the maximum load current.

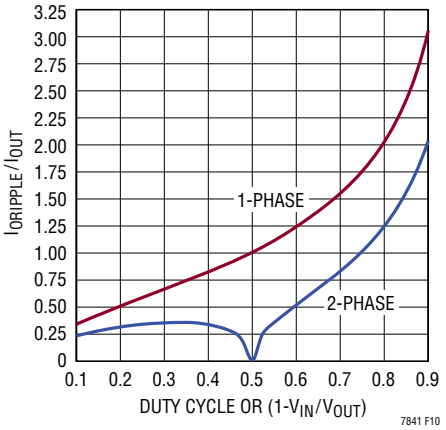

Figure 10. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings (e.g., OS-CON and POSCAP).

PolyPhase Operation

For output loads that demand high current, multiple LTC7841s can be cascaded to run out-of-phase to provide more output current and at the same time to reduce input and output voltage ripple. The PLLIN/MODE pin allows the LTC7841 to synchronize to the CLKOUT signal of another LTC7841. The CLKOUT signal can be connected to the PLLIN/MODE pin of the following LTC7841 stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to $INTV_{CC}$, SGND or floating generates a phase difference (between PLLIN/MODE and CLKOUT) of 240°, 60° or 90°, respectively, and a phase difference (between CH1 and CH2) of 120°, 180° or 180°. Figure 11 shows the connections necessary for 3-, 4-, 6- or 12-phase operation. A total of 12 phases can be cascaded to run simultaneously out-of-phase with respect to each other.

When making output voltage changes in poly-phase applications with multiple LTC7841's controlling the same output, it is important to synchronize the change between all LTC7841's. This can be done in 2 ways: (1) set a common address for all LTC7841's using the MFR_RAIL_ADDRESS command, then write the new output voltage value to this rail address so that all LTC7841's receive the new value simultaneously, or (2) use the Group Command Protocol (GCP). GCP ensures that all slaves receiving the output change command will start the change at the same time (when the STOP bit is detected).

Setting Output Voltage

The LTC7841 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 12. The regulated output voltage is determined by:

$$V_{OUT} = V_{REF}\left(1+\frac{R_B}{R_A}\right)$$

where V_{REF} is the 0 to 2.4V reference voltage set by the DAC.

Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also place the feedback resistor divider close to the VFB pin and keep the VFB node as small as possible to avoid noise pickup.

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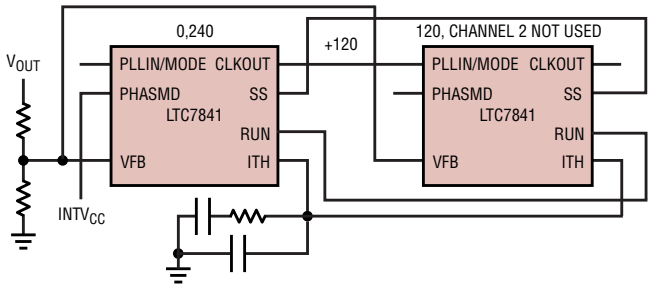
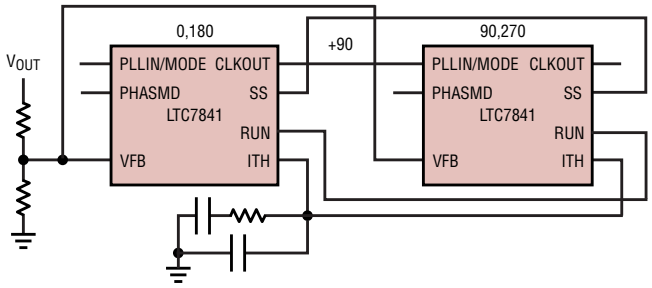
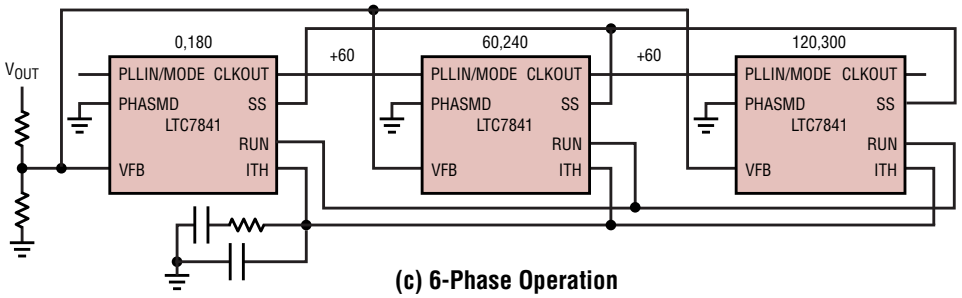


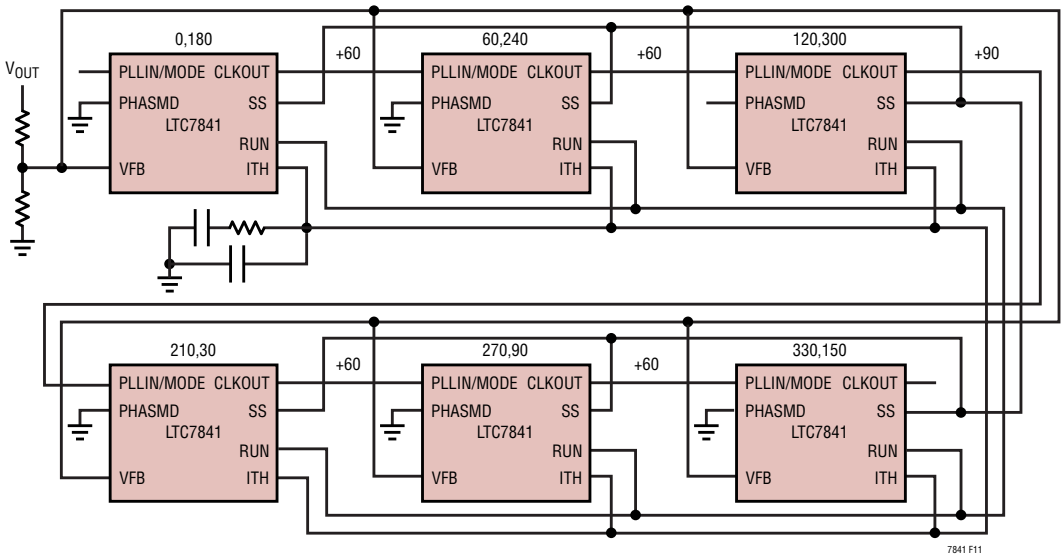
(a) 3-Phase Operation



(b) 4-Phase Operation



(c) 6-Phase Operation



(d) 12-Phase Operation

Figure 11. PolyPhase Operation

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Soft-Start (SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal reference, the LTC7841 regulates the VFB pin voltage to the voltage on the SS pin instead of V_{REF}.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 13. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC7841 will regulate the VFB pin (and hence, V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from V_{IN} to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{V_{REF}}{10\mu A}$$

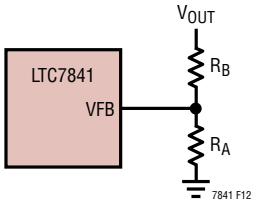

Figure 12. Setting Output Voltage

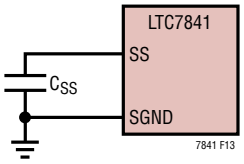

Figure 13. Using the SS Pin to Program Soft-Start

$INTV_{CC}$ Regulators

The LTC7841 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the VBIAS supply pin or the $EXTV_{CC}$ pin depending on the connection of the $EXTV_{CC}$ pin. $INTV_{CC}$ powers the gate drivers and much of the LTC7841's internal circuitry. The VBIAS LDO and the $EXTV_{CC}$ LDO regulate $INTV_{CC}$ to 5.4V. Each of these can supply at least 40mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7841 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the VBIAS LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.8V, the VBIAS LDO is enabled. In this case, power dissipation for the IC is highest and is equal to VBIAS • I_{INTVCC}. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, at 70°C ambient temperature, the LTC7841 $INTV_{CC}$ current is limited to less than 21mA in the QFN package from a 60V VBIAS supply when not using the $EXTV_{CC}$ supply:

T_J = 70°C + (21mA)(60V)(43°C/W) = 125°C

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.8V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.55V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 5.4V, so while $EXTV_{CC}$ is less than 5.4V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.4V, up to an absolute maximum of 14V, $INTV_{CC}$ is regulated to 5.4V.

Significant thermal gains can be realized by powering $INTV_{CC}$ from an external supply. Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to 77°C in a QFN package:

T_J = 70°C + (32mA)(5V)(43°C/W) = 77°C

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The following list summarizes possible connections for $EXTV_{CC}$:

$EXTV_{CC}$ Grounded. This will cause $INTV_{CC}$ to be powered from the internal 5.4V regulator resulting in an efficiency penalty at high input voltages.

$EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 14V range, it may be used to provide power. Ensure that $EXTV_{CC}$ is always lower than or equal to VBIAS.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Block Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate and source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{OUT} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the output voltage: $V_{BOOST} = V_{OUT} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{OUT(MAX)}$.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. Pay close attention to the reverse leakage at high temperatures, where it generally increases substantially.

Each of the topside MOSFET drivers includes an internal charge pump that delivers current to the bootstrap capacitor from the BOOST pin. This charge current maintains the bias voltage required to keep the top MOSFET on continuously during dropout/overvoltage conditions. The Schottky/silicon diodes selected for the topside drivers should have a reverse leakage less than the available output current the charge pump can supply. Curves displaying the available charge pump current under different operating conditions can be found in the Typical Performance Characteristics section.

A leaky diode D_B in the boost converter can not only prevent the top MOSFET from fully turning on but it can also completely discharge the bootstrap capacitor C_B and create a current path from the input voltage to the BOOST pin to $INTV_{CC}$. This can cause $INTV_{CC}$ to rise if the diode leakage exceeds the current consumption on $INTV_{CC}$. This is particularly a concern in Burst Mode operation where the load on $INTV_{CC}$ can be very small. The external Schottky or silicon diode should be carefully chosen such that $INTV_{CC}$ never gets charged up much higher than its normal regulation voltage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on-chip (such as an $INTV_{CC}$ short to ground), the overtemperature shutdown circuitry will shut down the LTC7841. When the junction temperature exceeds approximately 170°C, the overtemperature circuitry disables the $INTV_{CC}$ LDO, causing the $INTV_{CC}$ supply to collapse and effectively shut down the entire LTC7841 chip including the PMBus interface. Once the junction temperature drops back to approximately 155°C, the $INTV_{CC}$ LDO turns back on. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Since the shutdown may occur at full load, beware that the load current will result in high power dissipation in the body diodes of the top MOSFETs. In this case, the PGOOD output may be used to turn the system load off.

The READ_TEMPERATURE_1 command and overtemperature warning status bit can be used to take preventative action before the temperature gets high enough to shut down the IC.

Phase-Locked Loop and Frequency Synchronization

The LTC7841 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter and a voltage-controlled oscillator (VCO). This allows the

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turn-on of the bottom MOSFET of channel 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The turn-on of channel 2's bottom MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge-sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, C_{LP}, holds the voltage at the VCO input.

Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.2V.

Note that the LTC7841 can only be synchronized to an external clock whose frequency is within range of the LTC7841's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

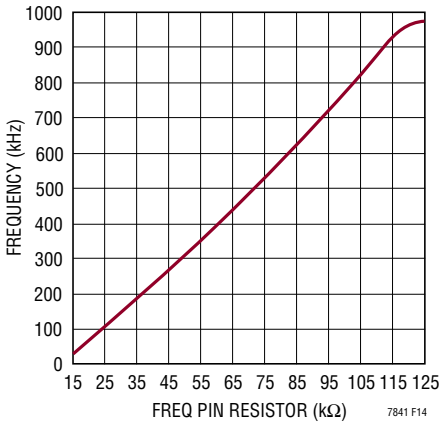

Figure 14. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Table 3 summarizes the different states in which the FREQ pin can be used.

Table 3.

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock	Phase Locked to External Clock

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7841 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the bottom MOSFET. Low duty cycle applications may approach this minimum on-time limit.

In forced continuous mode, if the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles but the output will continue to be regulated. More cycles will be skipped when V_{IN} increases. Once V_{IN} rises above V_{OUT}, the loop keeps the top MOSFET continuously on. The minimum on-time for the LTC7841 is approximately 110ns.

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the greatest improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC7841 circuits: 1) IC VBIAS current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) bottom MOSFET transition losses, 5) body diode conduction losses.

1. The VBIAS current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. VBIAS current typically results in a small (<0.1%) loss.
2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.
3. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
4. Transition losses apply only to the bottom MOSFET(s), and become significant only when operating at low input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\frac{V_{OUT}^3}{V_{IN}} \bullet \frac{I_{OUT(MAX)}}{2} \bullet C_{RSS} \bullet f$$

5. Body diode conduction losses are more significant at higher switching frequency. During the dead time, the loss in the top MOSFETs is $I_{OUT} \bullet V_{DS}$, where V_{DS} is around 0.7V. At higher switching frequency, the dead time becomes a good percentage of switching cycle and causes the efficiency to drop.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Figure 21 circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is complete and the particular output capacitor type and value have been determined. The output capacitors must be selected because the various types and values

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determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If RC is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Address Selection (ASEL pin)

The LTC7841 slave address is selected by the ASEL pin. The upper four bits of the address are hardwired internally to 0100 and the lower three bits are programmed by one or two resistors connected between the ASEL and SGND pins and the ASEL and $INTV_{CC}$ pins (see Table 4). This allows up to 8 different LTC7841's on a single board. The LTC7841 will also respond to the Global Address 0x5A and the 7-bit address stored in the MFR_RAIL_ADDRESS register.

The ASEL pin is sampled only at power on and at initialization after the rising edge of the RUN pin or OPERATION register ON bit. Changes to ASEL will not take affect until one of these events occur.

Table 4. ASEL Resistor Selection

ASEL-to-SGND Resistor	ASEL-to-$INTV_{CC}$ Resistor	SLAVE ADDRESS
0Ω	open	0100000
38.3kΩ	open	0100001
63.4kΩ	open	0100010
88.7Ω	open	0100011
49.9kΩ	324kΩ	0100100
49.9kΩ	215kΩ	0100101
17.8kΩ	44.2kΩ	0100110
Open	open	0100111

Margining/C_{SLEW} Selection/Margin Pin

Writing to the MFR_VOUT_COMMAND register via the PMBus allows the adjustment of the V_{OUT} reference from 0% to 100% of the maximum reference of 2.4V. This voltage can be adjusted in 0.2% increments by writing the appropriate 9-bit value to the register. The MFR_VOUT_MARGIN_HIGH and MFR_VOUT_MARGIN_LOW register can also be used to adjust the V_{OUT} reference value by selecting the desired register with the OPERATION command as specified in Table 5.

Table 5. V_{OUT} Margining with the OPERATION Command

OPERATION BITS [5:4]		
BIT 5	BIT 4	V_{OUT} REFERENCE
0	0	= MFR_VOUT_COMMAND(%) • 2.4V
0	1	= MFR_VOUT_MARGIN_LOW(%) • 2.4V
1	0	= MFR_VOUT_MARGIN_HIGH(%) • 2.4V
1*	1*	= MFR_VOUT_COMMAND(%) • 2.4V

* Setting both bits 4 and 5 high at the same time is illegal and will be ignored.

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The C_{SLEW} pin provides slew rate limiting during reference voltage changes. When the reference is changed by the OPERATION command or writing new values to the register, the LTC7841 counts up or down from the current value in the register to the new value at 0.2% per step. The step duration is set by the C_{SLEW} capacitor and the slew rate multiplier M (set in MFR_CONFIG). The slew rate during the transition is thus:

$$SR = \frac{0.1 \bullet M}{C_{SLEW}(nF) + 0.0043} \%/ms$$

where M can be 1 (nominal), 2 (fast) or 0.125 (slow).

If the C_{SLEW} pin is left open, SR defaults to 23%/ms. The slew rate limit can be disabled if desired by tying the C_{SLEW} pin to V_{CCF}. When disabled, the reference is immediately stepped from old value to new value in <100ns.

CONNECTING THE USB TO I²C/SMBus/PMBus CONTROLLER TO THE LTC7841 IN SYSTEM

The ADI USB to I²C/SMBus/PMBus controller can be interfaced to the LTC7841 on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system.

Figure 15 illustrates the application schematic for powering, programming and communication with one or more LTC7841s via the ADI I²C/SMBus/PMBus controller.

Any device sharing the I²C bus connections with the LTC7841 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power.

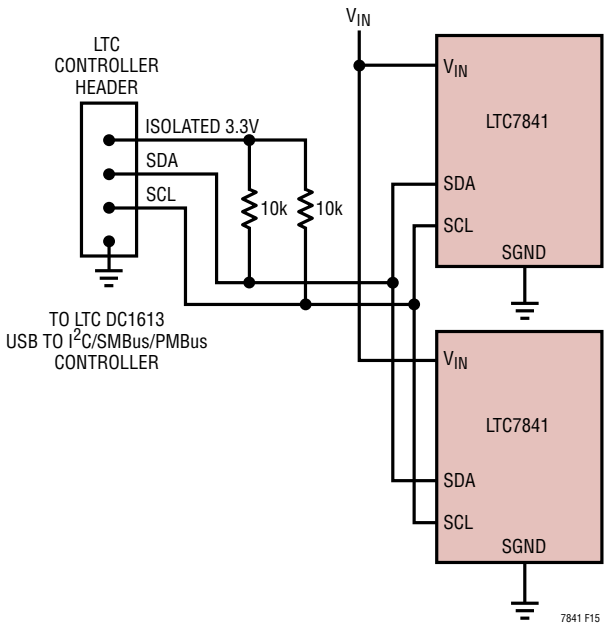

Figure 15. LTC Controller Connection

LTPOWERPLAY: AN INTERACTIVE GUI FOR DIGITAL POWER

LTpowerPlay is a powerful Windows-based development environment that supports Analog Devices power system management ICs and other digital ICs like the LTC7841. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Analog Devices ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build multiple IC configuration files that can be saved and reloaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bring up rails. LTpowerPlay utilizes Analog Devices' USB-to-I²C/SMBus/PMBus controller to communication with one of the many potential targets including the DC1590B-A/DC1590B-B demo board, the DC1709A socketed programming board, or a customer target system. The software also provides an automatic

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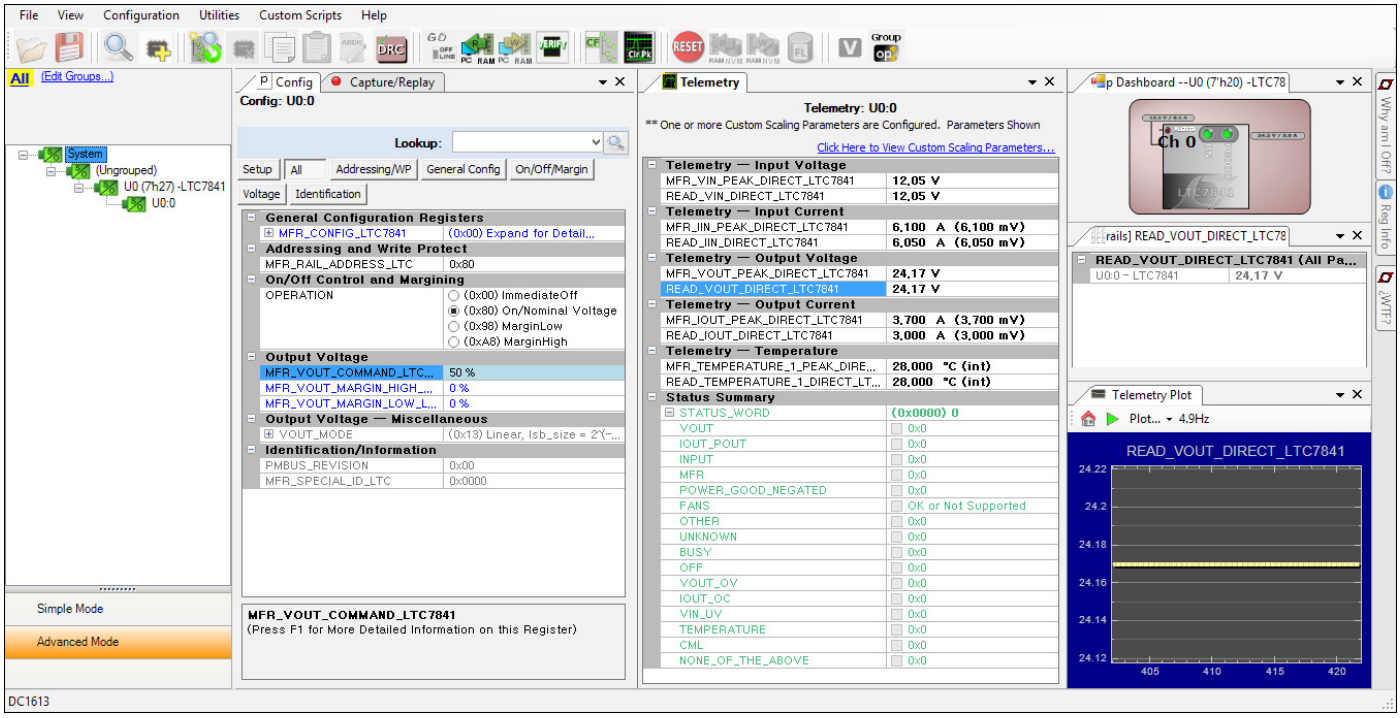

update feature to keep the revisions current with the latest set of device drivers and documentation. A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos. Complete information is available at LTpowerPlay.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (max), V_{OUT} = 24V, $I_{OUT(MAX)}$ = 8A, $V_{SENSE(MAX)}$ = 75mV, and f = 350kHz.

The components are designed based on single channel operation. The inductance value is chosen first based on a 30% ripple current assumption. Tie the PLLIN/MODE pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1-\frac{V_{IN}}{V_{OUT}}\right)$$

The largest ripple happens when $V_{IN} = 1/2V_{OUT} = 12V$, where the average maximum inductor current for each channel is:

$$I_{MAX} = \left(\frac{I_{OUT(MAX)}}{2}\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) = 8A$$

A 6.8µH inductor will produce a 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 9.25A.

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \leq \frac{75mV}{9.25A} = 0.008\Omega$$

Choose feedback resistors to regulate V_{OUT} at 24V for the 50% setting of MFR_VOUT_COMMAND (V_{REF} = 1.2V). For 1% resistors and V_{REF} = 1.2V, R_A = 5k and R_B = 95.3k. This yields an output voltage of 24.072V.

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The power dissipation on the top side MOSFET in each channel can be easily estimated. Choosing a Vishay Si7848BDP MOSFET results in: $R_{DS(ON)}$ = 0.012Ω, C_{MILLER} = 150pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{(24V-12V)\,24V}{(12V)^2}\bullet(4A)^2 \bullet\left[1+(0.005)(50°C-25°C)\right]\bullet 0.008\Omega + (1.7)(24V)^3\,\frac{4A}{12V}(150pF)(350kHz) = 0.7W$$

C_{OUT} is chosen to filter the square current in the output. The maximum output current peak is:

$$I_{OUT(PEAK)} = 8\bullet\left(1+\frac{31\%}{2}\right) = 9.3A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 46.5mV (assuming ESR dominates the ripple).

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 17. Figure 18 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Put the bottom N-channel MOSFETs MBOT1 and MBOT2 and the top N-channel MOSFETs MTOP1 and MTOP2 in one compact area with C_{OUT}.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the bottom N-channel MOSFET and the capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the source terminals of the bottom MOSFETs.
3. Does the LTC7841 VFB pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground and placed close to the VFB pin. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2) and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and, therefore, should be kept on the output side of the LTC7841 and occupy a minimal PC trace area.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

APPLICATIONS INFORMATION

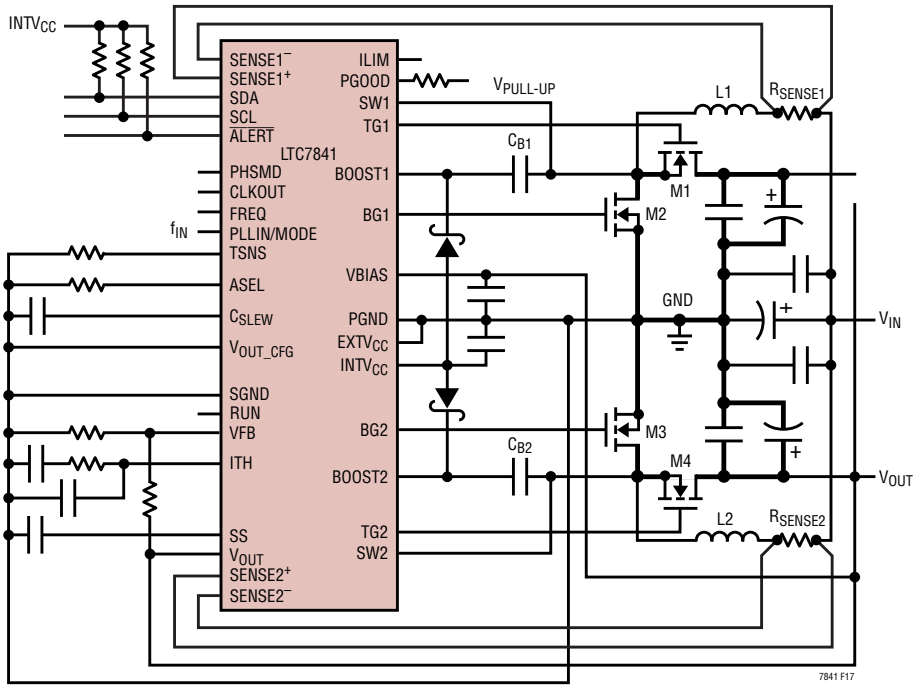


Figure 17. Recommended Printed Circuit Layout Diagram

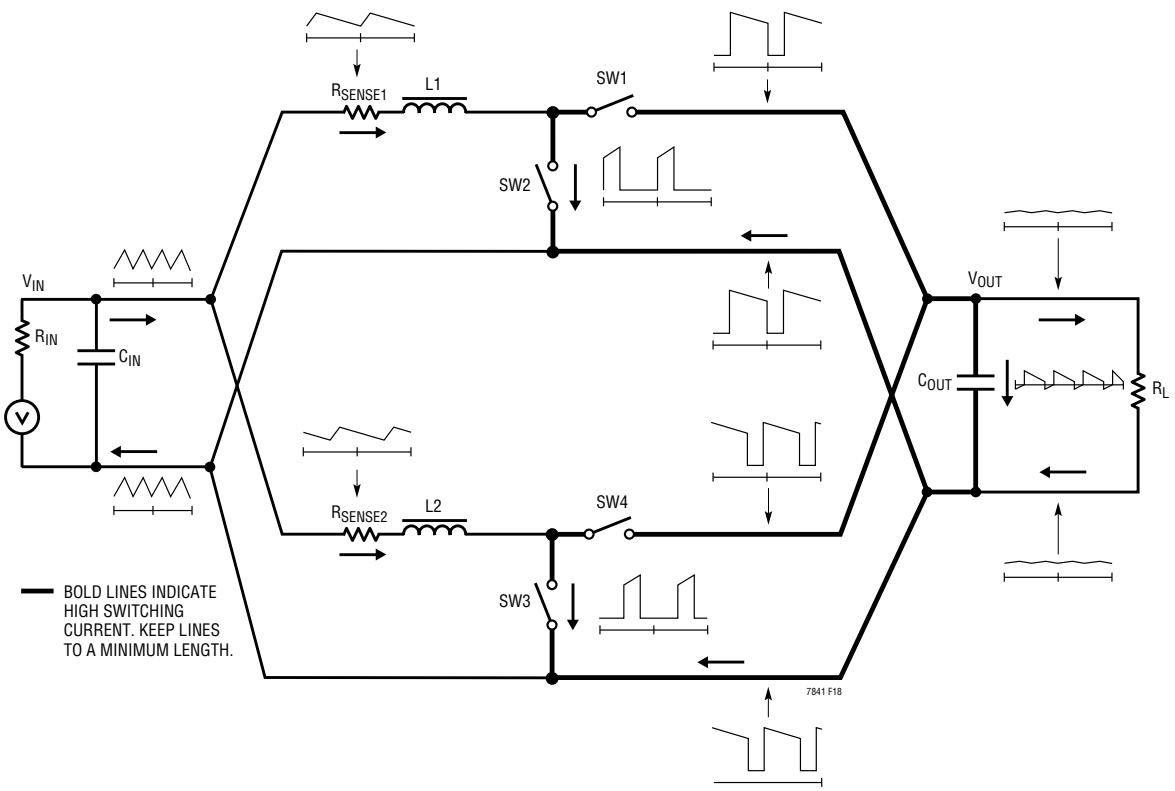


Figure 18. Branch Current Waveforms

APPLICATIONS INFORMATION

Special Layout Consideration

1. Exceeding ABS Max ratings on the sense pins can result in damage to the controller. As the Sense$^-$ pins are connected directly to V_{LOW}, it is recommended that a fast acting diode with an appropriately high voltage rating be used to clamp these pins to reduce voltage spiking below ground. The diodes should be placed close to the controller IC, with the cathode connected to SENSE1$^-$ or SENSE2$^-$ and the anode connected to ground.
2. The TG traces from the controller IC to the gate of the external MOSFET should be kept as short as possible to minimize the parasitic inductance. This inductance can cause voltage spikes that can potentially exceed the ABS Max rating of the drivers and damage them. A 3Ω resistor and 1nF capacitor can be used to filter these spikes as shown in Figure 19. If the TG traces are longer than 25mm, this filter network must be used on both TG1 and TG2. The 1nF capacitor should be placed as close to the TG/SW pins as possible.

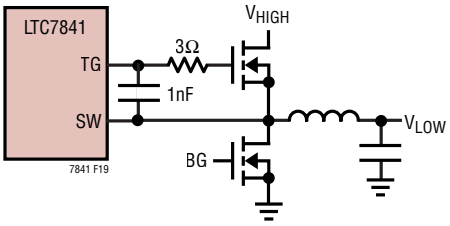


Figure 19. Filter for TG Traces > 25mm

PC Board Layout Debugging

Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point while the other channel is turning on its bottom MOSFET. This occurs around the 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation with high duty cycle. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling.

An embarrassing problem which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hook-up will still be maintained, but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

PMBus COMMAND DETAILS

MFR_RESET

This command provides a means by which the user can perform a reset of the LTC7841. All latched faults ($\overline{\text{ALERT}}$ and status register) and register (telemetry, margin, config etc) contents will be reset to a power-on condition by this command. ASEL config resistor is re-measured.

Since the power-on condition for OPERATION ON bit and MFR_VOUT_COMMAND are zero, V_{OUT} will be turned off by MFR_RESET and require writing to these registers again to turn V_{OUT} back on.

This write-only command accepts zero, one, or two data bytes but ignores them.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command allows all devices to share a common address, such as all devices attached to a single power supply rail. The desired 7-bit address value is written to the 7 bits of the data byte.

The MSB (bit B7) must be set low to enable communication using the MFR_RAIL_ADDRESS address. Setting this bit disables this address. The default setting of this register is disabled.

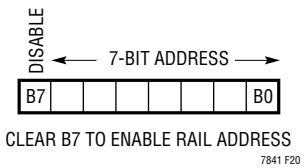


Figure 20. MFR_RAIL_ADDRESS Data Byte

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTC7841 will detect bus contention and set a CML communications fault.

This command accepts one or two data bytes but the second is ignored.

OPERATION

The OPERATION command is used to turn the unit on/off and for margining the output voltage.

Clearing the ON bit turns off the output voltage with PMBus interface still active and telemetry data refreshed at a slower 1Hz rate to minimize supply current. The ON bit is automatically reset to OFF after a master shutdown (RUN pin < 1.28V), power cycle, or MFR_RESET command.

The MARGIN_HIGH/LOW bits command the V_{OUT} reference to the value stored in either the MFR_VOUT_MARGIN_HIGH or MFR_VOUT_MARGIN_LOW, resp. at the slew rate set by the C_{SLEW} capacitor. Cycling the ON bit has no affect on the margin registers and thus when re-asserting ON, V_{OUT} will return to the state it was in prior to the shutdown.

Margin high (ignore faults) and margin low (ignore faults) operations are not supported by the LTC7841.

This command has one data byte. It will accept one or two but ignore the second byte.

Table 6. Supported OPERATION Command Register Values

ACTION	VALUE
Turn off immediately	0x00 (default)
Turn on	0x80
Margin Low	0x98
Margin High	0xA8

VOUT_MODE

VOUT_MODE command specifies the formatting for reading output voltage. The data byte always reads 0x3F for VID data format and cannot be changed. Attempts to write to VOUT_MODE will set a CML fault.

This read-only command has one data byte.

PMBus COMMAND DETAILS

MFR_CONFIG

The MFR_CONFIG command provides configuration bits to set the slew rate multiplier and to set whether the READ_TEMPERATURE_1 register reports internal die temperature or voltage measured from the external temperature sense element connected to the TSNS pin. The register contents are reset to 0x00 at power-on, MFR_RESET and by cycling RUN pin.

Bit	MEANING
[1:0] 00b 01b 10b 11b	Slew Rate Multiplier Nominal Slew Rate (SR) (default) Slow Slew Rate (SR÷8) Fast Slew Rate (SR×2) Illegal
2	READ_TEMPERATURE_1 command reporting 0: internal die temperature (1°C/bit) (default) 1: TSNS pin voltage (4mV/bit)

MFR_VOUT_COMMAND

The MFR_VOUT_COMMAND command sets the value of the internal reference voltage which, along with the external resistive feedback divider, determines the value of the output voltage. The units of the MFR_VOUT_COMMAND is in % of full range of the reference voltage where 100% is 2.4V. MFR_VOUT_COMMAND has a range of 0% to 100% which corresponds to a range of 0V to 2.4V for the reference voltage. Do not attempt to write values greater than 100% or unpredictable behavior may result. Values down to 0% can be written but datasheet specifications are not guaranteed below 25%.

This command has two data bytes and is formatted as a 9-bit unsigned number with 0.1953 %/bit scaling (0x1FF = 99.8%).

The C_{SLEW} capacitor and the slew rate multiplier (set in MFR_CONFIG) set the slew rate limit of the output voltage changes if this command is modified while the output is active and in a steady-state condition. Power-on, MFR_RESET, or cycling the RUN pin will reset this register to 0%.

MFR_MARGIN_LOW

The MFR_MARGIN_LOW command loads the LTC7841 with the value to which the internal reference is set when the OPERATION command is set to margin low. The units, range and restrictions are the same as MFR_VOUT_COMMAND. There is no restriction on the value relative to MFR_VOUT_COMMAND, i.e. the value is not required to be lower.

This command has two data bytes and is formatted as a 9-bit unsigned number with 0.1953%/bit scaling (0x1FF = 99.8%).

Slew rate limiting is the same as MFR_VOUT_COMMAND. Power-on, MFR_RESET, or cycling the RUN pin cause this register is reset to 0%.

MFR_MARGIN_HIGH

The MFR_MARGIN_HIGH command loads the LTC7841 with the value to which the internal reference is set when the OPERATION command is set to margin high. The units, range and restrictions are the same as MFR_VOUT_COMMAND. There is no restriction on the value relative to MFR_VOUT_COMMAND, i.e. the value is not required to be higher.

This command has two data bytes and is formatted as a 9-bit unsigned number with 0.1953 %/bit scaling (0x1FF = 99.8%).

Slew rate limiting is the same as MFR_VOUT_COMMAND. Power-on, MFR_RESET, or cycling the RUN pin cause this register is reset to 0%.

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTC7841 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

MFR_SPECIAL_ID

The 16-bit word representing the part name and revision. The word equals 0x40Dx and denotes the part is an LTC7841. The lower 4 bits are adjustable by the manufacturer.

This read-only command has 2 data bytes.

PMBus COMMAND DETAILS

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values and restarts the peak monitor routine.

This write-only command requires no data bytes, but will accept (and ignore) up to two.

STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition.

See Table 7 for a list of the status bits that are supported and the conditions in which each bit is set. Certain bits when set in the STATUS_WORD also cause the $\overline{\text{ALERT}}$ pin to be asserted.

Writing a "1" to a particular bit in the status word will attempt to reset that fault in the status word and the $\overline{\text{ALERT}}$ pin. If the fault is still present the status word bit and $\overline{\text{ALERT}}$ will remain asserted. If the $\overline{\text{ALERT}}$ has previously been cleared by an ARA message, the $\overline{\text{ALERT}}$ will be re-asserted. If the fault is no longer present, the $\overline{\text{ALERT}}$ pin will be de-asserted and the fault bit in the status word will be cleared.

All bits in the status word are also cleared by toggling the RUN pin or the ON bit in OPERATION. The bit will immediately be set again if the fault remains.

This command has two data bytes.

Table 7. Status Word Bit Descriptions and Conditions

BIT	DESCRIPTION	CONDITION	SET ALERT?	CLEARABLE BY WRITING '1' TO BIT?
0 (LSB)	None of the Above	If b[15] set due to V_{OUT} undervoltage	Yes	No
1	Communication Failure	(See Note 1)	Yes	Yes
2	Temperature Fault	Temp > 150°C	Yes	Yes
3	V_{IN} Undervoltage Fault	Not Implemented		
4	Output Overcurrent Fault	Not Implemented		
5	Output Overvoltage Fault	V_{OUT} > PGOOD High Threshold	Yes	Yes
6	OFF	No Power to the Output (Note 2)	No	No
7	Busy	Not Implemented		
8	Unknown	Not Implemented		
9	Other	Not Implemented		
10	Fans	Not Implemented		
11	$\overline{\text{PGOOD}}$	Inverted state of PGOOD pin	No	No
12	Manufacturer Specific	Not Implemented		
13	Input Voltage/ Current/Power Fault	Not Implemented	Yes	Yes
14	Output Current/Power Fault	Not Implemented		
15 (MSB)	Output Voltage Fault	V_{OUT} outside PGOOD window (Note 3)	Yes	Yes

Note 1: Communication failure is one of following faults: host sends too few bits, host reads too few bits, host writes too few bytes, host reads too many bytes, improper R/W bit set, unsupported command code, attempt to write to a read-only command. See PMBus Specification v1.2, Part II, Sections 10.8 and 10.9 for more information.

Note 2: Power may be off due to any one of the following conditions: OPERATION ON cleared or power on initialization not complete. When the power is off due to RUN low or due to a more serious fault conditions such as V_{IN} low or overtemperature fault, the PMBus interface is turned off instead of asserting the OFF bit.

Note 3: This bit is disabled when drivers are off for any reason, soft-start not complete, or the V_{OUT} has not reached the PGOOD window for the first time.

PMBus COMMAND DETAILS

All of the following telemetry registers are initialized to 0x8000 when cycling power, cycling RUN pin or sending a MFR_RESET command. The register will remain at this value until its first conversion is complete—typically within 50ms of the initialization event.

READ_V_{IN}

The READ_V_{IN} command returns the measured input voltage, in volts, at the V_{BIAS} pin.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mV/bit.

READ_VOUT

The READ_VOUT command returns the measured output voltage, in volts as specified by the VOUT_MODE command.

The output voltage is sensed at the V_{OUT} pin.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mV/bit.

READ_IIN

The READ_IIN command returns the average sense resistor voltage per channel, in Volts, measured between the $SENSE^+$ and the $SENSE^-$ pins of each channel. The average input current per channel is calculated by dividing the READ_IIN register value (volts) by the sense resistor value (Ω). For total input current (both channels), multiply the per channel current by 2, i.e. total input current = 2 • READ_IIN/R_{SENSE}.

The register is not updated in standby mode (OPERATION ON bit = 0) when drivers are off.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 50µV/bit

READ_IOUT

The READ_IOUT command returns the average sense resistor voltage per channel multiplied by the duty cycle to provide a measurement of output current. The average output current per channel is calculated by dividing the READ_IOUT register value (volts) by the sense resistor value (Ω). For total output current (both channels), multiply the per channel current by 2, i.e. total output current = 2 • READ_IOUT/R_{SENSE}.

The register is reset to 0x8000 in standby mode (OPERATION ON bit = 0) when drivers are off. This register is also reset to 0x8000 when the inductor current is discontinuous at light loads when operating in pulse skip or Burst Mode operation.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 50µV/bit

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns one of two values depending on the state of bit 2 of the MFR_CONFIG register. If bit 2 equals 0, the READ_TEMPERATURE_1 command returns the internal die temperature, in degrees Celsius, of the LTC7841. If bit 2 equals 1, the READ_TEMPERATURE_1 command returns the measured voltage, in volts, of the external temperature sense element connected to the TSNS pin.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled at 1°C/bit for internal die temperature or 4mV/bit for TSNS pin voltage.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_VOUT_PEAK. When writing to MFR_VOUT_PEAK, zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mV/bit.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

PMBus COMMAND DETAILS

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_VIN_PEAK. When writing to MFR_VIN_PEAK zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mV/bit.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature reported by the READ_TEMPERATURE_1 measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_TEMPERATURE_1_PEAK. When writing to MFR_TEMPERATURE_1_PEAK zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 1°C/bit.

For data consistency, it is important to clear this register when changing the READ_TEMPERATURE_1 reporting in the MFR_CONFIG register, i.e. changing reporting from internal to external temperature or visa versa.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current sense resistor voltage, in volts, reported by the READ_IOUT measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_IOUT_PEAK. When writing to MFR_IOUT_PEAK, zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 50µV/bit.

MFR_IIN_PEAK

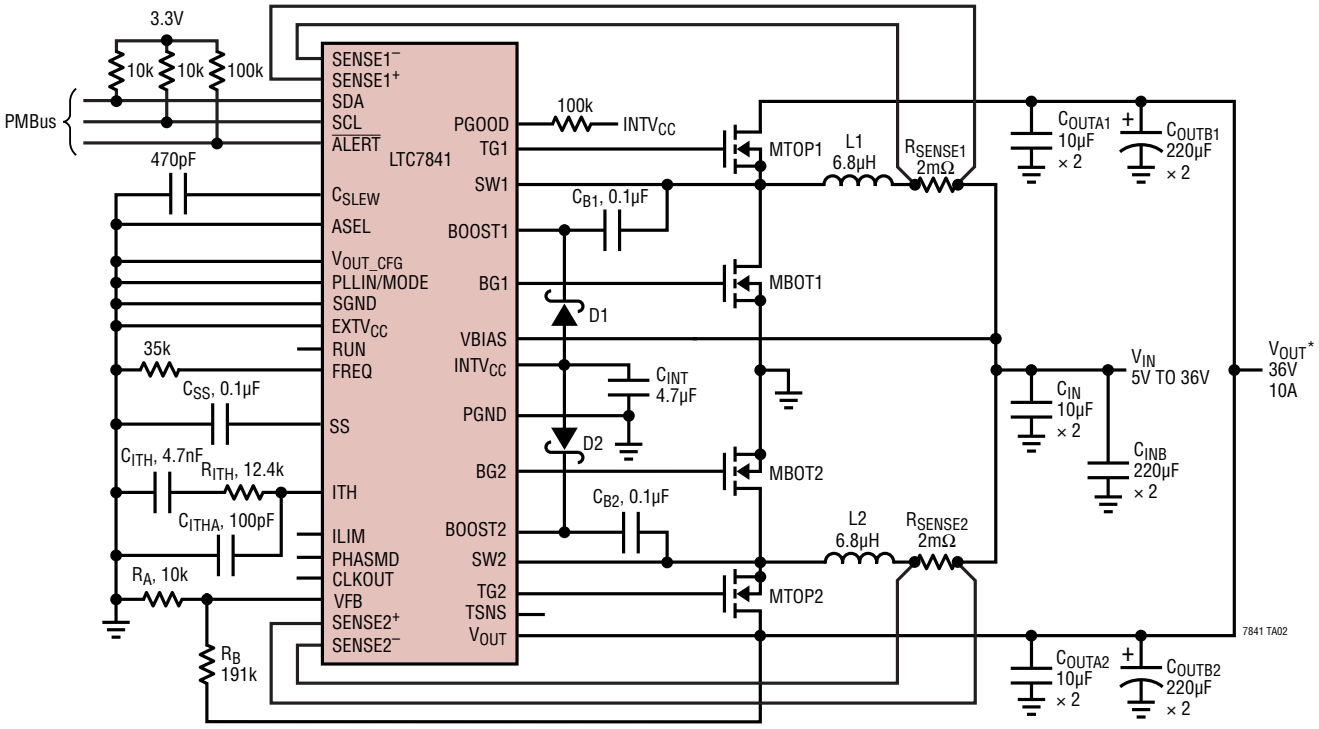
The MFR_IIN_PEAK command reports the highest current sense resistor voltage, in volts, reported by the READ_IIN measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_IIN_PEAK. When writing to MFR_IIN_PEAK, zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 50µV/bit.

TYPICAL APPLICATIONS

Figure 21. High Efficiency 2-Phase 36V Boost Converter with PMBus Interface

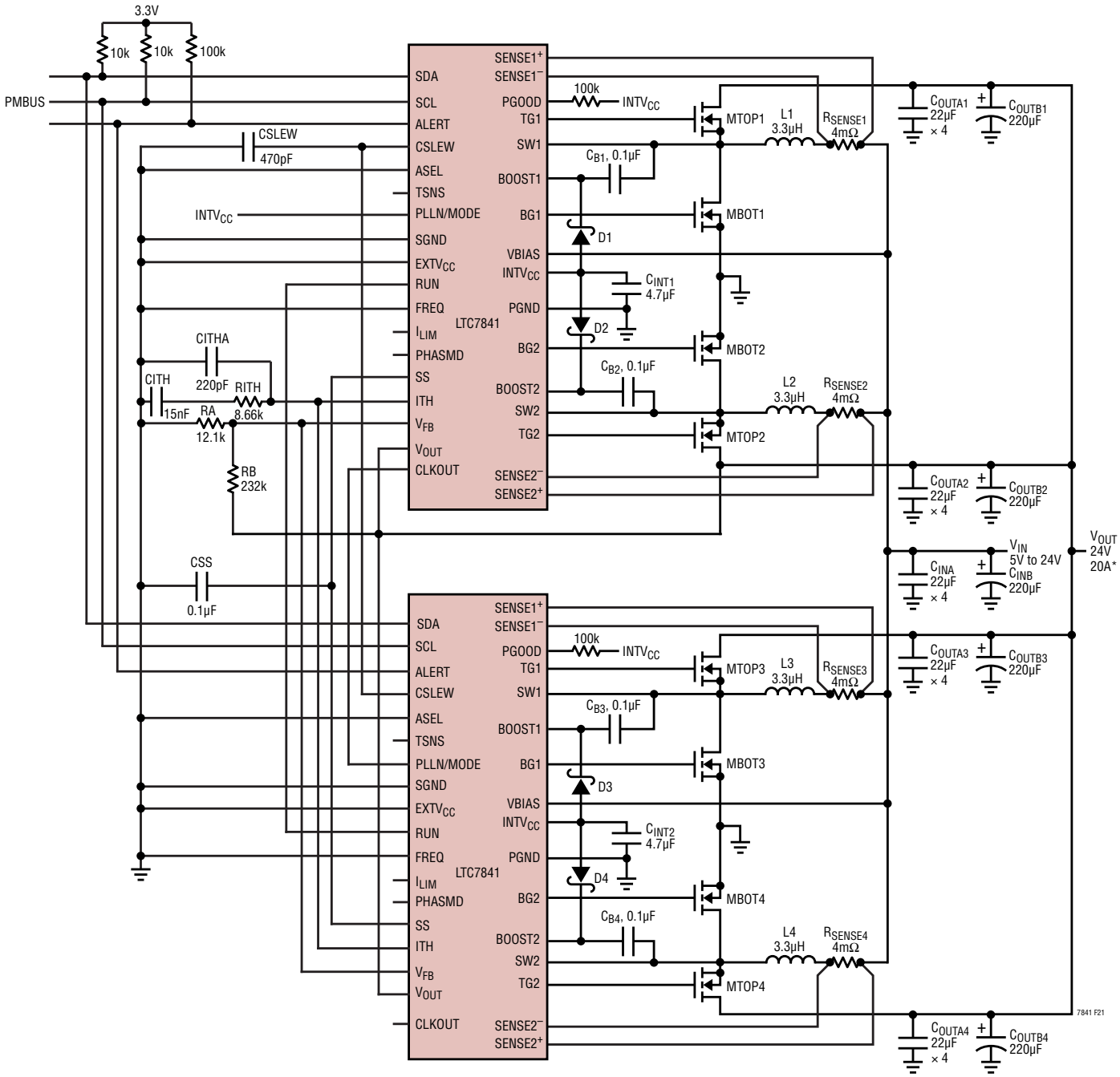


C_{INA}, C_{OUTA1}, C_{OUTA2}: MURATA GRM32ER71J106KA12L
C_{INB}, C_{OUTB1}, C_{OUTB2}: PANASONIC EEHZK1E221P
L1, L2: WURTH ELEKTRONIK 7443640680
MBOT1, MBOT2, MTOP1, MTOP2: INFINEON BSC065N06LS5
D1, D2: DIODES INC. DFLS1100-7

*V_{OUT} = 36V with MFR_VOUT_COMMAND set to 75%. V_{OUT} is adjustable from 12V to 48V.

TYPICAL APPLICATIONS

Figure 22. 4-Phase 480W Single Output Boost Converter

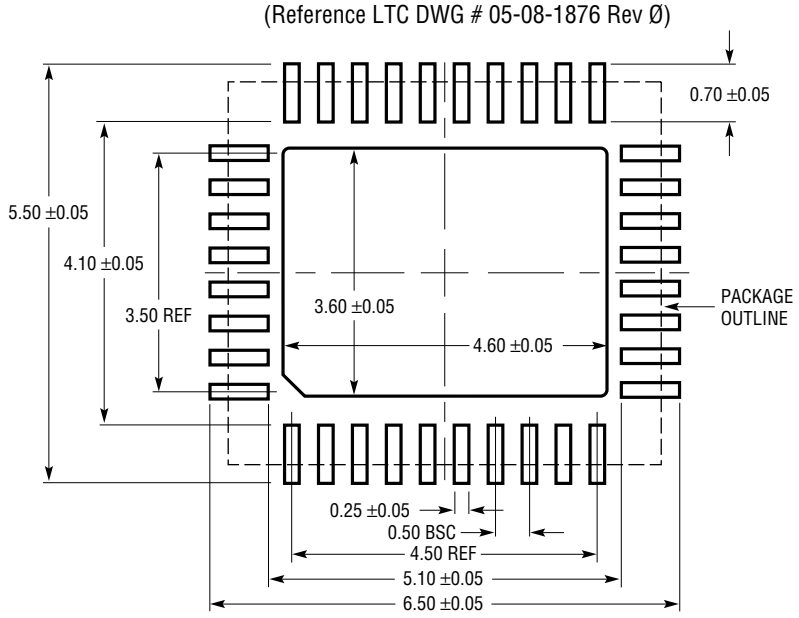


CINA, COUTA1, COUTA2, COUTA3, COUTA4: TDK C4532X5R1E226M
CINB, COUTB1, COUTB2, COUTB3, COUTB4: SANYO, 50CE220LX
L1, L2, L3, L4: PULSE PA1494.362NL
MBOT1, MBOT2, MBOT3, MBOT4, MTOP1, MTOP2, MTOP3, MTOP4: RENESAS HAT2169H
D1, D2, D3, D4: BAS140W

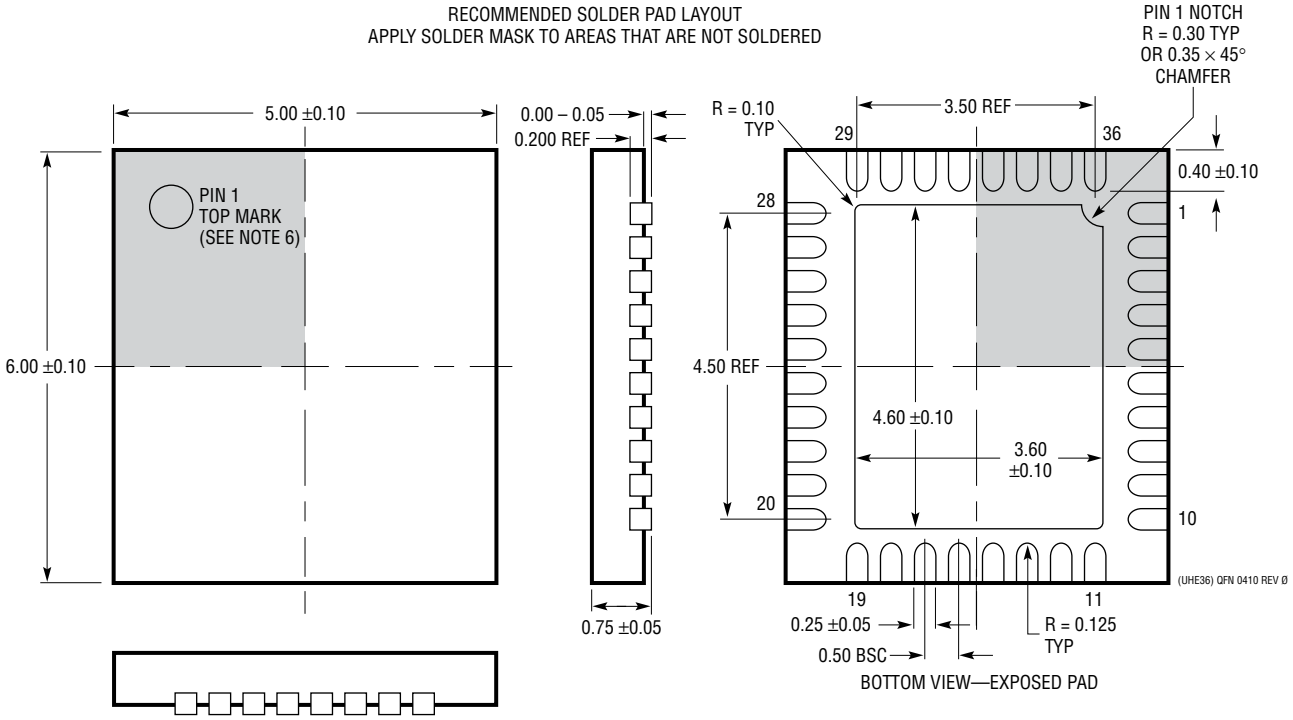
*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

PACKAGE DESCRIPTION

UHE Package
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1876 Rev Ø)



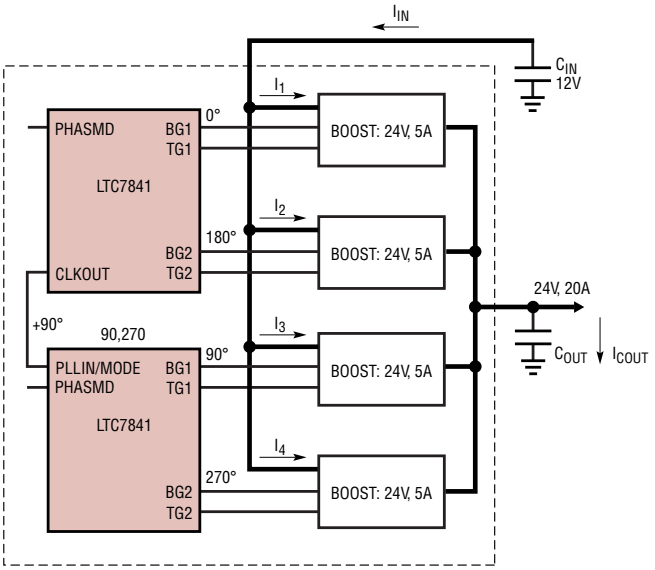
RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



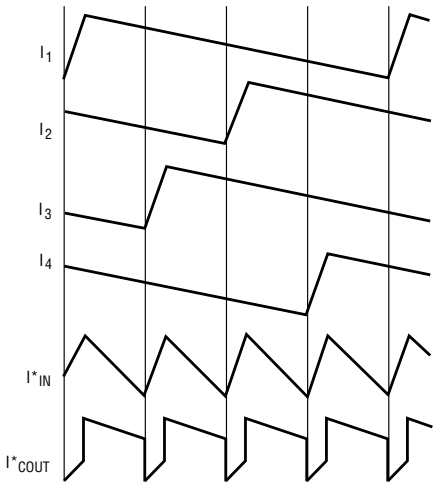
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Figure 23. PolyPhase Application



REFER TO FIGURE 15 FOR APPLICATION CIRCUITS



* RIPPLE CURRENT CANCELLATION INCREASES THE RIPPLE FREQUENCY AND REDUCES THE RMS INPUT/OUTPUT RIPPLE CURRENT, THUS SAVING INPUT/OUTPUT CAPACITORS

7841 F22

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3787	Single Output, Low I_Q Multiphase Synchronous Boost Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm x 5mm QFN-28, SSOP-28
LTC3788/ LTC3788-1	Dual Output, Low I_Q Multiphase Synchronous Boost Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 5mm x 5mm QFN-32, SSOP-28
LTC3786	38V Low I_Q Synchronous Boost Controller	4.5V (Down to 2.3V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 3mm x 3mm QFN-20, MSOP-16E
LTC3769	60V Low I_Q Synchronous Boost Controller	4.5V (Down to 2.3V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm x 4mm QFN-24, TSSOP-20
LTC3784	60V Single Output, Low I_Q Multiphase Synchronous Boost Controller	4.5V (Down to 2.3V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm x 5mm QFN-28, SSOP-28
LTC3862/ LTC3862-1	Single Output, Multiphase Current Mode Step-Up DC/DC Controller	4V ≤ V_{IN} ≤ 36V, 5V or 10V Gate Drive, 75kHZ to 500kHz Fixed Operating Frequency, SSOP-24, TSSOP-24, 5mm x 5mm QFN-24
LT3757/LT3758	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V/100V, 100kHz to 1MHz Fixed Operating Frequency, 3mm x 3mm DFN-10 and MSOP-10E
LTC3897/ LTC3897-1	Single Output, Low I_Q Synchronous Boost Controller with Input/ Output Protection	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 65V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm x 5mm QFN-28, SSOP-28, 5mm x 8mm QFN-44