

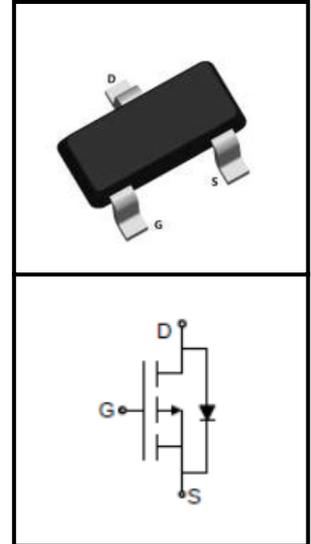
20V P-Channel Trench MOSFET

FEATURES

- Super Low Gate Charge
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- Load Switch
- Power Management
- Pulse Width Modulation(PWM)



Device Marking and Package Information

| Device | Package | Marking |
|----------|---------|---------|
| CTZ2305A | SOT-23 | 2305A |

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Value | Unit |
|---|----------------|----------|------------------|
| Drain-Source Voltage ($V_{GS} = 0\text{V}$) | V_{DSS} | -20 | V |
| Continuous Drain Current $T_A = 25^\circ\text{C}$ (note1) | I_D | -4.2 | A |
| Pulsed Drain Current (note2) | I_{DM} | -14 | A |
| Gate Source Voltage | V_{GSS} | ± 12 | V |
| Power Dissipation (note3) | P_D | 1 | W |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55~150 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Value | Unit |
|--|-----------------|-------|--------------------|
| Thermal Resistance, Junction-Ambient (note1) | $R_{\theta JA}$ | 125 | $^\circ\text{C/W}$ |

| Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified | | | | | | |
|--|---------------|---|-------|-------|-----------|-----------|
| Parameter | Symbol | Test Conditions | Value | | | Unit |
| | | | Min. | Typ. | Max. | |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0V, I_D = -250\mu A$ | -20 | -- | -- | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -20V, V_{GS} = 0V, T_J = 25^\circ\text{C}$ | -- | -- | -1 | μA |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 12V$ | -- | -- | ± 100 | nA |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\mu A$ | -0.5 | -0.6 | -1.0 | V |
| Drain-Source On-Resistance (note2) | $R_{DS(on)}$ | $V_{GS} = -4.5V, I_D = -4.2A$ | -- | 38 | 50 | $m\Omega$ |
| | | $V_{GS} = -2.5V, I_D = -3A$ | -- | 46 | 60 | $m\Omega$ |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0V,$ $V_{DS} = -10V,$ $f = 1.0MHz$ | -- | 740 | -- | pF |
| Output Capacitance | C_{oss} | | -- | 290 | -- | |
| Reverse Transfer Capacitance | C_{rss} | | -- | 190 | -- | |
| Total Gate Charge | Q_g | $V_{DD} = -10V, I_D = -3.2A,$ $V_{GS} = -4.5V$ | -- | 6.1 | -- | nC |
| Gate-Source Charge | Q_{gs} | | -- | 1.7 | -- | |
| Gate-Drain Charge | Q_{gd} | | -- | 1.2 | -- | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DS} = -10V, I_D = -1A$ $V_{GS} = -4.5V, R_G = 6\Omega, RL = 2.8\Omega$ | -- | 12.5 | -- | ns |
| Turn-on Rise Time | t_r | | -- | 35 | -- | |
| Turn-off Delay Time | $t_{d(off)}$ | | -- | 30 | -- | |
| Turn-off Fall Time | t_f | | -- | 10 | -- | |
| Body Diode Characteristics | | | | | | |
| Continuous Body Diode Current | I_S | | -- | -- | -4.2 | A |
| Pulsed Diode Forward Current | I_{SM} | | -- | -- | -14 | |
| Body Diode Voltage | V_{SD} | $T_J = 25^\circ\text{C}, I_{SD} = -3.1A, V_{GS} = 0V$ | -- | -0.81 | -1.2 | V |

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
4. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

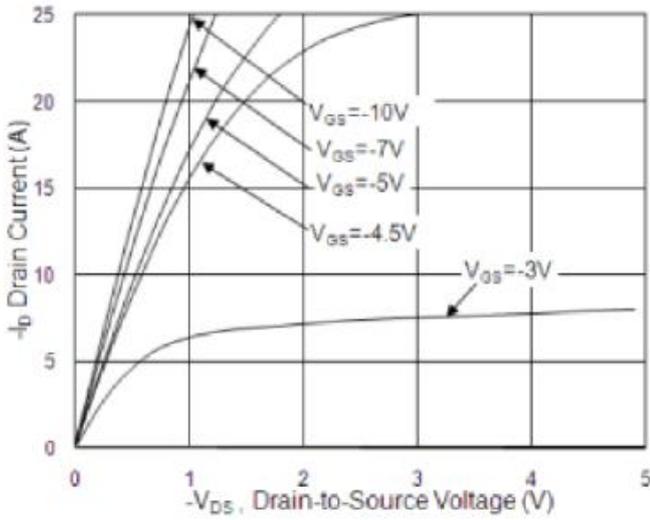


Fig.1 Typical Output Characteristics

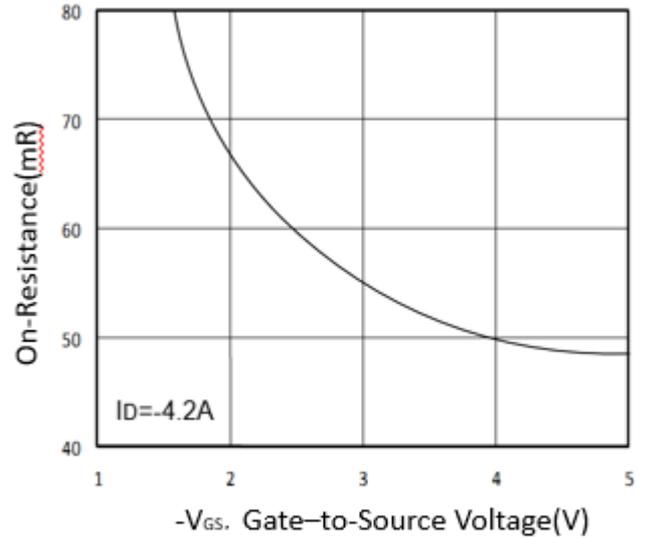


Fig.2 On-Resistance vs. G-S Voltage

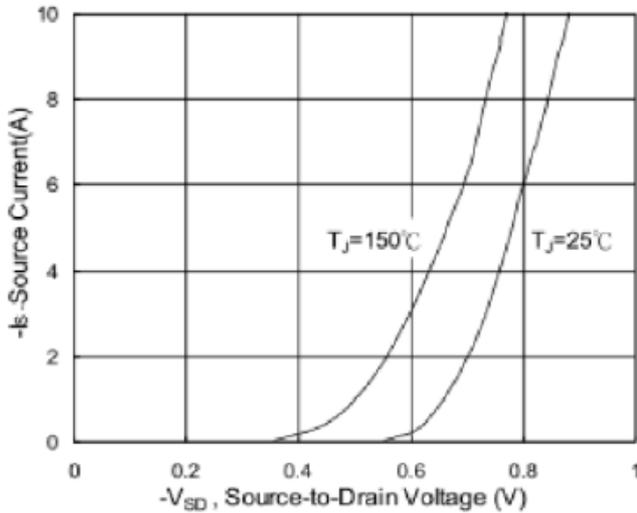


Fig.3 Forward Characteristics of Reverse Diode

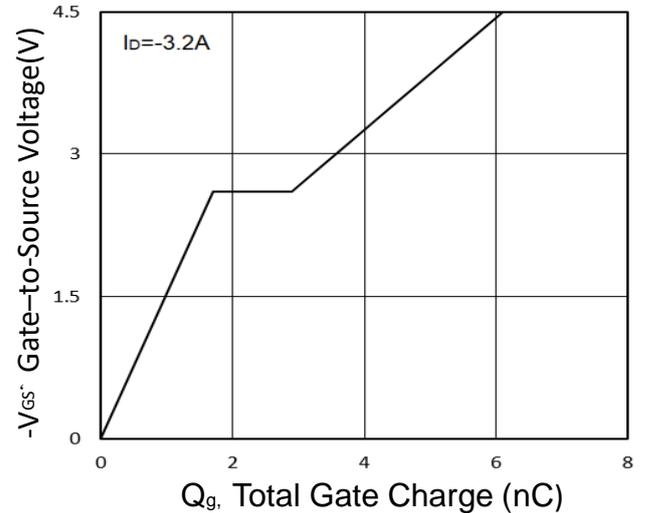


Fig.4 Gate-Charge Characteristics

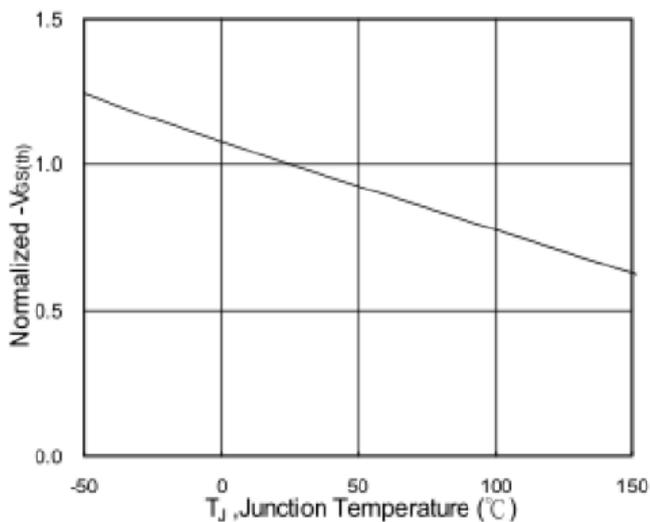


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

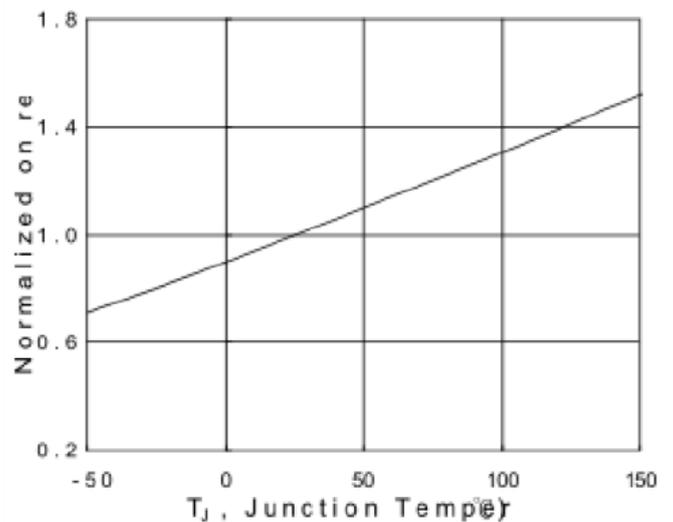


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

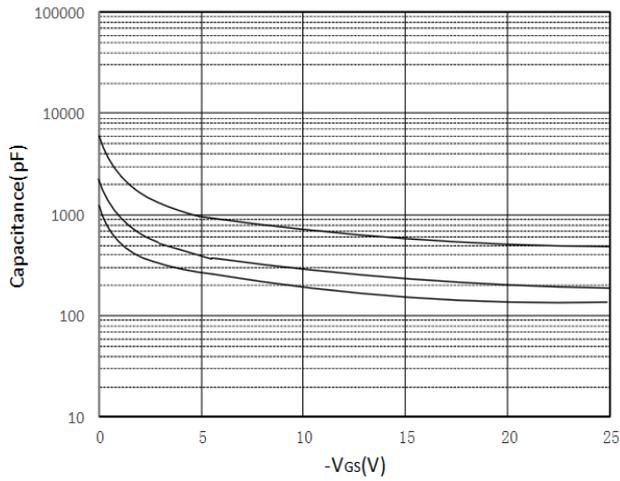
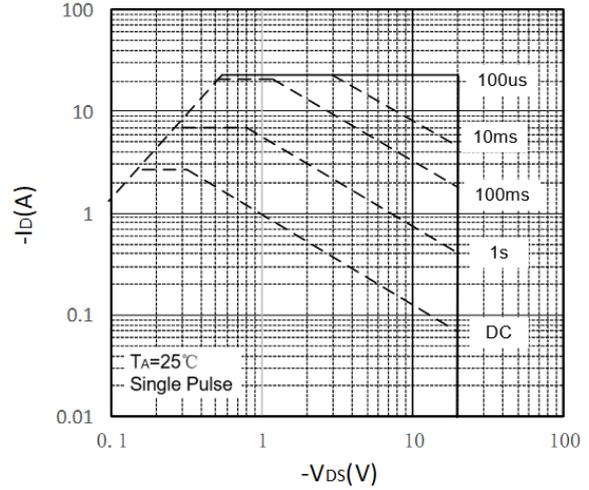
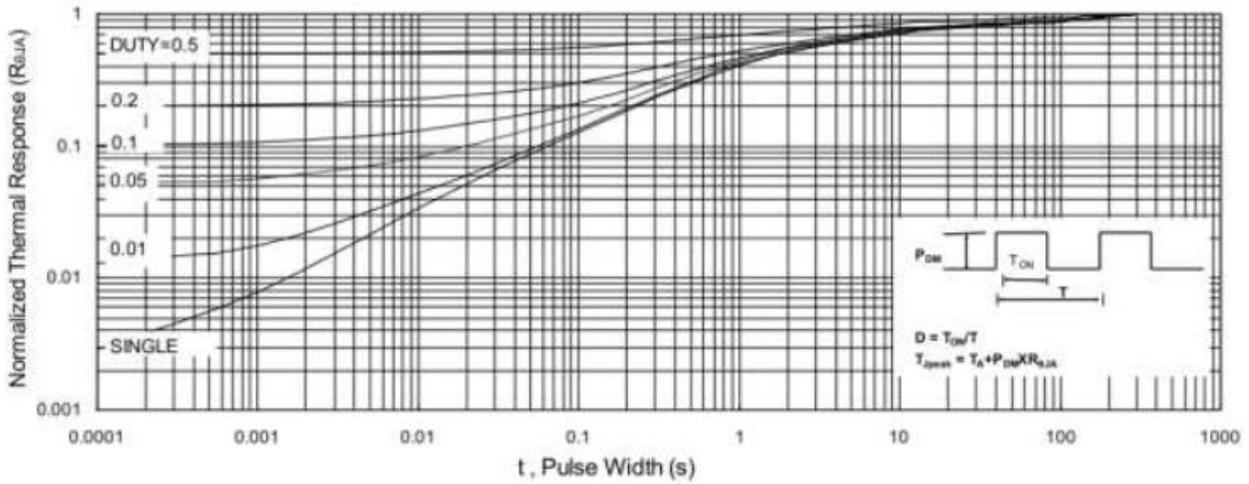
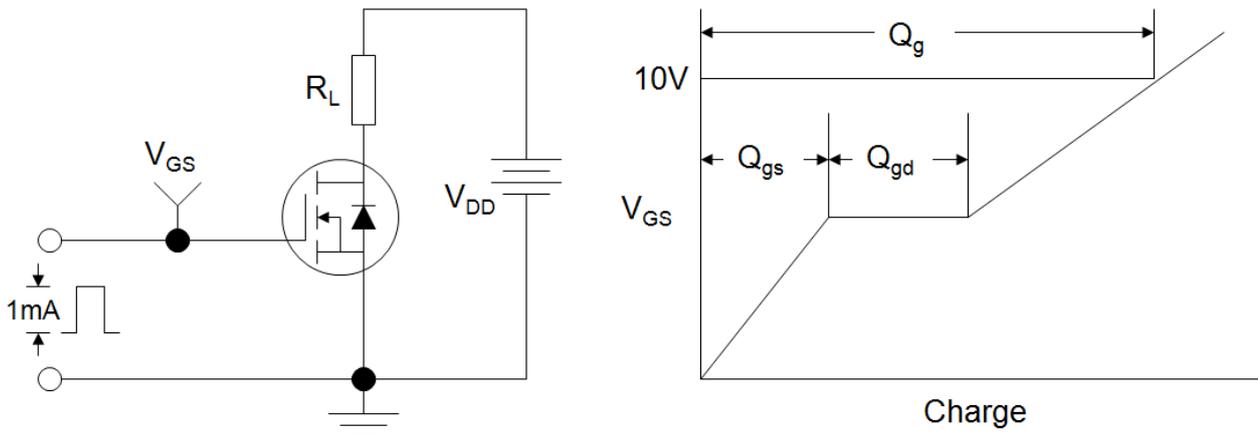
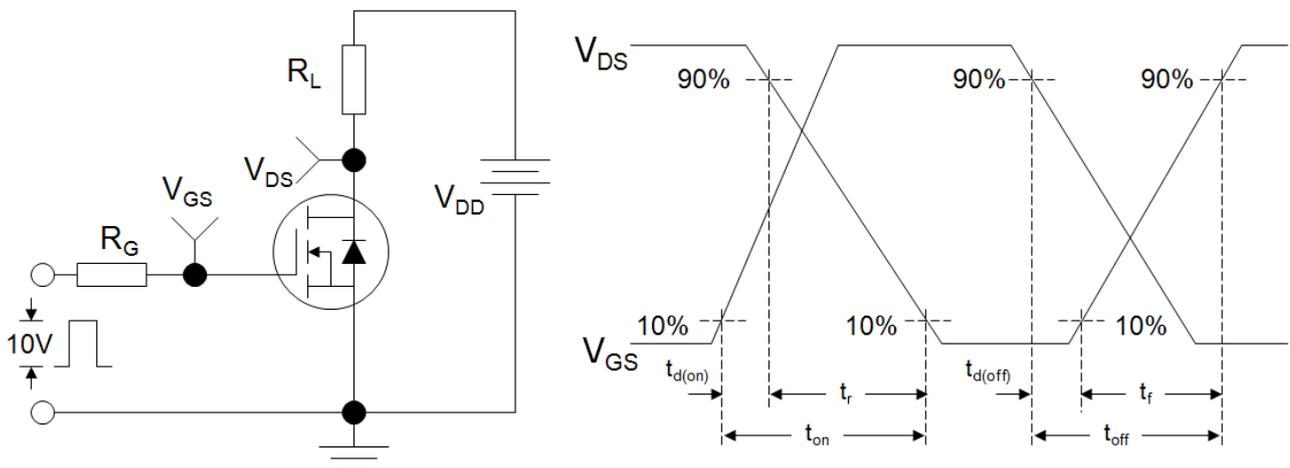
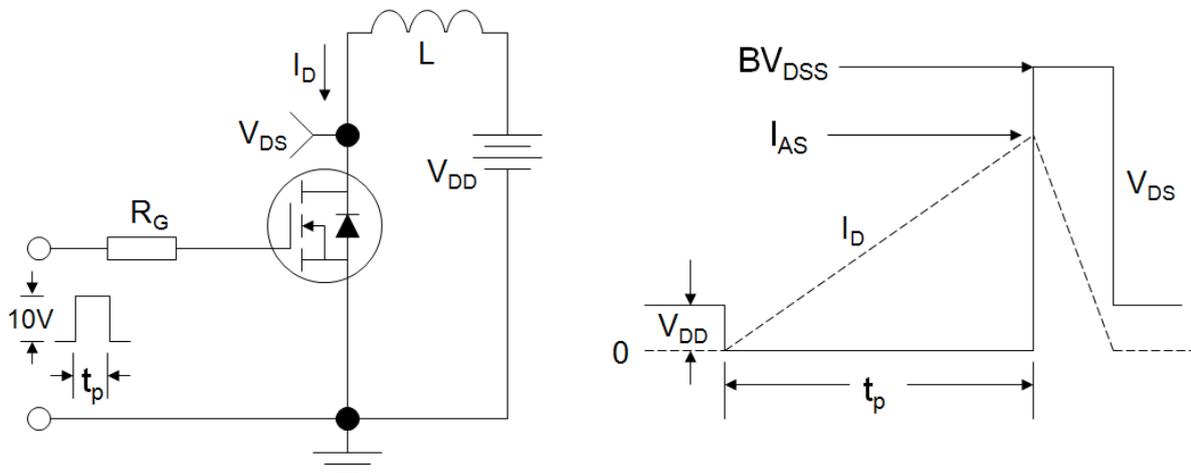
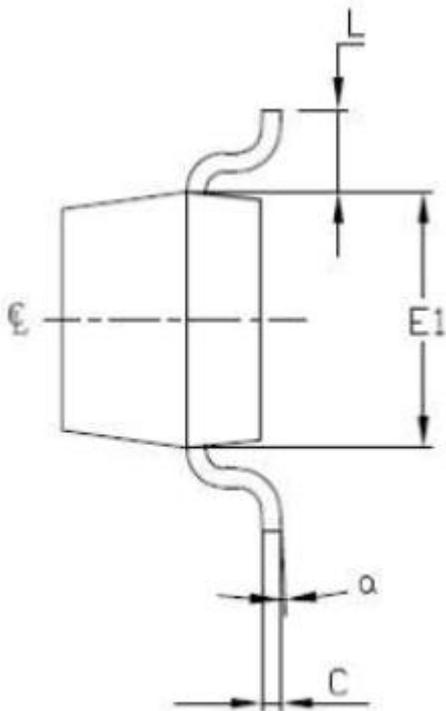
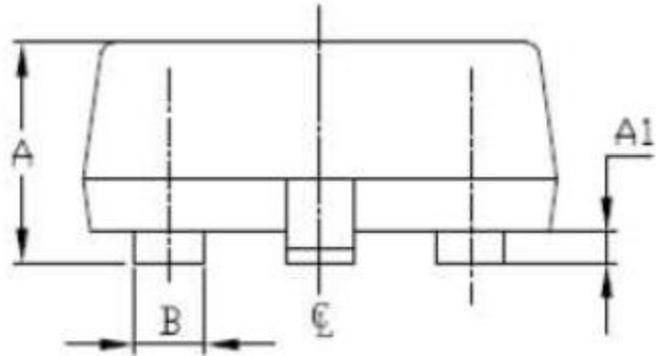
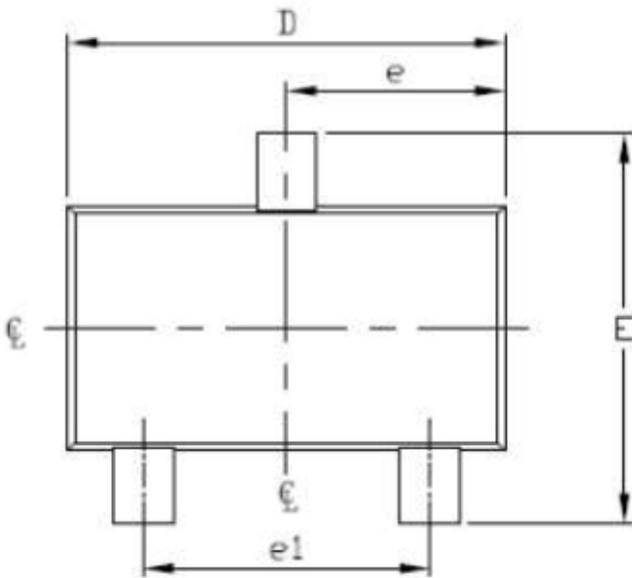
Typical Characteristics $T_J = 25^{\circ}\text{C}$, unless otherwise noted

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


SOT23


| COMMON DIMENSIONS | | | |
|-------------------|------|------|------|
| SYMBOL | mm | | |
| | MIN | NOM | MAX |
| A | 0.9 | 1.0 | 1.1 |
| A1 | 0.00 | 0.06 | 0.1 |
| B | 0.3 | 0.4 | 0.5 |
| C | 0.07 | 0.09 | 0.18 |
| D | 2.8 | 2.9 | 3.04 |
| E | 2.1 | 2.33 | 2.64 |
| E1 | 1.2 | 1.3 | 1.4 |
| e | 1.4 | 1.45 | 1.5 |
| e1 | 1.80 | 1.90 | 2.00 |
| L | 0.45 | 0.54 | 0.63 |
| a | 0° | 2.5° | 7° |

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