GENERAL DESCRIPTION

OB2632Q is a highly integrated Quasi-Resonant(QR) controller with adaptive multi-mode regulation, optimized for high performance, low standby power consumption and wide output voltage range PD adapter solutions, together with PD secondary controller, such as OB2612. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range.

At normal load condition, it operates in QR mode in high line input voltage. To minimize switching loss, the maximum switching frequency in QR mode is internally limited to 82 KHz. When the loading goes low, it operates in PFM mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. Additionally, in the low line input voltage, the IC operates in fixed frequency (65KHz) CCM mode at the heavy loading. As a result, high conversion efficiency can be achieved in the whole loading range.

High voltage startup is implemented in OB2632QCP, which features with short startup time and low standby power loss.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2632QMP.

OB2632Q offers complete protection coverage including cycle-by-cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), output short(SCP), output and VDD over voltage protection. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 22KHz is minimized to avoid audio noise during operation.

OB2632Q is offered in SOP8 or SOT23-6 package.

APPLICATIONS

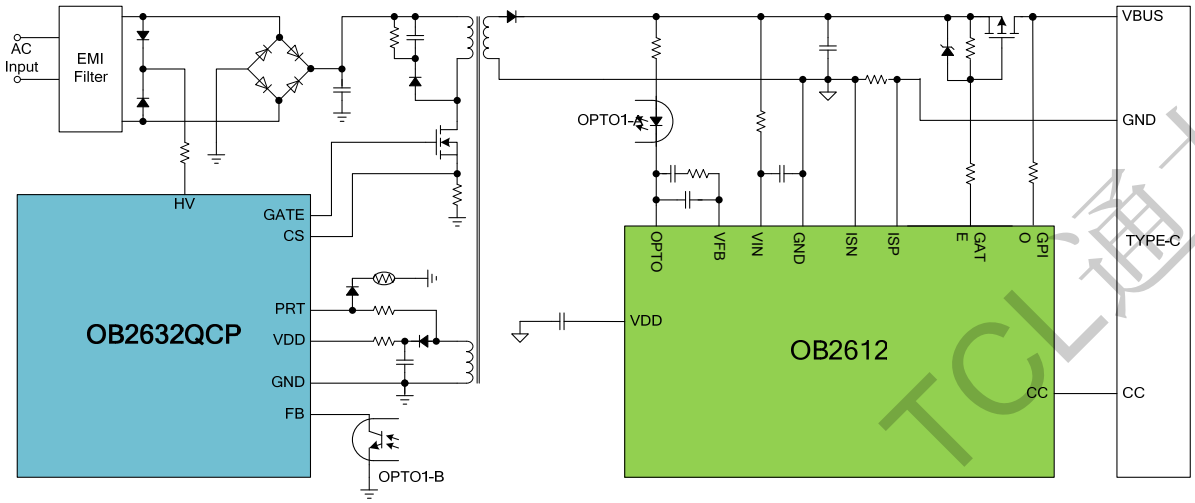
Offline AC/DC flyback converter for

- PD adapters
- Wide output range adapters

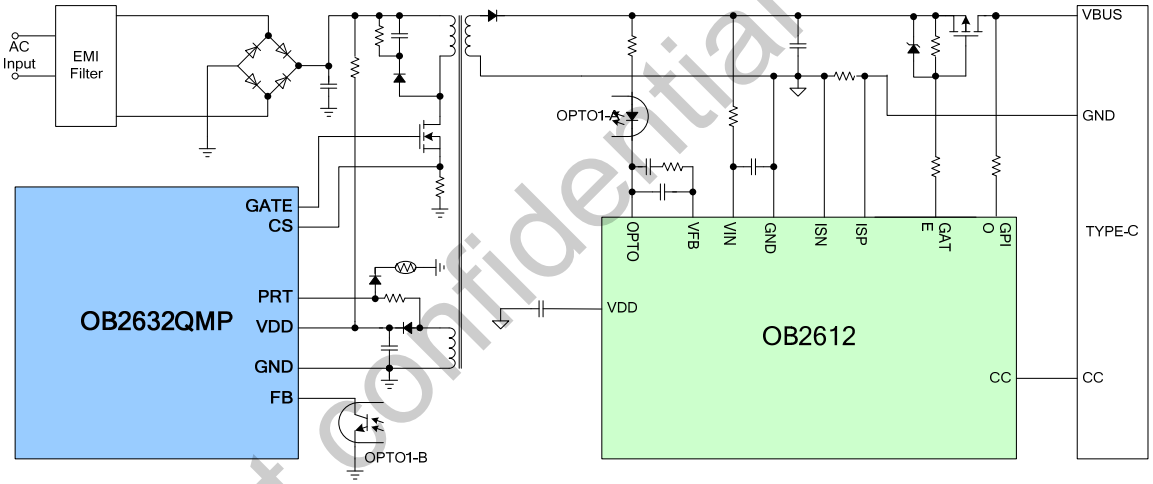
FEATURES

- Multi-Mode Operation
  - 100KHz maximum operation frequency in CCM mode @ Peak Load in low line voltage
  - 82KHz maximum clamping frequency in QR mode @ Full Load in high line voltage
  - 65KHz minimum clamping frequency in CCM mode @ Heavy Load in low line voltage
  - Valley switching operation @ Green mode
  - Burst Mode @ Light Load & No Load
- Very wide range of supply voltage
- Low operating current at light/no load
- Internal OCP compensation for universal line voltage
- Extended burst mode control for improved efficiency and low standby power
- Power on soft start reducing MOSFET Vds stress
- Frequency shuffling for EMI
- Audio noise free operation
- High voltage startup integrating intelligent brownout detection, AC off detection with X-CAP discharge function(OB2632QCP only)
- Comprehensive protection coverage
  - VDD under voltage lockout with hysteresis (UVLO)
  - Cycle-by-cycle over current protection (OCP) with auto-recovery
  - Overload protection (OLP) with auto-recovery
  - Over temperature protection (OTP) with latch shut down
  - VDD over voltage protection with latch shut down
  - Output over voltage protection with latch shut down
  - Output short protection (SCP) with auto-recovery
  - Brownout protection with auto-recovery (OB2632QCP only)
  - Output diode short protection with auto-recovery

TYPICAL APPLICATION



OB2632QCP Typical Application

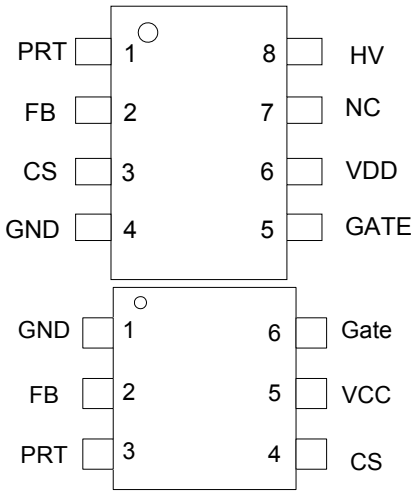


OB2632QMP Typical Application

GENERAL INFORMATION

Pin Configuration

The OB2632Q is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
OB2632QCP	SOP8, Halogen-free, Tube
OB2632QCPA	SOP8, Halogen-free, T&R
OB2632QMP	SOT23-6, Halogen-free, T&R

Package Dissipation Rating

Package	RθJA(℃/W)
SOP8	90
SOT23-6	200

Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	56V
High-Voltage Pin, HV (OB2632QCP only)	-0.3 to 500 V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-40 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

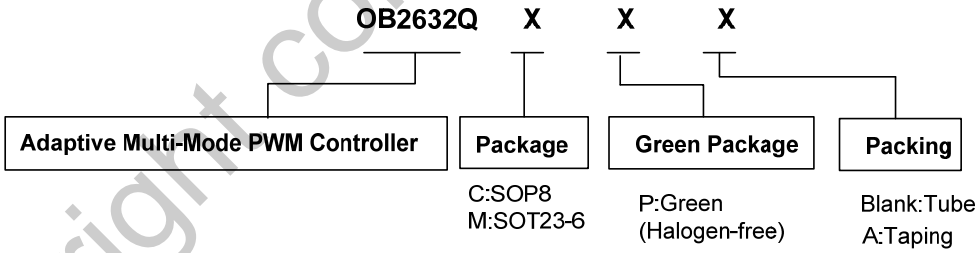
Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

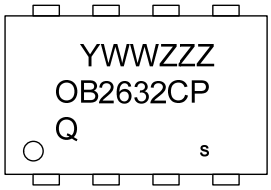
Note2: Rating values of FB/BO/CS/GATE pin refer to DC only. For small duty cycle pulse in less than 200ns in one period (typical 15.4us), negative spike value is relaxed to -2V.

Recommended Operating Condition

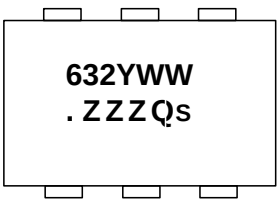
Symbol	Parameter	Range
VDD	VCC Supply Voltage	12 to 52V

Marking Information





Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
C:SOP8 Package
P:Green Package(Halogen-free)
S:Internal Code(Optional)



Y:Year Code
WW:Week Code(01-52)
ZZZ: Lot code
S: Internal code

TERMINAL ASSIGNMENTS

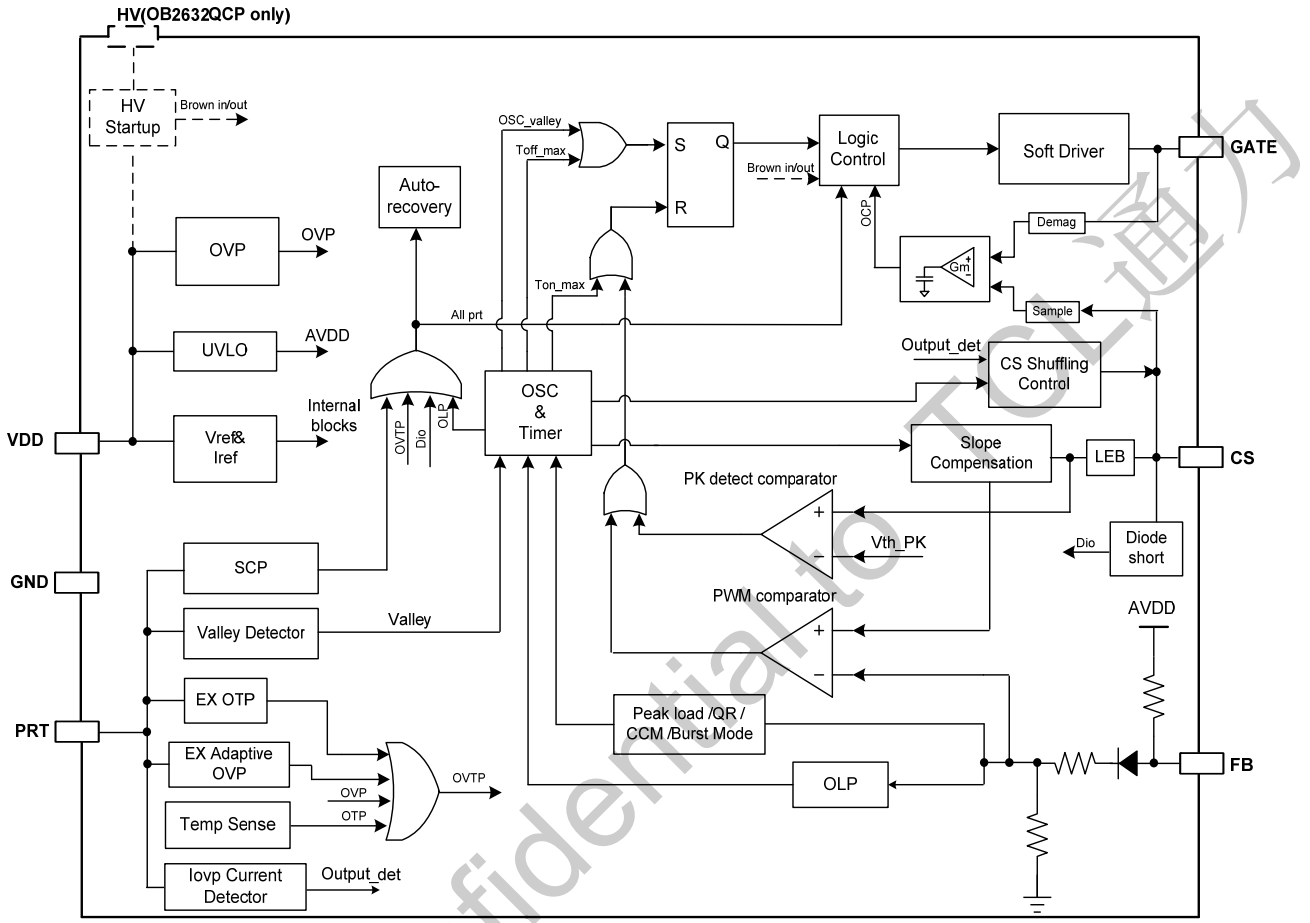
For OB2632QCP

Pin NO.	Pin Name	I/O	Description
1	PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust IOVP/ISCP trigger current and detect transformer core demagnetization. If both OTP and OVP/SCP are needed, a diode should be connected between PRT pin and the NTC resistor.
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	CS	I	Current sense input
4	GND	P	Ground
5	Gate	O	Totem-pole gate driver output for power Mosfet
6	VDD	P	Power Supply
7	NC		
8	HV	P	Connected to the line input via resistors and diodes for startup and x-cap discharge, this PIN allows the brownout detection as well.

For OB2632QMP

Pin NO.	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust IOVP/ISCP trigger current and detect transformer core demagnetization. If both OTP and OVP/SCP are needed, a diode should be connected between PRT pin and the NTC resistor.
4	CS	I	Current sense input
5	VDD	P	Power Supply
6	Gate	O	Totem-pole gate driver output for power Mosfet

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_A = 25℃, VDD=18V, unless otherwise noted)

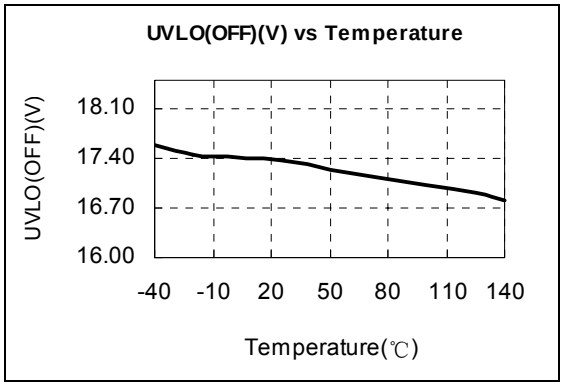
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
HV Startup (OB2632QCP only)						
IHV1	Supply current from HV pin @VDD>1V	VDD=2V, HV=100V	1	2	3.5	mA
IHV2	Supply current from HV pin @VDD<1V	VDD=0.5V,HV=100V	0.3	0.57	0.85	mA
leakage	HV pin leakage current after startup	VDD=18V, HV=500V		5	10	uA
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
Iop_VDD	Normal Operation Current	V_{FB}=3V, CL=1nF		2.8	3.5	mA
Iop_VDD_Burst	Burst Operation Current	V_{FB}=0.5V, CL=1nF		0.45	0.65	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		6.7	7.2	7.7	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		15.5	16.5	17.5	V
Vpull-up	Pull-up PMOS active			10		V
OVP	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	53	54.5	56	V
Vth_latch	Latch release voltage			4.8		V
T_{D}_recovery (OB2632QCP only)	Restart time for auto-recovery protection			1.4		s
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS			3.3		V/V
Maximum duty cycle	Max duty cycle @ VDD=14V,VFB=3V,VCS=0.3V			85		%
Vref_rising	The threshold enter rising frequency mode	Iovp>153uA		3.5		V
Vref_green	The threshold enter green mode			2.0		V
Vref_burst_H	The threshold exit burst mode	Iovp>80uA		1.2		V
		Iovp<75uA		0.95		V
Vref_burst_L	The threshold enter burst mode	Iovp>80uA		1.1		V
		Iovp<75uA		0.85		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		210		uA
V_{TH}_Openloop	The open loop FB Threshold Voltage			4.5		V
T_{D}_ Openloop	The open loop protection			40		ms

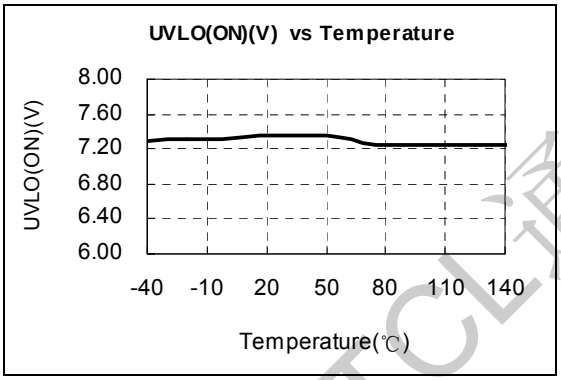
	debounce Time					
Z_{FB}_IN	Input Impedance			30		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time of CS threshold			4		ms
T_blanking	Leading edge blanking time			300		ns
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		90		ns
Vref_PK	Internal Current Limiting Threshold Voltage with zero duty cycle			0.48		V
Vref_PK_clamp	CS voltage clamper			0.76		V
Vref_OCP	Internal OCP protection voltage threshold		0.24	0.25	0.26	V
Td_cs_pk_ADJ	The delay time from PWM off to CS peak clamping adjustment start point			2.5		us
I_{PK}_ADJ	Output current from CS pin when PWM turns off		92	100	108	uA
T_D_OCP	OCP Debounce Time			60		ms
Oscillator						
Fosc_PK	Peak frequency	VDD=15V,FB=4.5V, Iovp>153uA		100		KHz
Fosc_QR	Average max clamp oscillation frequency in QR mode	VDD=15V, FB=3V,		82		KHz
Δf_OSC_QR	Frequency jittering of average clamp fmax_QR			±7		%
Fosc_CCM	Min clamp oscillation frequency in CCM mode	VDD=15V,FB=3V,		65		KHz
Δf_OSC	Frequency jittering			±5		%
F_shuffling	Shuffling frequency			240		Hz
Δf_Temp	Frequency Temperature Stability			1		%
Δf_VDD	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			23		KHz
Gate driver						
VOL	Output low level @ VDD=15V, Io=20mA				1	V
VOH	Output high level @ VDD=15V, Io=20mA		8			V
V_clamping	Output clamp voltage			13		V
T_r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			380		ns
T_f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			55		ns
Brownout protection(OB2632QCP only)						

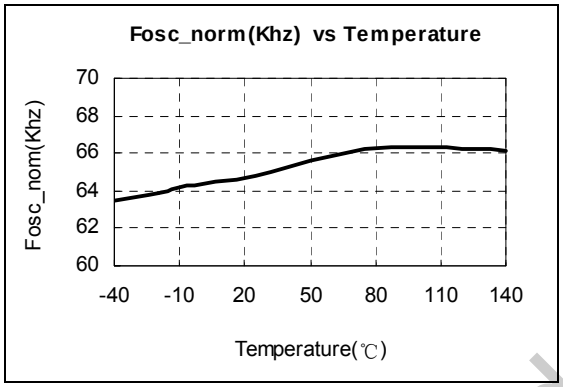
Vth_bo_L	Threshold voltage for Brownout	RHV=200 KΩ	63	70	77	VAC
Vth_bo_H	Threshold voltage for Brownout release	RHV=200 KΩ	70	77	85	VAC
Td_brownout	Brownout debounce time		27	32	37	ms
PRT pin						
Ibias	Output bias current expect during OVP detection			10		uA
IRT	Output current for external OTP detection		94	100	106	uA
Vref_OTP	Threshold voltage for external OTP		0.94	1.00	1.06	V
Td_ex_OTP	EX OTP debounce time			50		Cycles
Ioutput_ovp	Current threshold for adjustable output OVP		285	300	315	uA
Td_output_ovp	Output OVP debounce time			8		Cycles
Tsamp_OVP	The time from Gate off to OVP detecting turn-off point	FB=2.5V		2.5		us
		FB=1.5V		1.8		us
Iscp	SCP threshold			20		uA
Td_scp	SCP detect after startup			15		ms
On Chip OTP						
OTP Level				155		℃
OTP exit				125		℃

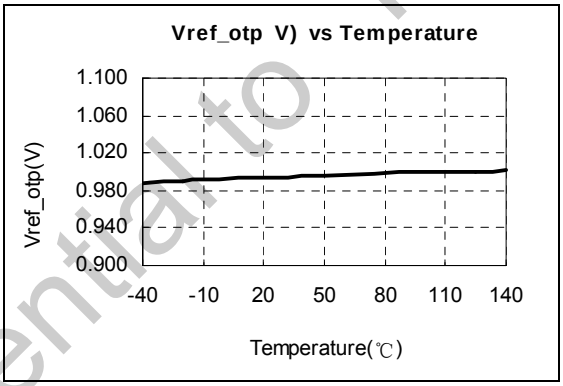
CHARACTERIZATION PLOTS

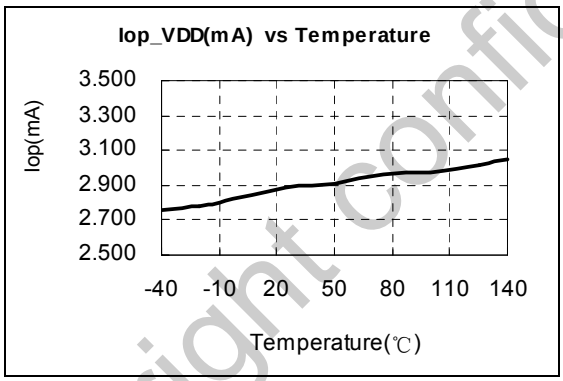
VDD = 18V, TA = 25℃ condition applies if not otherwise noted.

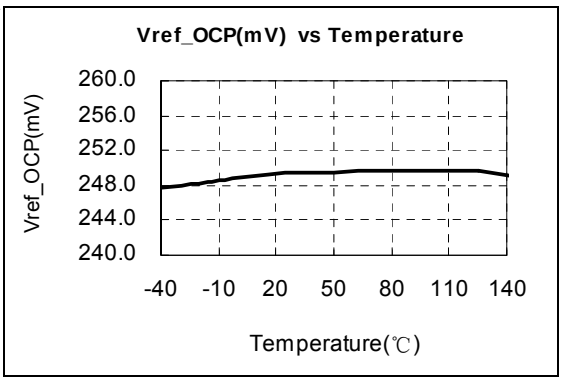


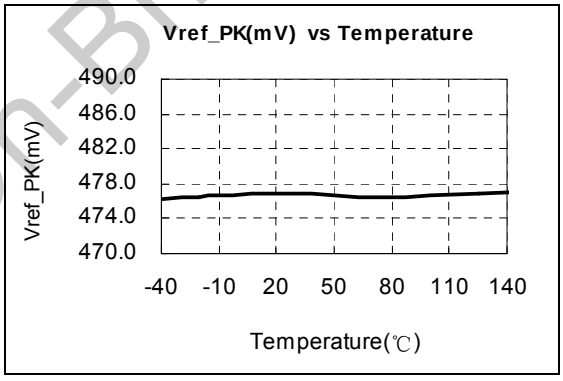


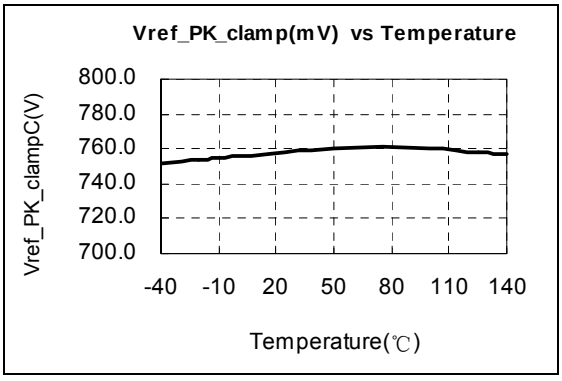


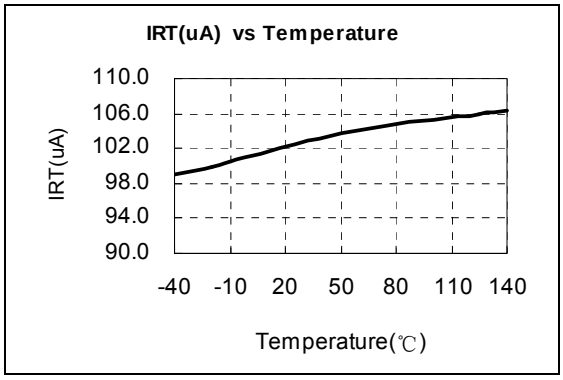


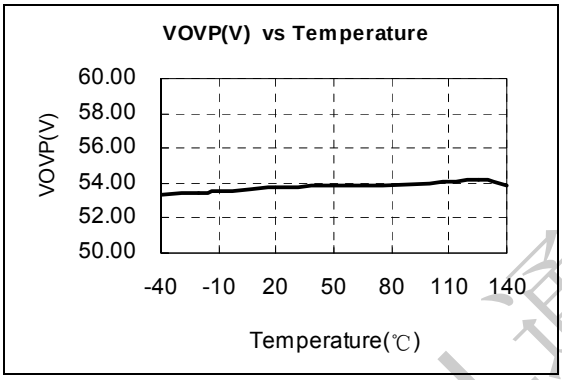












OPERATION DESCRIPTION

Quasi-Resonant (QR) converter typically features lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency. OB2632Q is a highly integrated Quasi-Resonant(QR) controller with adaptive multi-mode regulation, optimized for high performance, low standby power consumption and wide output voltage range PD adapter solutions, together with PD secondary controller, such as OB2612. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Internal High Voltage Startup and Under Voltage Lockout (UVLO) (OB2632QCP only)

OB2632Q integrates HV startup circuit, and provides about 2mA current to charge VDD pin during power on state from HV pin. When VDD voltage is higher than UVLO(OFF), the charge current is switched off. At this moment, the VDD capacitor provides current to OB2632Q until the auxiliary winding of the main transformer starts to provide the operation current.

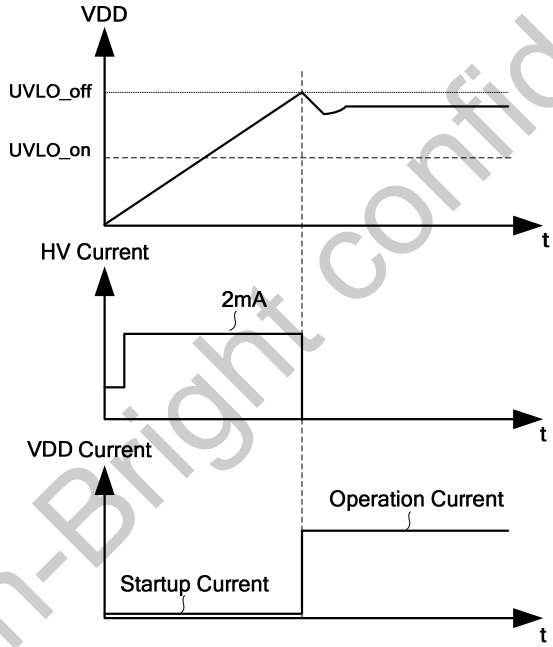


Fig1 Startup current timing

Startup Current and Start up Control (OB2632QMP only)

Startup current of OB2632Q is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The typical operating current of OB2632Q is 2.8mA. Good efficiency is achieved with this low operating current together with the 'Extended burst mode' control features.

Soft Start

OB2632Q features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0V to the maximum level. Every restart up begins with a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in OB2632Q. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Multi Mode Operation for High Efficiency

OB2632Q is a multi-mode QR/PWM controller. The controller changes the operation mode according to line voltage, output voltage and load conditions.

At normal full load conditions (Vth2<VFB, Figure 2), there are two situations: firstly, when the system input is in low line input range, the IC operates in fixed frequency CCM mode. Thus,

small size transformer can be used with high power conversion efficiency. Secondly, when the system input is in high line input range, the IC operates in QR mode. In this way, high power conversion efficiency can be achieved in the universal input range when system is at full loading conditions. The efficiency and system cost is controlled at an optimal level.

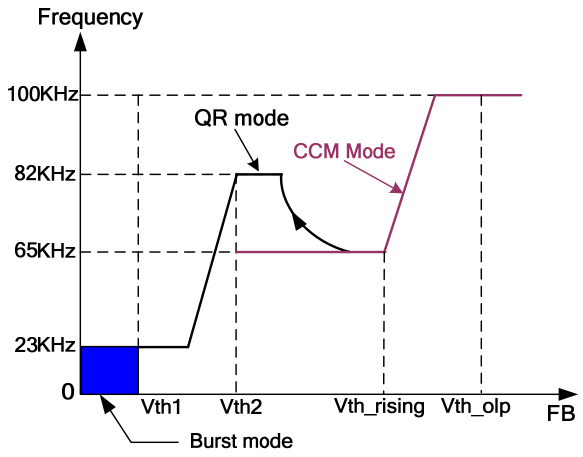


Fig2 Frequency vs Feedback voltage

At light load conditions (Vth1<VFB<Vth2, Figure 2), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

At no load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 22KHz is minimized to avoid audio noise during operation.

Additionally, a peak power mode (VFB>Vth_rising) is implemented based on On-Bright proprietary technology to supply a peak current output requirement (Iovp>153uA). In peak power mode, frequency is increased from 65KHz (typical) to 100KHz (typical).

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2632Q current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense voltage and the FB voltage.

Internal Synchronized Slope Compensation

In OB2632Q, when the fixed frequency CCM mode is reached, the slope compensation will be automatically added to the system. Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage. When the system exits fixed frequency CCM mode, the slope compensation will automatically disappear.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at 85mV(typical) at the PRT pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at PRT is below 85mV in falling edge.

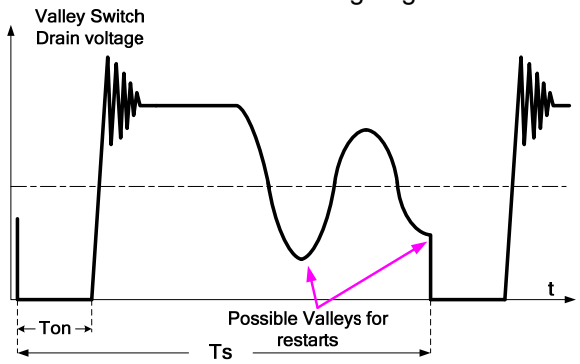


Fig3 Valley detection

Dual Function of External OTP and Output OVP/SCP

On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is

realized through time-division technology as shown in the figure 4.

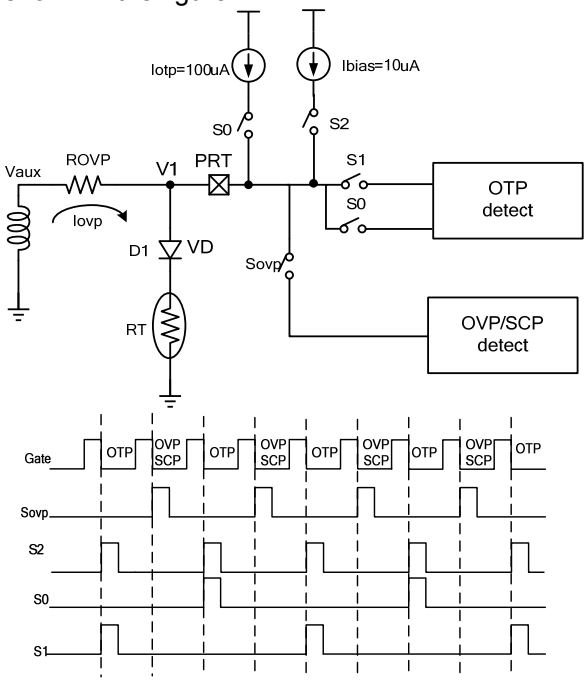


Fig4 PRT Pin protection timing

There is a 10uA(typical) bias current outflow when S2=1, that's S0= "1" or S1= "1". For external OTP detection, when switch control signal S1= "1", the 10uA (typical) current flows out from PRT pin. When switch control signal S0= "1", another 100uA (typical IRT) current flows out from PRT pin in addition to 10uA.

So the PRT pin voltage V1(s0) at phase S1="1" is:

$$V1(s1) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP \cdot 10uA}{ROVP + RT}$$

The PRT pin voltage V1(s1) at phase S0="1" is

$$V1(s0) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP(10uA + 100uA)}{ROVP + RT}$$

Vaux is the auxiliary winding demagnetization voltage.

VD is D1 forward voltage.

ROVP and RT are shown in fig4.

Voltage difference of ΔVotp at phase S0 and S1 phase is

$$\Delta V_{otp} = V1(s0) - V1(s1) = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 100uA$$

This voltage difference cancels the effect of D1 diode forward voltage.

When ΔVotp< VOTP (1.0V typical), external OTP latch protection is triggered after 60 (typical) PWM cycles debounce.

For output OVP detection, when Sovp= "1", Iovp is equal to (Naux/Nsec)*(Vout+Vdiode)/ROVP. If Iovp is larger than 300uA (typical Ioutput_ovp), larger output OVP is triggered. The output OVP voltage is calculated as

$$V_{outovp} = \frac{Iovp\_th \cdot N_{sec} \cdot ROVP}{N_{aux}} - V_{diode}$$

Nsec is transformer secondary winding turns, Naux is transformer auxiliary winding turns, Vdiode is the secondary output diode forward voltage .

OVP latch protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

For output SCP detection, when Sovp= "1", Iscp is equal to (Naux/Nsec)*(Vout+Vdiode)/ROVP. During the 15ms after the IC startup, if Iscp is less than 20uA (typical Iscp), SCP is triggered. The output SCP voltage calculation method is the same as output OVP detection.

SCP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output SCP level can be programmed.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including OCP, output short protection, Under Voltage Lockout on VDD (UVLO) and peak load protection, and latched shutdown features including Over Temperature Protection (OTP), VDD and output Over Voltage Protection (OVP).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit. For protection with latched shut down mode, control circuit shuts down (latch) the power MOSFET when an over temperature condition or over voltage condition is detected until VDD drops below 4.8V (typical) (Latch release voltage), and the device enters power on restart-up sequence thereafter.

Programmable OCP and Peak output Current Controls

In order to meet peak current output requirement, OB2632Q sets up two levels output current protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively. When output current exceeds the OCP threshold for 60ms (typical), OCP protection occurs. The OCP loop ensures the output OCP has a very tight range and is only related with turns ratio and Rsense.

The specification for output OCP protection voltage threshold, Vref_OCP, is 0.25V (typical).

$$I_{out\_OCP} = \frac{N \cdot Vref\_OCP}{Rsense}$$

N is the ratio of transformer primary winding turns to secondary winding turns.

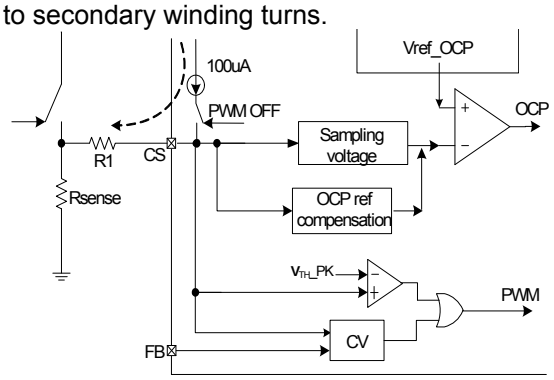


Fig.5 Programmable OCP and PK load protection

OB2632Q provides an adaptive cycle-by-cycle OCP compensation method varying with gate on duty cycle in Fig6. The maximum cycle-by-cycle OCP threshold voltage, Vth_PK, is 0.76V(typical). At PWM off state, 100uA current flows out of CS pin to generate a voltage through R1 and Rsense. The final CS peak clamping voltage threshold is adjusted by the added voltage.

$$V_{th\_PK\_final} = V_{th\_PK} + 100uA \cdot R1$$

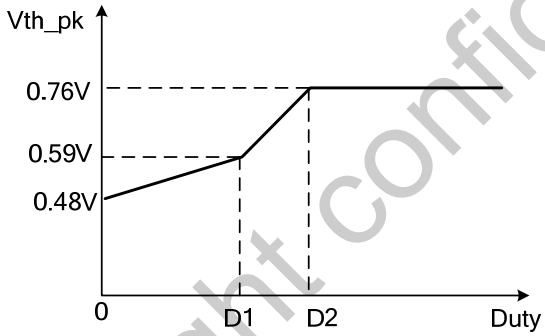


Fig6 Cycle by cycle OCP compensation

Two level OCP Controls

In order to meet peak current output requirement under high output level (Iovp>153uA), OB2632Q sets up two levels OCP protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively, and these two threshold values are internally compensated. When primary side inductor current exceeds the OCP threshold, OCP timer will begin counting. After 60ms (typical), OCP protection occurs.

When primary side inductor current exceeds the peak power threshold, over peak power timer will begin counting. After 40ms (typical), peak load protection occurs. OCP and peak power protection are mutually independent and do not affect each.

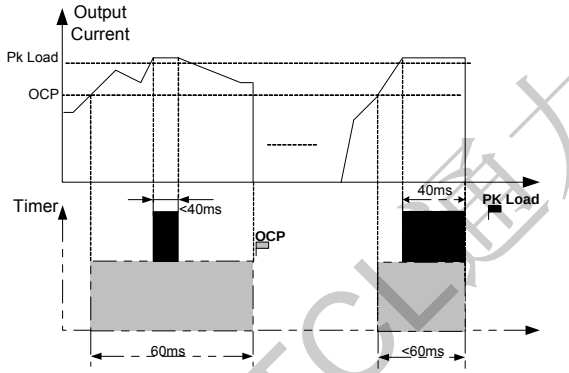


Fig7 Two level OCP Timing

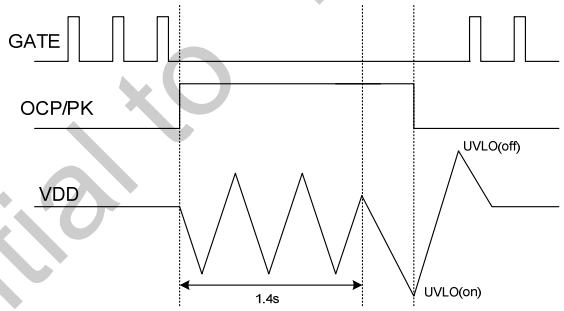


Fig8 Restart Timing when two level OCP occurs

When OCP or peak power protection occurs, no GATE output and VDD begins discharging and charging until the duration is longer than 1.4s(OB2632QCP only). Then VDD begins to drop until to UVLO(on) and later restarts.

Pin Floating and Short Protection

OB2632Q provides PIN floating protection for all the pins and pin short protection for adjacent pins. In the cases when a pin is floating or two adjacent pins are shorted, Gate switching is disabled.

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Intelligent Brown-in and Brown-out protection, AC off detection with X-CAP discharge function(OB2632QCP only)

A precise brown-in and brown-out detection is implemented by monitoring the rectified AC

voltage on HV pin. The final brown in or out threshold is adjusted by the HV resistor in Fig. 9.

$$VHV_{Brow-in/out}(AC) = \frac{(R1 + R2 + 4.2K\Omega) \cdot 70VAC}{200K\Omega + 4.2K\Omega}$$

4.2KΩ is the internal divided programmable resistor of OB2632QCP and its variation is within ±10%. 70VAC Brown-out threshold is obtained by set 200KΩ HV resistor.

The HV pin is also used for AC off detection. When AC is off, the AC off state can be detected through HV pin. Then IC will provide a discharge path from HV pin to GND for the X-CAP discharge. OB2632QCP meets IEC62368-1 requirements.

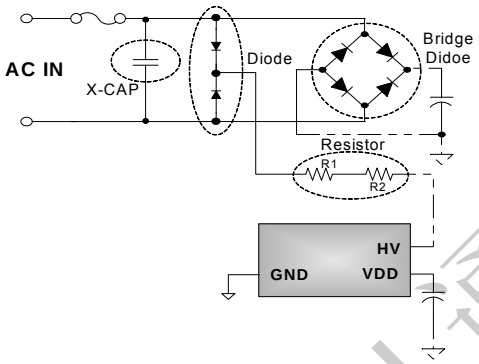


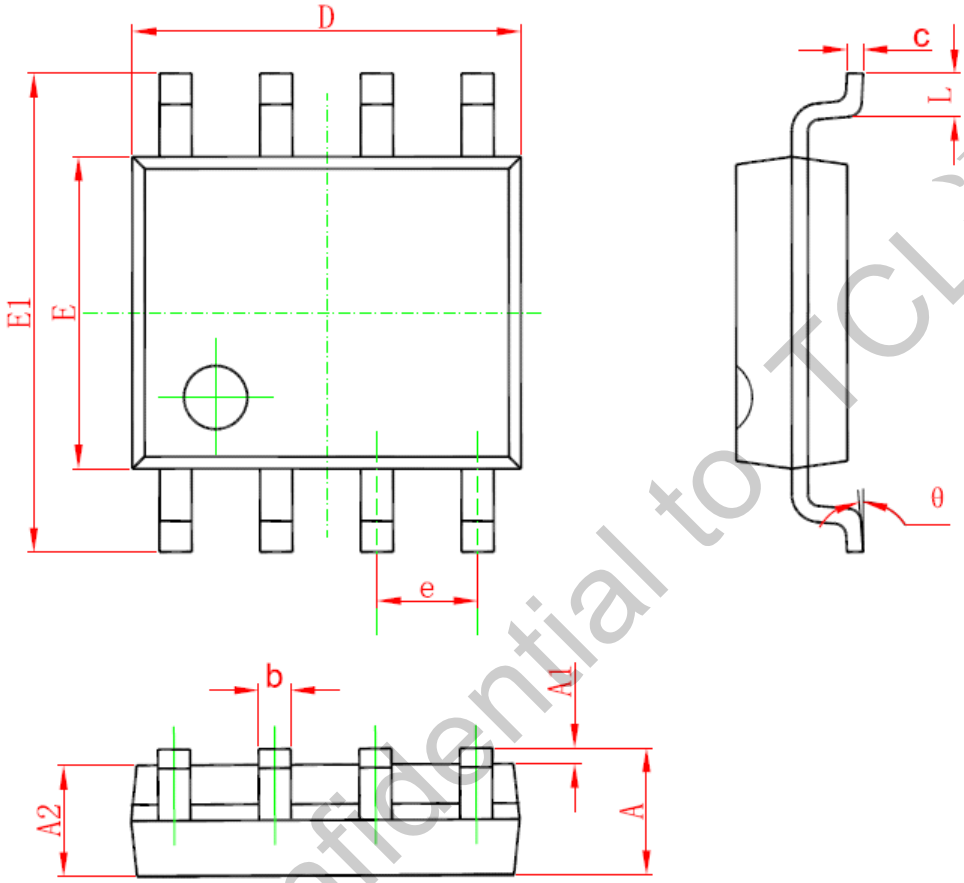
Fig9 X-CAP discharge circuit

Discharge circuit main components selection

Components	Voltage/Current Stress Range
Bridge Diode	600-1000V, 0.5-20A.
Diode	1000V,1A
Resistor(R1,R2)	10K-120Kohm, 1/4W, SMD1206
X-CAP	0.1uF – 2.04uF

PACKAGE MECHANICAL DATA

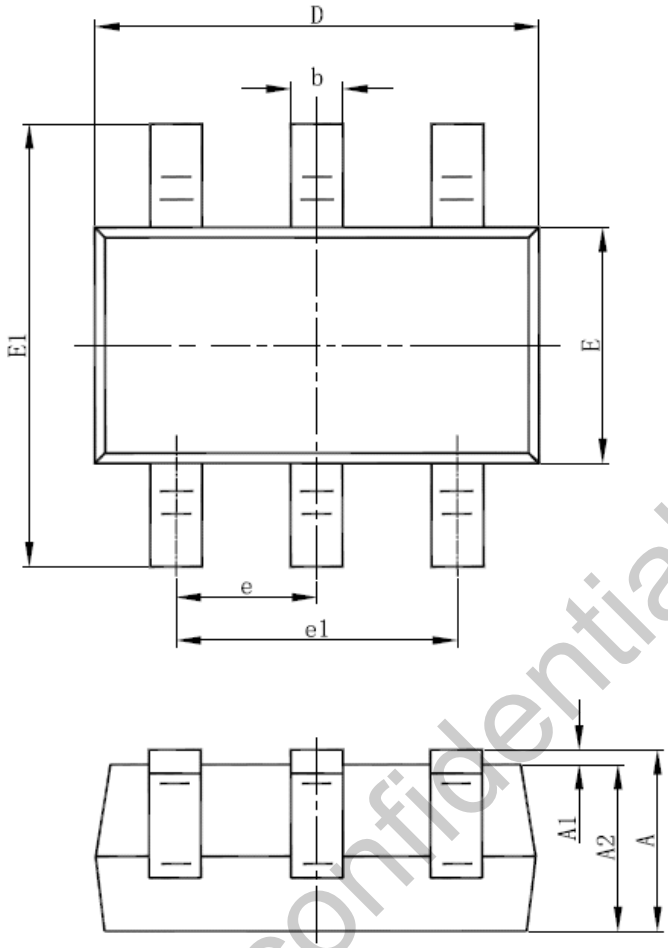
SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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