에이디반도체

TS02N

2-Channel Self Calibration Capacitive Touch Sensor

SPECIFICATION

VER. 1.6

General

The TS02N is 2-Channel capacitive sensor with auto sensitivity calibration. And the supply voltage range is from 2.5 to 5.5V.

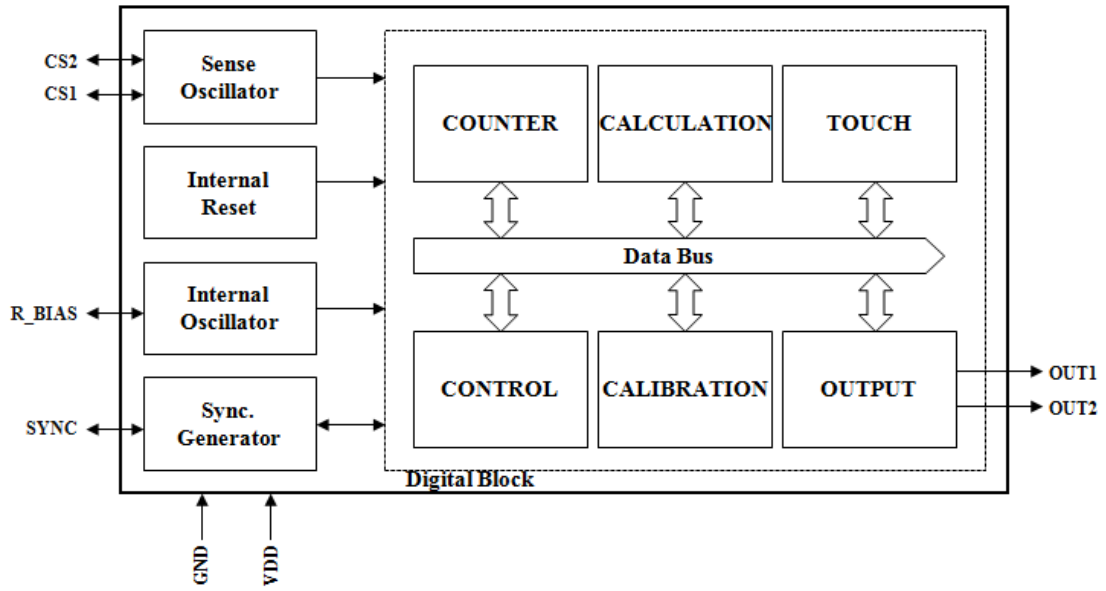
The result of touch sensing can be checked by parallel output port(OUT1 and OUT2).

Over two TS02N can work on the one application at the same time thanks to SYNC function.

Feature

■ 2-Channel capacitive touch sensor with self sensitivity calibration
■ Low power consumption
■ Sync function for parallel operation
■ Adjustable internal clock frequency with external resister
■ Open-drain digital output
■ Embedded noise elimination circuit
■ Embedded Internal power reset circuit
■ RoHS compliant 8SOP package
■ 2.5V to 5.5V operation
■ Typical current consumption 28 uA (@3.3V, R_BIAS 510K Ohm)
■ Typical current consumption 56 uA (@5.0V, R_BIAS 510K Ohm)

Block Diagram



Application

■ Home appliance
■ Membrane switch replacement
■ Human interface for toys & interactive games
■ Sealed control panels, keypads

Ordering Information

Part No.	Package
TS02N	8 SOP

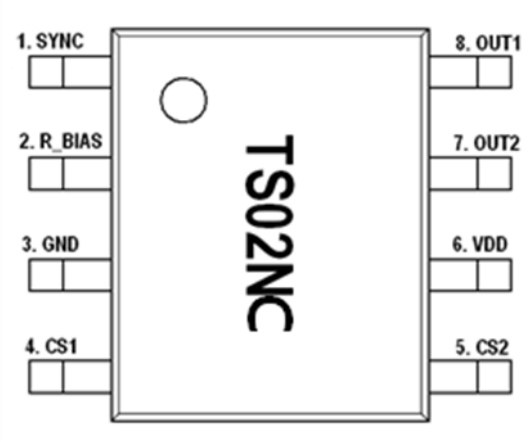
■ Revision History

Rev.	Description of change	Date	Originator
1.0	First creation	06. 07. 26.	KD PARK
1.1	Spec. supplementation	06. 09. 29.	KD PARK
1.2	Mechanical drawing modification	07. 03. 04.	KD PARK
1.3	Additional mechanical drawing modification	07. 04. 06.	KD PARK
1.4	Current consumption modification	17. 06. 16.	CH LEE
1.5	Marking name modification	17. 09. 15.	CH LEE
1.6	Add an overview Revise the Operating Temperature : -20 ~ 75℃ -> -40 ~ 85℃	18. 06. 21.	KD PARK

Content

1 Pin Configuration

1.1 8 SOP



TS02N 8SOP (Drawings not to scale)

2 Pin Description

VDD, GND
Supply voltage and ground pin.

CS1, CS2
Capacitive sensor input pins.

R_BIAS
Internal bias adjust input. Normally 510K-ohm resistor is connected between this port and ground.

SYNC
The IC operation signal output and peripheral IC operation signal input.

OUT1, OUT2
Parallel output ports of CS1 and CS2 respectively. The structure of these parallel output ports is open drain NMOS for active low output level operation.

2.1 Pin Map – 8 SOP

PIN Number	Name	I/O	Description	Protection
1	SYNC	Analog Input	Self sense operation signal output Peripheral sense operation signal input	VDD/GND
2	R_BIAS	Analog Input	Internal bias adjust input	VDD/GND
3	GND	Ground	Supply ground	VDD
4	CS1	Analog Input	Sense channel 1	VDD/GND
5	CS2	Analog Input	Sense channel 2	VDD/GND
6	VDD	Power	Power (2.5V ~ 5.0V)	GND
7	OUT2	Digital Output	Ch2 touch detect output Open drain output (Active Low)	VDD/GND
8	OUT1	Digital Output	Ch1 touch detect output Open drain output (Active Low)	VDD/GND

3 Absolute Maximum Rating

Supply voltage	5.5 V
Maximum voltage on any pin	VDD+0.3 V
Maximum current on any PAD	100mA
Continuous power Dissipation	800mW
Storage Temperature	-50 ~ 150℃
Operating Temperature	-40 ~ 85℃
Junction Temperature	150℃

Note Unless otherwise noted, all above are operated in normal temperature

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	3500V	VDD
		6250V	VSS
		8000V	P to P
M.M	Pos / Neg	700V	VDD
		700V	VSS
		700V	P to P
C.D.M	Pos / Neg	800V	DIRECT

4.2 Latch-up Characteristics

Mode	Polarity	Max	Test Step
I Test	Positive	200mA	25mA
	Negative	-200mA	
V supply over 5.0V	Positive	8.0V	1.0V

5 Electrical Characteristics

▪ V_{DD}=3.3V, R_B =510k, (Unless otherwise noted), T_A = 25℃

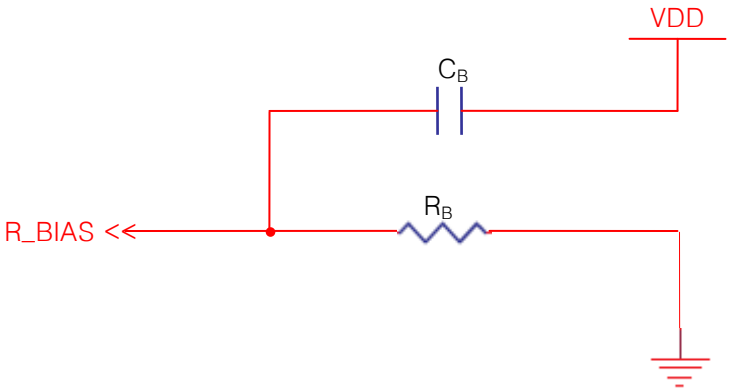
Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.3	5.5	V
Current consumption	I_{DD}	V_{DD}= 3.3V R_B=510k	-	28	52	μA
		V_{DD}= 5.0V R_B=510k	-	56	105	
Output maximum sink current	I_{OUT}	T_A = 25℃	-	-	4.0	mA
Sense input capacitance range Note1	C_{S1} C_{S2}		-	10	100	pF
Sense input resistance range	R_S		-	200	1000	Ω
Minimum detectable capacitance difference	ΔC	C_S = 10pF	0.2	-	-	pF
Output impedance (open drain)	Zo	ΔC > 0.2pF	-	12	-	Ω
		ΔC < 0.2pF	-	30M	-	
Self calibration time after power on	T_{CAL}	V_{DD} = 3.3V R_B = 510k	-	100	-	ms
		V_{DD} = 5.0V R_B = 510k	-	80	-	
Recommended bias resistance range Note2	R_B	V_{DD} = 3.3V	200	510	820	kΩ
		V_{DD} = 5.0V	330	620	1200	
Maximum bias capacitance	C_{B_MAX}		-	820	1000	pF
Recommended sync resistance range	R_{SYNC}		1	2	20	MΩ

Note 1: The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

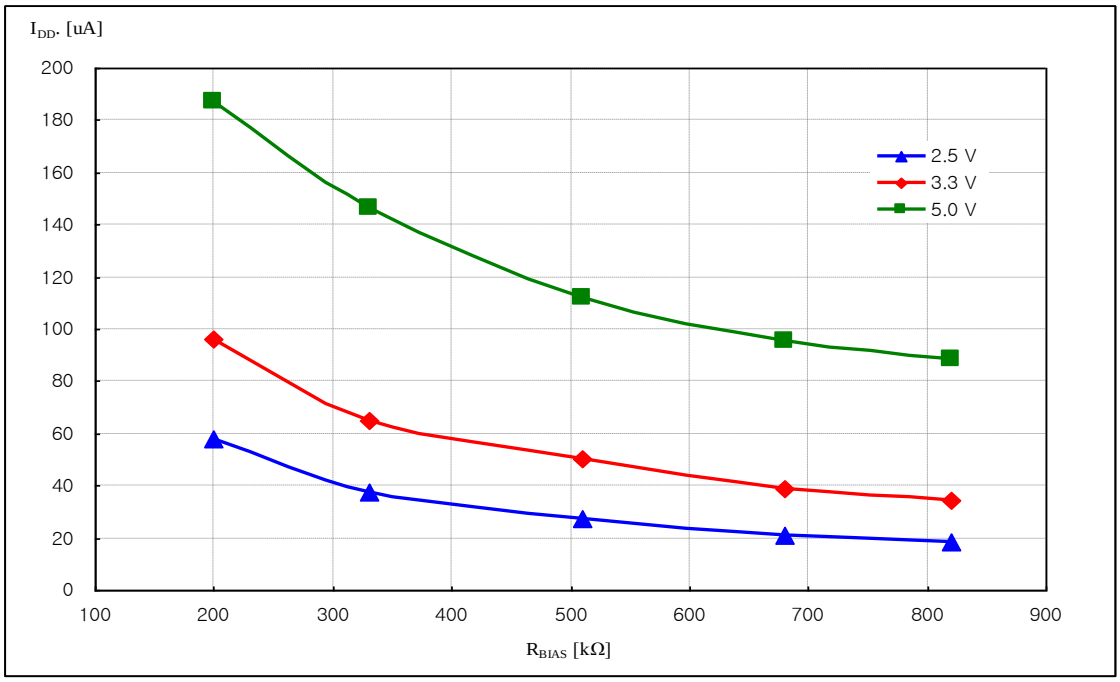
Note 2: The lower R_B is recommended in noisy condition.

6 Implementation of TS02N

6.1 R_BIAS implementation



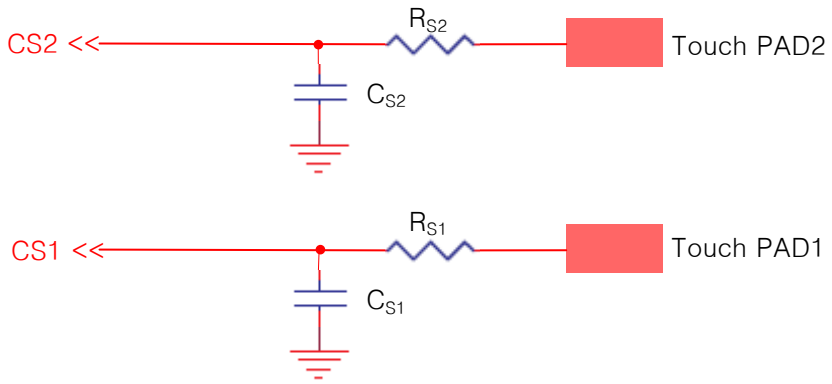
The R_BIAS is connected to the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore able to be adjusted with R_B. A voltage ripple on R_BIAS can make critical internal error, so C_B connected to the VDD (not GND) is recommended. (The typical value of C_B is 820pF and the maximum Value is 1nF.)



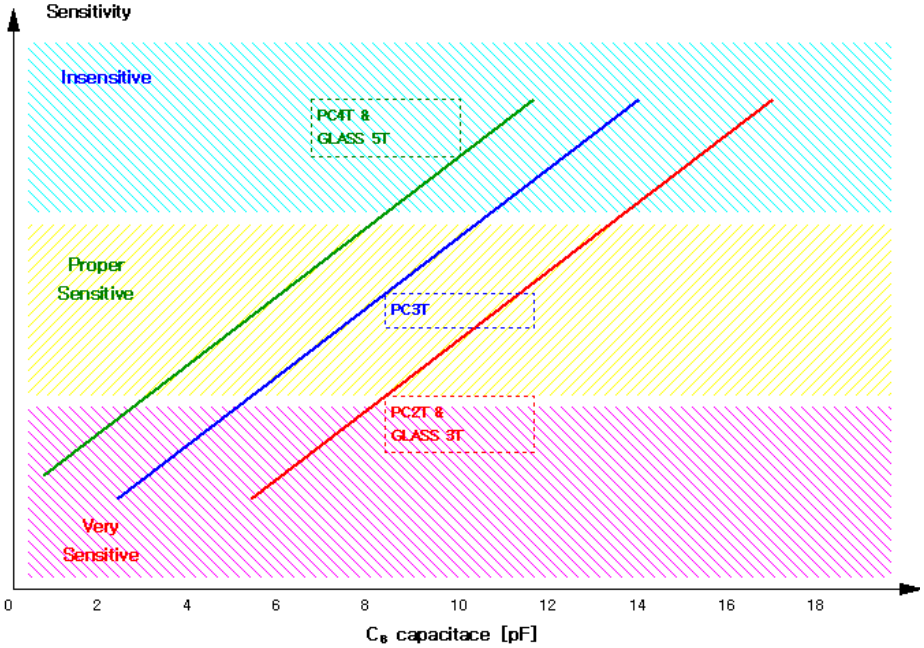
Current consumption curve

The current consumption curve of TS02N is represented in accordance with R_B value as above. The lower R_B requires more current consumption but it is recommended in noisy application. For example, refrigerator, air conditioner and so on.

6.2 CS implementation



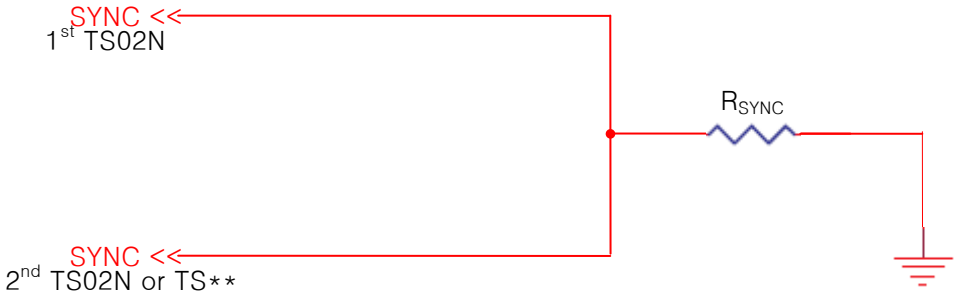
The parallel capacitor C_{S2} is added to CS2 and C_{S1} to CS1 to adjust sensitivity. The sensitivity will be increased when smaller value of C_{S2} and C_{S1} are used. (Ref. below Sensitivity Example Figure) It could be useful in case detail sensitivity mediation is required. The TS02N has two independent touch sensor input CS1 and CS2. Internal touch decision processes of CS1 and CS2 are separated from each other. Therefore two channel touch key board can be designed by using only one TS02N. R_{S1} and R_{S2} are serial connection resistors to avoid mal-function from external surge and ESD. From 200Ω to 1kΩ is recommended for R_{S1} and R_{S2} values. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 and CS2 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.



Sensitivity Example Figure

6.3 SYNC implementation

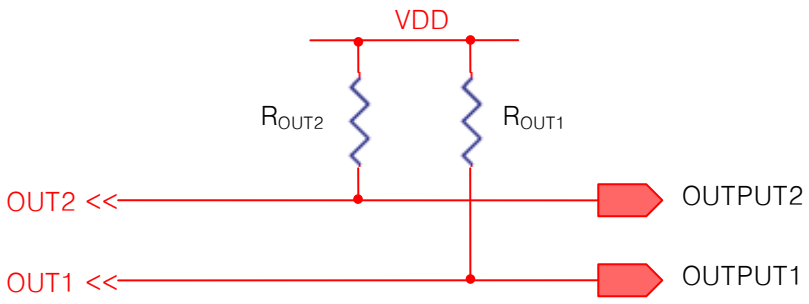
Over two TS02N can work on the one application at the same time thanks to SYNC function with this pin. The SYNC pulse prevents over two sensing signal from interfering with each other. R_{SYNC} is pull-down resistor of SYNC pin. Too big value of R_{SYNC} makes the SYNC pulse falling delay, and too small value of R_{SYNC} makes rising delay. Typical value of R_{SYNC} is 2MΩ.The Sync pin should be implemented as below. TS02N also can be used with the other TSxx series by employing this SYNC function.
The SYNC pin should be tied to GND in case of low sensitivity application. In this case, the sensitivity will be decreased with an half of that in normal use and the SYNC function is not available.



SYNC pin option

Connection	Operation
R_{SYNC} Connection	Normal SYNC operation with the other TSXX series / High Sensitivity Application
GND	No SYNC / Low Sensitivity Application
VDD	Forbidden

6.4 OUTPUT implementation

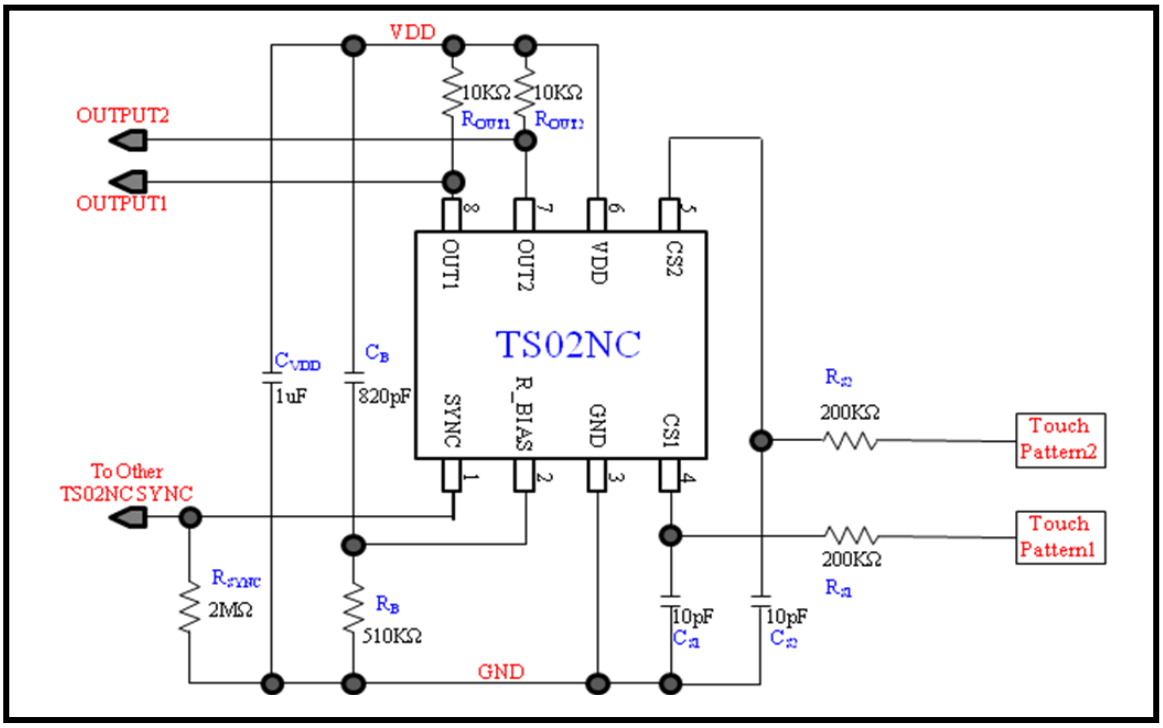


The OUT1 and OUT2 have open drain output structure. For this reason, the connection of pull-up resistor R_{OUT} is required between OUT1, OUT2 and VDD. The maximum output sink current is 4mA, so over a few kΩ must be used as R_{OUT1} and R_{out2}. Normally 10kΩ is used as R_{OUT1} and R_{out2}. The reset value of OUT1 and OUT2 is high in normal situation, and the value is low when a touch is detected on CS1 or CS2.

7 Recommended Application

Two channel touch key board can be designed by using only one TS02N. The TS02N is embedded intelligent internal power reset circuit that makes possible to save circuit cost because of reducing external components for reset.

The sensitivity calibration operation can help to prevent abnormal detection caused by external noise, temperature variation, and supply voltage drop.

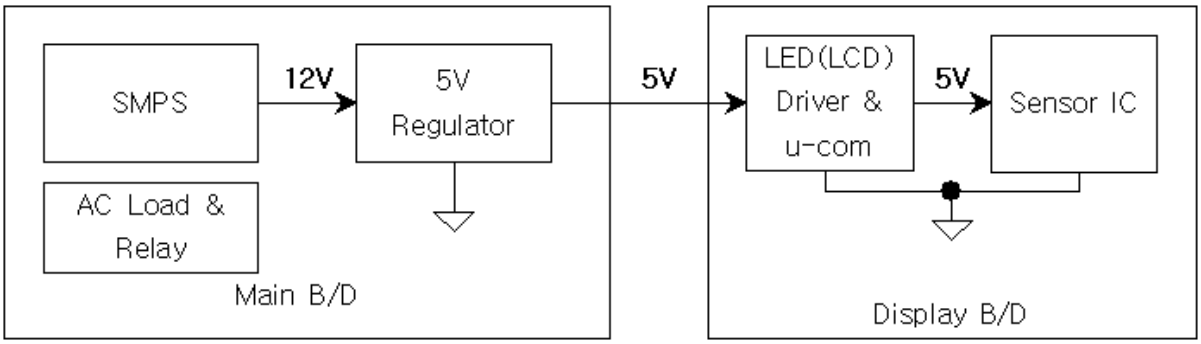


TS02N Application Example Circuit

- VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- When TS02N used in noisy environment, Lower R_B is recommended.
- In PCB layout, R_B should not be placed on touch pattern. If not, C_B has to be connected. The R_B pattern should be routed as short as possible.
- The C_S pattern also should be routed as short as possible and the width of line might be about 0.25mm.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS02N.
- The C_S pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency

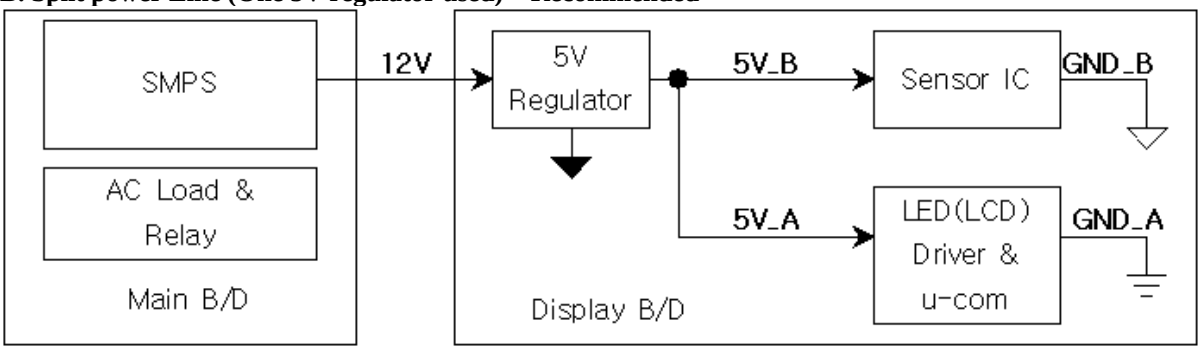
7.1 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

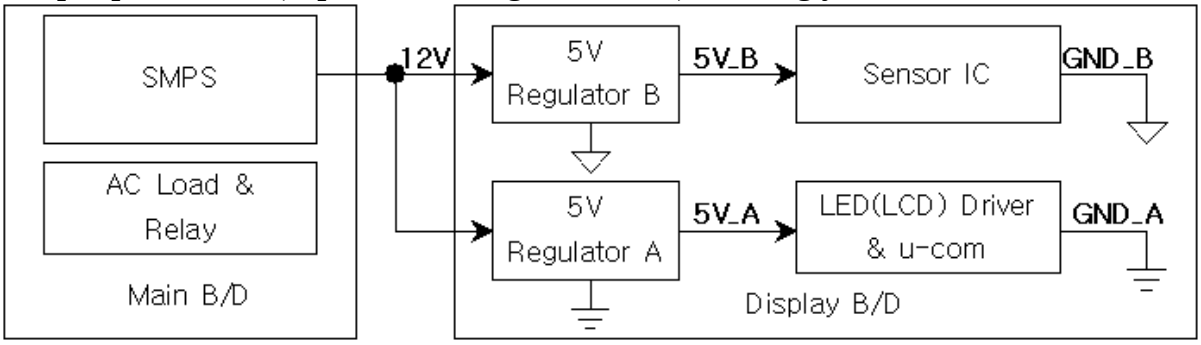


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

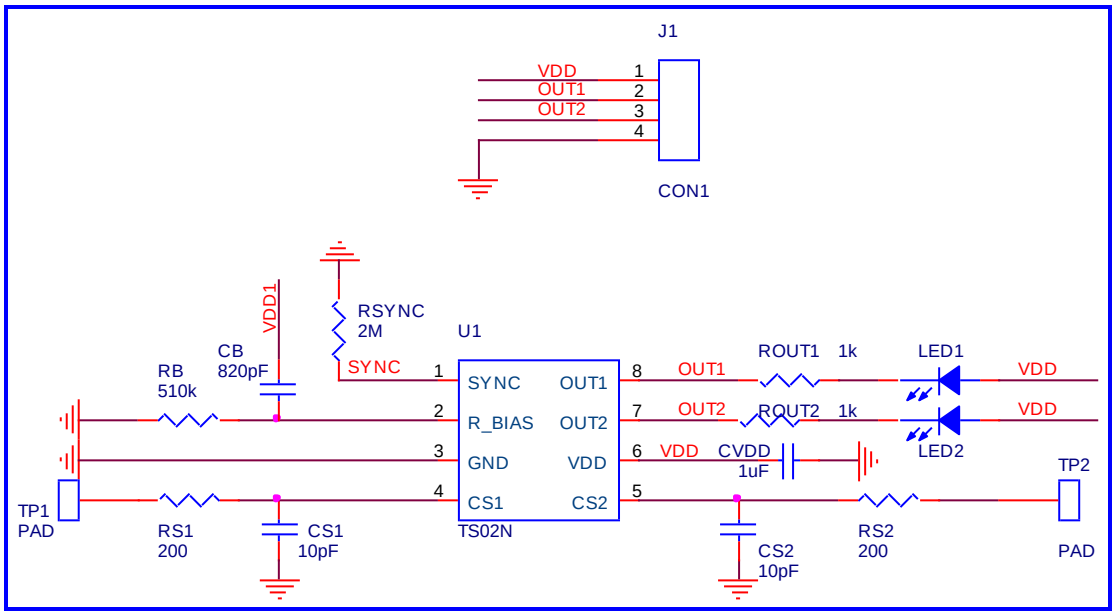
B. Split power Line (One 5V regulator used) – Recommended



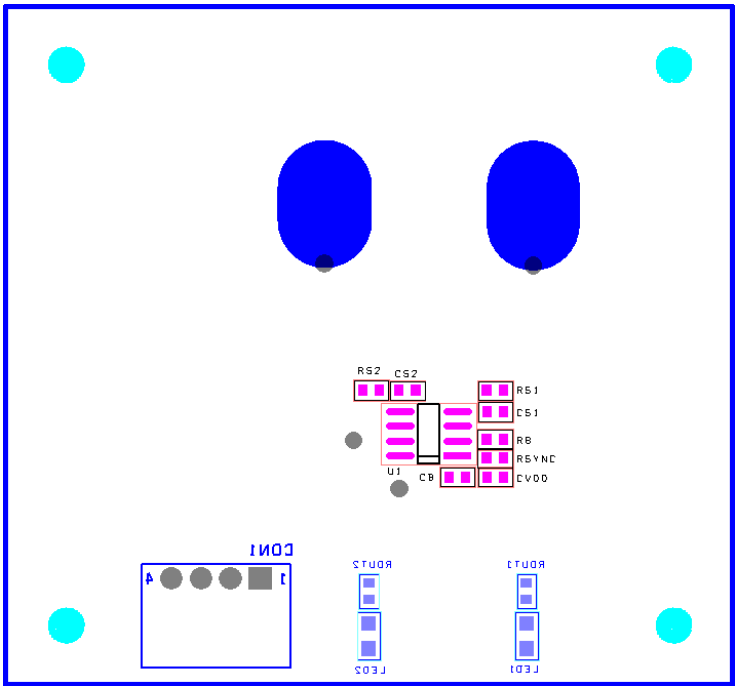
C. Split power Line (Separated 5V regulator used) – Strongly recommended



7.2 Example – PCB Layout (2 Channel Touch button with LED Display)



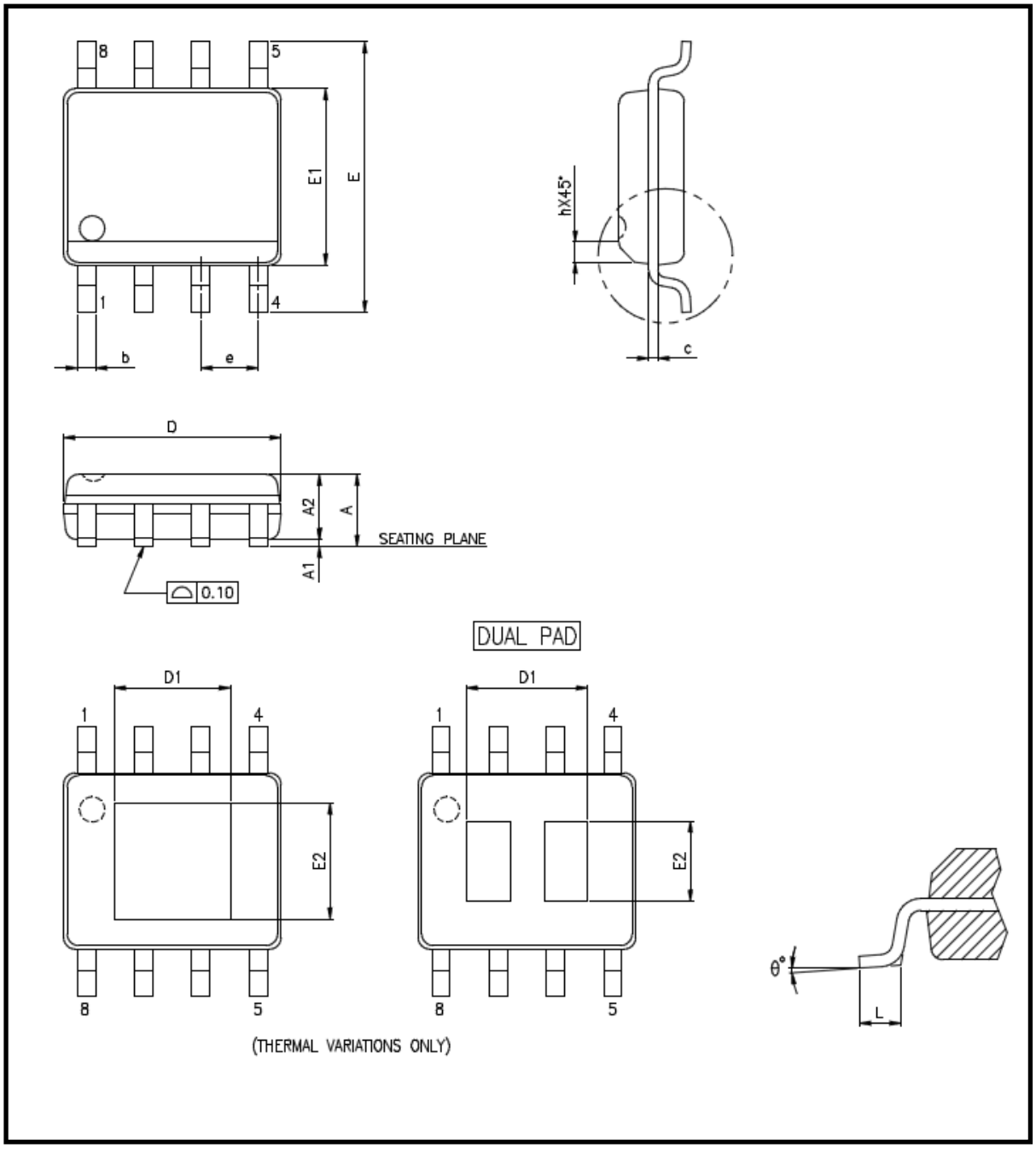
Schematic for PCB layout



Components placement

8 PACKAGE DESCRIPTION

8.1 Mechanical Drawing - GREATEK



	STANDARD		THERMAL	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	-	1.25	-
b	0.31	0.51	0.31	0.51

c	0.10	0.25	0.10	0.25
D	4.90 BSC		4.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θº	0	8	0	8

UNIT : mm

THERMALLY ENHANCED DIMENSIONS

PAD SIZE	**E2**		**D1**	
	MIN.	**MAX.**	**MIN.**	**MAX.**
90X90E	1.94	2.29	1.94	2.29
95X13E	2.05	2.41	2.81	3.30
96X65E (DUAL PAD)	1.78	2.44	2.90	3.56

UNIT : mm

NOTES :

1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
   MS-012 BA REV.F (THERMAL)
2. DIMENSIONS “D” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS “E1” DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

8.2 Marking Description

Device Code : **T S 0 2 NC**

- **NC** → Type of version
- **02** → Channel Number
- **TS** → Touch Switch Group

Weekly Code : **YY ZZ**

- **ZZ** → Manufacturing Week
- **YY** → Manufacturing Year

NOTES:

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