

N-Channel Trench Power MOSFET

General Description

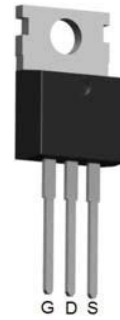
The CS55N50 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching .

Features

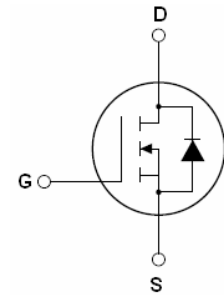
- $V_{DS}=55V$; $I_D=105A@ V_{GS}=10V$;
 $R_{DS(ON)}<6.0m\Omega @ V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



To-220 Top View



Schematic Diagram

$$V_{DS} = 55 V$$

$$I_D = 105 A$$

$$R_{DS(ON)} = 5.0 m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CS55N50	CS55N50	TO-220	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	55	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	105	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	74	A
$I_{DM(pulse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	420	A
dv/dt	Peak Diode Recovery Voltage	6.9	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	147	W
	Derating Factor	0.98	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	625	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=40V, V_G=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	1.02	$^{\circ}C/W$

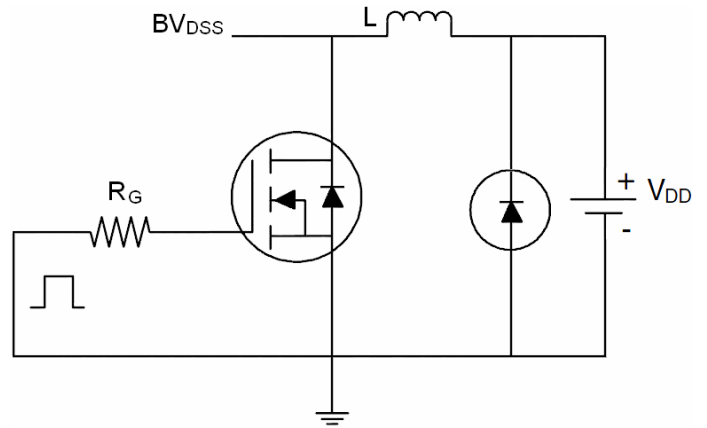
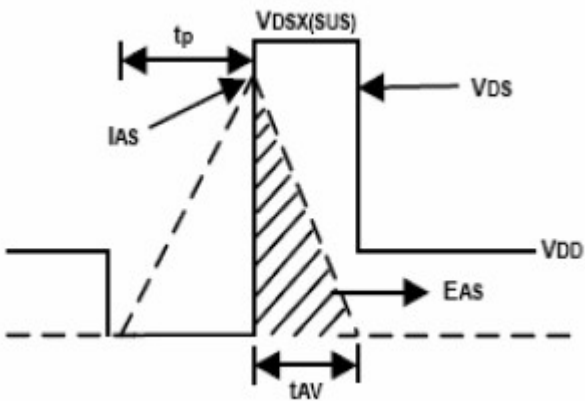
Table 3. Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	55			V
I_{DSS}	Zero Gate Voltage Drain Current($T_C=25^{\circ}C$)	$V_{DS}=55V, V_{GS}=0V$			1	μA
I_{DSS}	Zero Gate Voltage Drain Current($T_C=125^{\circ}C$)	$V_{DS}=55V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$		5.0	6.0	m Ω
Dynamic Characteristics						
g_{FS}	Forward Transconductance	$V_{DS}=25V, I_D=40A$	18			S
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$		4061		PF
C_{oss}	Output Capacitance			485		PF
C_{rss}	Reverse Transfer Capacitance			227		PF
Q_g	Total Gate Charge	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$		91		nC
Q_{gs}	Gate-Source Charge			17		nC
Q_{gd}	Gate-Drain Charge			40		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		27		nS
t_r	Turn-on Rise Time			33		nS
$t_{d(off)}$	Turn-Off Delay Time			67		nS
t_f	Turn-Off Fall Time			34		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-drain Current(Body Diode)			105		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			420		A
V_{SD}	Forward On Voltage ^(Note 1)	$T_J=25^{\circ}C, I_{SD}=40A, V_{GS}=0V$		0.87	0.99	V
t_{rr}	Reverse Recovery Time ^(Note 1)	$T_J=25^{\circ}C, I_F=75A$ $di/dt=100A/\mu s$		32		nS
Q_{rr}	Reverse Recovery Charge ^(Note 1)			49		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

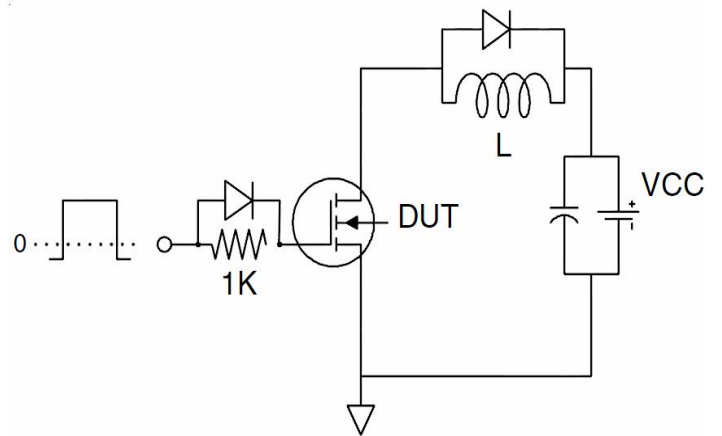
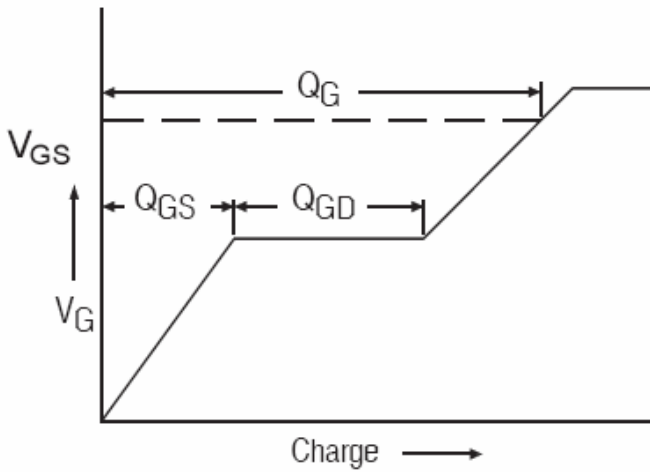
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_{\theta}=25\Omega$, Starting $T_J=25^{\circ}C$

Test Circuit

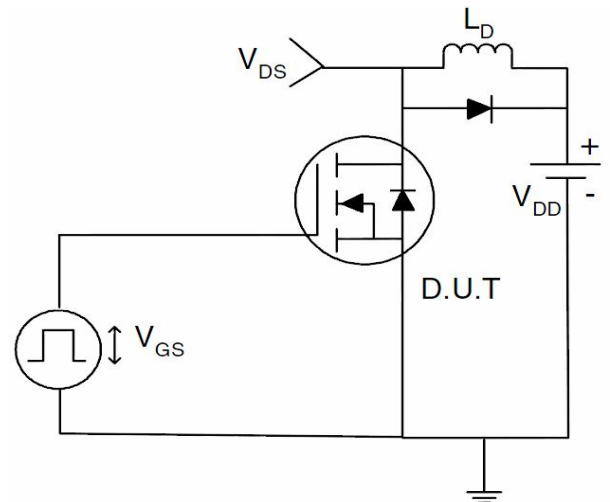
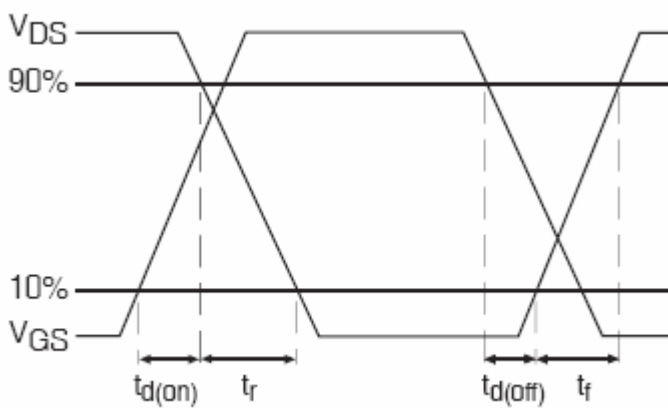
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

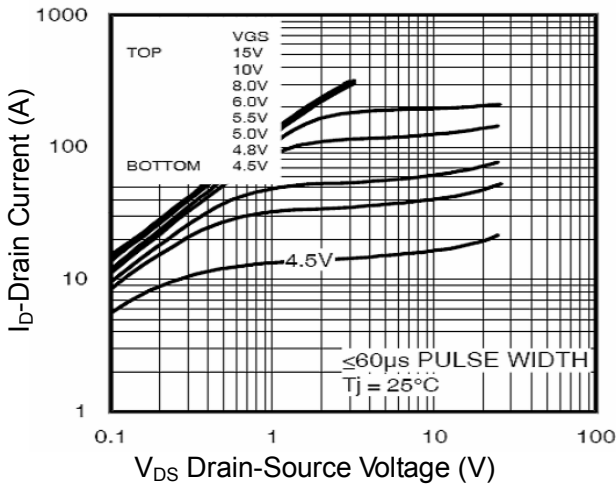


Figure2. Transfer Characteristics

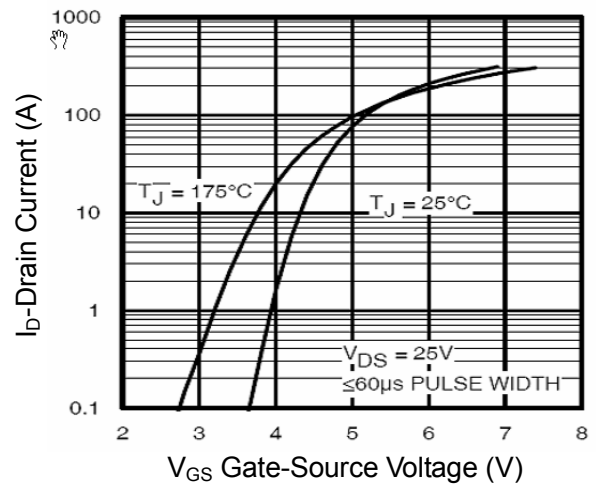


Figure3. ID vs Junction Temperature

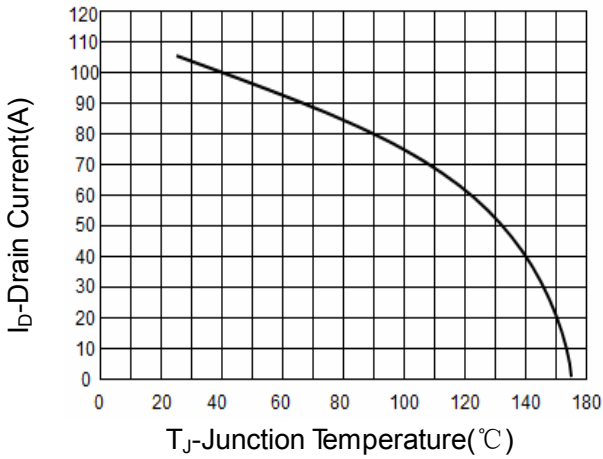


Figure4. Rds(on) Vs Junction Temperature

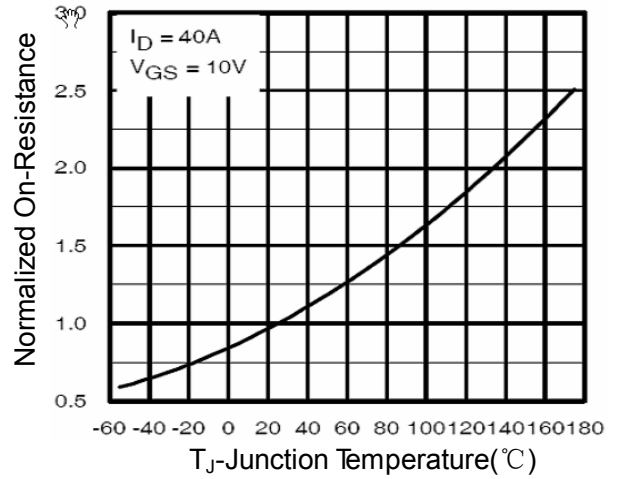


Figure5. BVDS vs Junction Temperature

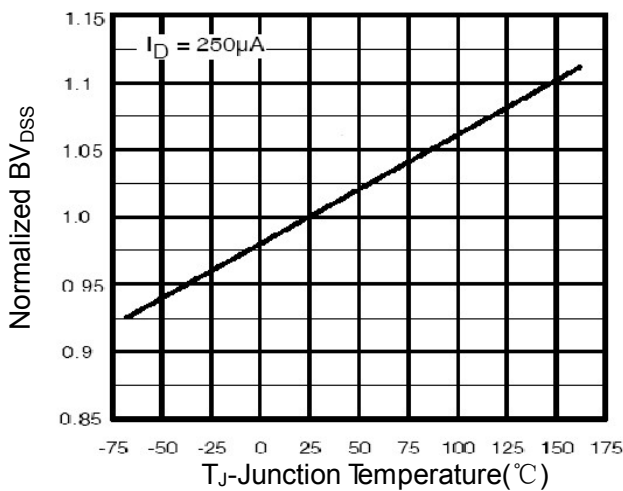


Figure6. VGS(th) vs Junction Temperature

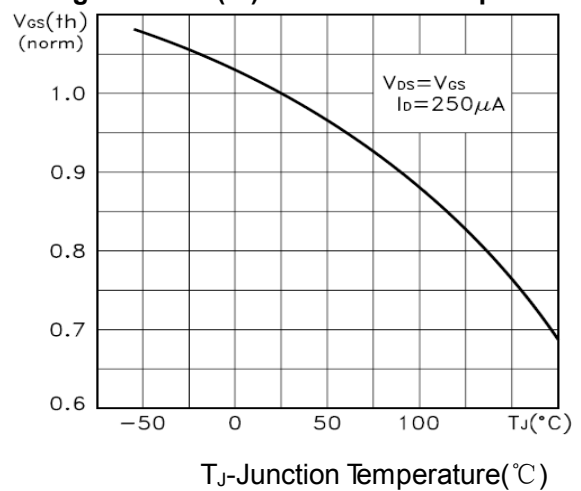


Figure7. Gate Charge

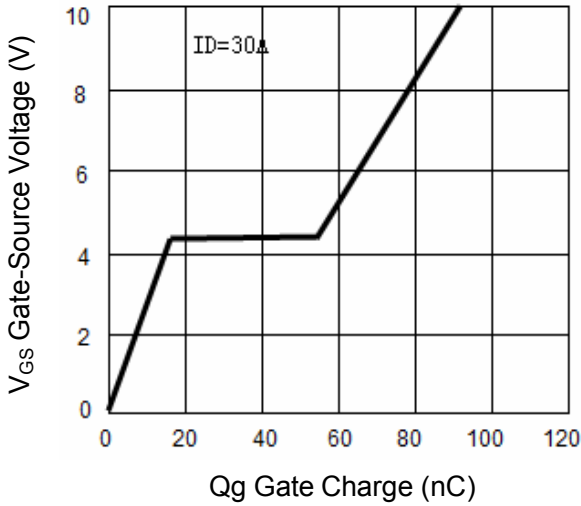


Figure8. Capacitance vs Vds

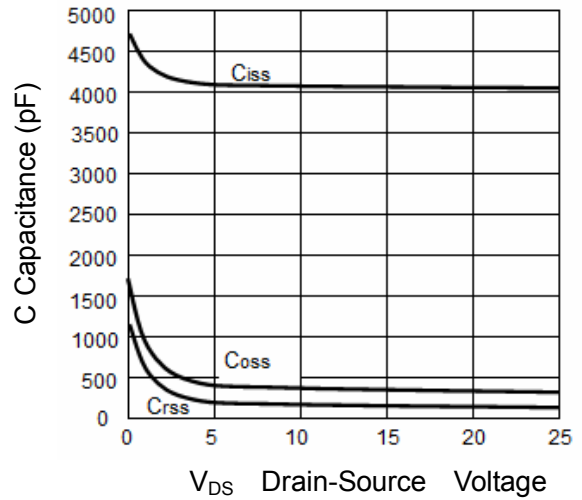


Figure9. Source- Drain Diode Forward

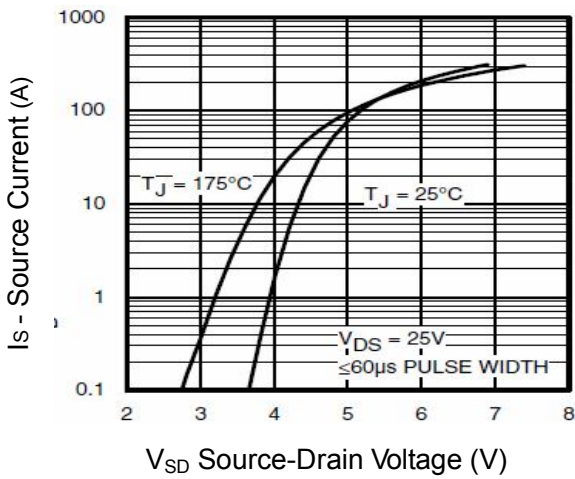


Figure10. Safe Operation Area

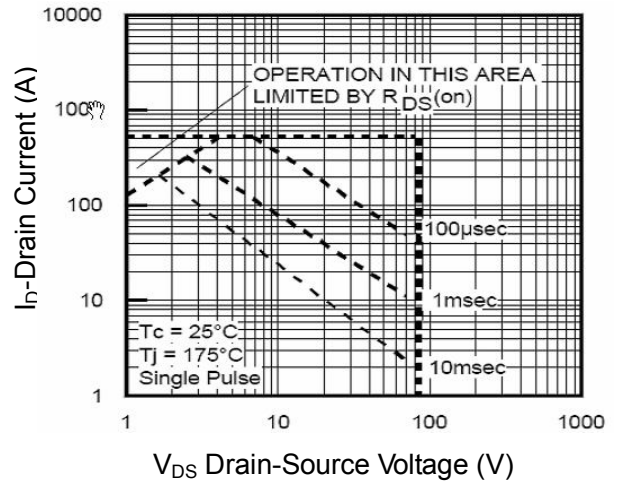
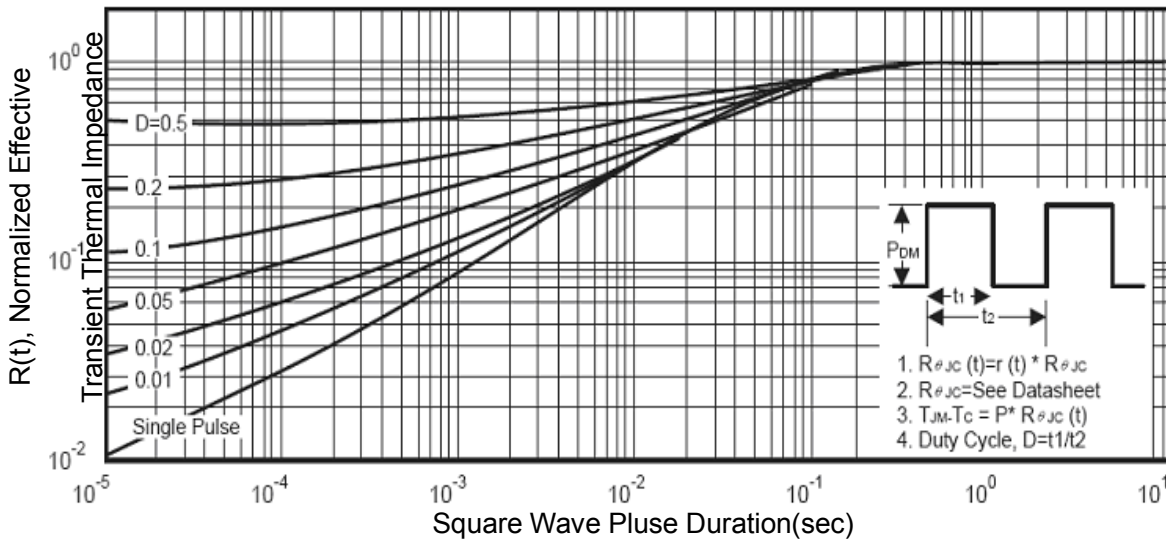
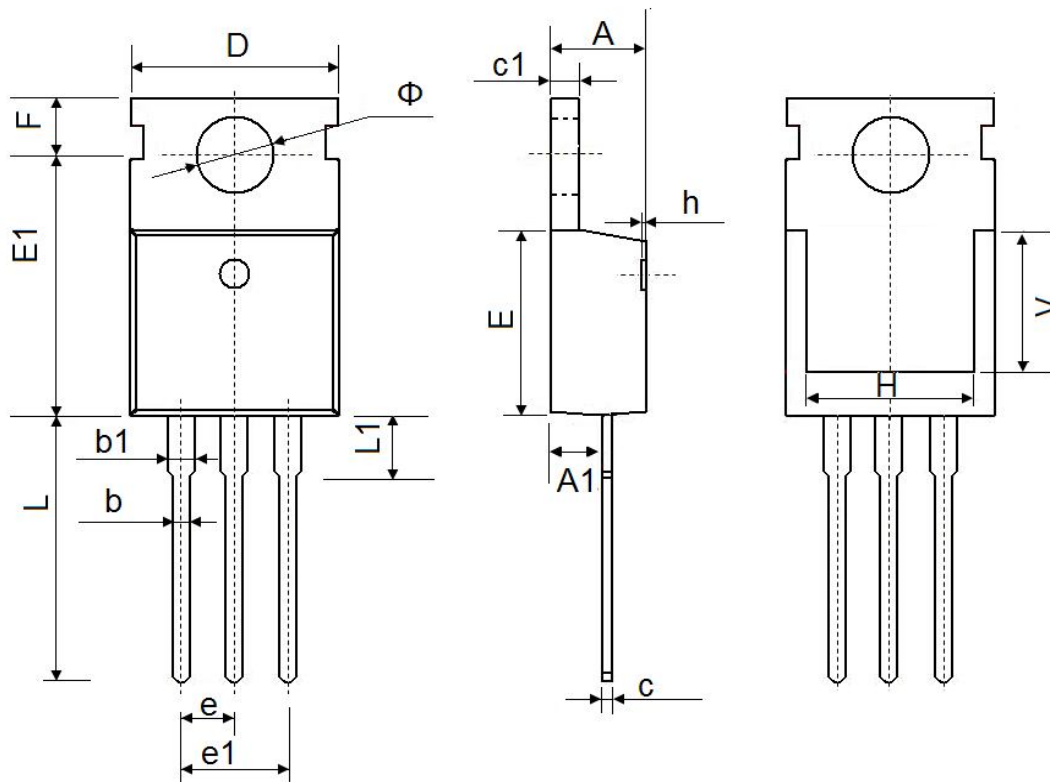


Figure11. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	2.200	2.600	0.087	0.102
b	0.700	0.950	0.028	0.037
b1	1.170	1.410	0.046	0.056
c	0.450	0.650	0.018	0.026
c1	1.200	1.400	0.047	0.055
D	9.600	10.400	0.378	0.409
E	8.8500	9.750	0.348	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.750	14.300	0.502	0.563
L1	2.850	3.950	0.112	0.156
V	7.500 REF.		0.295 REF.	
Φ	3.400	4.000	0.134	0.157