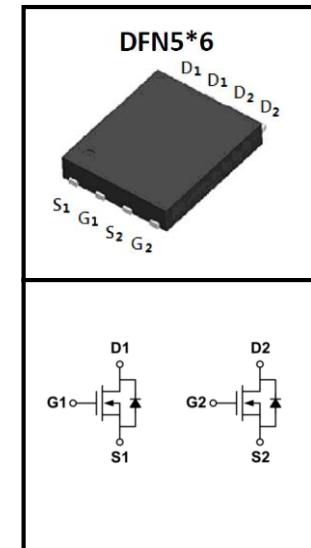


40V N-Channel Trench MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



Device Marking and Package Information

Device	Package	Marking
CTN04NN7P5	DFN5*6	CTN04NN7P5

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	40	V
Drain Current-Continuous($T_c = 25^\circ\text{C}$) (note1)	I_D	65	A
Drain Current-Continuous($T_c = 100^\circ\text{C}$) (note1)		40	
Pulsed Drain Current	I_{DM}	140	A
Gate Source Voltage	V_{GSS}	± 20	V
Power Dissipation $T_c = 25^\circ\text{C}$ (note4)	P_D	1.5	W
Single Pulse Avalanche Energy	Eas	16.3	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance,Junction-ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	$^\circ\text{C/W}$
Thermal Resistance,Junction-to-Ambient	$R_{\theta JA}$	55	$^\circ\text{C/W}$

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 32\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^\circ\text{C}$	--	--	1	uA
Zero Gate Voltage Drain Current		$V_{\text{DS}} = 32\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 55^\circ\text{C}$	--	--	5	
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.2	1.5	2.5	V
Drain-Source On-Resistance (note2)	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 30\text{A}$	--	6.3	7.5	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 20\text{A}$	--	8.5	10	$\text{m}\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1.0\text{MHz}$	--	2332	--	pF
Output Capacitance	C_{oss}		--	193	--	
Reverse Transfer Capacitance	C_{rss}		--	138	--	
Total Gate Charge (4.5V)	Q_g	$V_{\text{DS}} = 20\text{V}, I_D = 20\text{A}, V_{\text{GS}} = 4.5\text{V}$	--	18.8	--	nC
Gate-Source Charge	Q_{gs}		--	4.7	--	
Gate-Drain Charge	Q_{gd}		--	8.2	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = 15\text{V}, I_D = 1\text{A}$ $V_{\text{GS}} = 10\text{V}, R_G = 3.3\Omega$	--	14.3	--	ns
Turn-on Rise Time	t_r		--	2.6	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	77	--	
Turn-off Fall Time	t_f		--	4.8	--	
Body Diode Characteristics						
Source-Drain Current(Body Diode)	I_{SD}		--	--	65	A
Pulsed Source-Drain Current(Body Diode)	I_{SDM}		--	--	140	A
Body Diode Voltage	V_{SD}	$I_{\text{SD}} = 1\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{\text{DD}} = 25\text{V}, V_{\text{GS}} = 10\text{V}, L = 0.1\text{mH}$
4. The power dissipation is limited by 175°C junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

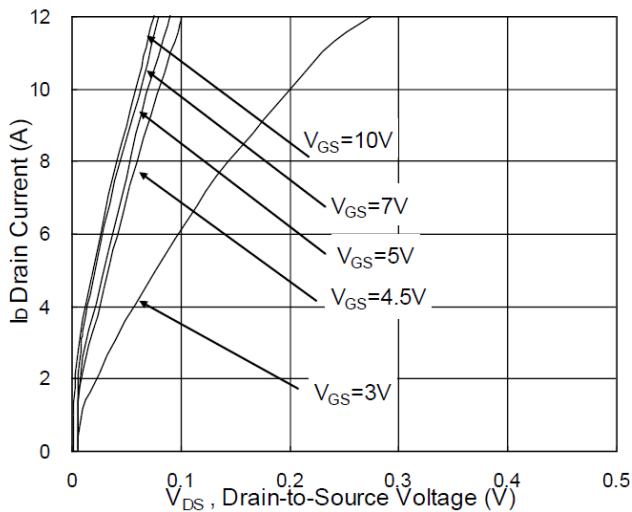


Fig.1 Typical Output Characteristics

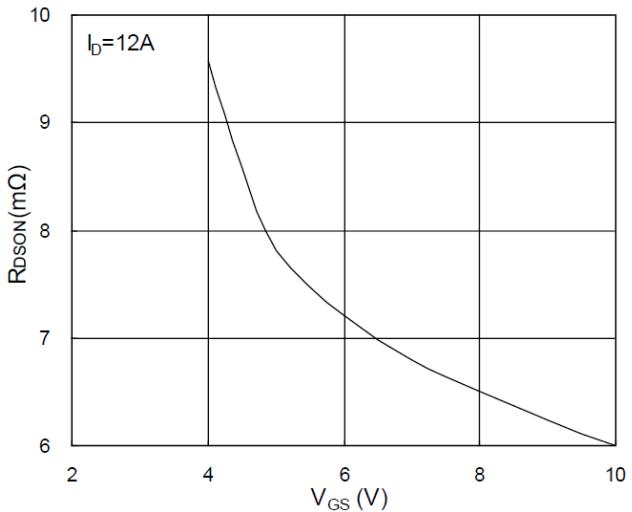


Fig.2 On-Resistance vs. G-S Voltage

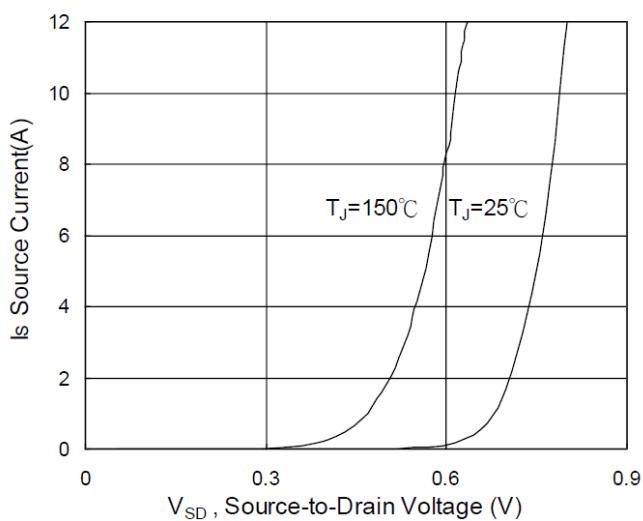


Fig.3 Forward Characteristics Of Reverse

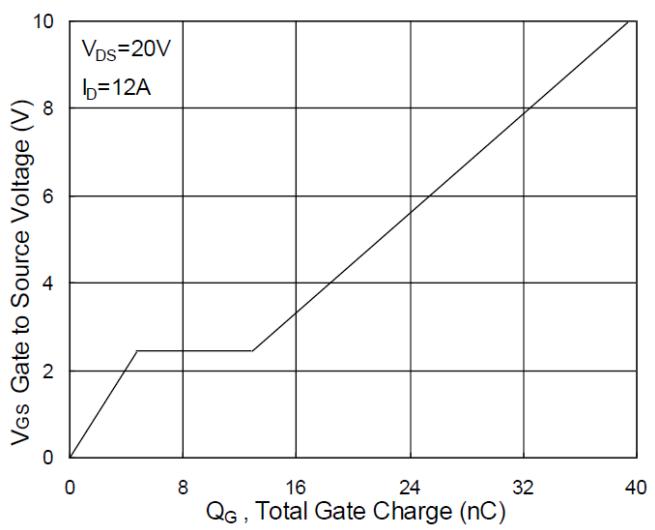


Fig.4 Gate-Charge Characteristics

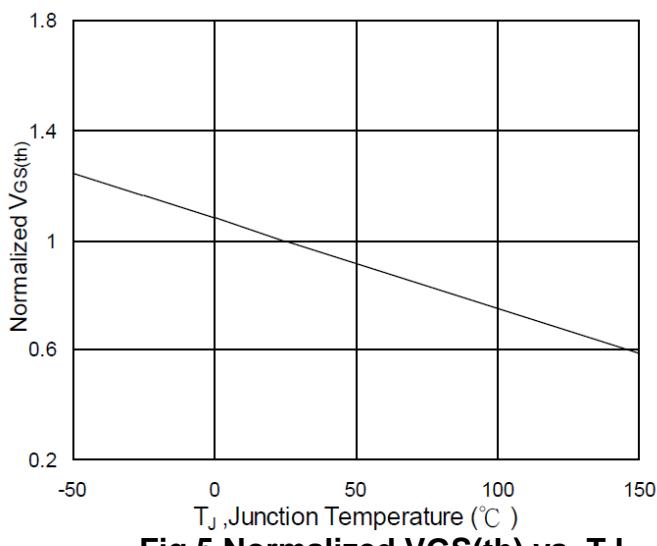


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

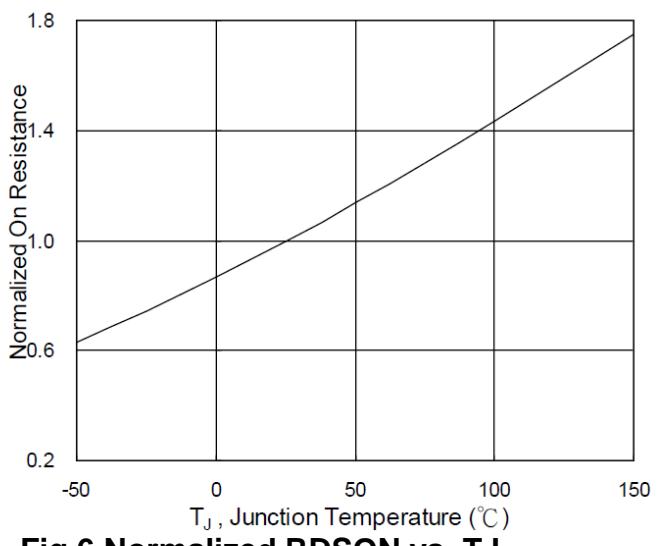


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

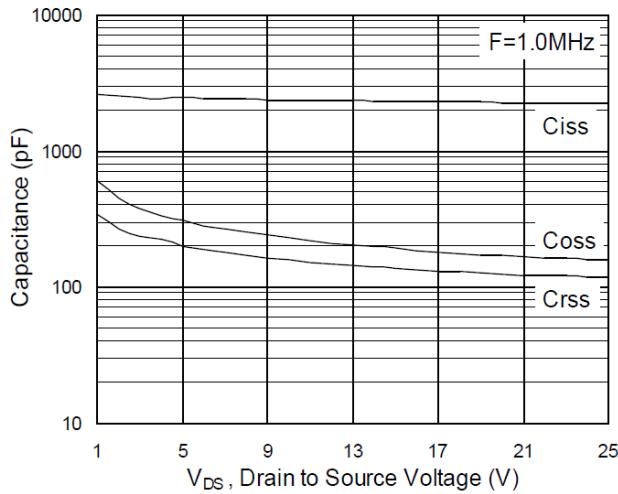


Fig.7 Capacitance

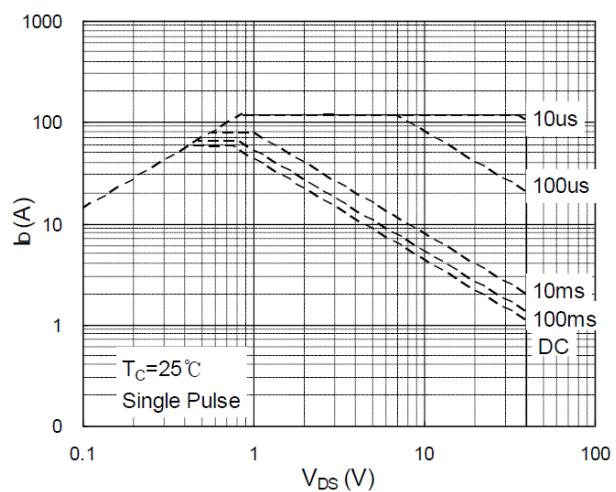


Fig.8 Safe Operating Area

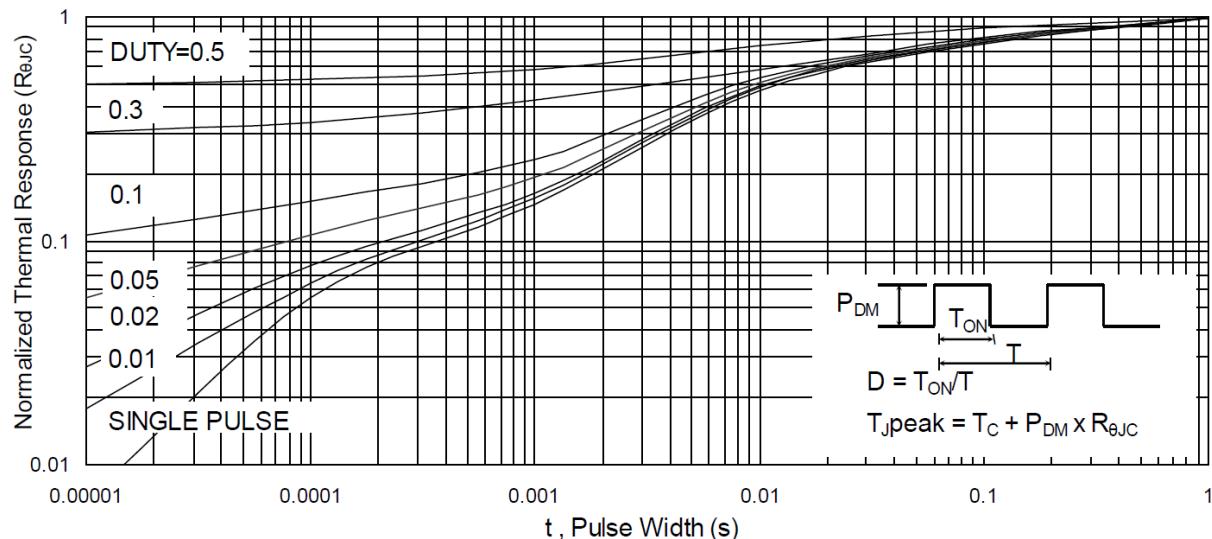
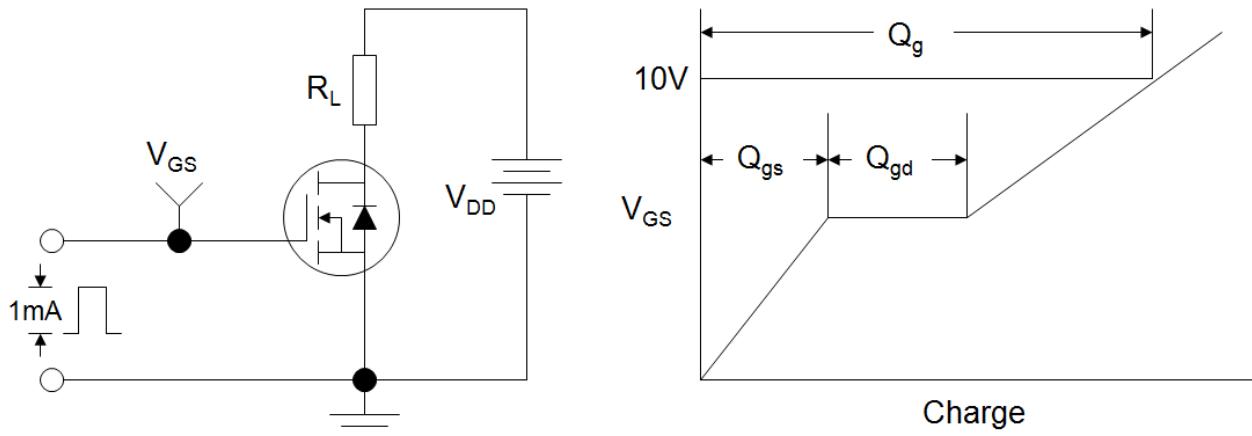
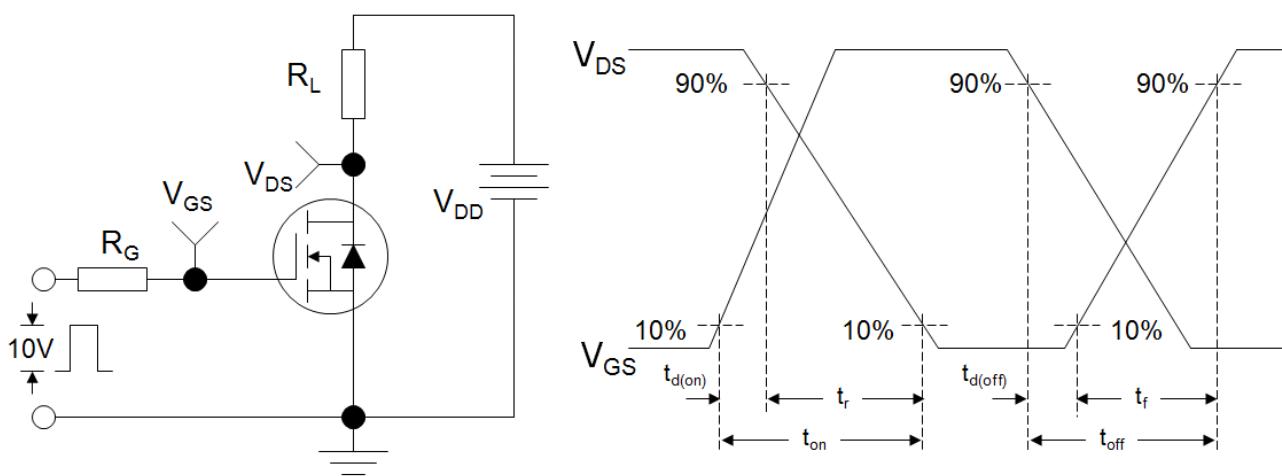
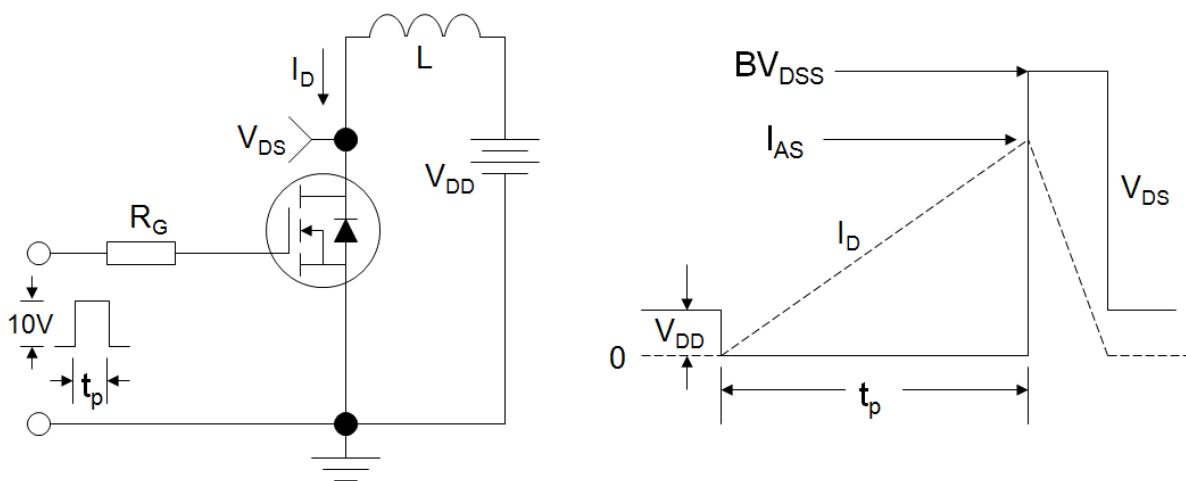
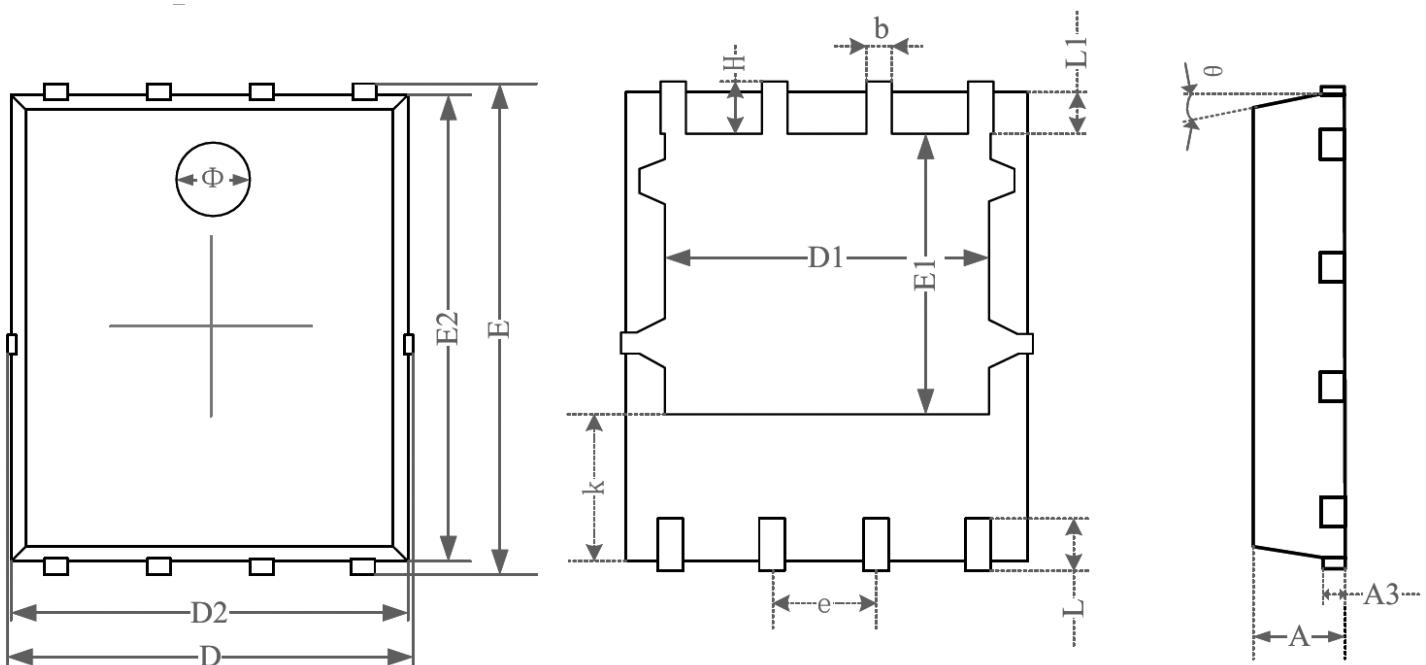


Fig.9 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


DFN5*6



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.870	0.900	0.930	0.034	0.035	0.036	
A3	0.152REF.			0.006REF.			
D	4.944	5.020	5.096	0.195	0.198	0.201	
E	5.974	6.050	6.126	0.235	0.238	0.241	
D1	3.910	4.010	4.110	0.154	0.158	0.162	
E1	3.375	3.475	3.575	0.133	0.137	0.141	
D2	4.870	4.900	4.930	0.192	0.193	0.194	
E2	5.720	5.750	5.780	0.226	0.227	0.228	
k	1.190	1.290	1.390	0.047	0.051	0.055	
b	0.350	0.380	0.410	0.014	0.015	0.016	
e	1.270TYP.			0.050TYP.			
L	0.559	0.635	0.711	0.022	0.025	0.028	
L1	0.424	0.500	0.576	0.017	0.020	0.023	
H	0.574	0.650	0.726	0.023	0.026	0.029	
θ	10°	11°	12°	10°	11°	12°	
Φ	1.150	1.200	1.250	0.045	0.047	0.049	

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