JSMICRO SEMICONDUCTOR

JSM4N65F

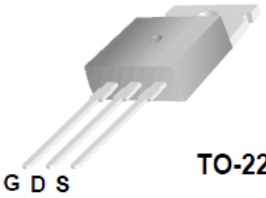
650V N-Channel MOSFET

General Description

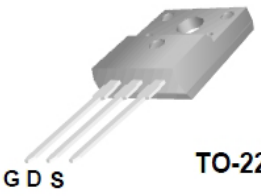
This Power MOSFET is produced using SL semi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters and high efficiency switching for power management in portable and battery operated products.

Features

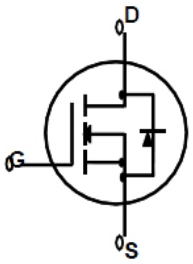
- 4.0A, 650V, $R_{DS(on)}$ = 3.0Ω @V_{GS} = 10 V
- Low gate charge (typical 15nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220



TO-220F



Absolute Maximum Ratings T_C = 25°Cunless otherwise noted

Symbol	Parameter	SLS4N65C	SSS4N65C	Units
			SSS4N65	
V_{DSS}	Drain-Source Voltage		650	V
I_D	Drain Current - Continuous (T_C = 25°C)		4.0	A
I_{DM}	Drain Current - Pulsed (Note 1)		16	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		180	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)		10	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		104	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

* Drain current limited by maximum junction temperature.

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	650	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 520 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.0 A	--	2.5	3.0	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	560	--	pF
C_{oss}	Output Capacitance		--	55	--	pF
C_{rss}	Reverse Transfer Capacitance		--	7	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325 V, I_D = 4.0 A, R_G = 25 Ω (Note 4, 5)	--	10	--	ns
t_r	Turn-On Rise Time		--	40	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	--	ns
t_f	Turn-Off Fall Time		--	50	--	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 4.0 A, V_{GS} = 10 V (Note 4, 5)	--	16	-	nC
Q_{gs}	Gate-Source Charge		--	2.5	--	nC
Q_{gd}	Gate-Drain Charge		--	6.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	16	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 4.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 4.0 A, dI_F / dt = 100 A/μs (Note 4)	--	300	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.0	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 22 mH, I_{AS} = 4.0 A, V_{DD} = 25V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.0 A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

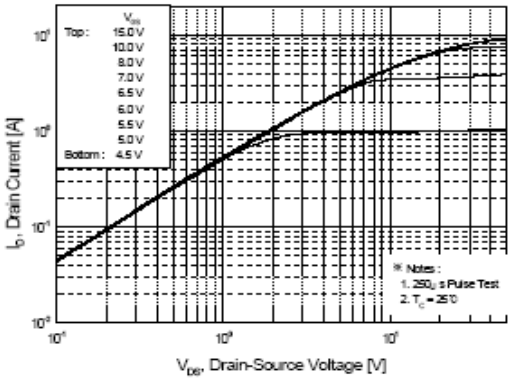


Figure 1. On-Region Characteristics

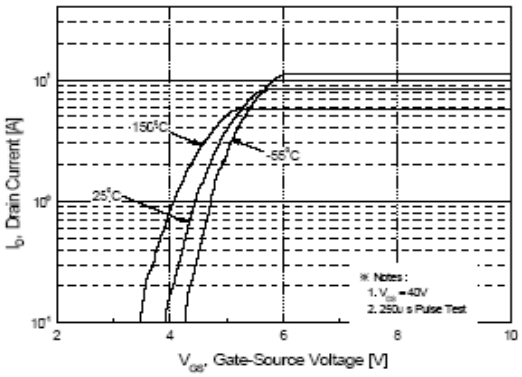


Figure 2. Transfer Characteristics

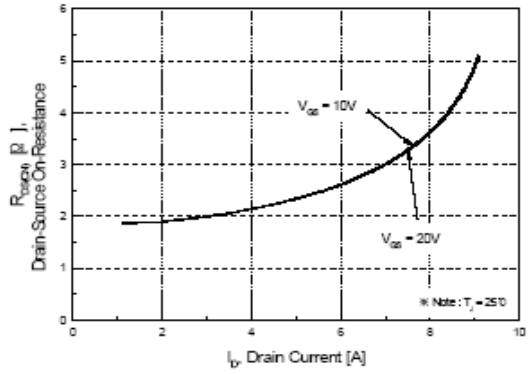


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

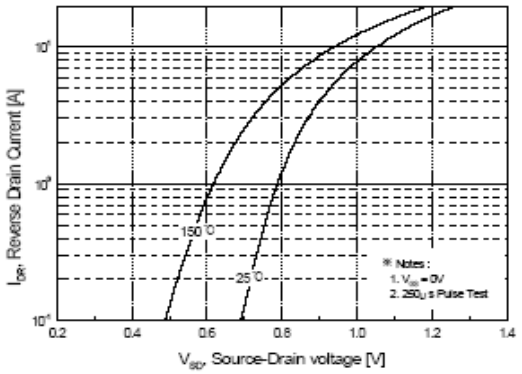


Figure 4. Body Diode Forward Voltage Variation with Source Current

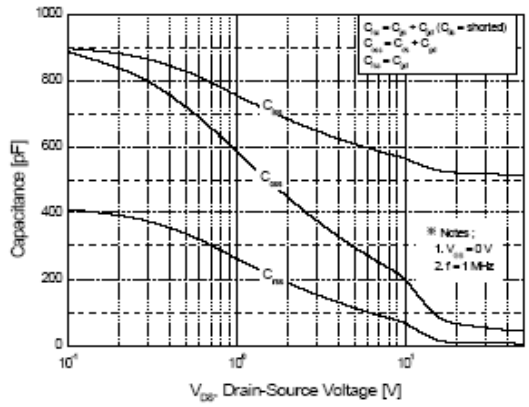


Figure 5. Capacitance Characteristics

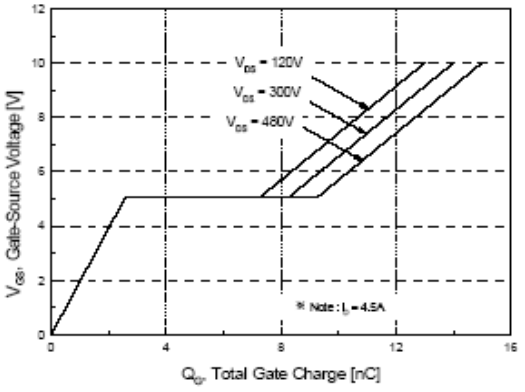


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

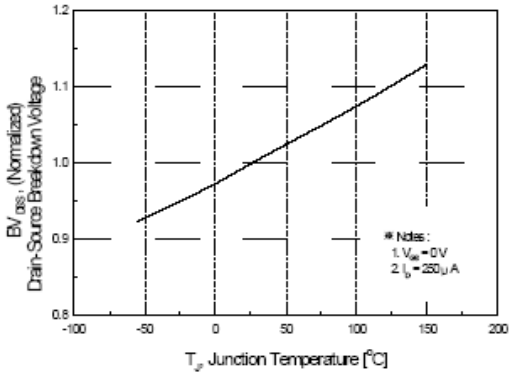


Figure 7. Breakdown Voltage Variation vs Temperature

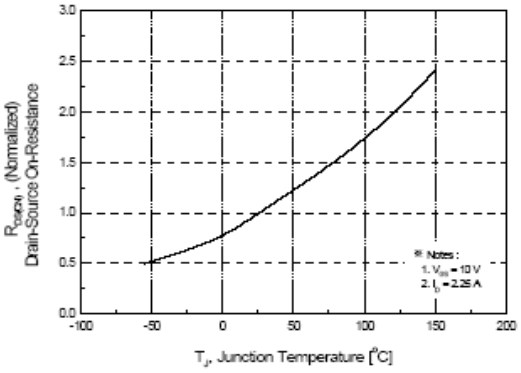


Figure 8. On-Resistance Variation vs Temperature

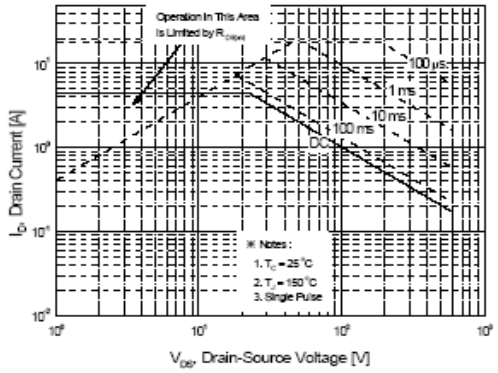


Figure 9-1. Maximum Safe Operating Area for SSS4N65C

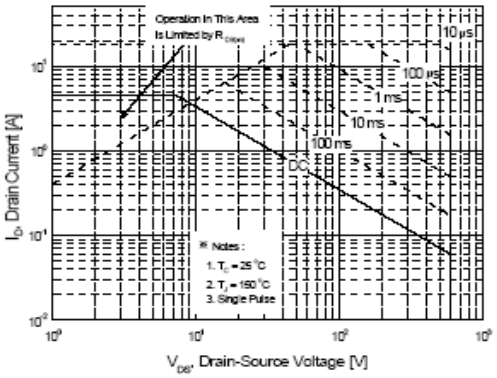


Figure 9-2. Maximum Safe Operating Area for SSS4N65C

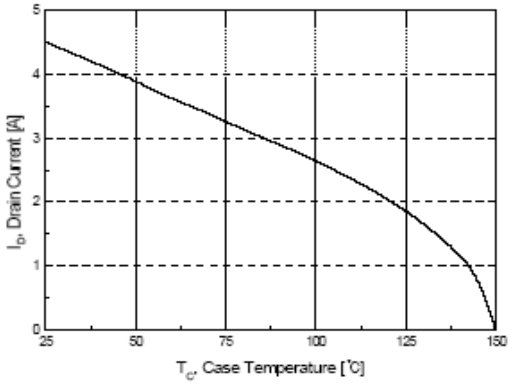


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

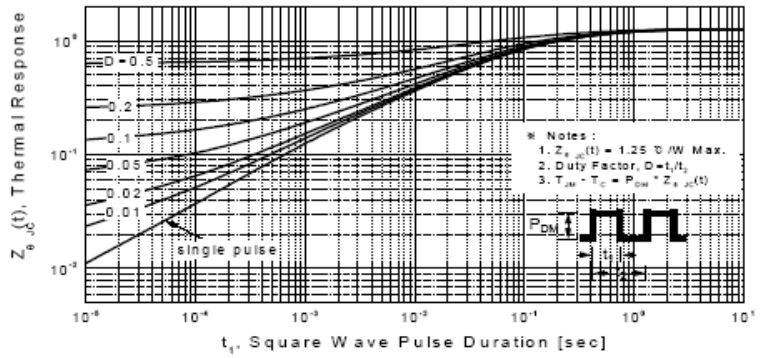


Figure 11-1. Transient Thermal Response Curve for SSS4N65

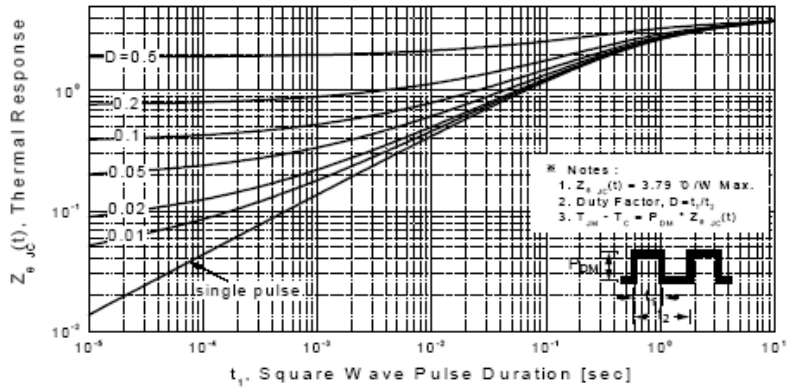
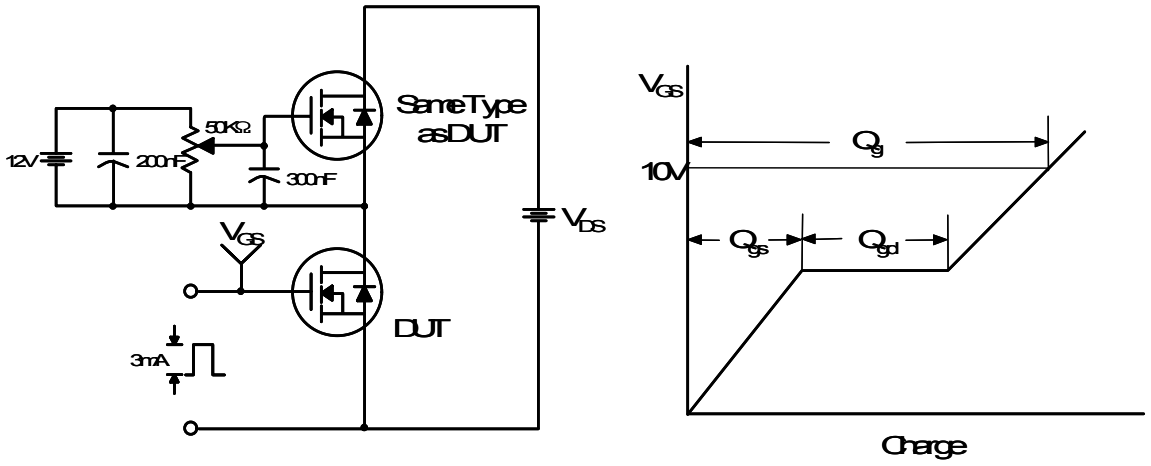
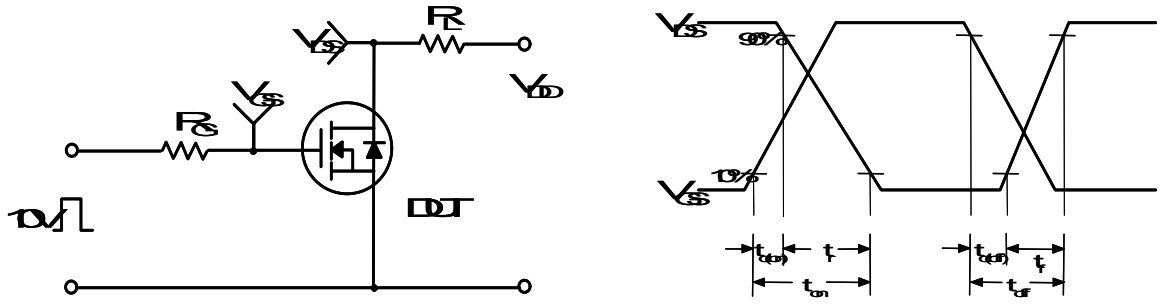


Figure 11-2. Transient Thermal Response Curve for SSS4N65

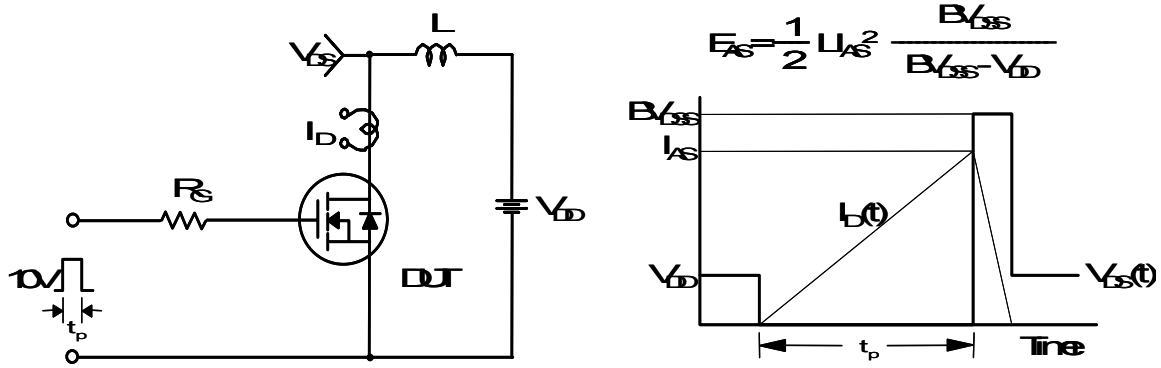
Gate Charge Test Circuit & Waveform



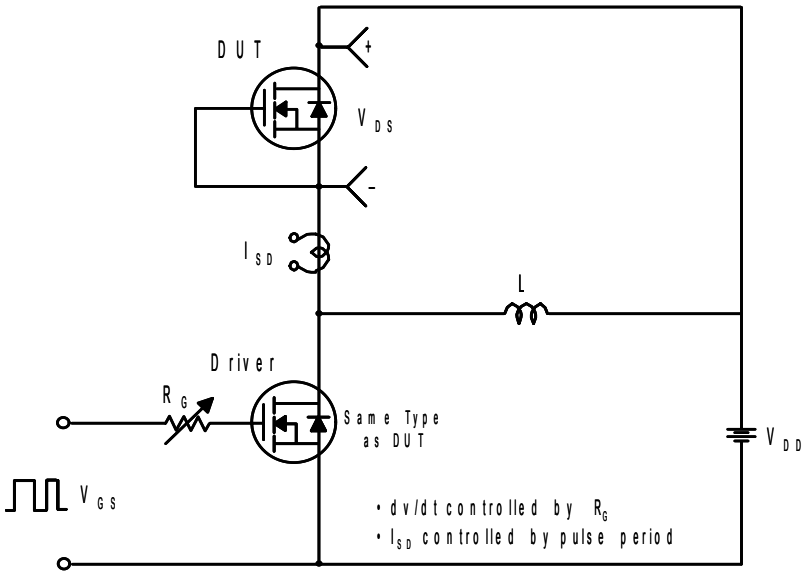
Resistive Switching Test Circuit & Waveforms

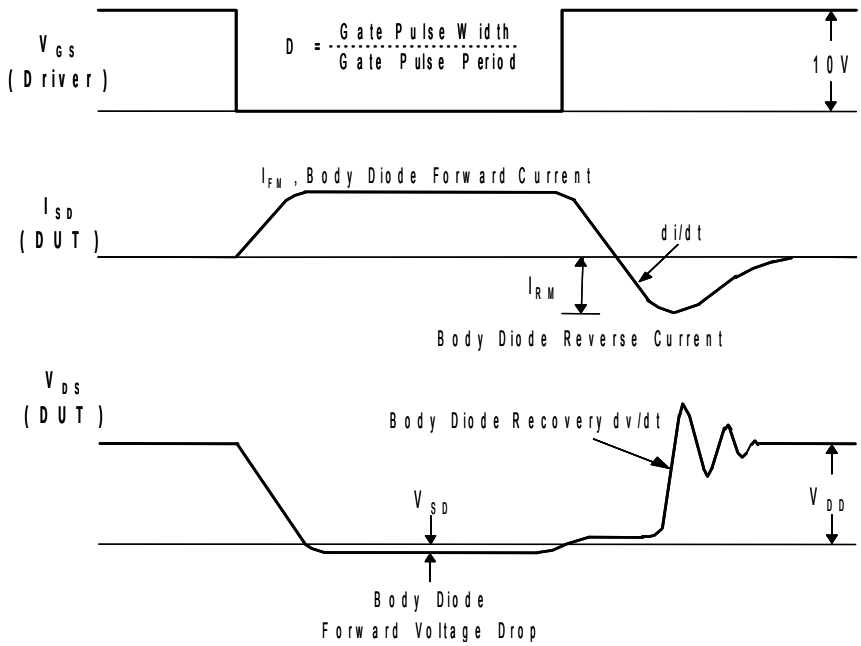


Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

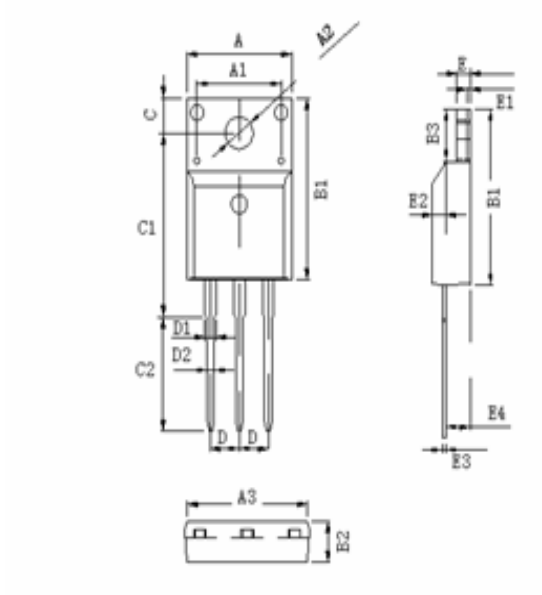




Package Dimensions

TO-220F

TO-220F 外形尺寸图



DIM.	MILLIMETERS	
A	10.03 ± 0.20	
A1	7.00	
A2	3.12 ± 0.10	
A3	9.70 ± 0.20	
B1	15.75 ± 0.20	
B2	4.72 ± 0.20	
B3	6.70 ± 0.20	
C	3.30 ± 0.10	
C1	15.80 ± 0.20	
C2	9.80 ± 0.2	
D	Typical 2.54	
D1	1.47(MAX)	
D2	0.80 ± 0.10	
E	2.55 ± 0.20	
E1	0.70	
E2	1.00×45°	
E3	0.50	+0.1
		-0.05
E4	2.80 ± 0.20	