

MAX14756/MAX14757/ MAX14758

Quad SPST +70V Analog Switches

General Description

The MAX14756/MAX14757/MAX14758 are analog switches with a low on-resistance of 10Ω (max) that conduct equally well in both directions. All devices have a rail-to-rail analog-signal range. They operate with a single +10V to +70V supply in unipolar applications or ±35V dual supplies in bipolar applications. The bipolar supplies can be offset and do not have to be symmetrical.

The MAX14756 is a quad normally closed (NC) single-pole/single-throw (SPST) switch, the MAX14757 is a quad normally open (NO) SPST switch, and the MAX14758 has two NO and two NC SPST switches. These switches have 5Ω (typ) on-resistances and low on-leakage currents of 0.01nA (typ). The on-resistance flatness is 0.004Ω (typ).

The devices are suitable for a multitude of analog signal routing and switching applications. They are specified over an extended temperature range of -40°C to +85°C, but can be operated up to +125°C with elevated leakage currents.

Applications

- Industrial Control Systems
- Instrumentation
- Battery Management
- Environmental Control Systems
- Medical Systems
- ATE System
- Audio Signal Routing/Switching

Features

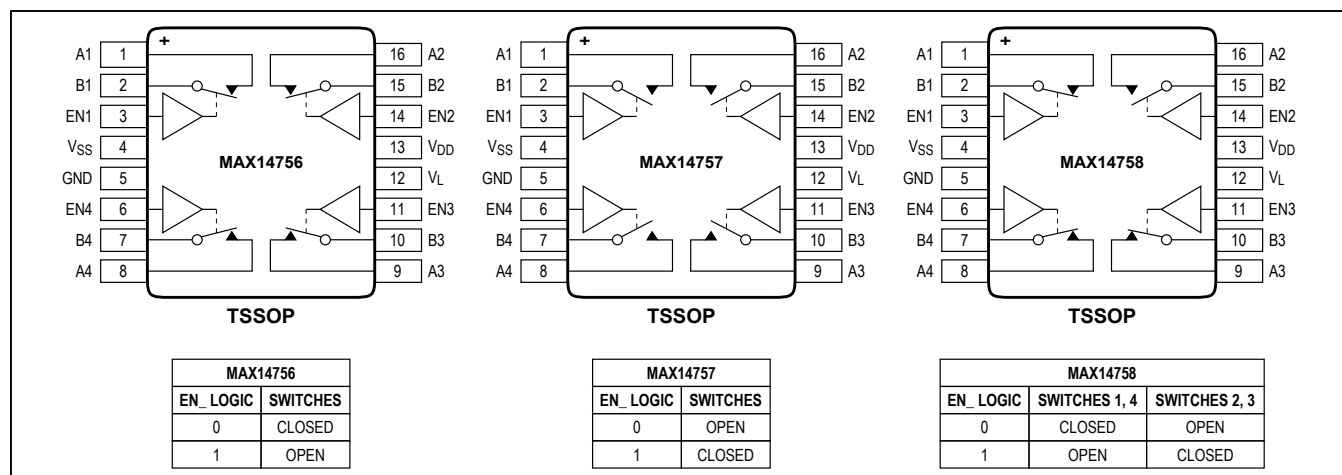
- Single-Supply Operation from +10V to +70V
- Bipolar-Supply Operation Up to ±35V
- On-Resistance of 10Ω (max)
- R_{ON} Flatness of 0.004Ω (typ)
- 2.5nA (max) Off-Leakage Currents at +85°C
- Overvoltage/Undervoltage Clamping Through Protection Diodes
- 500μA (typ) Supply Current
- TSSOP 16-Pin Package
- -40°C to +85°C Ambient Temperature Range
- Functionally Compatible to DG411, DG412, and DG413
- Functionally Operational Up to +125°C

Ordering Information

| PART | FUNCTION | TEMP RANGE | PIN-PACKAGE |
|--------------|-------------------|----------------|-------------|
| MAX14756EUE+ | Quad NC SPST | -40°C to +85°C | 16 TSSOP |
| MAX14757EUE+ | Quad NO SPST | -40°C to +85°C | 16 TSSOP |
| MAX14758EUE+ | Dual NO + NC SPST | -40°C to +85°C | 16 TSSOP |

+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagrams



Absolute Maximum Ratings

| | |
|---|--|
| V _{DD} to V _{SS} | -0.3V to +72V |
| V _{SS} to GND..... | -36V to +0.3V |
| V _L , EN ₋ to GND..... | -0.3V to the lesser of (+12V, V _{DD} + 0.3V) |
| A ₋ , B ₋ to V _{SS} | -0.3V to (V _{DD} + 2V) or 100mA (whichever occurs first) |
| Continuous Current into A ₋ , B ₋ | ±100mA |

| | |
|---|-----------------|
| Continuous Power Dissipation (T _A = +70°C) | |
| TSSOP (derate 11.1mW/°C above +70°C) | 889mW |
| Operating Temperature Range..... | -40°C to +85°C |
| Storage Temperature Range..... | -65°C to +150°C |
| Junction Temperature..... | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Soldering Temperature (reflow)..... | +260°C |

Package Thermal Characteristics (Note 1)

TSSOP

| | |
|---|--------|
| Junction-to-Ambient Thermal Resistance (θ _{JA}) | 90°C/W |
| Junction-to-Case Thermal Resistance (θ _{JC})..... | 27°C/W |

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics—Dual Supplies

(V_{DD} = +35V, V_{SS} = -35V, V_{GND} = 0V, V_L = +3.3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------------------------|---|-----------------|-------|-----------------|-------|
| POWER SUPPLY | | | | | | |
| V _{DD} Supply-Voltage Range | V _{DD} | | +10 | | +35 | V |
| V _{SS} Supply-Voltage Range | V _{SS} | | -10 | | -35 | V |
| V _L Logic Supply-Voltage Range | V _L | | +1.6 | | +11 | V |
| V _{DD} Supply Current | I _{DD(OFF)} | V _{EN} to switch off state, V _A , V _B = +20V | | 200 | 450 | μA |
| | I _{DD(ON)} | V _{EN} to switch on state, V _A , V _B = +20V | | 500 | 800 | |
| V _{SS} Supply Current | I _{SS(OFF)} | V _{EN} to switch off state, V _A , V _B = +20V | | 200 | 450 | μA |
| | I _{SS(ON)} | V _{EN} to switch on state, V _A , V _B = +20V | | 500 | 800 | |
| V _L Current | I _L | V _L = +11V, V _{EN1} = V _{EN2} = V _{EN3} = V _{EN4} = (0.25 x V _L) or (0.75 x V _L) | | | 0.4 | mA |
| SWITCH | | | | | | |
| Analog-Signal Range | V _A , V _B | Figure 1 | V _{SS} | | V _{DD} | V |
| Current Through Switch | I _A , I _B | V _A , V _B = +20V | -50 | | +50 | mA |
| On-Resistance | R _{ON} | I _A , I _B = 10mA, V _A , V _B = ±20V, Figure 1 | | 5 | 10 | Ω |
| On-Resistance Matching Between Channels | ΔR _{ON} | I _A , I _B = 10mA, V _A , V _B = ±20V, 0V (Note 2) | | 0.3 | 0.5 | Ω |
| On-Resistance Flatness | R _{FLAT(ON)} | I _A , I _B = 10mA, V _A , V _B = ±20V | | 0.004 | | Ω |
| On-Leakage Current | I _{A/B(ON)} | V _B = ±20V, V _A = unconnected, Figure 2 | -5 | | +5 | nA |
| | | V _B = ±20V, V _A = unconnected, T _A = +25°C, Figure 2 | | 0.01 | | |
| Off-Leakage Current | I _{A/B(OFF)} | V _B = ±20V, V _A = -20V, Figure 3 | -2.5 | | +2.5 | nA |
| | | V _B = ±20V, V _A = -20V, T _A = +25°C, Figure 3 | | 0.01 | | |

Electrical Characteristics—Dual Supplies (continued)

($V_{DD} = +35V$, $V_{SS} = -35V$, $V_{GND} = 0V$, $V_L = +3.3V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|-----------|--|-------------------|-------|-------------------|---------|
| LOGIC (EN1, EN2, EN3, EN4) | | | | | | |
| Input-Voltage Low | V_{IL} | | | | $0.25 \times V_L$ | V |
| Input-Voltage High | V_{IH} | | $0.75 \times V_L$ | | | V |
| Input Leakage Current | | $V_{EN} = 0V$ or V_L | -1 | | +1 | μA |
| DYNAMIC CHARACTERISTICS | | | | | | |
| V_{DD}/V_{SS} Power-On Time | | $R_L = 10k\Omega$ | | 1 | | μs |
| Enable Turn-On Time | t_{ON} | $V_A, V_B = \pm 10V$, $R_L = 10k\Omega$, Figure 4 | | 35 | 60 | μs |
| Enable Turn-Off Time | t_{OFF} | $V_A, V_B = \pm 10V$, $R_L = 10k\Omega$, Figure 4 | | 2 | 3 | μs |
| Off-Isolation | V_{ISO} | $V_A, V_B = 1V$ RMS, $f = 100kHz$, $R_L = 1k\Omega$, $C_L = 15pF$, Figure 5 | | 65 | | dB |
| Crosstalk | V_{CT} | $R_S = R_L = 1k\Omega$, Figure 6 | | 96 | | dB |
| -3dB Bandwidth | BW | $R_S = 50\Omega$, $R_L = 1k\Omega$, Figure 7 | | 145 | | MHz |
| Total Harmonic Distortion Plus Noise | THD+N | $R_S = R_L = 1k\Omega$, $f = 20Hz$ to $20kHz$ | | 0.001 | | % |
| Charge Injection | Q | $A_-, B_- = GND$, $C_L = 1nF$, Figure 8 | | 580 | | pC |
| Switch-On Capacitance | C_{IN} | $V_{DD} = +50V$, $V_{SS} = 0V$, $V_{A_-}, V_{B_-} = +4V$, $f = 1MHz$ | | 40 | | pF |
| Switch-Off Capacitance | C_{IN} | $V_{DD} = +50V$, $V_{SS} = 0V$, $V_{A_-}, V_{B_-} = +4V$, $f = 1MHz$ | | 35 | | pF |

DC Electrical Characteristics—Single Supply

($V_{DD} = +70V$, $V_{SS} = V_{GND} = 0V$, $V_L = +3.3V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|---|------|-----|------|----------|
| POWER SUPPLY | | | | | | |
| V_{DD} Supply-Voltage Range | V_{DD} | | +10 | | +70 | V |
| SWITCH | | | | | | |
| On-Resistance | R_{ON} | $I_{A_-} = 10mA$, $V_{A_-}, V_{B_-} = +20V$, Figure 1 | | 5 | 10 | Ω |
| On-Resistance Matching Between Channels | DR_{ON} | $I_{A_-}, I_{B_-} = 10mA$, $V_{A_-}, V_{B_-} = +70V$, $0V$ (Note 2) | | 0.3 | 0.5 | Ω |
| Off-Leakage Current | $I_{A/B_}(OFF)$ | $V_{B_-} = +40V$, $V_{A_-} = +10V$, Figure 3 | -2.5 | | +2.5 | nA |

Note 2: Guaranteed by design; not production tested.

Note 3: All parameters in single-supply operation are expected to be the same as in dual-supply operation.

Test Circuits/Timing Diagrams

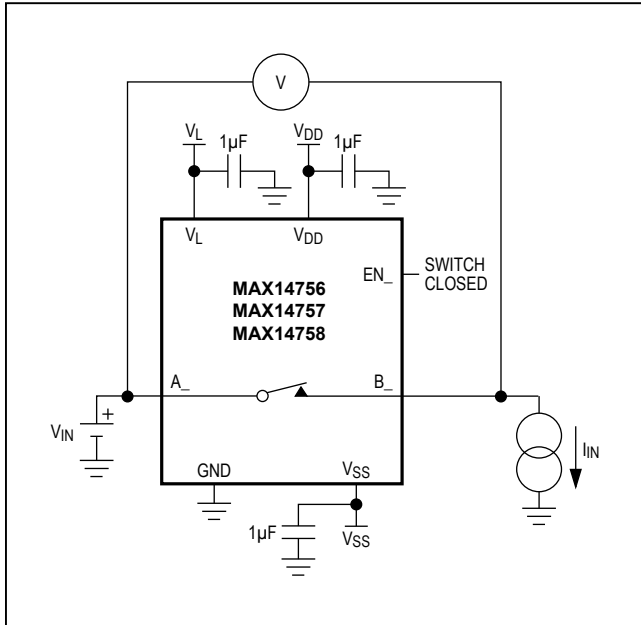


Figure 1. On-Resistance Measurement

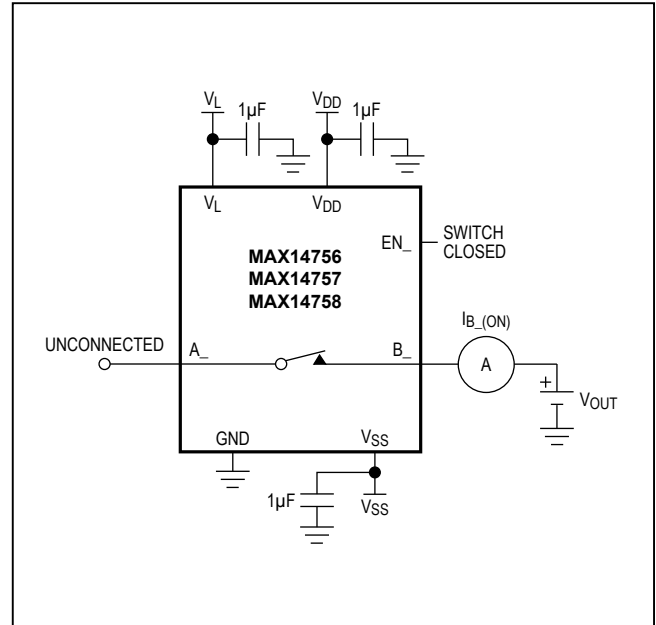


Figure 2. On-Leakage Current

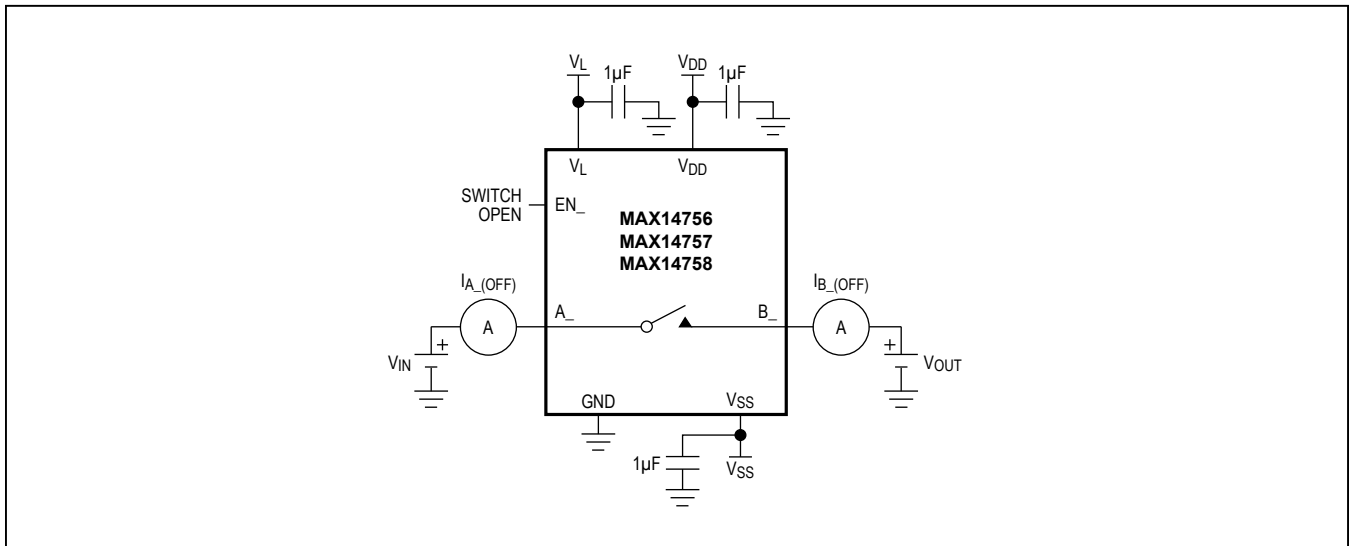


Figure 3. Off-Leakage Current

Test Circuits/Timing Diagrams (continued)

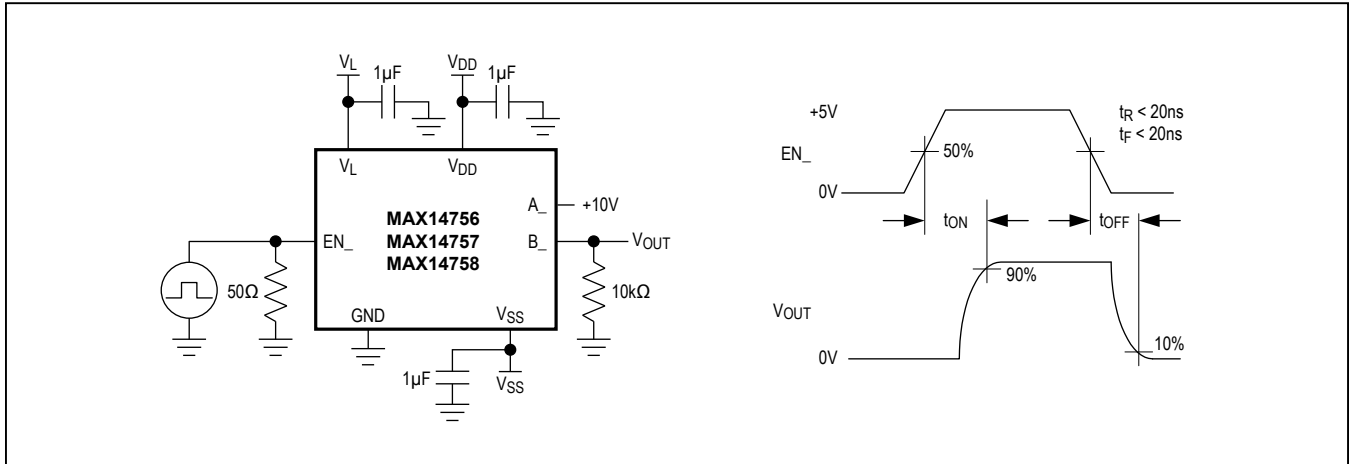


Figure 4. Enable Switching Time

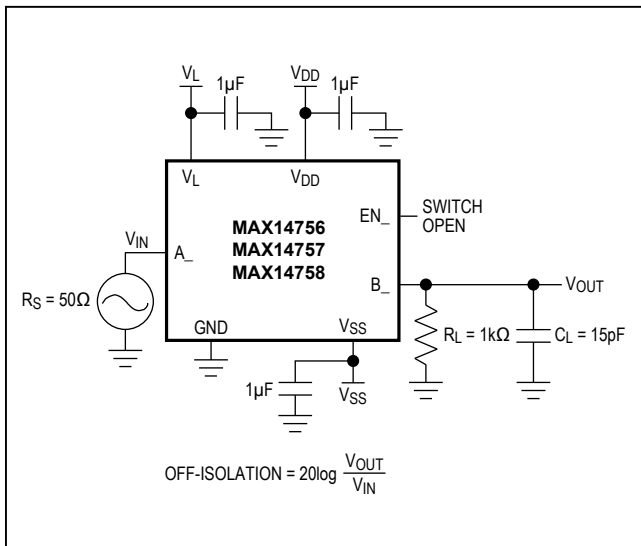


Figure 5. Off-Isolation

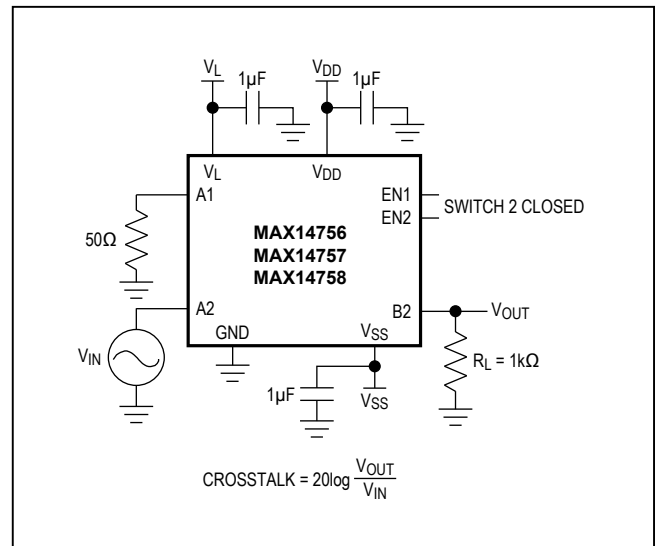


Figure 6. Crosstalk

Test Circuits/Timing Diagrams (continued)

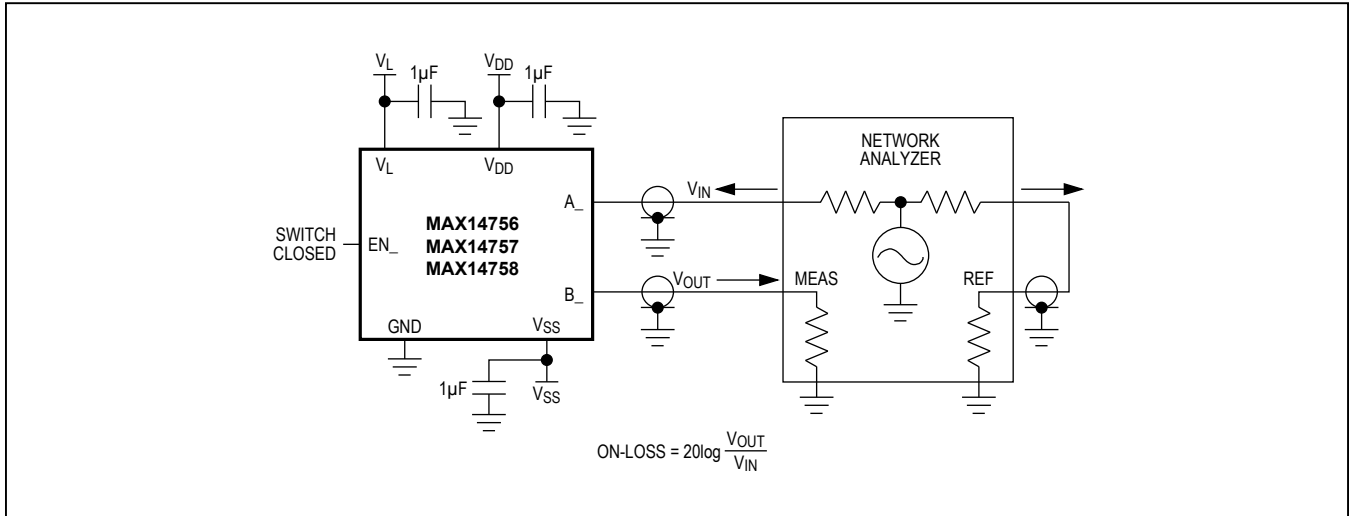


Figure 7. Frequency Response

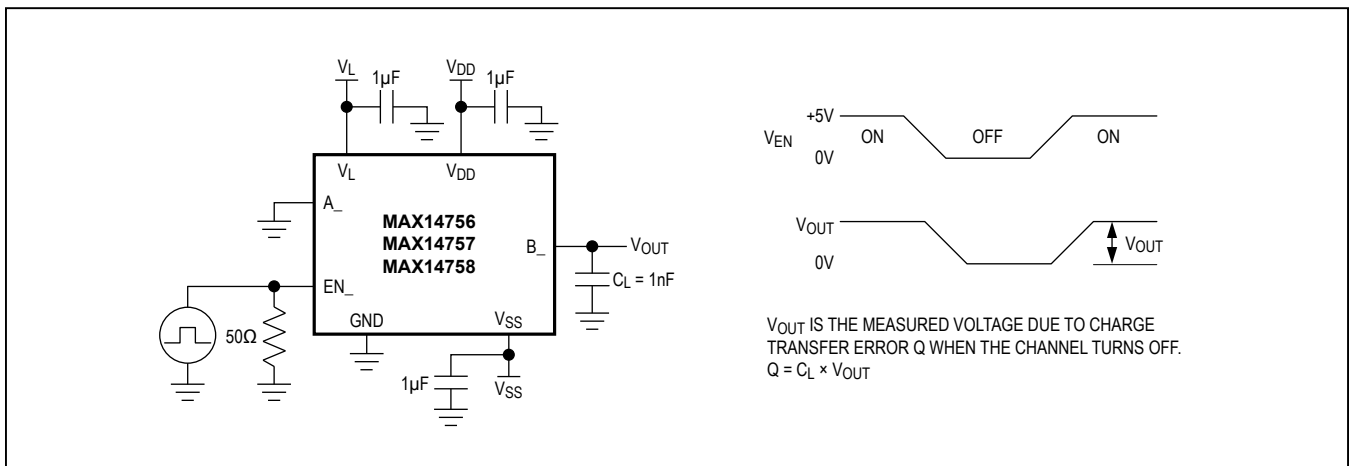
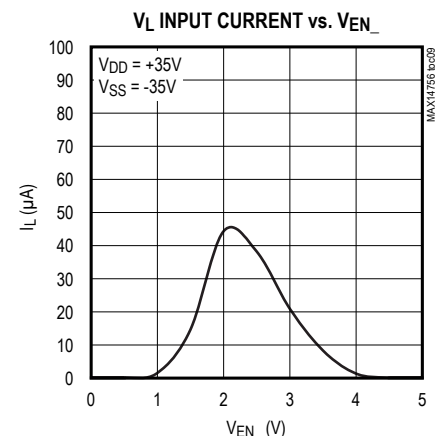
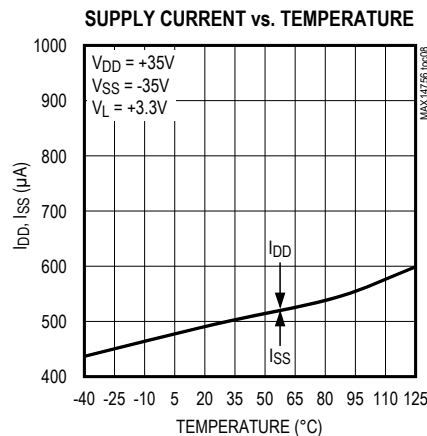
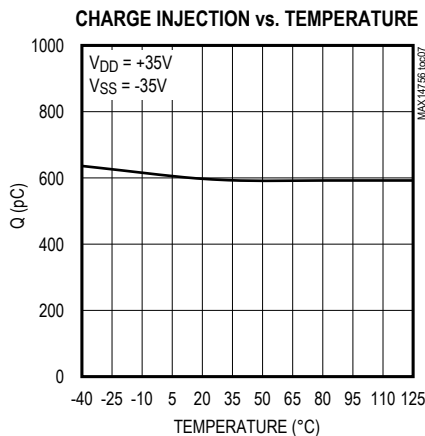
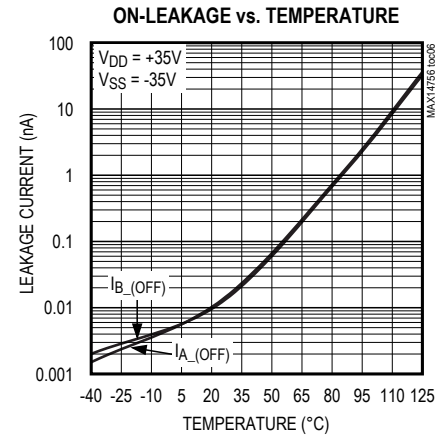
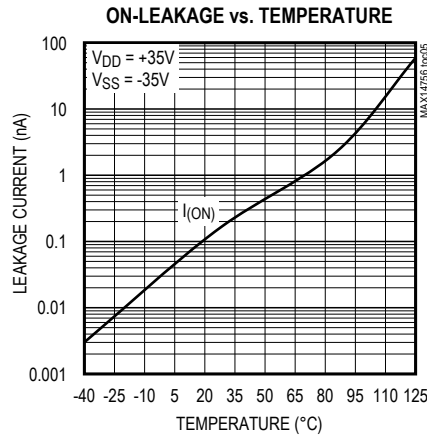
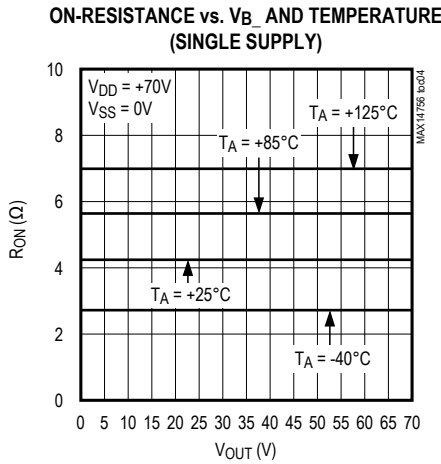
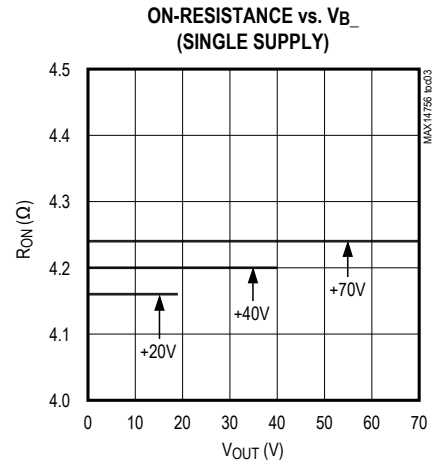
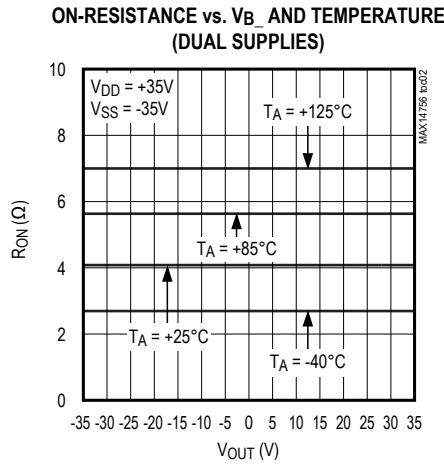
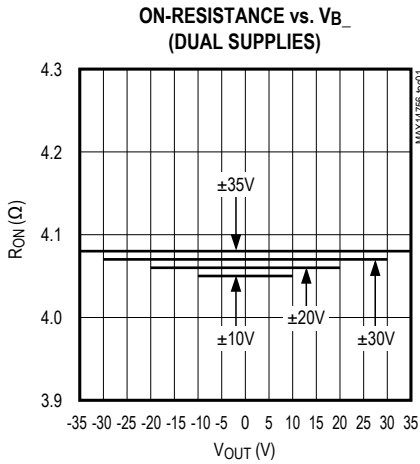


Figure 8. Charge Injection

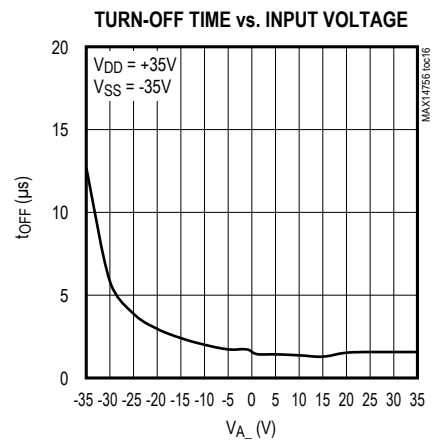
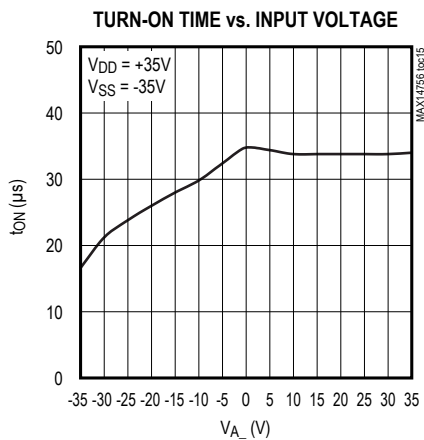
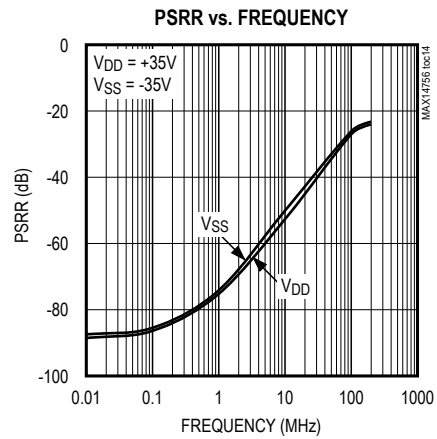
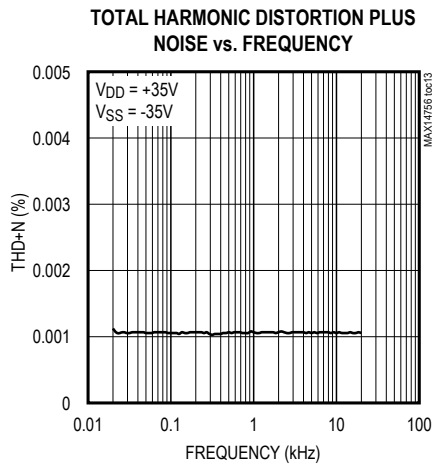
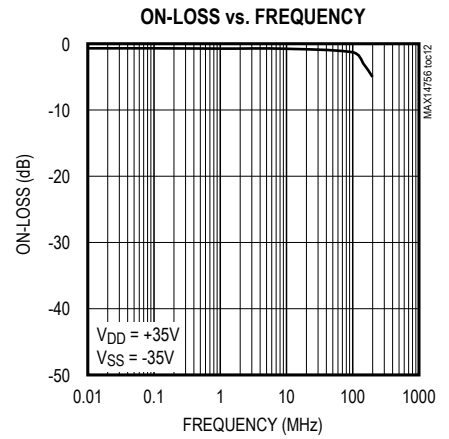
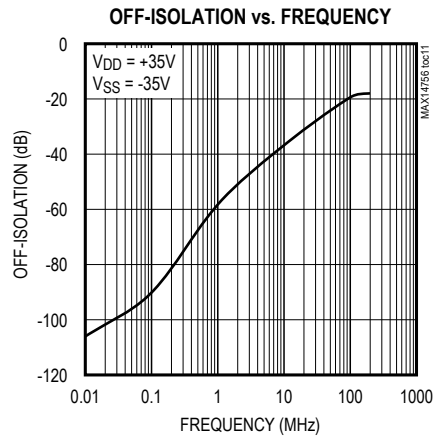
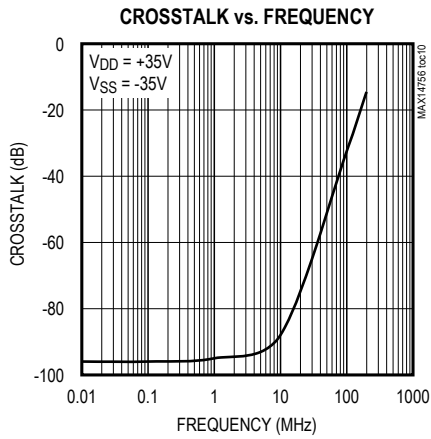
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, $V_L = +3.3\text{V}$, unless otherwise noted.)

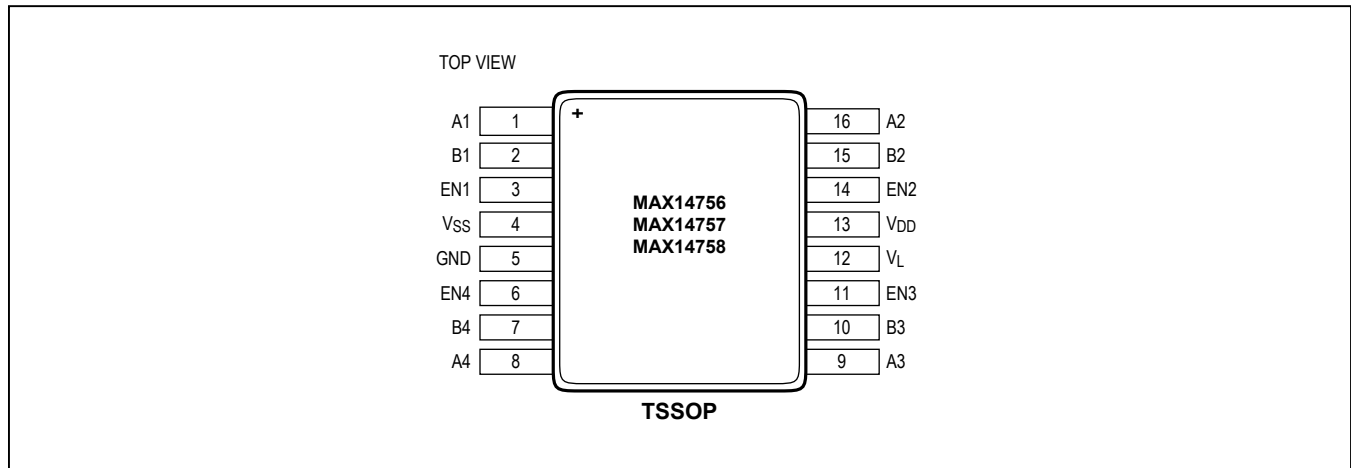


Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, $V_L = +3.3\text{V}$, unless otherwise noted.)



Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|-----|-----------------|---|
| 1 | A1 | Terminal A of Switch 1 |
| 2 | B1 | Terminal B of Switch 1 |
| 3 | EN1 | Enable Input of Switch 1. When EN1 is driven high, the switch's state (NO/NC) changes (see Table 1 , Table 2 , and Table 3). |
| 4 | V _{SS} | Negative Supply Voltage. Bypass V _{SS} to GND with a 1μF ceramic capacitor (100V rated) as close as possible to the pin. |
| 5 | GND | Ground |
| 6 | EN4 | Enable Input of Switch 4. When EN4 is driven high, the switch's state (NO/NC) changes (see Table 1 , Table 2 , and Table 3). |
| 7 | B4 | Terminal B of Switch 4 |
| 8 | A4 | Terminal A of Switch 4 |
| 9 | A3 | Terminal A of Switch 3 |
| 10 | B3 | Terminal B of Switch 3 |
| 11 | EN3 | Enable Input of Switch 3. When EN3 is driven high, the switch's state (NO/NC) changes (see Table 1 , Table 2 , and Table 3). |
| 12 | V _L | Logic Supply Voltage. Bypass V _L to GND with a 1μF ceramic capacitor as close as possible to the pin. |
| 13 | V _{DD} | Positive Supply Voltage. Bypass V _{DD} to GND with a 1μF ceramic capacitor (100V rated) as close as possible to the pin. |
| 14 | EN2 | Enable Input of Switch 2. When EN2 is driven high, the switch's state (NO/NC) changes (see Table 1 , Table 2 , and Table 3). |
| 15 | B2 | Terminal B of Switch 2 |
| 16 | A2 | Terminal A of Switch 2 |

Detailed Description

The MAX14756/MAX14757/MAX14758 are analog switches with low on-resistance of 10Ω (max) that conduct equally well in both directions. All devices have a rail-to-rail analog-signal range. They operate with a single +70V supply in unipolar applications or ±35V dual supplies in bipolar applications. The bipolar supplies can be offset and do not have to be symmetrical.

The MAX14756 is a quad NC SPST switch, the MAX14757 is a quad NO SPST switch, and the MAX14758 has two NO and two NC SPST switches. These switches have 5Ω (typ) on-resistances and low on-leakage currents of 5nA (max). The on-resistance flatness is 0.004Ω (typ). These devices are suitable for a multitude of analog-signal routing and switching applications, and are functionally operational up to +125°C with increased leakage currents.

Applications Information

Low-Distortion Audio

The MAX14756/MAX14757/MAX14758 switches, having low R_{ON} and very low R_{ON} variation with signal amplitude, are well suited for low-distortion audio applications. The *Typical Operating Characteristics* section shows Total Harmonic Distortion (THD) vs. Frequency graphs for several signal amplitudes.

Current Through the Switches

The current flowing through every switch must be limited to ±50mA for normal operation. If the current exceeds this limit, an internal leakage current flows from the switch to V_{SS}. Larger input currents do not destroy the device, as long as the *Absolute Maximum Ratings* are not exceeded.

Input-Voltage Clamping

For applications that require input voltages beyond the supplies rails, the internal input diodes to V_{DD} and V_{SS} can be used to limit the input voltages. As shown in Figure 9, series resistors can be employed at the inputs to limit the currents flowing into the diodes during undervoltage and overvoltage conditions. Choose the limiting resistors such that the input currents are limited to I_{IN}(MAX) = 100mA. The values of the current-limit resistors can be calculated as the larger of R_{LIM+} and R_{LIM-}.

$$R_{LIM+} = \frac{V_{IN(MAX)} - V_{DD}}{I_{IN_}(MAX)}$$

$$R_{LIM-} = \frac{V_{SS} - V_{IN(MIN)}}{I_{IN_}(MAX)}$$

Table 1. MAX14756 Truth Table

| LOGIC | | SWITCH | |
|-------|---|--------|--------|
| EN1 | 0 | A1/B1 | Closed |
| EN2 | 0 | A2/B2 | Closed |
| EN3 | 0 | A3/B3 | Closed |
| EN4 | 0 | A4/B4 | Closed |
| EN1 | 1 | A1/B1 | Open |
| EN2 | 1 | A2/B2 | Open |
| EN3 | 1 | A3/B3 | Open |
| EN4 | 1 | A4/B4 | Open |

Table 2. MAX14757 Truth Table

| LOGIC | | SWITCH | |
|-------|---|--------|--------|
| EN1 | 0 | A1/B1 | Open |
| EN2 | 0 | A2/B2 | Open |
| EN3 | 0 | A3/B3 | Open |
| EN4 | 0 | A4/B4 | Open |
| EN1 | 1 | A1/B1 | Closed |
| EN2 | 1 | A2/B2 | Closed |
| EN3 | 1 | A3/B3 | Closed |
| EN4 | 1 | A4/B4 | Closed |

Table 3. MAX14758 Truth Table

| LOGIC | | SWITCH | |
|-------|---|--------|--------|
| EN1 | 0 | A1/B1 | Closed |
| EN2 | 0 | A2/B2 | Open |
| EN3 | 0 | A3/B3 | Open |
| EN4 | 0 | A4/B4 | Closed |
| EN1 | 1 | A1/B1 | Open |
| EN2 | 1 | A2/B2 | Closed |
| EN3 | 1 | A3/B3 | Closed |
| EN4 | 1 | A4/B4 | Open |

During an undervoltage or overvoltage condition, the input impedance is equal to R_{LIM}. The additional power dissipation due to the fault currents needs to be calculated. During an overvoltage or undervoltage clamping condition on one switch input, the other switches of the MAX14756/MAX14757/MAX14758 operate normally.

Beyond-the-Rail Input

If input voltages are expected to go beyond the supply voltages, but within the absolute maximum supply voltages of the MAX14756/MAX14757/MAX14758, add two diodes in series with the supplies as shown in Figure 10.

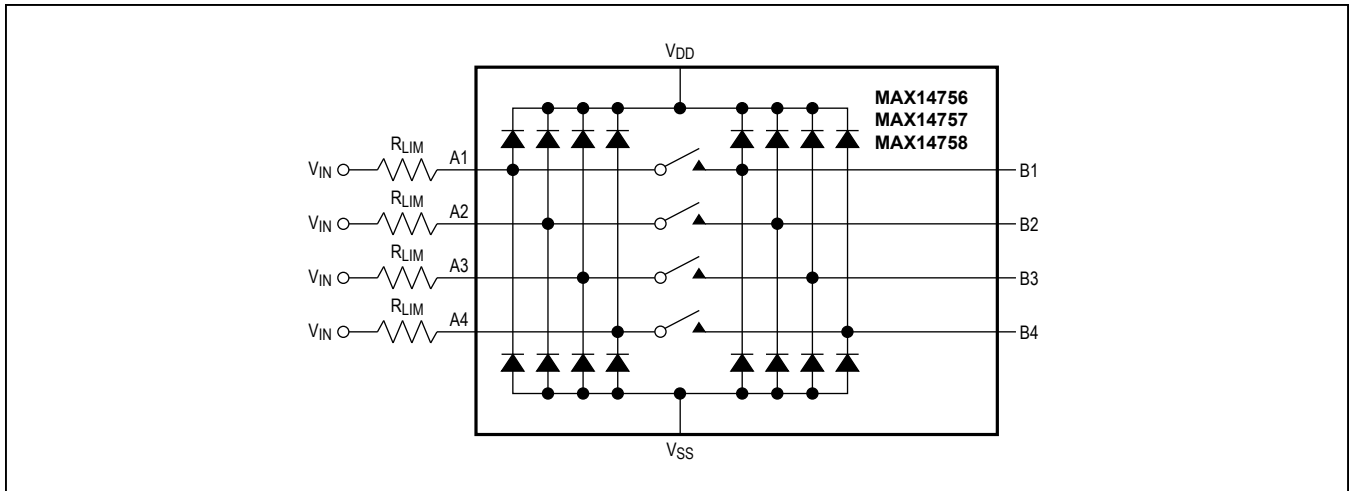


Figure 9. Input Overvoltage and Undervoltage Clamping

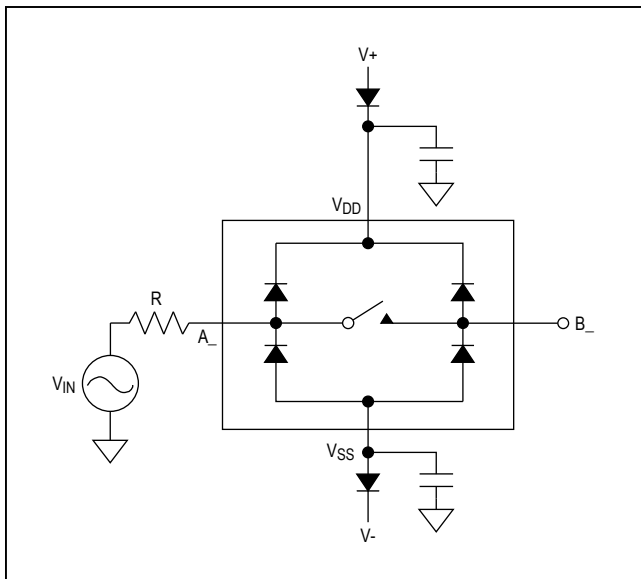


Figure 10. Beyond-the-Rail Application

During undervoltage and overvoltage events, the internal diodes pull V_{DD}/V_{SS} supplies up/down. An advantage of this scheme is that the input impedance is high and currents do not flow through the MAX14756/MAX14757/MAX14758 during overvoltage and undervoltage events. The input voltages must be limited to the voltages specified in the *Absolute Maximum Ratings* section.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 16 TSSOP | U16+1 | 21-0066 | 90-0117 |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|---|---------------|
| 0 | 12/10 | Initial release | — |
| 1 | 11/14 | Removed automotive reference in <i>Applications</i> section | 1 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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