



V2000

**Ambient Light Sensor and Proximity Sensor with
I2C interface**

Datasheet

Version – 1.0

Sensortek Technology Corporation

1. OVERVIEW

Description

The V2000 is an integrated ambient and infrared light to digital converter with I²C interface. This device provides not only ambient light sensing to allow robust backlight/display brightness control but also infrared sensing to allow proximity estimation featured with interrupt function.

For ambient light sensing, the V2000 incorporates a photodiode, timing controller and ADC in a single chip. The excellent spectral response is designed to be close-to human eye. The V2000 is suitable for detecting a wide range of light intensity environment.

For proximity sensing, the V2000 also incorporates a photodiode, timing controller and ADC in the same chip. The spectral response of V2000 is optimized for wavelength 940nm infrared light. The V2000 provides programmable current setting to drive IR LED and employs a noise cancellation scheme to highly reject unwanted ambient IR noise.

The V2000 has excellent temperature compensation, robust on-chip refresh rate setting without external components. Software shutdown mode control is provided for power saving application. The V2000 operating voltage range is 1.7V to 3.0V.

Feature

- Integrated ambient light sensor and proximity sensor in one package.

Proximity Sensor

- 16 bits resolution for proximity detection
- Built-in LED driver with flexible setting
 - LED turn-on time : 7 steps IT
 - LED current : 3.125 / 6.25 / 12.5 / 25 / 50 / 100 / 150 mA
- Flexible interrupt setting
 - Several interrupt modes meet application requirements.
 - Flag modes are included.
 - Intelligent persistence to speed up the response time : 1/2/4/16 times
- Low noise design
- High ambient light suppression

Ambient Light Sensor

- Convert ambient light intensity to 16-bit digital data format
- 3rd generation ambient light sensor which closes to human-eye response and suppress IR portion.
- Flexible digital settings
 - Integration time : 7 steps IT
- Flexible interrupt setting
 - Interrupt while out-of- window
 - Persistence : 1/2/4/8 times
- Clear channel for different light source compensation.

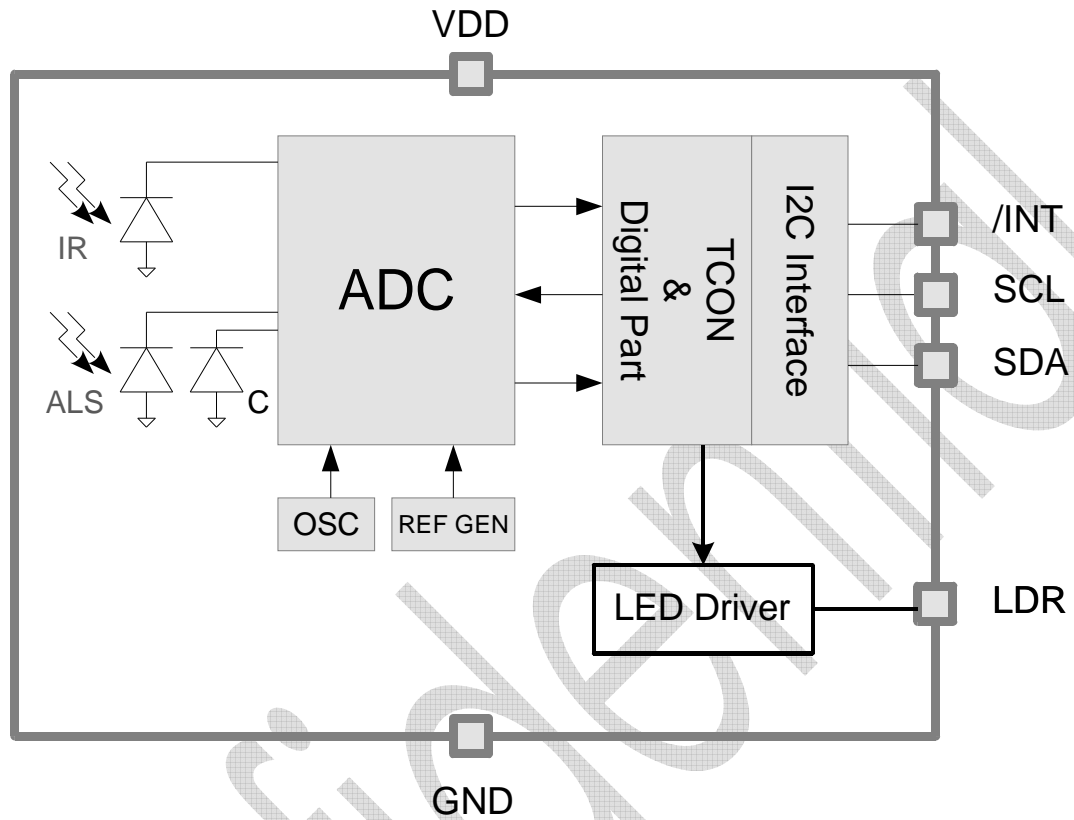
General

- Fully digital control with I²C interface
 - 1.7 ~ 3.6V I²C interface
- Low power design
 - Standby mode
 - Wait mode
- V_{DD} wide operation voltage : 1.7~3.0V
- Excellent temperature compensation: -40 to 85°C
- Available package options: OLGA
 - V2000 : 2.15 x 1.4 x 0.6 (mm)
- Lead-free package (RoHS compliant)
- Moisture Sensitivity Level 3

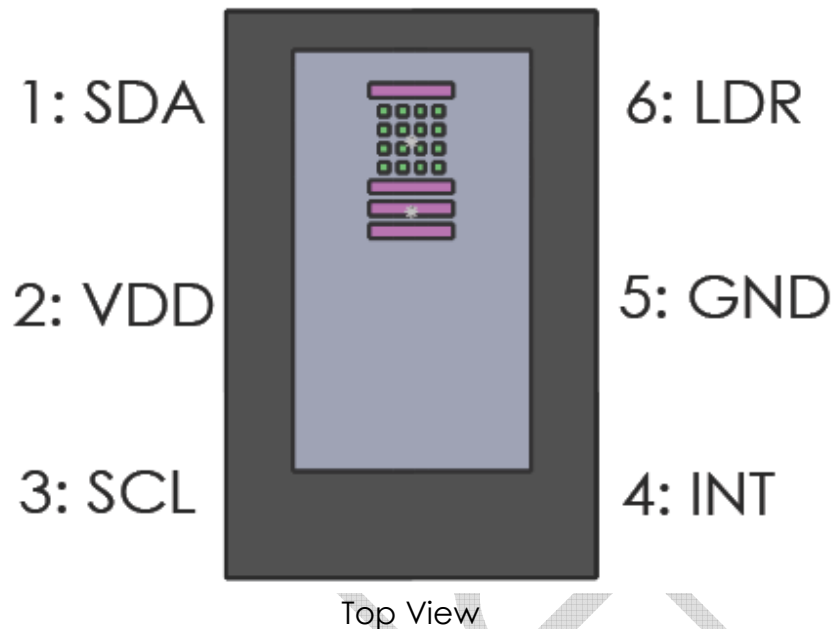
Applications

- Mobile Phone, Smart-phone, PDA

2. FUNCTION BLOCK



3. PINOUT DIAGRAM



4. PIN DESCRIPTION

| Pin No. | Pin Name | Dir. | Pin Function |
|---------|----------|------|--|
| 1 | SDA | B | I ² C serial data line. (Open Drain) |
| 2 | VDD | PWR | Power supply: 1.7V to 3.0V. |
| 3 | SCL | I | I ² C serial clock line. |
| 4 | /INT | O | Interrupt pin, LO for interrupt alarming. (Open Drain) |
| 5 | GND | GND | Ground. The thermal pad is also connected to the GND pin. |
| 6 | LDR | I | IR LED driver pin connecting to the cathode of the external IR LED. The sink current of the IR LED driver can be programmed through I ² C or the external resistor. |

Direction denotation:

| | | | |
|-----|--------|-----|--------------|
| O | Output | GND | Ground |
| I | Input | B | Bi-direction |
| PWR | Power | NC | Not Connect |

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|------------------------|------|------|------|
| V _{DD} | Supply voltage | -0.3 | 3.6 | V |
| V _{LEDA} | Voltage of LED's anode | -0.3 | 4.7 | V |
| V _{LDR} | Voltage of LDR | | 3.6 | V |
| T _a | Operation temperature | -40 | 85 | °C |

NOTE: All voltages are measured with respect to GND

Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|-------------------------------------|------|------|------|
| V _{DD} | Supply voltage | 1.7 | 3.0 | V |
| V _{LEDA} | Voltage of LED's anode | 2.8 | 4.6 | V |
| f _{I2C} | Clock frequency of I ² C | — | 400 | KHz |
| T _a | Operation temperature | -40 | 85 | °C |

NOTE: All voltages are measured with respect to GND

| Symbol | Parameter | Max. | Unit |
|--------|------------------------------------|----------------|------|
| ESD | Electrostatic discharge protection | 2 (HBM) | kV |
| | | 200 (MM) | V |
| | | 100 (Latch Up) | mA |

NOTE: All voltages are measured with respect to GND

5.1 Electrical and Optical Characteristics

$V_{DD} = V_{LED} = 2.8V$, under room temperature 25°C (unless otherwise noted)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|--|------------------------|-------|-------|----------|---------|
| Operation Characteristics | | | | | | |
| I_{ALS} | ALS only supply current | Note1,2 | 192 | 240 | 288 | μA |
| I_{PS} | PS only supply current | Note1,2 | 208 | 260 | 312 | μA |
| I_{SD} | Shutdown current | Note1,2 | | 1.36 | 30 | μA |
| V_{IH} | Logic high, I ² C | Note6 | 1.3 | | V_{DD} | V |
| V_{IL} | Logic low, I ² C | Note7 | — | | 0.4 | V |
| ALS Characteristics | | | | | | |
| λ_{p1} | Peak sensitivity wavelength for ALS | | | 550 | | nm |
| ALS_{FSCNT} | Full scale ALS counts | | | | 65535 | counts |
| ALS_{DARK} | ALS dark offset | Note2,3,4 | | 0 | 4 | counts |
| ALS_{SENSE} | ALS sensing tolerance | Note2,3 | -12.5 | | +12.5 | % |
| Proximity Characteristics | | | | | | |
| λ_{p2} | High sensitivity wavelength range for PS | | 800 | | 1000 | nm |
| PS_{FSCNT} | Full scale PS counts | | | | 65535 | counts |
| $I_{LED_{SINK}}$ | LED sink current | IRDR_LED[2:0] Note5 | | | | |
| | | 000 | | 3.125 | | mA |
| | | 001 | | 6.25 | | mA |
| | | 010 | | 12.5 | | mA |
| | | 011 | | 25 | | mA |
| | | 100 | | 50 | | mA |
| | | 101 | | 100 | | mA |
| | | 110 | | 150 | | mA |
| AMB_{SUPP} | Ambient Light Suppression | Note8 | | | TBD | Lux |

Note 1 : No LED operation.

Note 2 : GAIN_ALS[1:0] = 2'b00, .IT_ALS[3:0] = 4'b0010, GAIN_PS[1:0] = 2'b00, .IT_PS[3:0] = 4'b0000.

Note 3 : White LED parallel light source.

Note 4 : $E_{ambient} = 0$ Lux.

Note 5 : The voltage of LDR pin is fixed at 1.2V.

Note 6 : I²C logical high voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical high level is different when different supply voltage is applied.

Note 7 : I²C logical low voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical low level is different when different supply voltage is applied.

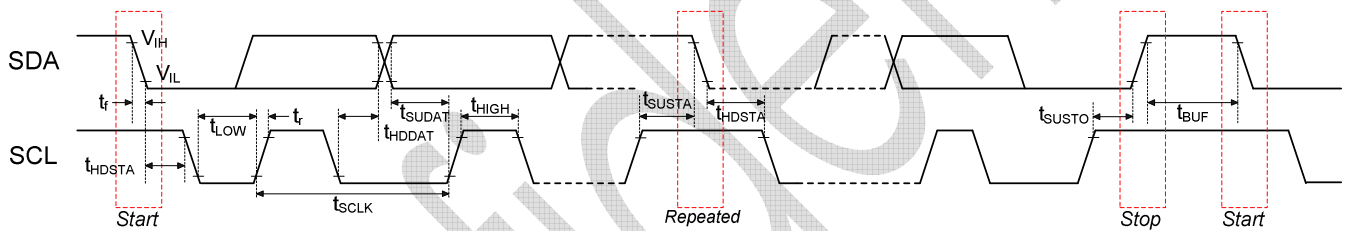
Note 8 : Sunlight environment.

5.2 Timing Chart

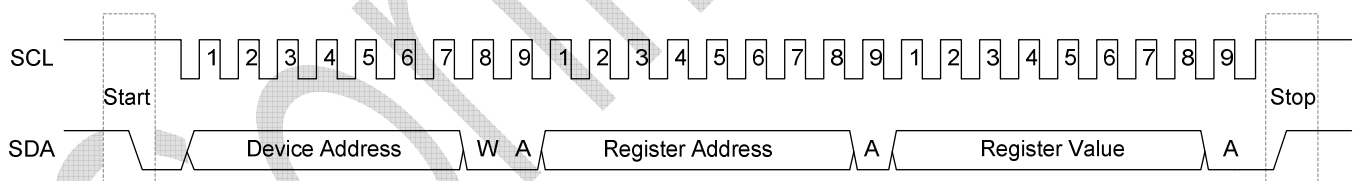
Characteristics of the SDA and SCL I/O

| Symbol | Parameter | Standard Mode | | Fast Mode | | Unit |
|-------------|---|---------------|------|-----------|------|---------|
| | | Min. | Max. | Min. | Max. | |
| f_{SCLK} | SCL clock frequency | 10 | 100 | 10 | 400 | KHz |
| t_{HDSTA} | Hold time after (repeated) start condition. After this period, the first clock is generated | 4.0 | — | 0.6 | — | μ s |
| t_{LOW} | LOW period of the SCL clock | 4.7 | — | 1.3 | — | μ s |
| t_{HIGH} | HIGH period of the SCL clock | 4.0 | — | 0.6 | — | μ s |
| t_{SUSTA} | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | μ s |
| t_{HDDAT} | Data hold time | 0 | — | 0 | — | ns |
| t_{SUDAT} | Data set-up time | 250 | — | 100 | — | ns |
| t_r | Rise time of both SDA and SCL signals | — | 1000 | — | 300 | ns |
| t_f | Fall time of both SDA and SCL signals | — | 300 | — | 300 | ns |
| t_{SUSTO} | Set-up time for STOP condition | 4.0 | — | 0.6 | — | μ s |
| t_{BUF} | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | μ s |

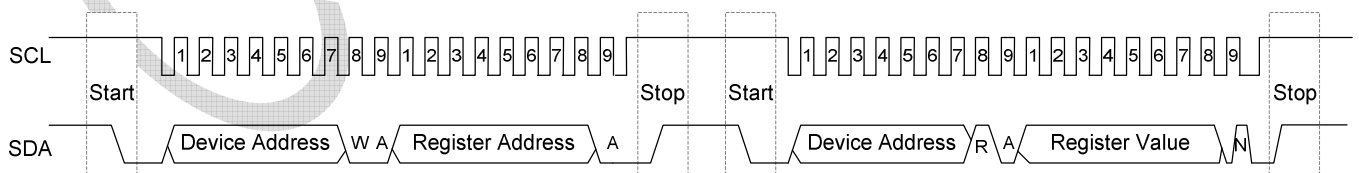
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



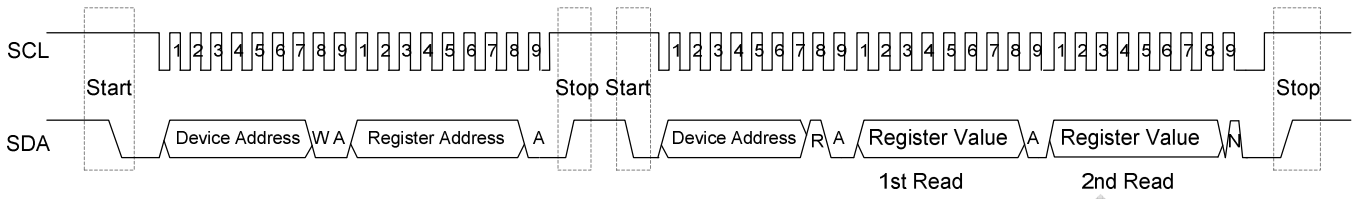
Timing Chart of the SDA and SCL



Write Command



Read Data



Sequential Read Data

Confidential

6. FUNCTION DESCRIPTION

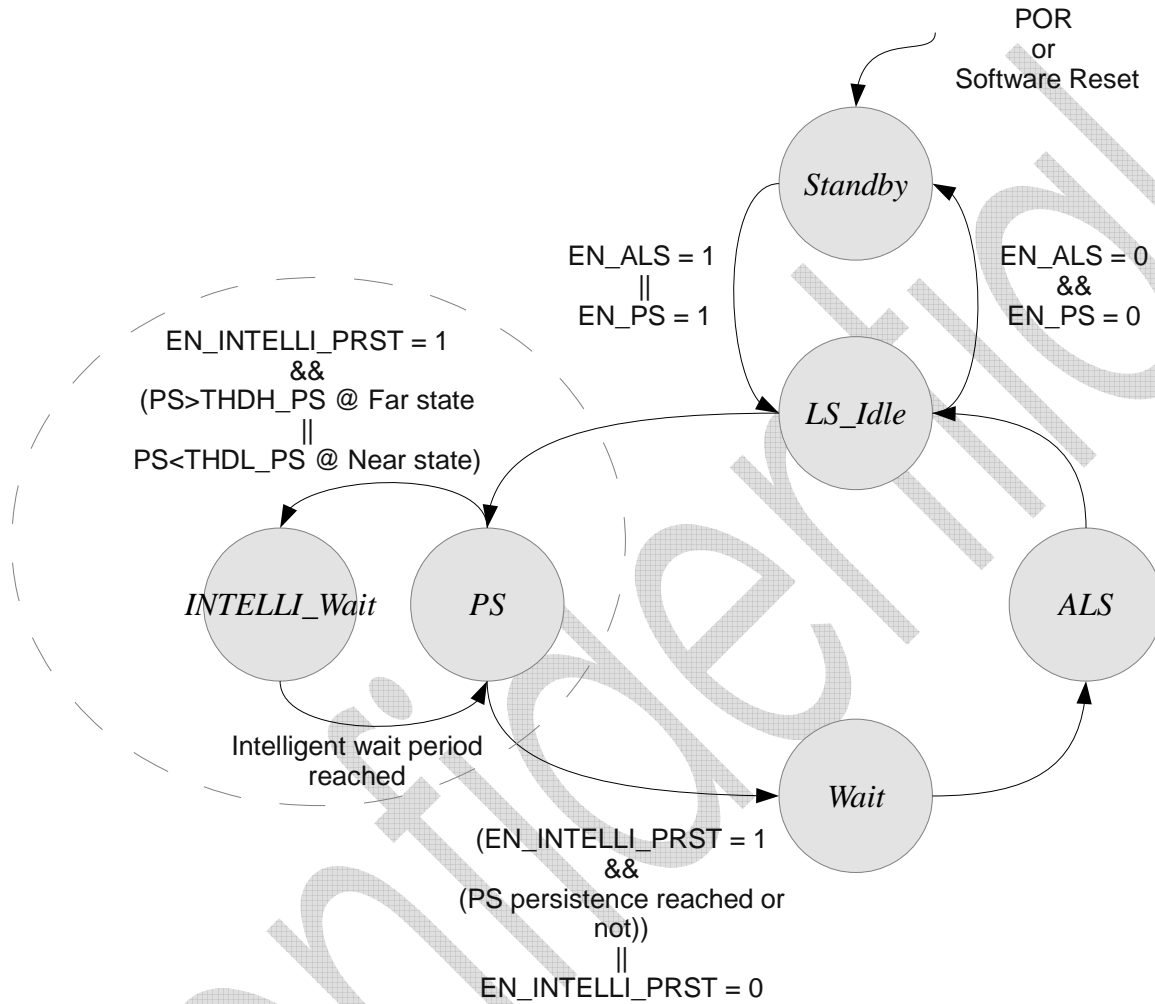
6.1 Digital Interface

V2000 contains eight-bit registers accessed via the I²C bus. All operations can be controlled by the command register. The simple command structure makes user easy to program the operation setting and latch the output data from V2000. Section 5.2 Timing chart displays the V2000 I²C command format for reading and writing operation between host and V2000.

V2000 provides fixed I²C slave address of 0x57 using 7 bit addressing protocol.

| Slave Address | R/W Command Bit | OPERATION |
|---------------------------|-----------------|------------------------|
| 0x57 | 0 | Write Command to V2000 |
| (followed by the R/W bit) | 1 | Read Data from V2000 |

6.2 System Operation



6.3 ALS Operation

6.3.1 ALS General Operation

The related ALS control bits are summarized below.

| ALS Control Bits | |
|------------------------------|---|
| General Control | |
| EN_ALS | Enable ALS sensing function |
| IT_ALS[3:0] | ALS integration time |
| GAIN_ALS[1:0] | ALS gain control |
| PRST_ALS[1:0] | ALS persistence number |
| GAIN_C[1:0] | Clear channel gain control |
| ALS Interrupt Control | |
| EN_ALS_INT | Enable ALS function interrupt |
| EN_ALS_DR_INT | Enable ALS data ready interrupt |
| THDH_ALS[15:0] | ALS out-of-windows high threshold |
| THDL_ALS[15:0] | ALS out-of-windows low threshold |
| ALS Data/Status Bits | |
| Data | |
| DATA_ALS[15:0] | 16-bits ALS channel raw data |
| DATA_C[15:0] | 16-bits Clear channel raw data |
| Status | |
| FLG_ALS_DR | Indicate the ALS data ready event |
| FLG_ALS_INT | Indicate the Green channel out-of-windows event |

V2000 uses the coated photodiode array to measure the Lux of the incoming light and also an un-filtered clear photodiode array to improve the ALS sensing accuracy.

The ALS sensing function is enabled by the EN_ALS bit and the gain control bit GAIN_ALS[1:0]/GAIN_C[1:0] and IT period IT_ALS[3:0] shall be set before the EN_ALS.

The FLG_ALS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after one of the DATA_ALS[15:0]/DATA_C[15:0] is be read out through I²C.

The ALS/C data are 16-bit output and are stored in two bytes register. Higher byte register must be read first than lower byte. Data reading word protection is implemented to make sure the conversion data within the same conversion cycle could be read correctly. When the higher byte register is read, the lower 8-bit data will be stored into a shadow register which is read by the following sequential read or another single read to the lower byte register.

6.3.2 ALS Interrupt Description

ALS Out-of-Windows Interrupt

V2000 provides the ALS data out-of-windows interrupt. Once the EN_ALS_INT is set to 1, then the V2000 shall issue an ALS interrupt and assert the FLG_ALS_INT bit if the ALS data DATA_ALS[15:0] are outside the user's programmed window defined by THDH_ALS[15:0] and THDL_ALS[15:0]. The FLG_ALS_INT shall be cleared by

write the bit 0 and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_INT will also clear the FLG_ALS_INT bit to 0.

ALS persistence numbers PRST_ALS[1:0] is used to avoid the false alarm of ALS out-of-windows event due to environment noise. If ALS persistence is set larger than 1, then the ALS out-of-windows interrupt will not be issued until continuous persistence numbers of ADC conversion results outside the defined windows.

ALS Data Ready Interrupt

V2000 also provides the ALS data ready interrupt. Once the EN_ALS_DR_INT is set to 1, then the V2000 shall issue an ALS data ready interrupt every ADC conversion cycle and assert the FLG_ALS_DR bit. The FLG_ALS_DR shall be cleared automatically after any one of the DATA_R/G/B/C[15:0] is be read out through I²C and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_DR_INT will not influence the FLG_ALS_DR status.

6.4 PS Operation

6.4.1 PS General Operation

The related PS control bits are summarized below.

PS Control Bits

| General Control | |
|-----------------------------|--|
| EN_PS | Enable PS function |
| EN_INTELLI_PRST | Enable PS intelligent persistence |
| IT_PS[3:0] | PS integration time |
| GAIN_PS[1:0] | PS gain control |
| PRST_PS[1:0] | PS persistence number |
| DATA_PS_OFFSET[15:0] | PS digital offset cancel |
| INTELLI_WAIT_PS[6:0] | PS intelligent persistence wait period |
| LED Control | |
| IRDR_LED[2:0] | Choose LED driving current |
| PS Interrupt Control | |
| PS_INT_MODE[2:0] | Choose PS interrupt mode. |
| EN_PS_INT | Enable PS function interrupt |
| EN_PS_DR_INT | Enable PS data ready interrupt |
| THDH_PS[15:0] | PS near-far detect high threshold |
| THDL_PS[15:0] | PS near-far detect low threshold |

PS Data/Status Bits

| Data | |
|---------------|--|
| DATA_PS[15:0] | 16-bits PS raw data |
| Status | |
| FLG_NF | Indicate the current object near/far state |
| FLG_PS_INT | Indicate the object near/far state changed event |
| FLG_PS_DR | Indicate the PS data ready event |

The proximity function is used for object detection by IR-sensitivity photodiode detection of reflected IR energy emitted by the built-in IR LED.

The DATA_PS[15:0] will be the ADC output subtract offset data defined in DATA_PS_OFFSET[15:0]. The PS data are 16-bit output and are stored in two bytes register. Higher byte register must be read first than lower byte. Data reading word protection is implemented to make sure the conversion data within the same conversion cycle could be read correctly. When the higher byte register is read, the lower 8-bit data will be stored into a shadow register which is read by the following sequential read or another single read to the lower byte register.

The FLG_NF is used to indicate the current object is in near or far state and persistence is also applied to this flag if PRST_PS > 1.

The FLG_PS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after the DATA_PS[15:0] is be read out through I²C.

IRDR_LED[2:0] is used to choose different LED constant driving current. V2000 has 8 different LED current

levels 3.125/6.25/12.5/25/50/100/150 mA.

6.4.2 PS Interrupt Description

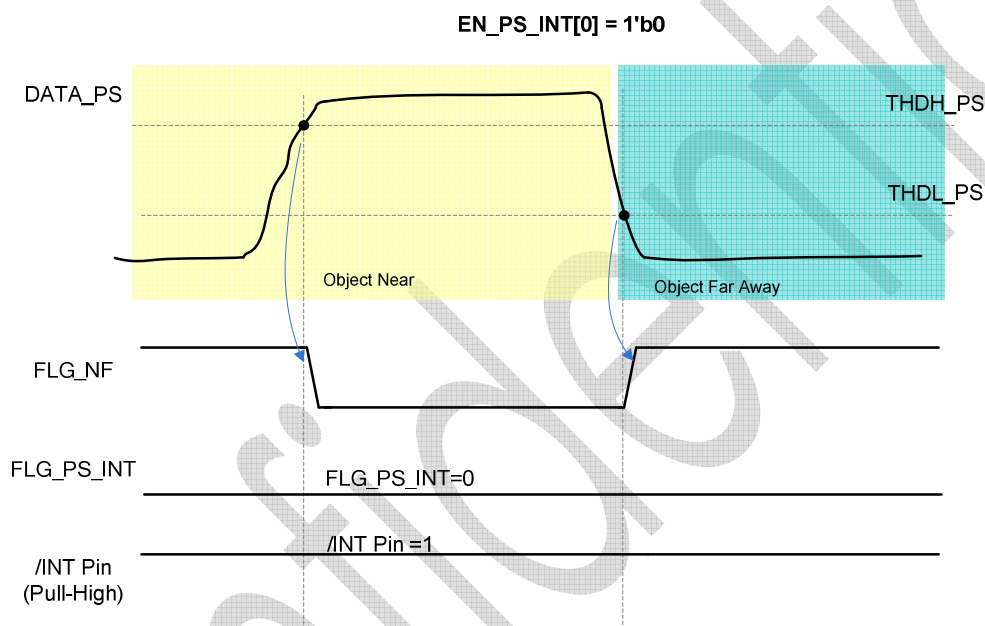
The EN_PS_INT[0] register is used to control PS interrupt function for enable or disable

The PS_NF_MODE[1] register is used to select how STK3630 reports the object near/far state to application.

The PS_INT_MODE[2] register is PS interrupt modes for near/far state change are described as below.

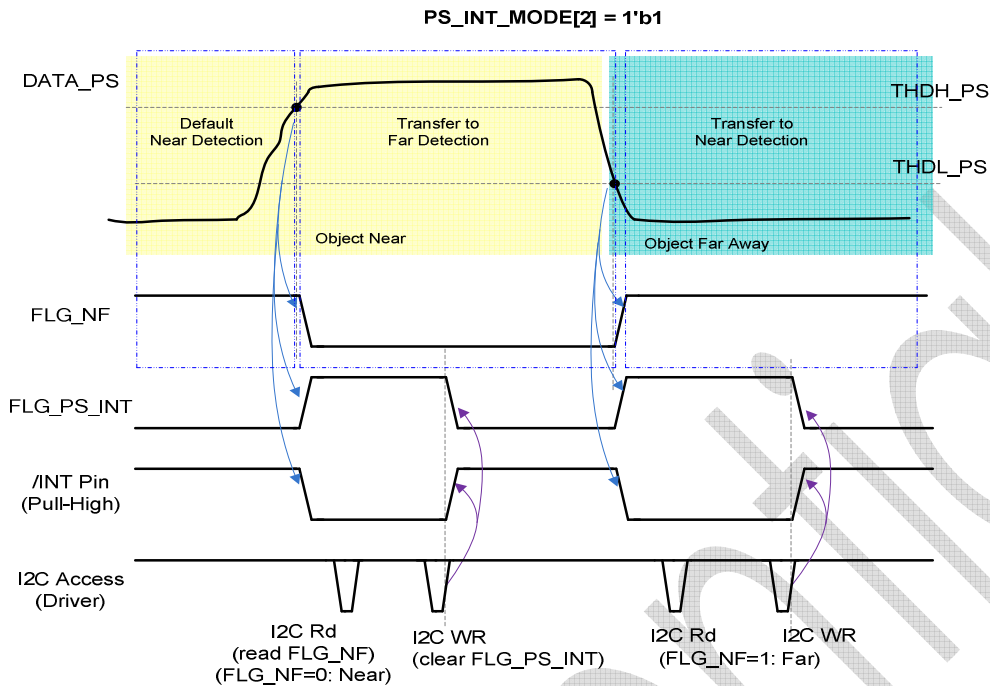
PS INT Function (EN_PS_INT[0] = 1'b0) & PS Near/Far Flag Mode (PS_NF_Mode[1] = 1'b0)

If EN_PS_INT[0] is set to 1'b0, then the polling mode is used and the INT pin is non-active when near/far event detected. In this mode, the INT output level is fixed to pull-high and the FLG_PS_INT will never be asserted. The application simply polls the FLG_NF to check the object in near or far state.



PS INT Function (EN_PS_INT[0] = 1'b1) & PS Near/Far Flag Mode (PS_NF_Mode[1] = 1'b0)

The INT pin is treated as interrupt signal. The FLG_NF is used to indicate whether the object is in near or far state. The V2000 is default in object far state and the FLG_NF = 1. Once the object moving close to the V2000 and PS code exceed the high threshold THDH_PS, V2000 will switch to object near state and the FLG_NF is cleared to 0. V2000 will issue a PS interrupt to inform the object near/far state changed and also set the FLG_PS_INT to 1. If the object move far away from the V2000 and PS code lower than the low threshold THDL_PS, V2000 will switch to object far state and the FLG_NF is set to 1. V2000 will also issue a PS interrupt to inform and set FLG_PS_INT. The FLG_PS_INT shall be cleared by write the bit 0 and shall be reset to 0 if POR/SWRst or EN_PS = 0. The FLG_NF shall be reset to 1 if POR/SWRst or EN_PS = 0. Change the PS_MODE will also clear the FLG_PS_INT to 0, but keep the current PS code and FLG_NF state.



PS persistence numbers PRST_PS[1:0] is used to avoid the false alarm of PS interrupt event due to environment noise. If PS persistence is set larger than 1, then the PS interrupt will not be issued until continuous persistence numbers of ADC conversion results meet the interrupt condition describe above.

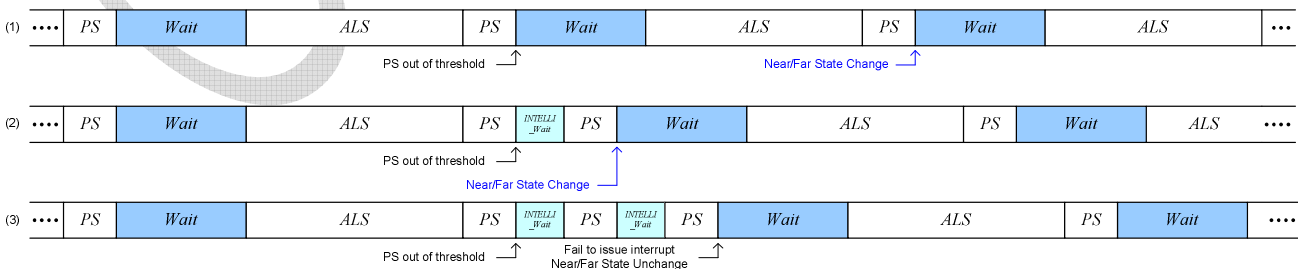
V2000 also provides intelligent persistence to speed up the response time and can be enabled by set EN_INTELLI_PRST to 1. Once the PS signal is exceed the high threshold when object in far state or lower than low threshold when in near state, EN_INTELLI_PRST = 1 and the PS persistence number PRST_PS[1:0] large than 1, the V2000 will enter the *PS_INTELLI_WAIT* PS function sub-state and use a shorter INTELLI_WAIT_PS period to perform the PS persistence check. This is used to shorten the PS response time and also avoid the flicker noise influence when choosing the right wait period. The V2000 shall return to the normal operation state loop no matter what PS persistence success or fail.

For example:

(1) PRST_PS[1:0] = 2'b01 (x2), EN_ALS = 1, EN_PS = 1, EN_WAIT = 1, EN_INTELLIGENT_PRST = 0

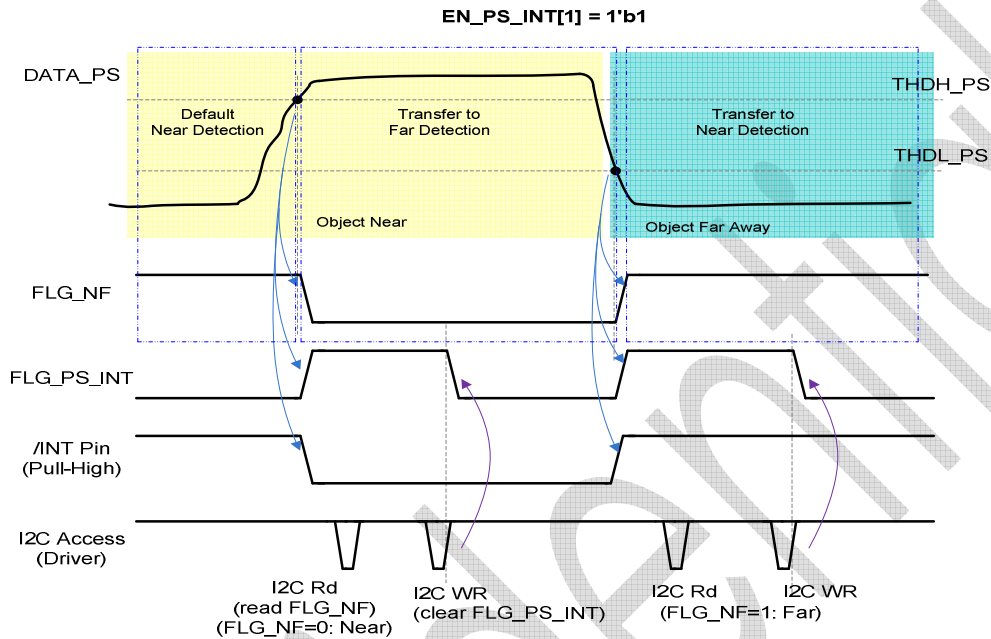
(2) PRST_PS[1:0] = 2'b01 (x2), EN_ALS = 1, EN_PS = 1, EN_WAIT = 1, EN_INTELLIGENT_PRST = 1

(3) PRST_PS[1:0] = 2'b10 (x4), EN_ALS = 1, EN_PS = 1, EN_WAIT = 1, EN_INTELLIGENT_PRST = 1 and fail to issue interrupt (no continue persistence numbers of PS ADC conversion results is out of threshold),



PS INT Function (EN PS INT[0] = 1'b1) & PS Near/Far Flag Mode (PS NF Mode[1] = 1'b1)

If PS_NF_MODE[1] = 1'b1, then the polling mode is used and the INT pin is treated as a near/far flag signal, not an interrupt signal. In this mode, the INT output level is same with the FLG_NF signal level and the FLG_PS_INT will never be asserted. The application simply polls the INT level (high or low) to check the object in near or far state. INT Pin is only from PS FLG_NF, and the ALS interrupt, Invalid PS interrupt is ignored.



PS Data Ready Interrupt

V2000 provides the PS data ready interrupt. Once the EN_PS_DR_INT is set to 1, then the V2000 shall issue a PS data ready interrupt every ADC conversion cycle and assert the FLG_PS_DR bit. The FLG_PS_DR shall be cleared automatically after the DATA_PS[15:0] is be read out through I2C and shall be reset to 0 if POR/SWRst or EN_PS = 0. Clear the EN_PS_DR_INT will not influence the FLG_PS_DR status.

6.5 Wait State Operation

6.5.1 Wait State General Operation

The related Wait control bits are summarized below.

| Wait Control Bits | |
|--------------------------|-------------------|
| General Control | |
| EN_WAIT | Enable Wait state |
| WAIT[7:0] | Wait period |

Wait state is used for power saving

7. CONTROL REGISTER MAP

| ADDR | REG NAME | BIT | | | | | | | | Default |
|------|---------------------------------|-------------------------|---------------|------------------------|----------------|--------------------|-----------------|-------------------------|------------------|---------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x00 | STATE | | | | EN_CTAU TOK | EN_INTELLI PRST | EN_WAIT | EN_ALS | EN_PS | 0x00 |
| 0x01 | PSCTRL | PRST_PS[1:0] | | GAIN_PS[1:0] | | IT_PS[3:0] | | | | 0x00 |
| 0x02 | ALSCTRL1 | PRST_ALS[1:0] | | GAIN_ALS[1:0] | | IT_ALS[3:0] | | | | 0x02 |
| 0x03 | LEDCTRL | IRDR_LED[2:0] | | | | | | EN_CTIRFC | EN_CTIR | 0xAC |
| 0x04 | INTCTRL1 | INT_CTRL | | EN_INVALID D_PS_INT | | EN_ALS_I NT | PS_INT_M ODE | PS_NF_MO DE | EN_PS_I NT | 0x00 |
| 0x05 | WAIT | WAIT[7:0] | | | | | | | | 0x00 |
| 0x06 | THDH1_PS | THDH_PS[15:8] | | | | | | | | 0xFF |
| 0x07 | THDH2_PS | THDH_PS[7:0] | | | | | | | | 0xFF |
| 0x08 | THDL1_PS | THDL_PS[15:8] | | | | | | | | 0x00 |
| 0x09 | THDL2_PS | THDL_PS[7:0] | | | | | | | | 0x00 |
| 0x0A | THDH1_ALS | THDH_ALS[15:8] | | | | | | | | 0xFF |
| 0x0B | THDH2_ALS | THDH_ALS[7:0] | | | | | | | | 0xFF |
| 0x0C | THDL1_ALS | THDL_ALS[15:8] | | | | | | | | 0x00 |
| 0x0D | THDL2_ALS | THDL_ALS[7:0] | | | | | | | | 0x00 |
| 0x10 | FLAG | FLG_ALS_ DR | FLG_PS_D R | FLG_ALS_I NT | FLG_PS_I NT | | FLG_ALS_S AT | FLG_INVALID D_PS_INT | FLG_NF | 0x01 |
| 0x11 | DATA1_PS | DATA_PS[15:8] | | | | | | | | 0x00 |
| 0x12 | DATA2_PS | DATA_PS[7:0] | | | | | | | | 0x00 |
| 0x13 | DATA1_ALS | DATA_ALS[15:8] | | | | | | | | 0x00 |
| 0x14 | DATA2_ALS | DATA_ALS[7:0] | | | | | | | | 0x00 |
| 0x1B | DATA1_C | DATA_C[15:8] | | | | | | | | 0x00 |
| 0x1C | DATA2_C | DATA_C[7:0] | | | | | | | | 0x00 |
| 0x1D | DATA1_PS_OFFSET | DATA_PS_OFFSET[15:8] | | | | | | | | 0x00 |
| 0x1E | DATA2_PS_OFFSET | DATA_PS_OFFSET[7:0] | | | | | | | | 0x00 |
| 0x20 | DATA_CTIR1 | DATA_CTIR1[7:0] | | | | | | | | 0x00 |
| 0x21 | DATA_CTIR2 | DATA_CTIR2[7:0] | | | | | | | | 0x00 |
| 0x22 | DATA_CTIR3 | DATA_CTIR3[7:0] | | | | | | | | 0x00 |
| 0x23 | DATA_CTIR4 | DATA_CTIR4[7:0] | | | | | | | | 0x00 |
| 0x3E | PDT_ID | PDT_ID[7:0] | | | | | | | | 0x5B |
| 0x3F | Reserved | Reserved | | | | | | | | |
| 0x4E | ALSCTRL2 | | | GAIN_C[1:0] | | | | | | 0x00 |
| 0x4F | INTELLI_WAIT_PS | INTELLI_WAIT_PS[6:0] | | | | | | | | 0x00 |
| 0x80 | SOFT_RESET | Write any to soft reset | | | | | | | | |
| 0xA1 | PSPDCTRL | PS_SEL | | | | | | | | 0x00 |
| 0xA5 | INTCTRL2 | | | | | | | EN_ALS_DR _INT | EN_PS_ DR_INT | 0x00 |
| 0xDB | AGCTRL | Reserved | | | | | | PS_CI[1:0] | | 0x15 |

STATE Register (0x00)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|----------------|---------------------|---------|--------|-------|
| ITEM | | | | EN_CTAU TOK | EN_INTEL LI_WAIT | EN_WAIT | EN_ALS | EN_PS |
| Access | | | | R/W | R/W | R/W | R/W | R/W |
| Default | | | | 0 | 0 | 0 | 0 | 0 |

| Bit | ITEM | Description |
|-----|-----------------|---|
| 0 | EN_PS | Enable the PS function. 0 : Disable 1 : Enable |
| 1 | EN_ALS | Enable the ALS/C function. 0 : Disable 1 : Enable |
| 2 | EN_WAIT | Enable the Wait state. 0 : Disable 1 : Enable |
| 3 | EN_INTELLI_PRST | Enable the intelligent persistence function. 0 : Disable 1 : Enable |
| 4 | EN_CTAUTOK | Enable the CTAUTOK function. 0 : Disable 1 : Enable |

PSCTRL Register (0x01)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|---|--------------|---|------------|---|---|---|
| ITEM | PRST_PS[1:0] | | GAIN_PS[1:0] | | IT_PS[3:0] | | | |
| Access | R/W | | R/W | | R/W | | | |
| Default | 2'b00 | | 2'b00 | | 4'b0000 | | | |

| Bit | ITEM | Description | | | | | | | | | | | | | | | | |
|---------|--------------|--|---------|-----------|---------|-----------|---------|-----------|---------|-----------|---------|---------|---------|---------|---------|---------|--------|----------|
| 3:0 | IT_PS[3:0] | PS integration time. <table border="1"> <tr> <td>4'b0000</td> <td>96 us</td> </tr> <tr> <td>4'b0001</td> <td>192 us</td> </tr> <tr> <td>4'b0010</td> <td>384 us</td> </tr> <tr> <td>4'b0011</td> <td>768 us</td> </tr> <tr> <td>4'b0100</td> <td>1.54 ms</td> </tr> <tr> <td>4'b0101</td> <td>3.07 ms</td> </tr> <tr> <td>4'b0110</td> <td>6.14 ms</td> </tr> <tr> <td>others</td> <td>Reserved</td> </tr> </table> | 4'b0000 | 96 us | 4'b0001 | 192 us | 4'b0010 | 384 us | 4'b0011 | 768 us | 4'b0100 | 1.54 ms | 4'b0101 | 3.07 ms | 4'b0110 | 6.14 ms | others | Reserved |
| 4'b0000 | 96 us | | | | | | | | | | | | | | | | | |
| 4'b0001 | 192 us | | | | | | | | | | | | | | | | | |
| 4'b0010 | 384 us | | | | | | | | | | | | | | | | | |
| 4'b0011 | 768 us | | | | | | | | | | | | | | | | | |
| 4'b0100 | 1.54 ms | | | | | | | | | | | | | | | | | |
| 4'b0101 | 3.07 ms | | | | | | | | | | | | | | | | | |
| 4'b0110 | 6.14 ms | | | | | | | | | | | | | | | | | |
| others | Reserved | | | | | | | | | | | | | | | | | |
| 5:4 | GAIN_PS[1:0] | PS gain setting. <table border="1"> <tr> <td>2'b00</td> <td>x 1 times</td> </tr> <tr> <td>2'b01</td> <td>x 2 times</td> </tr> <tr> <td>2'b10</td> <td>x 4 times</td> </tr> <tr> <td>2'b11</td> <td>x 8 times</td> </tr> </table> | 2'b00 | x 1 times | 2'b01 | x 2 times | 2'b10 | x 4 times | 2'b11 | x 8 times | | | | | | | | |
| 2'b00 | x 1 times | | | | | | | | | | | | | | | | | |
| 2'b01 | x 2 times | | | | | | | | | | | | | | | | | |
| 2'b10 | x 4 times | | | | | | | | | | | | | | | | | |
| 2'b11 | x 8 times | | | | | | | | | | | | | | | | | |

| | | | |
|-----|--------------|---|------------|
| 7:6 | PRST_PS[1:0] | PS persistence setting. The PS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-threshold PS occurrences before an interrupt is triggered. | |
| | | 2'b00 | x 1 times |
| | | 2'b01 | x 2 times |
| | | 2'b10 | x 4 times |
| | | 2'b11 | x 16 times |

ALSCTRL1 Register (0x02)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---------------|---|-------------|---|---|---|
| ITEM | PRST_ALS[1:0] | | GAIN_ALS[1:0] | | IT_ALS[3:0] | | | |
| Access | R/W | | R/W | | R/W | | | |
| Default | 2'b00 | | 2'b00 | | 4'b0010 | | | |

| Bit | ITEM | Description | |
|-----|---------------|--|------------|
| 3:0 | IT_ALS[3:0] | ALS integration time. | |
| | | 4'b0000 | 25 ms |
| | | 4'b0001 | 50 ms |
| | | 4'b0010 | 100 ms |
| | | 4'b0011 | 200 ms |
| | | 4'b0100 | 400 ms |
| | | 4'b0101 | 800 ms |
| | | 4'b0110 | 1600 ms |
| | | others | Reserved |
| 5:4 | GAIN_ALS[1:0] | ALS gain setting. GAIN_ALS[1:0] is used to control of the ALS channel signal gain. The Clear channel is controlled by GAIN_C[1:0]. | |
| | | 2'b00 | x 1 times |
| | | 2'b01 | x 4 times |
| | | 2'b10 | x 16 times |
| | | 2'b11 | x 64 times |
| 7:6 | PRST_ALS[1:0] | ALS persistence setting. The ALS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-windows ALS occurrences before an interrupt is triggered. | |
| | | 2'b00 | x 1 times |
| | | 2'b01 | x 2 times |
| | | 2'b10 | x 4 times |
| | | 2'b11 | x 8 times |

| BIT[3:0] | REFRESH TIME | Multiple of Base Refresh Time | Lux/LSB under GAIN_ALS=2'11 |
|----------|--------------|-------------------------------|-----------------------------|
| 0000 | 25ms | x1 | 0.0128 |
| 0001 | 50ms | x2 | 0.0064 |
| 0010 | 100ms | x4 | 0.0032 |

| | | | |
|------|--------|-----|--------|
| 0011 | 200ms | x8 | 0.0016 |
| 0100 | 400ms | x16 | 0.0008 |
| 0101 | 800ms | x32 | 0.0004 |
| 0110 | 1600ms | x64 | 0.0002 |

| BIT[5:4] | Gain | LUX/LSB under IT_ALS=4'b0010 |
|----------|------|------------------------------|
| 00 | x1 | 0.2051 |
| 01 | x4 | 0.0513 |
| 10 | x16 | 0.0128 |
| 11 | x64 | 0.0032 |

LEDCTRL Register (0x03)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|-----------|---------|
| ITEM | IRDR_LED[2:0] | | | | | | EN_CTIRFC | EN_CTIR |
| Access | R/W | | | | | | R/W | R/W |
| Default | 3'b101 | | | | | | 0 | 0 |

| Bit | ITEM | Description | | | | | | | | | | | | | | |
|--------|-----------------------|---|---------|-----------------------|-----------|----------------------|--------|----------------------|--------|--------------------|--------|--------------------|--------|---------------------|--------|---------------------|
| 7:5 | IRDR_LED[2:0] | <p>LED constant current setting. The V2000 provides different sinking ability for IRLED through setting IRDR.</p> <table border="1"> <tr> <td>3'b000</td> <td>3.125 mA current sink</td> </tr> <tr> <td>3'b001</td> <td>6.25 mA current sink</td> </tr> <tr> <td>3'b010</td> <td>12.5 mA current sink</td> </tr> <tr> <td>3'b011</td> <td>25 mA current sink</td> </tr> <tr> <td>3'b100</td> <td>50 mA current sink</td> </tr> <tr> <td>3'b101</td> <td>100 mA current sink</td> </tr> <tr> <td>3'b110</td> <td>150 mA current sink</td> </tr> </table> | 3'b000 | 3.125 mA current sink | 3'b001 | 6.25 mA current sink | 3'b010 | 12.5 mA current sink | 3'b011 | 25 mA current sink | 3'b100 | 50 mA current sink | 3'b101 | 100 mA current sink | 3'b110 | 150 mA current sink |
| 3'b000 | 3.125 mA current sink | | | | | | | | | | | | | | | |
| 3'b001 | 6.25 mA current sink | | | | | | | | | | | | | | | |
| 3'b010 | 12.5 mA current sink | | | | | | | | | | | | | | | |
| 3'b011 | 25 mA current sink | | | | | | | | | | | | | | | |
| 3'b100 | 50 mA current sink | | | | | | | | | | | | | | | |
| 3'b101 | 100 mA current sink | | | | | | | | | | | | | | | |
| 3'b110 | 150 mA current sink | | | | | | | | | | | | | | | |
| 1 | EN_CTIRFC | <p>If EN_CTIR and EN_CTAUTOK always set to 1. 0 : CTIR is auto mode. 1 : CTIR is manual mode. (To set DATA_CTIRn data can reduce sunlight effect.)</p> <table border="1"> <thead> <tr> <th>mode</th> <th>EN_CTAUTOK</th> <th>EN_CTIRFC</th> <th>EN_CTIR</th> </tr> </thead> <tbody> <tr> <td>Auto</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>Manual</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table> | mode | EN_CTAUTOK | EN_CTIRFC | EN_CTIR | Auto | 1 | 0 | 1 | Manual | 0 | 1 | 1 | | |
| mode | EN_CTAUTOK | EN_CTIRFC | EN_CTIR | | | | | | | | | | | | | |
| Auto | 1 | 0 | 1 | | | | | | | | | | | | | |
| Manual | 0 | 1 | 1 | | | | | | | | | | | | | |
| 0 | EN_CTIR | <p>Enable the CTIR function. 0 : Disable 1 : Enable</p> | | | | | | | | | | | | | | |

INTCTRL1 Register (0x04)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|---|-------------------|---|------------|------------------|---|---|
| ITEM | INT_CTRL | | EN_INVALID_PS_INT | | EN_ALS_INT | PS_INT_MODE[2:0] | | |
| Access | R/W | | R/W | | R/W | R/W | | |
| Default | 0 | | 0 | | 0 | 3'b000 | | |

| Bit | ITEM | Description |
|-----|-------------------|--|
| 2:0 | PS_INT_MODE[2:0] | Select PS interrupt mode. Refer to the PS interrupt description. |
| 3 | EN_ALS_INT | Enable the ALS out-of-windows interrupt. 0 : Disable 1 : Enable |
| 5 | EN_INVALID_PS_INT | Enable the Invalid PS interrupt. 0 : Disable 1 : Enable |
| 7 | INT_CTRL | 0 : Set /INT pin low if FLG_ALS_INT or FLG_ALS_DR or FLG_PS_INT or FLG_PS_DR high (logical OR) 1 : Set /INT pin low if FLG_ALS_INT and FLG_ALS_DR and FLG_PS_INT and FLG_PS_DR high (logical AND) |

WAIT Register (0x05)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---|---|---|---|---|---|---|
| ITEM | WAIT[7:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

| Bit | ITEM | Description |
|-----|-----------|---|
| 7:0 | WAIT[7:0] | PS/GS wait state period. wait period = (WAIT[7:0] + 1) * 1.54 ms |

THDH1_PS Register (0x06)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|---|
| ITEM | THDH_PS[15:8] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b11111111 | | | | | | | |

THDH2_PS Register (0x07)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|---|---|---|---|---|---|---|
| ITEM | THDH_PS[7:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b11111111 | | | | | | | |

THDL1 PS Register (0x08)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|---|
| ITEM | THDL_PS[15:8] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

THDL2 PS Register (0x09)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|---|---|---|---|---|---|---|
| ITEM | THDL_PS[7:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

| Bit | ITEM | Description |
|------|---------------|--------------------|
| 15:0 | THDH_PS[15:0] | PS high threshold. |
| 15:0 | THDL_PS[15:0] | PS low threshold. |

THDH1 ALS Register (0x0A)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|---|---|---|---|---|---|---|
| ITEM | THDH_ALS[15:8] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b11111111 | | | | | | | |

THDH2 ALS Register (0x0B)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|---|
| ITEM | THDH_ALS[7:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b11111111 | | | | | | | |

THDL1 ALS Register (0x0C)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|---|---|---|---|---|---|---|
| ITEM | THDL_ALS[15:8] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

THDL2 ALS Register (0x0D)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|---|
| ITEM | THDL_ALS[7:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

| Bit | ITEM | Description |
|------|----------------|---------------------|
| 15:0 | THDH_ALS[15:0] | ALS high threshold. |
| 15:0 | THDL_ALS[15:0] | ALS low threshold. |

FLAG Register (0x10)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------------|-----------|-------------|------------|---|-------------|--------------------|--------|
| ITEM | FLG_ALS_DR | FLG_PS_DR | FLG_ALS_INT | FLG_PS_INT | | FLG_ALS_SAT | FLG_INVALID_PS_INT | FLG_NF |
| Access | R/W | R/W | R/W | R/W | | RO | R/W | RO |
| Default | 0 | 0 | 0 | 0 | | 0 | 0 | 1 |

| Bit | ITEM | Description |
|-----|--------------------|---|
| 0 | FLG_NF | Object near/far flag. Default FLG_NF = 1, object in far state. 0 : Object in near state 1 : Object in far state |
| 1 | FLG_INVALID_PS_INT | Indicate if interrupt event is related to INVALID_PS_INT. Write bit 0 to clear. 0 : No INVALID_PS_INT event 1 : INVALID_PS_INT event |
| 2 | FLG_ALS_SAT | Indicate the ALS channel circuit saturation. 0 : No ALS channel circuit saturation, the data is valid. 1 : ALS channel circuit saturation, the data is not valid. |
| 4 | FLG_PS_INT | Indicate if interrupt event is related to PS_INT. Write bit 0 to clear. 0 : No PS_INT event 1 : PS_INT event |
| 5 | FLG_ALS_INT | Indicate if interrupt event is related to ALS_INT. Write bit 0 to clear. 0 : No ALS_INT event 1 : ALS_INT event |
| 6 | FLG_PS_DR | Indicate PS data conversion complete. Automatically cleared after DATA_PS[15:0] is read. 0: PS data is not ready 1: PS data is ready |
| 7 | FLG_ALS_DR | Indicate ALS data conversion complete. Automatically cleared after DATA_ALS[15:0] is read. 0: ALS data is not ready 1: ALS data is ready |

DATA1 PS Register (0x11)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|---|
| ITEM | DATA_PS[15:8] | | | | | | | |
| Access | RO | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA2 PS Register (0x12)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|---|---|---|---|---|---|---|
| ITEM | DATA_PS[7:0] | | | | | | | |
| Access | RO | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

The V2000 has two 8-bit read-only registers to hold the data from ADC of PS. The most significant bit (MSB) is accessed at register 0x11, and the least significant bit (LSB) is accessed at register 0x12. The registers are updated for every PS integration time (conversion cycle).

DATA1 ALS Register (0x13)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|---|---|---|---|---|---|---|
| ITEM | DATA_ALS[15:8] | | | | | | | |
| Access | RO | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA2 ALS Register (0x14)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|---|
| ITEM | DATA_ALS[7:0] | | | | | | | |
| Access | RO | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA1 C Register (0x1B)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|---|---|---|---|---|---|---|
| ITEM | DATA_C[15:8] | | | | | | | |
| Access | RO | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA2 C Register (0x1C)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---|---|---|---|---|---|---|
| ITEM | DATA_C[7:0] | | | | | | | |
| Access | RO | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

The V2000 has two 8-bit read-only registers to hold each data from ADC of ALS/C. The registers are updated for every ALS/C integration time (conversion cycle).

DATA1 PS OFFSET Register (0x1D)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------------|---|---|---|---|---|---|---|
| ITEM | DATA_PS_OFFSET[15:8] | | | | | | | |
| Access | RW | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA2 PS OFFSET Register (0x1E)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------------|---|---|---|---|---|---|---|
| ITEM | DATA_PS_OFFSET[7:0] | | | | | | | |
| Access | RW | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA CTIR1 Register (0x20)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|---|---|---|---|---|---|---|
| ITEM | DATA_CTIR1[7:0] | | | | | | | |
| Access | RW | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA CTIR2 Register (0x21)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|---|---|---|---|---|---|---|
| ITEM | DATA_CTIR2[7:0] | | | | | | | |
| Access | RW | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA CTIR3 Register (0x22)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|---|---|---|---|---|---|---|
| ITEM | DATA_CTIR3[7:0] | | | | | | | |
| Access | RW | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

DATA CTIR4 Register (0x23)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|---|---|---|---|---|---|---|
| ITEM | DATA_CTIR4[7:0] | | | | | | | |
| Access | RW | | | | | | | |
| Default | 8'b00000000 | | | | | | | |

Product ID (0x3E)

Read Only; PDT_ID = Product ID=0x5A to indicate the product information.

Reserved (0x3F)

Read Only; RSRVD = Reserved for engineering mode.

ALSCTRL2 Register (0x4E)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---|---|---|---|---|---|---|
| ITEM | GAIN_C[1:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 2'b00 | | | | | | | |

| Bit | ITEM | Description | | | | | | | | |
|-------|-------------|---|-------|-----------|-------|-----------|-------|------------|-------|------------|
| 5:4 | GAIN_C[1:0] | Clear channel gain setting. GAIN_C[1:0] is used to control of the Clear channel signal gain. The ALS are controlled by GAIN_ALS[1:0]. | | | | | | | | |
| | | <table border="1"> <tr> <td>2'b00</td> <td>x 1 times</td> </tr> <tr> <td>2'b01</td> <td>x 4 times</td> </tr> <tr> <td>2'b10</td> <td>x 16 times</td> </tr> <tr> <td>2'b11</td> <td>x 64 times</td> </tr> </table> | 2'b00 | x 1 times | 2'b01 | x 4 times | 2'b10 | x 16 times | 2'b11 | x 64 times |
| 2'b00 | x 1 times | | | | | | | | | |
| 2'b01 | x 4 times | | | | | | | | | |
| 2'b10 | x 16 times | | | | | | | | | |
| 2'b11 | x 64 times | | | | | | | | | |

INTELLI WAIT PS Register (0x4F)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------------|---|---|---|---|---|---|---|
| ITEM | INTELLI_WAIT_PS[6:0] | | | | | | | |
| Access | R/W | | | | | | | |
| Default | 7'b0000000 | | | | | | | |

| Bit | ITEM | Description |
|-----|----------------------|---|
| 6:0 | INTELLI_WAIT_PS[6:0] | PS wait state period for intelligent persistence. wait period = (INTELLI_WAIT_PS[6:0] + 1) * 390us |

Soft reset (0x80)

Write any data to this register will reset the chip.

PSPDCTRL Register (0xA1)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--------|--------|--------|--------|
| ITEM | | | | | PS_PS3 | PS_PS2 | PS_PS1 | PS_PS0 |
| Access | | | | | R/W | R/W | R/W | R/W |
| Default | | | | | 1 | 1 | 1 | 1 |

| Bit | ITEM | Description |
|-----|--------|--|
| 0 | PS_PS0 | Enable the PS0 PD . 0 : Disable 1 : Enable |
| 1 | PS_PS1 | Enable the PS1 PD . 0 : Disable |

| | | |
|---|--------|--|
| | | 1 : Enable |
| 2 | PS_PS2 | Enable the PS2 PD . 0 : Disable 1 : Enable |
| 3 | PS_PS3 | Enable the PS3 PD . 0 : Disable 1 : Enable |

INTCTRL2 Register (0xA5)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---------------|--------------|
| ITEM | | | | | | | EN_ALS_DR_INT | EN_PS_DR_INT |
| Access | | | | | | | R/W | R/W |
| Default | | | | | | | 0 | 0 |

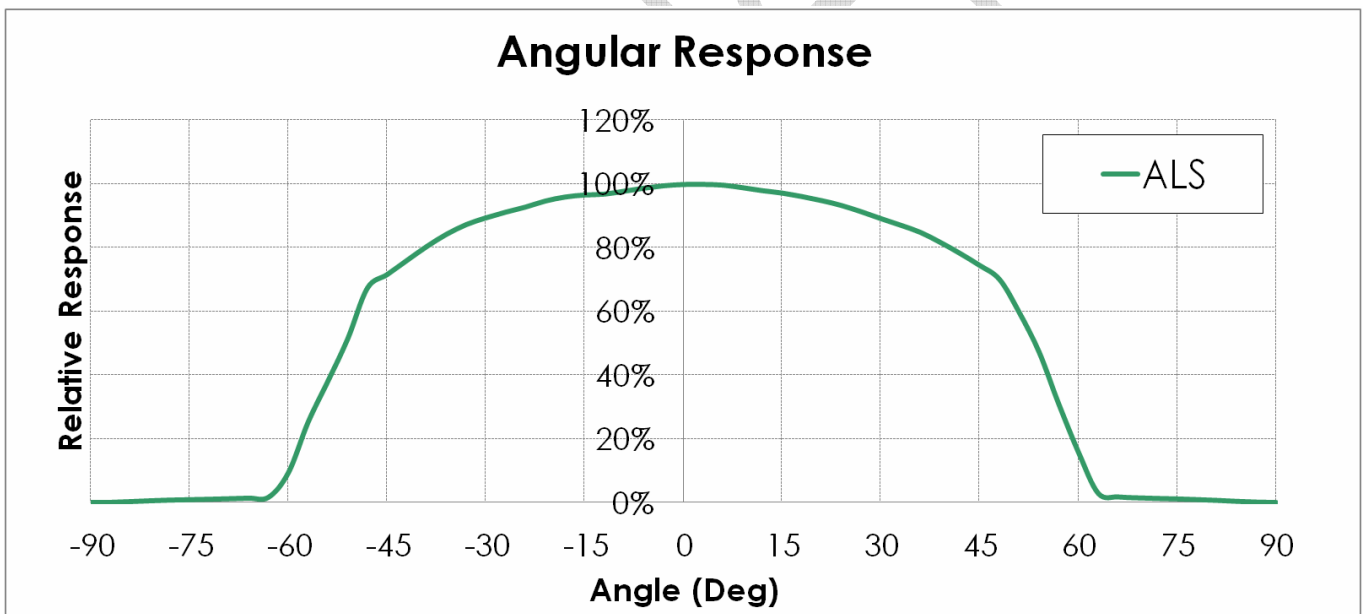
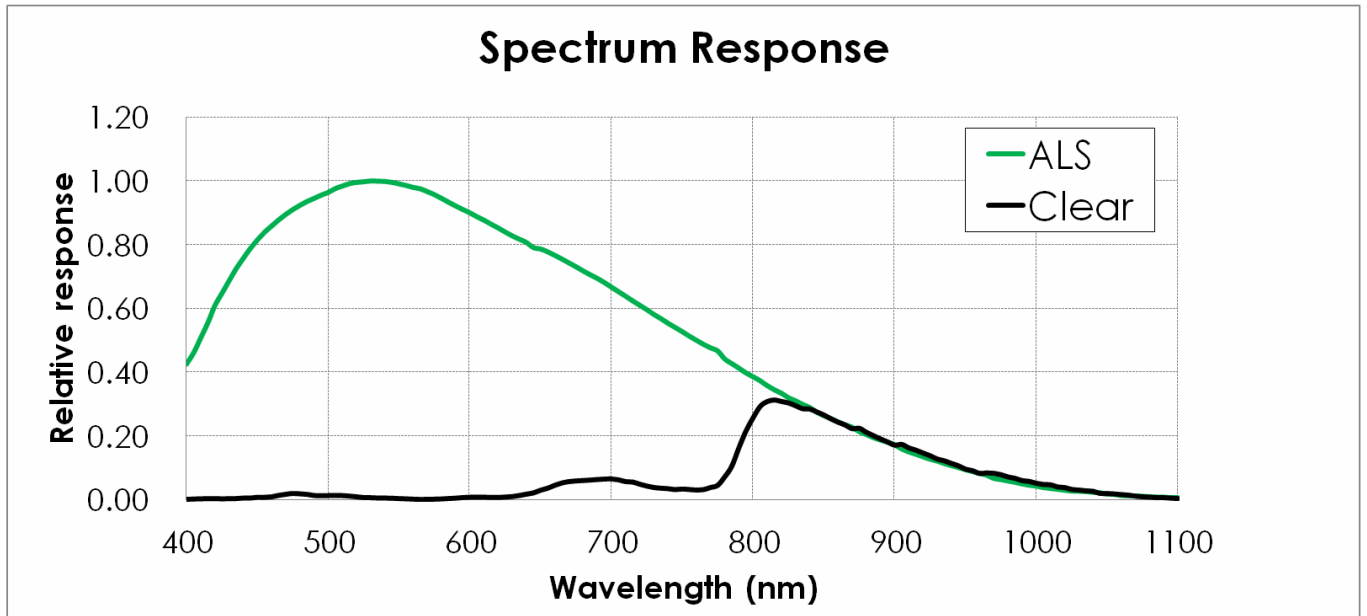
| Bit | ITEM | Description |
|-----|---------------|---|
| 0 | EN_PS_DR_INT | Enable the PS Data Ready interrupt. 0 : Disable 1 : Enable |
| 1 | EN_ALS_DR_INT | Enable the ALS Data Ready interrupt. 0 : Disable 1 : Enable |

AGCTRL Register (0xDB)

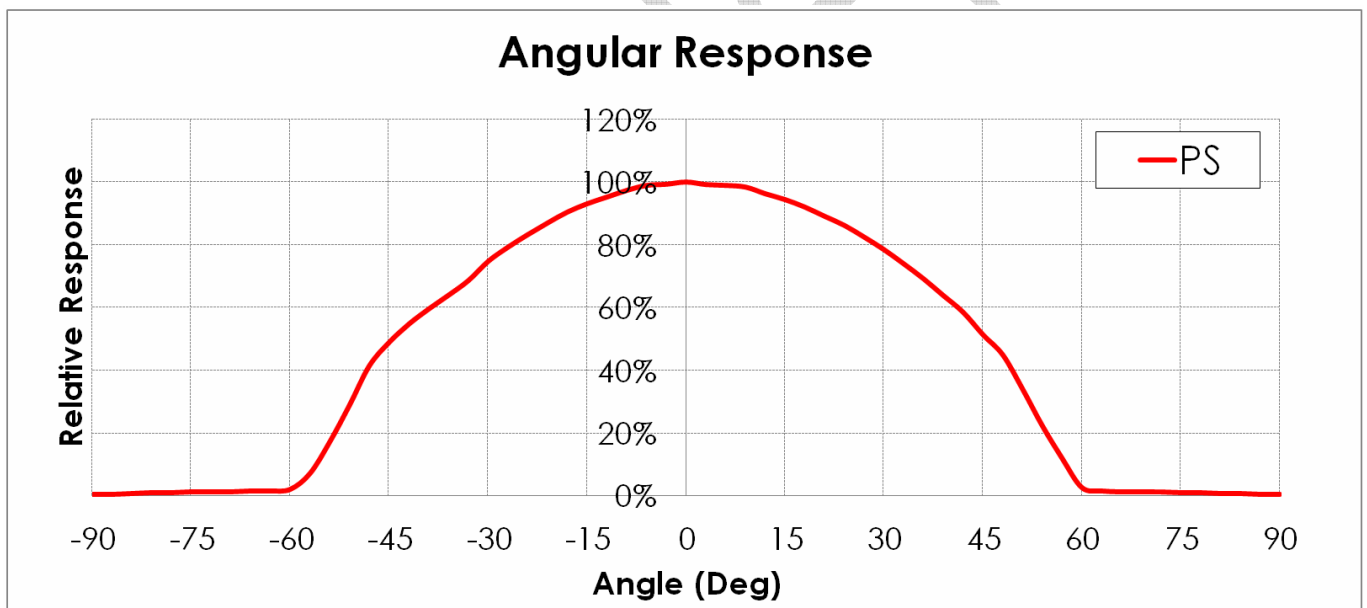
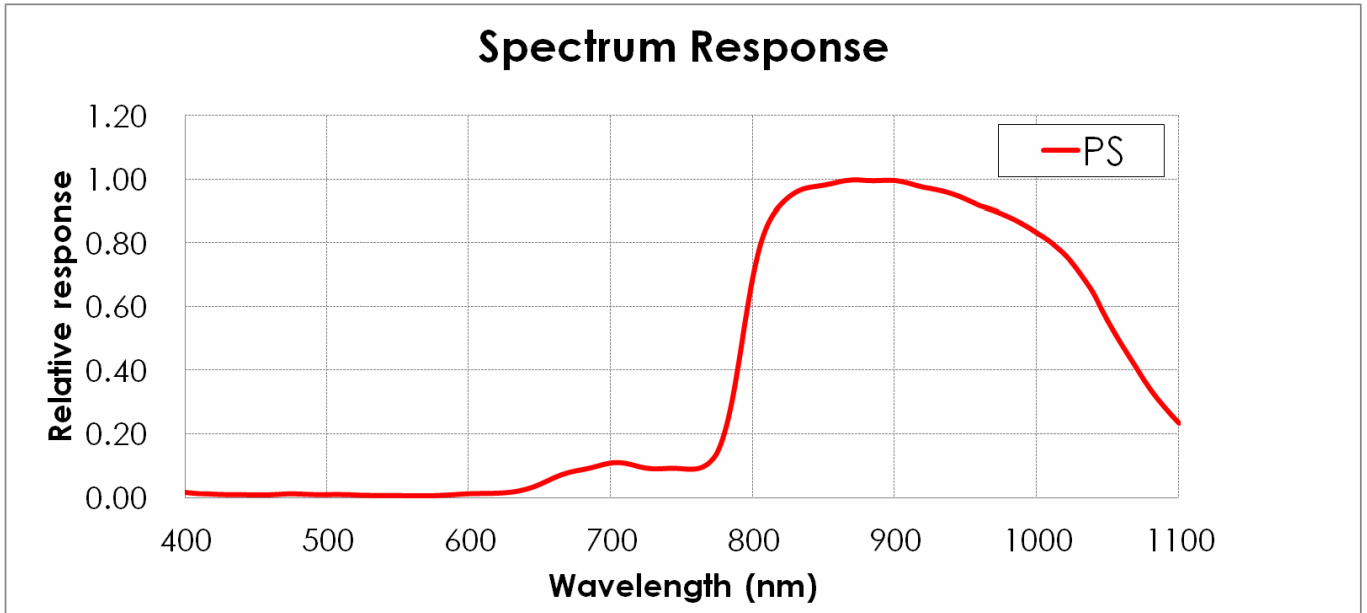
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---------|------------|---|
| ITEM | | | | | | | PS_CI[1:0] | |
| Access | | | | | | R/W | R/W | |
| Default | | | | | | 4'b0101 | 2'b01 | |

| Bit | ITEM | Description | | | | | | | | |
|-------|------------|---|-------|-----|-------|-----|-------|-------|-------|--------|
| 1:0 | PS_CI[1:0] | PS channel analog gain setting. <table border="1" data-bbox="502 1444 837 1579"> <tr> <td>2'b00</td> <td>x 2</td> </tr> <tr> <td>2'b01</td> <td>x 1</td> </tr> <tr> <td>2'b10</td> <td>x 0.5</td> </tr> <tr> <td>2'b11</td> <td>x 0.25</td> </tr> </table> | 2'b00 | x 2 | 2'b01 | x 1 | 2'b10 | x 0.5 | 2'b11 | x 0.25 |
| 2'b00 | x 2 | | | | | | | | | |
| 2'b01 | x 1 | | | | | | | | | |
| 2'b10 | x 0.5 | | | | | | | | | |
| 2'b11 | x 0.25 | | | | | | | | | |

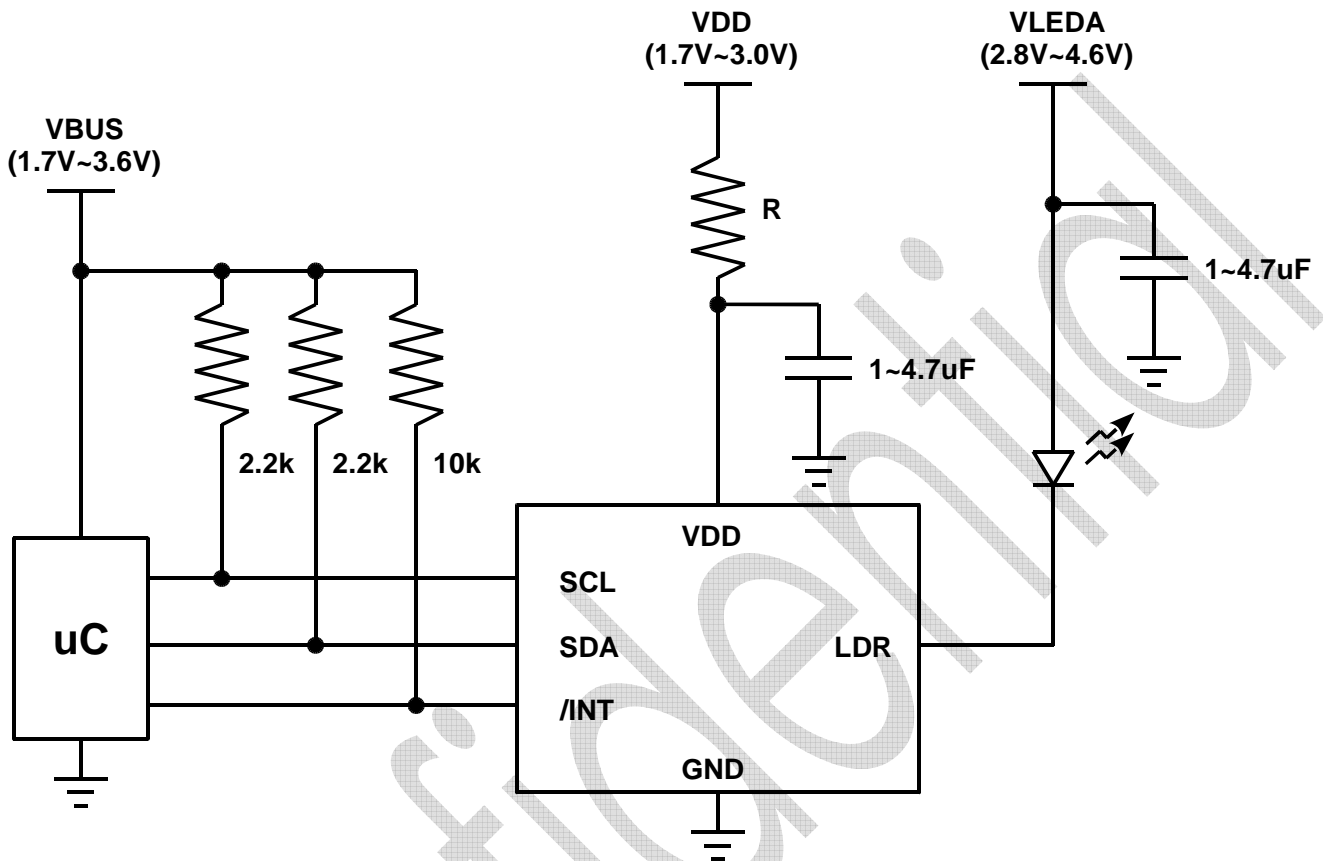
8. ALS RESPONSE CHARTS



9. PROXIMITY CHARACTERISTIC



10. APPLICATION NOTE



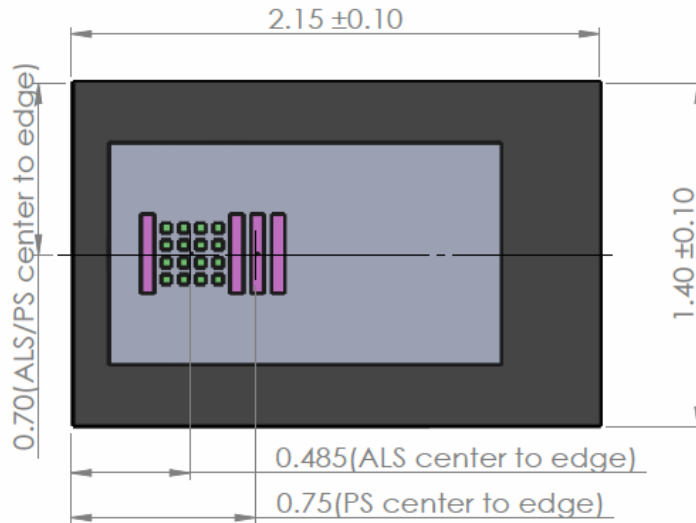
V2000 Typical Application Circuit with Independent VDD and VLED Supply Voltage

10.1 Power Noise Consideration

It is suggested that IC power and V_{LED} comes from individual source to get the best performance of V2000 and an R/C low pass filter is also suggested to be added in the V_{DD} path of V2000 to reduce the switching noise from whole system. The recommended R value is 22 Ohm.

11. PACKAGE OUTLINE

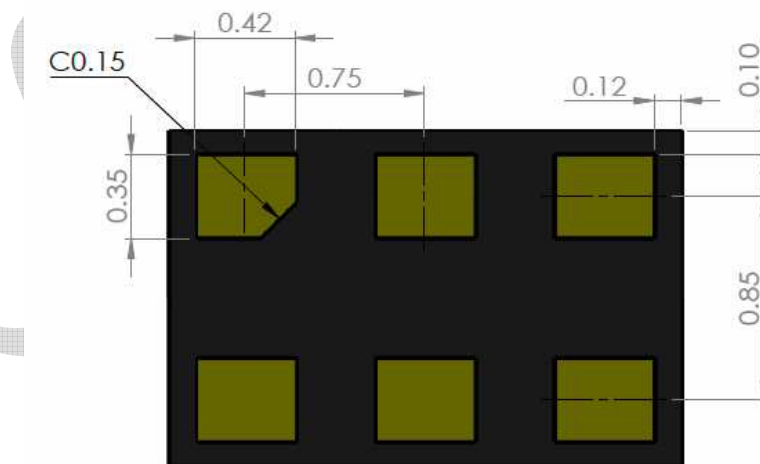
Top View



Side View



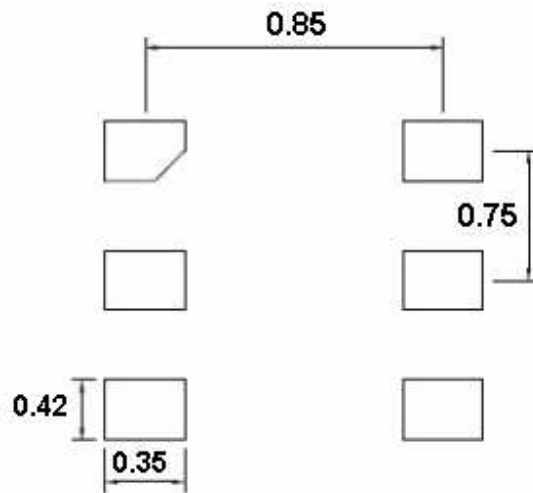
Bottom View



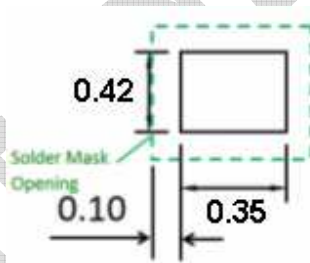
PCB Pad Layout and Solder Mask Define Recommendation

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are shown below.

PCB Pad Layout



Solder Mask Define

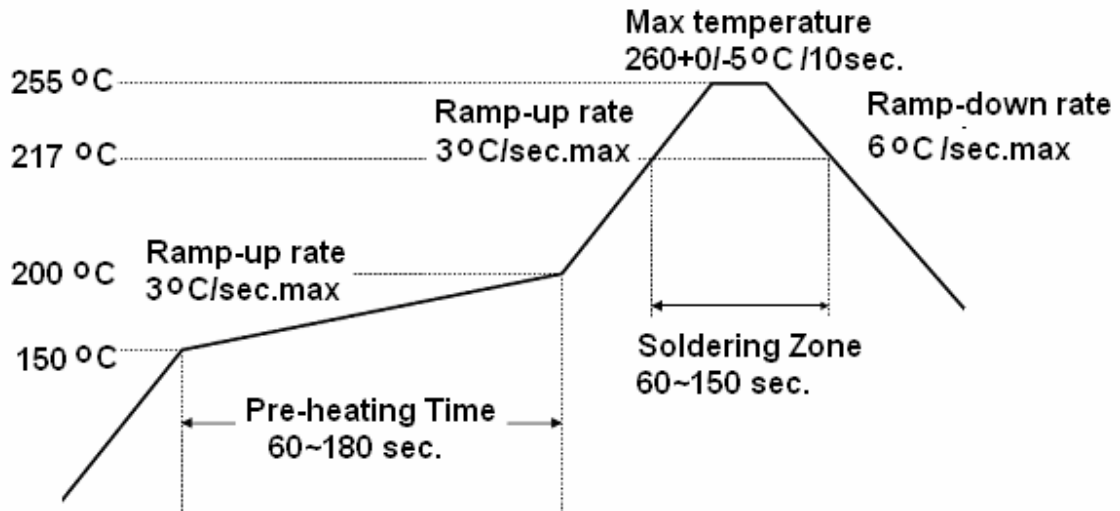


Notes: all linear dimensions are in mm.

12. SOLDERING INFORMATION

12.1 Soldering Condition

0. Pb-free solder temperature profile



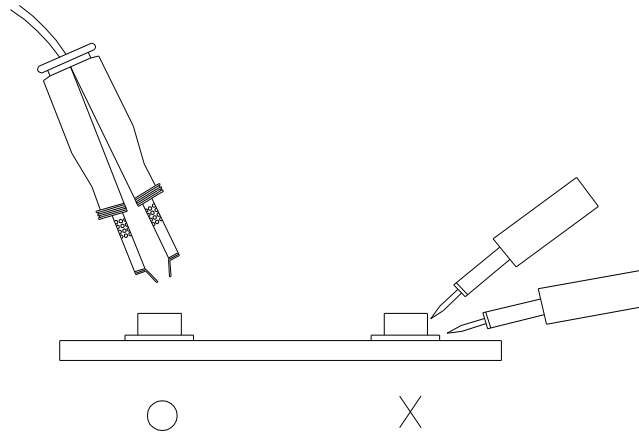
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the ICs during heating.
4. After soldering, do not warp the circuit board.

12.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350°C for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

12.3 Repairing

Repair should not be done after the ICs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the ICs will or will not be damaged by repairing.



13. STORAGE INFORMATION

13.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

| | |
|---------------------|-------------|
| Storage Temperature | -40 to 85°C |
| Relatively Humidity | below 60%RH |

13.2 Treatment After Unsealed

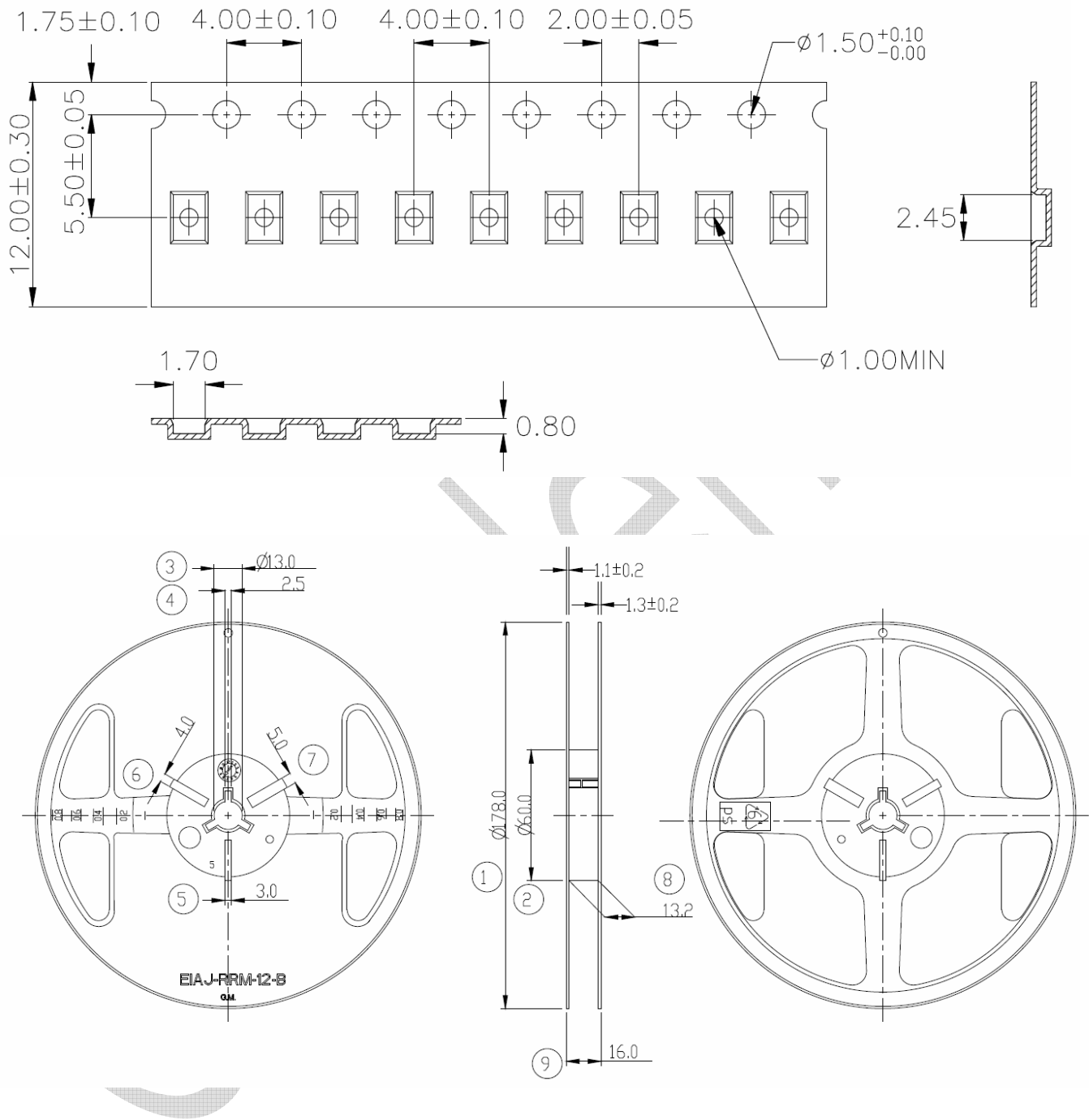
1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

| | |
|---------------------|-------------|
| Floor Life | 168 Hours |
| Storage Temperature | 10 to 30°C |
| Relatively Humidity | below 60%RH |

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

| | |
|----------------|----------|
| Temperature | 60°C |
| Re-Baking Time | 12 Hours |

14. TAPE AND REEL DIMENSION



Notes: all linear dimensions are in mm.

Revision History

| Date | Version | Modified Items |
|------------|---------|------------------|
| 2018/09/18 | 1.0 | Initial release. |
| | | |

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