MINGDA MICROELECTRONICS

MD8942
36V, 1.1MHz, 0.6A Synchronous Step-Down Converter

FEATURES

- 130uA Quiescent Current
- Wide Operating Input Range 4V to 36V
- Standoff Input Voltage: 42V
- 650mΩ/650mΩ Internal Power MOSFET
- 1.1MHz Fixed Switching Frequency
- Internal Compensation
- High Efficiency: > 90%
- Cycle-by-Cycle Over Current Protection
- Internal Soft-Start
- 3uA Low Shutdown Supply Current
- SOT23-6L Package

APPLICATIONS

- High Voltage Power Conversion
- Automotive Applications
- Industrial distributed power applications
- Battery Powered Equipment
- OA instrument

PRODUCT DESCRIPTION

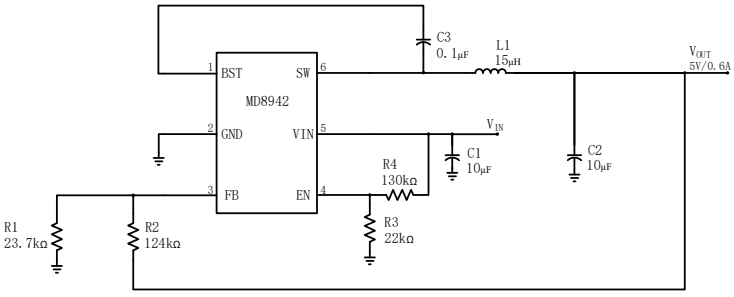
The MD8942 is a high frequency (1.1MHz) synchronous step-down, DC-DC converter with integrated internal high-side and low-side high voltage power MOSFET. It provides 0.6A (or less) highly efficient output.

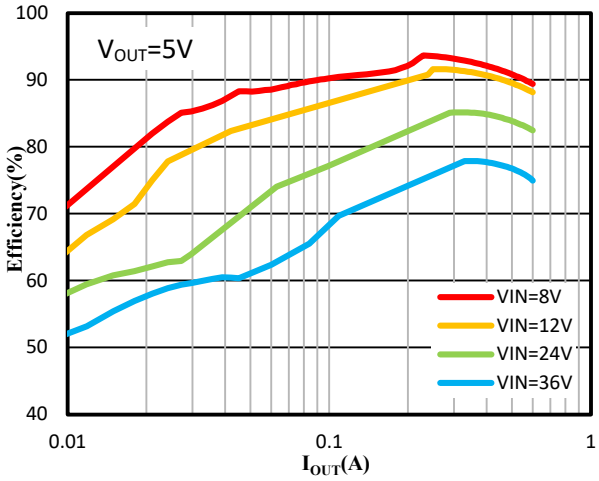
The wide 4V to 36V input range allows a variety of applications in automotive environment, and 3uA shutdown quiescent current allow applications in battery power systems.

Additional protection features are included such as Over Current Protection, Thermal Shutdown and Under Voltage Lockout.

The MD8942 is available in the cost-effective SOT23-6L packages.

TYPICAL APPLICATION

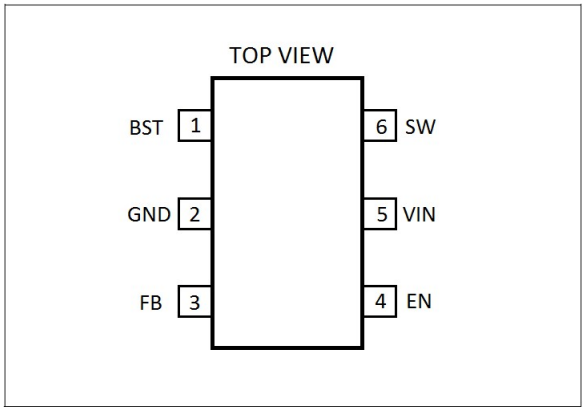




ORDER INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING INFORMATION
MD8942	--	SOT23-6L	Tape and Reel, 3000	--

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}).....-0.3V to 42V
Switch Voltage (V_{SW})….....-0.3V to $V_{IN\ (MAX)}$ + 0.3V
BST to SW.....-0.3V to 6V
Enable (V_{EN}) 6V
Enable Sink Current (V_{EN}) 100μA
All Other Pins..... -0.3V to 6V Storage
Temperature Range…….-65 ℃ to +150
Junction Temperature.....150℃
Operating Temperature Range.....-40℃ to +85℃

Package Thermal Resistance @ T_A = +25℃
SOT23-6L, θ_{JA}.....220℃/W
Lead Temperature (Soldering 10sec).....260℃

NOTE:

1) Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device.
2) These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.
3) Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD		2	kV

ELECTRICAL CHARACTERISTICS

T_A=25℃, V_{IN} = 12V, V_{EN} = 2V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Standoff Voltage	V_{IN_S}	V_{EN} = 0V	42			V
Input Voltage Range	V_{IN_R}		4		36	V
VIN UVLO Up Threshold	V_{UVLO_U}		3.2	3.6	3.9	V
VIN UVLO Hysteresis	V_{UVLO_HYS}			0.3		V
Feedback Voltage	V_{FB}	4.8V < V_{IN} < 36V, Iout=10mA	0.778	0.794	0.810	V
High-Side Switch on Resistance	R_{ON_HS}	V_{BST}-V_{SW}=5V		650		mOhms
Low-Side Switch on Resistance	R_{ON_LS}			650		mOhms
High-Side Switch Leakage	$I_{SW\_HS\_LKG}$	V_{EN} = 0V, V_{SW} = 0V		0.1		μA
Low-Side Switch Leakage	$I_{SW\_LS\_LKG}$	V_{EN} = 0V, V_{SW} = V_{IN}		0.2		μA
Peak Inductor Current Limit	I_{HS_Limit}			1.2		A
COMP to Current Sense Transconductance	G_{CS}			2.7		A/V
Soft-start time	T_{SS}	V_{FB} from 0 to 0.8V		0.5		msec
Oscillator Frequency	f_{SW}		880	1100	1320	kHz
Foldback Frequency	f_{SW_F}			80		kHz
Minimum Switch on Time	τ_{ON}			100		ns
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		3		μA
Average Quiescent Supply Current	I_Q	No load, V_{FB} = 0.9V		130		μA
Thermal Shutdown	T_{SD}			155		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			20		℃
Enable up Threshold	V_{EN_U}			1		V
Enable Threshold Hysteresis	V_{EN_HYS}			0.16		V
Enable Clamping Voltage				5		V
Enable Pull-Down Resistance				430		kOhms

PIN FUNCTIONS

Pin#	Name	Description
1	BST	SW FET Gate Bias voltage. Connect Cboot cap between BST and SW
2	GND	Ground Connection. It should be connected as close as possible to the output capacitor avoiding the high current switch paths
3	FB	Feedback Pin: Set feedback voltage divider ratio with V_{OUT} = V_{FB} (1+(R2/R1))
4	EN	Enable input. Pulling this pin below the specified threshold shuts the chip down. Pulling it above the specified threshold enables the chip. Floating this pin shuts the chip down
5	VIN	Input Supply.
6	SW	Switch node. This is the output from the high-side switch and low-side switch.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10uF, C2 = 10uF, L1 = 15uH and T_A=25℃, unless otherwise noted.

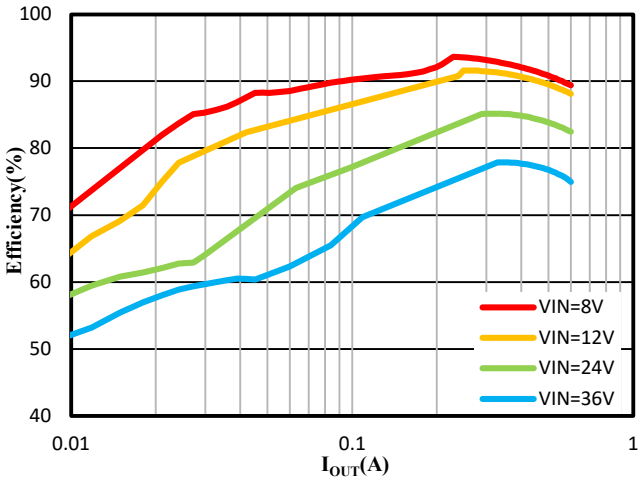


Figure 1. Efficiency, V_{OUT}=5V

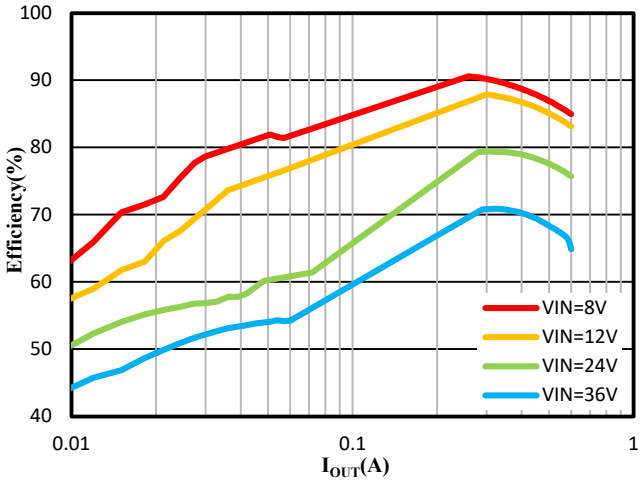


Figure 2. Efficiency, V_{OUT}=3.3V

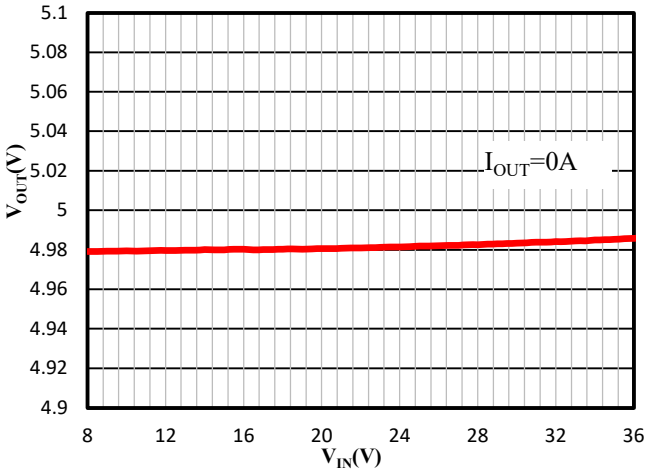


Figure 3. Line Regulation

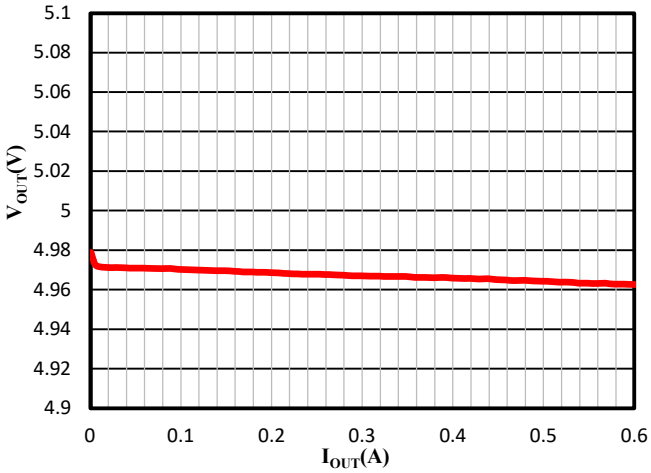


Figure 4. Load Regulation

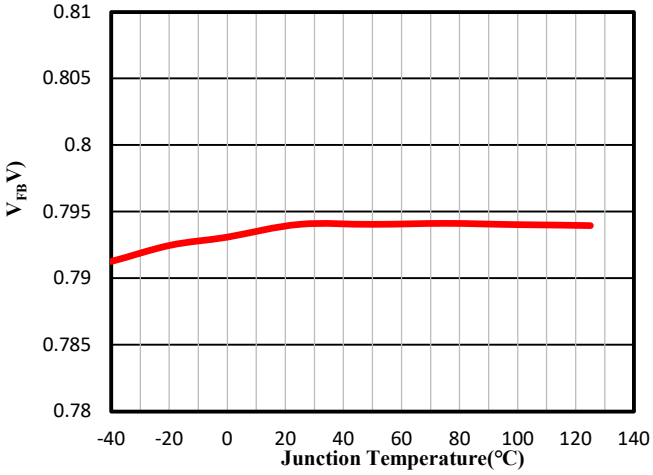


Figure 5. V_{FB} vs. Junction Temperature

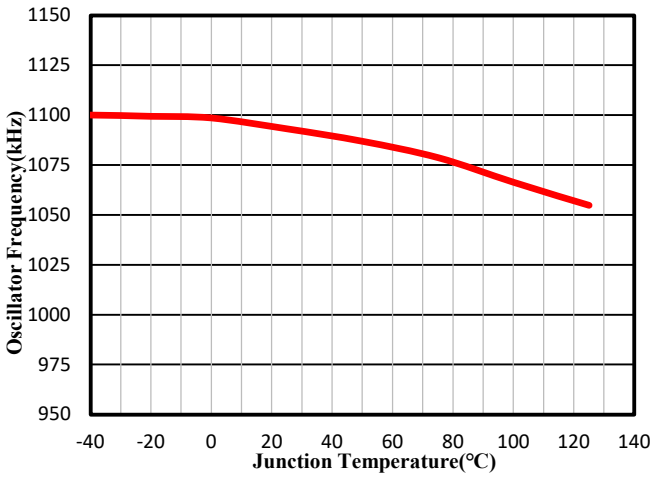


Figure 6. Oscillator Frequency vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10uF, C2 = 10uF, L1 = 15uH and T_A=25℃, unless otherwise noted.

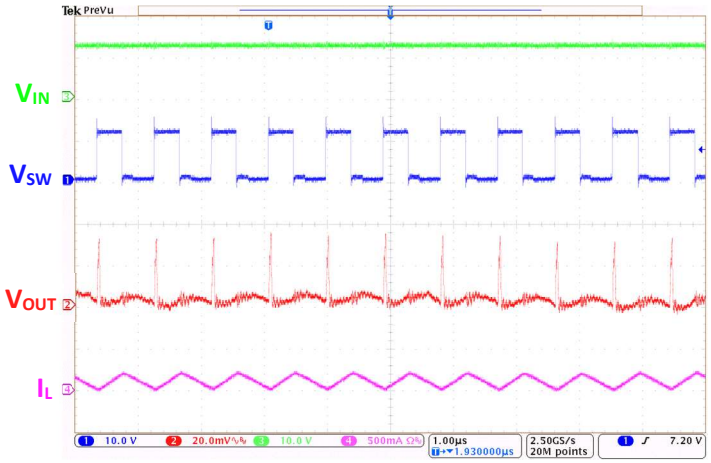


Figure 7. Steady State, I_{OUT}=0.1A

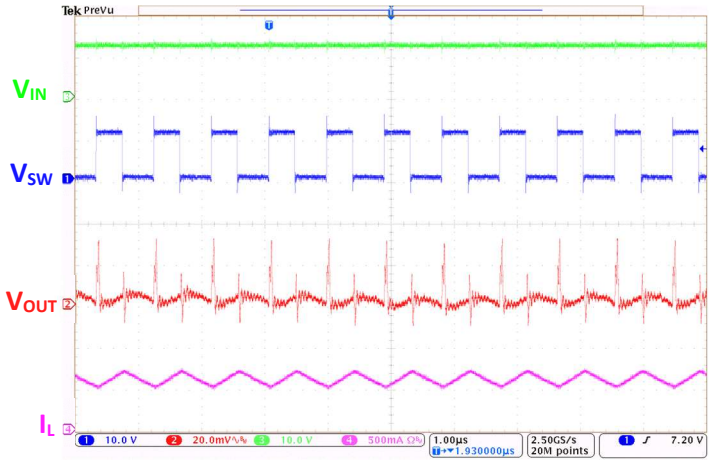


Figure 8. Steady State, I_{OUT}=0.6A

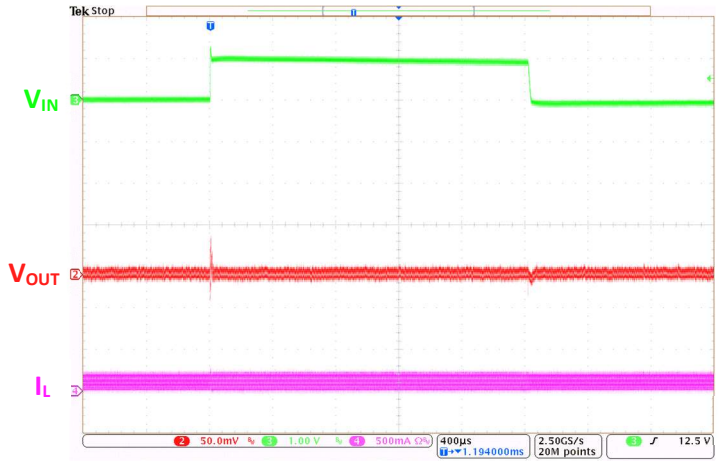


Figure 9. Line Transient V_{IN}=12V to 13V, I_{OUT}=0.1A

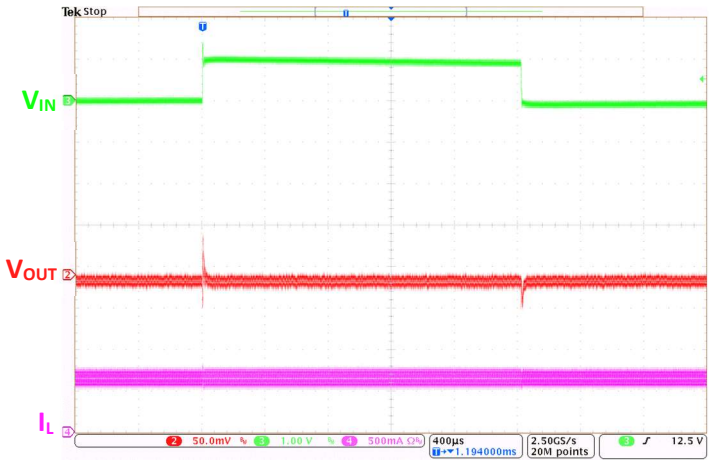


Figure 10. Line Transient V =12V to 13V, I_{OUT}=0.6A

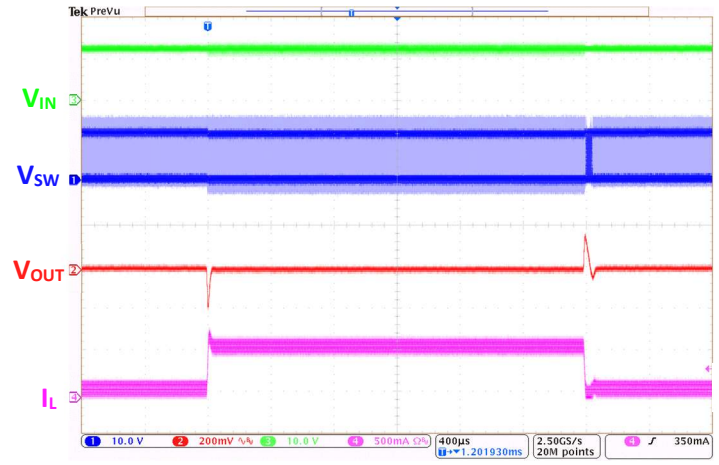


Figure 11. Load Transient, I_{OUT}=0.1A to 0.6A

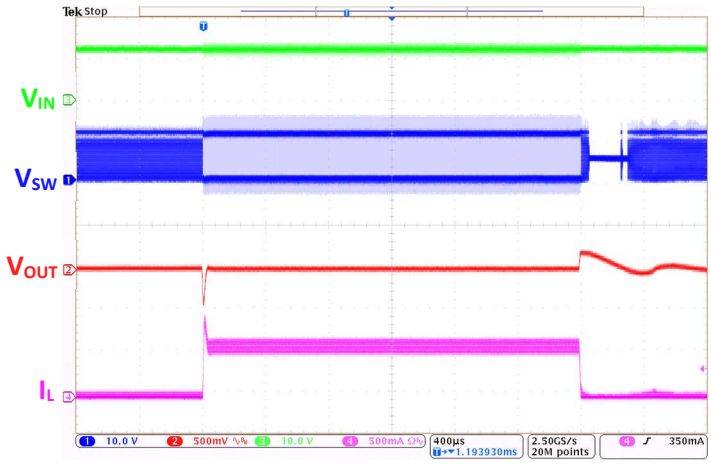


Figure 12. Load Transient, I_{OUT}=0.01A to 0.6A

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10uF, C2 = 10uF, L1 = 15uH and T_A=25℃, unless otherwise noted.

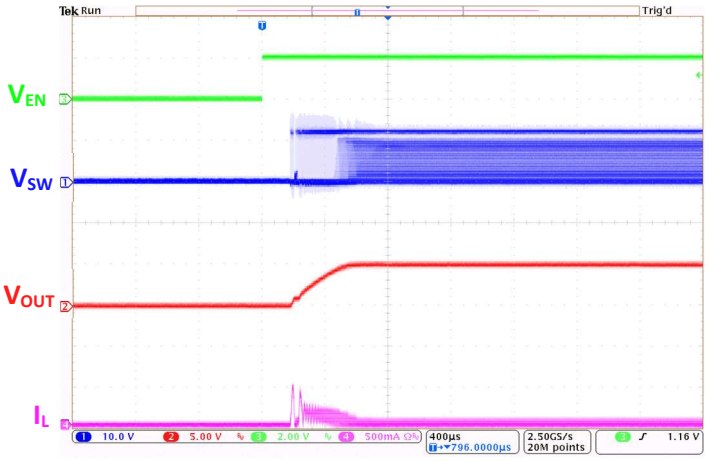


Figure 13. Startup Through EN, I_{OUT}=0.01A

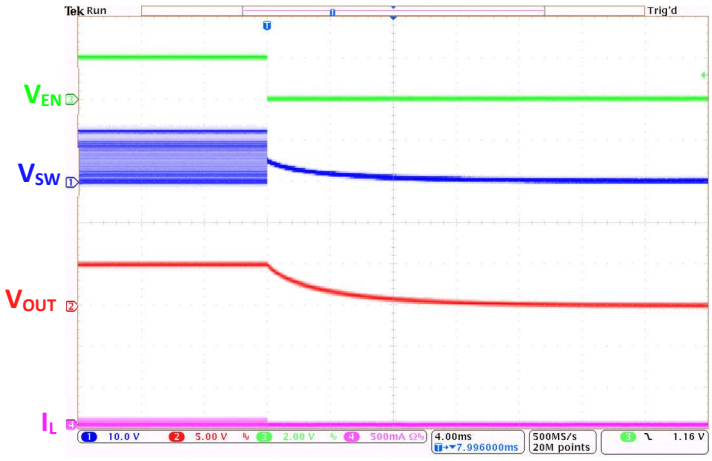


Figure 14. Shutdown Through EN, I_{OUT}=0.01A

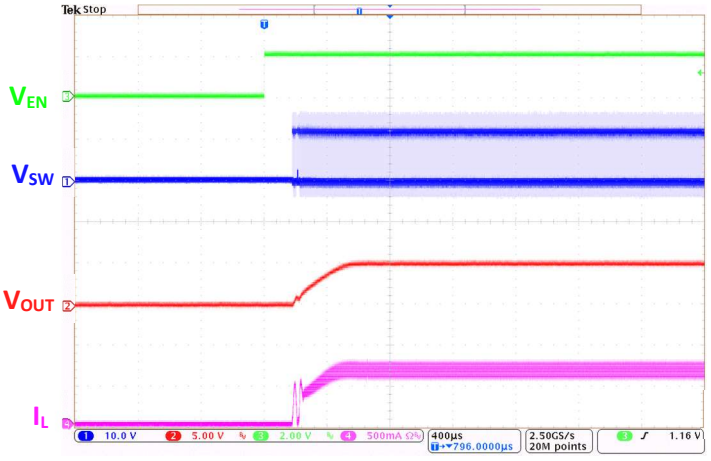


Figure 15. Startup Through EN, I_{OUT}=0.6A

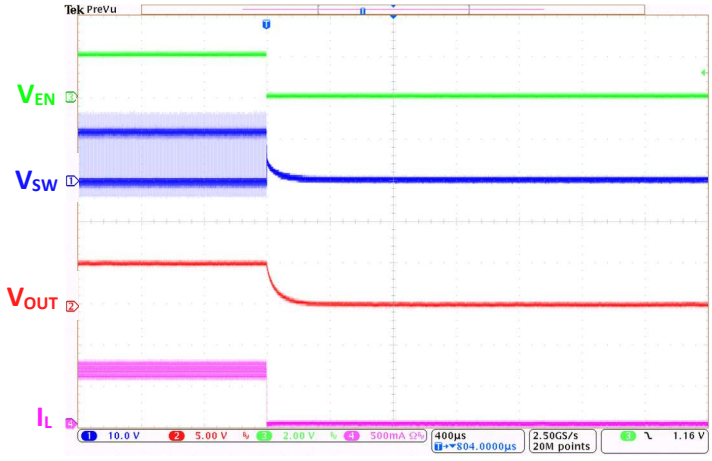


Figure 16. Shutdown Through EN, I_{OUT}=0.6A

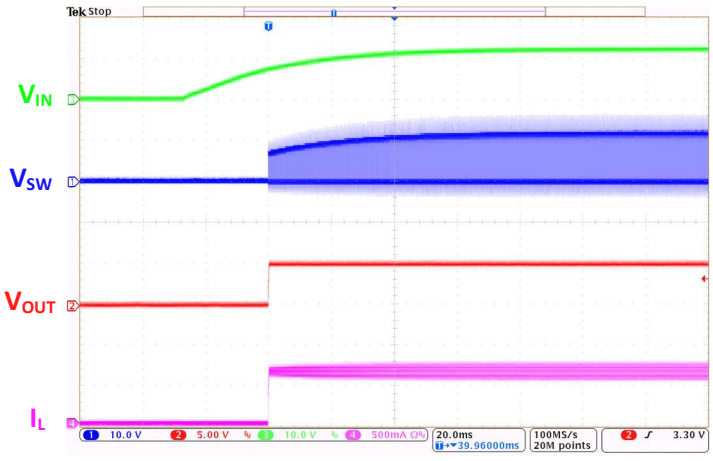


Figure 17. Power Ramp Up, I_{OUT}=0.6A

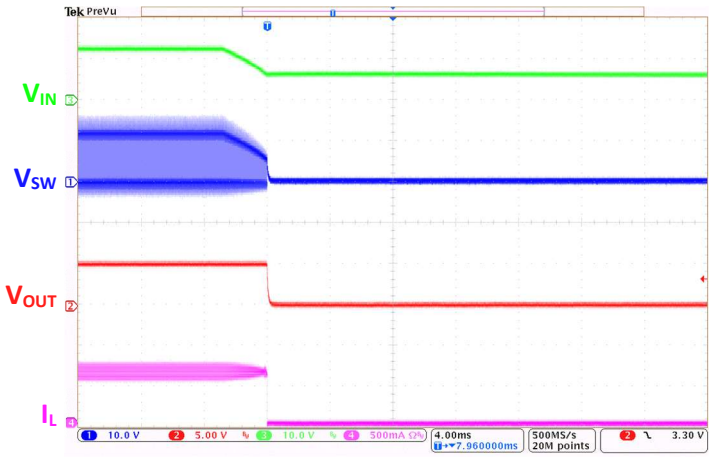


Figure 18. Power Ramp Down, I_{OUT}=0.6A

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, C1 = 10uF, C2 = 10uF, L1 = 15uH and T_A=25℃, unless otherwise noted.

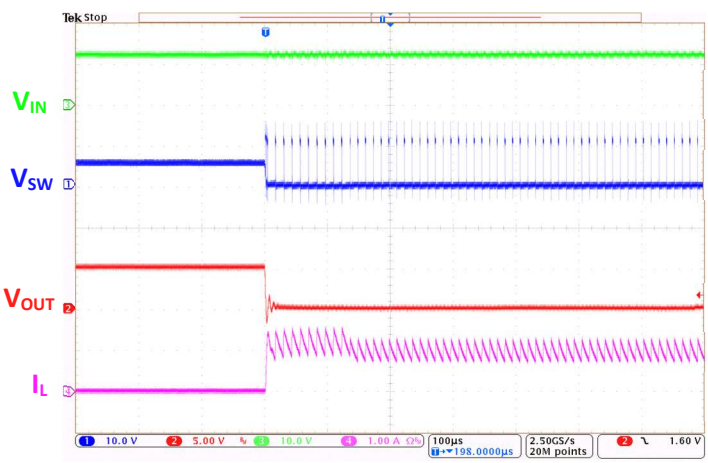


Figure 19. Short Circuit Entry, I_{OUT}=0A to Short

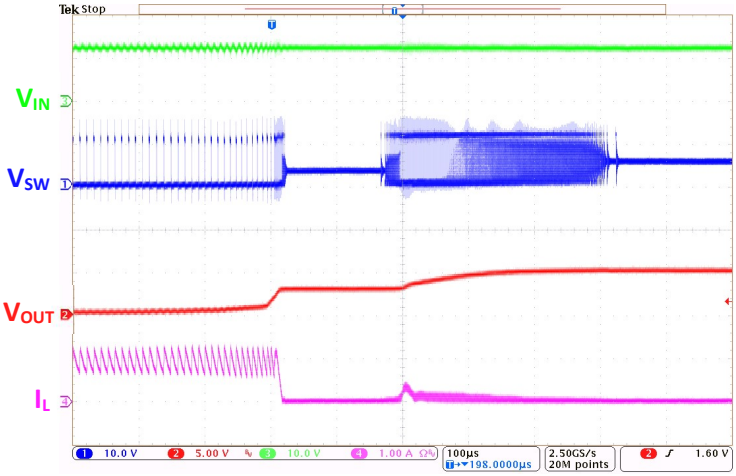


Figure 20. Short Circuit Recovery, I_{OUT}=Short to 0A

FUNCTION BLOCK DIAGRAM

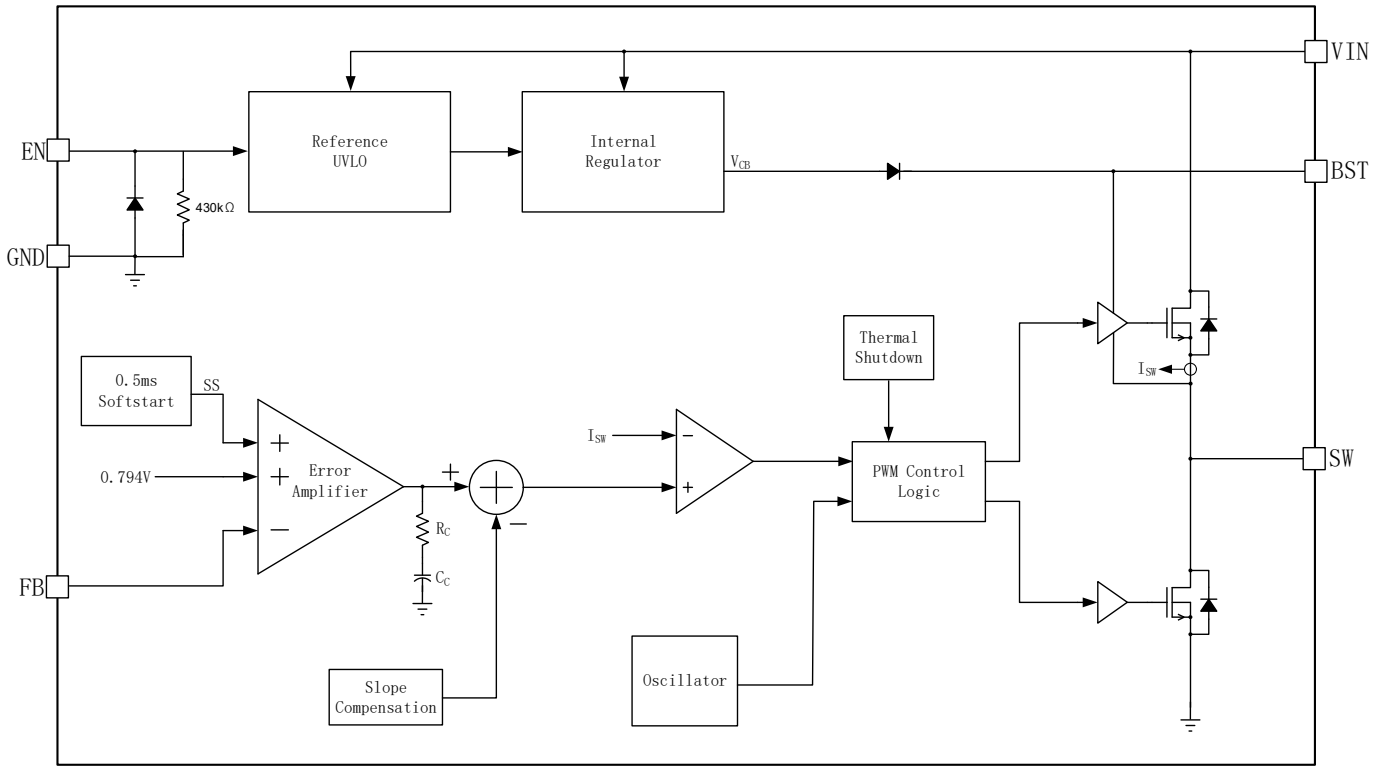


Figure 21. Function Block Diagram

OPERATION

The MD8942 is a 1.1MHz, synchronous, step-down switching regulator with integrated internal high-side and low-side high voltage power MOSFET. It provides internally compensated single 0.6A highly efficient output with current mode control. It features wide input voltage range, internal soft- start control, and precision current limit. Its very low operational quiescent current suits it for battery powered applications.

PWM Control

At moderate to high output current, the MD8942 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The power MOSFET is turned on and remains on until its current reaches the value set by COMP voltage. When the power switch is off, it remains off for at least 50ns before the next cycle starts. If, in one PWM period, the current in the power MOSFET does not reach COMP set current value, the power MOSFET remains on until that maximum duty cycle has reached.

Pulse Skipping Mode

At light load condition, the MD8942 goes into pulse skipping mode to improve light load efficiency. Pulse skipping decision is based on its internal COMP voltage. If COMP is lower than the internal sleep threshold, a PAUSE command is generated to block the turn-on clock pulse so the power MOSFET is not commanded ON subsequently, saving gate driving and switching losses. This PAUSE command also puts the whole chip into sleep mode, consuming very low quiescent current to further improve the light load efficiency. When COMP voltage is higher than the sleep threshold, the PAUSE signal is reset so the chip is back into normal PWM operation. Every time when the PAUSE changes states from low to high, a turn-on signal is generated right away, turning on the power MOSFET.

Error Amplifier

The Error amplifier is composed of an internal OP-AMP with an R-C Compensation network connected between its output node (internal COMP node) and its GND node (GND). When FB is lower than its internal reference voltage (REF), the COMP output is then driven higher by the OP-AMP, causing higher switch peak current output hence more energy delivered to the output. Vise versus.

When connecting to the FB pin, normally there is a voltage divider composed of R_{UP} and R_{DN} where R_{DN} is between FB and GND while R_{UP} is between the voltage output node and FB. R_{UP} serves also to control the gain of the error amplifier along with the internal compensation R- C network.

Internal Regulator

Most of the internal circuitry is powered on by the 4V internal regulator. This regulator takes V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 4.5V, the output of the regulator is in full regulation. When V_{IN} is lower, the output degrades.

Enable Control

The MD8942 has a dedicated enable control pin EN. With high enough V_{IN}, the chip can be enabled and disabled by EN pin. This is a HIGH effective logic. Its rising threshold is 1V typically and its trailing threshold is about 160mV lower. When floating, EN pin is internally pulled down to GND so the chip is disabled.

When EN is pulled down to 0V, the chip is put into the lowest shutdown current mode. When EN is higher than zero but lower than its rising threshold, the chip is still in shutdown mode but the shutdown current increases slightly.

Internally a zener diode is connected from EN pin to GND pin. An internal 430kΩ resistor from EN to GND allows EN to be floated to shut down the chip. The typical clamping voltage of the zener diode is 5V. So, V_{IN} can be connected to EN through a high ohm resistor if the system doesn't have logic input acting as enable signal. The resistor needs to be designed to limit the EN pin sink current less than 100μA.

Under Voltage Lockout (UVLO)

V_{IN} Under voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 4.5V while its trailing threshold is about 200mV lower.

Internal Soft-start

Reference type soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V at a slow pace set by the soft-start time. When it is lower than the internal reference REF, SS overrides the REF so the error amplifier uses SS instead of REF as the reference. When SS is higher than REF, REF gains the control back.

A function is designed to accommodate the short-circuit recovery situation. When a short-circuit is removed, the SS ramps up as if it is a fresh soft-start process. This prevents output voltage overshoot.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. When the silicon die temperature is higher than its upper threshold, it shuts down the whole chip. When the temperature is lower than its lower threshold, thermal shutdown is gone so the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is about 1.6V with a threshold of about 100mV. The bootstrap capacitor is charged to about 5V by the dedicated internal supply V_{CB}. When the voltage between SW and GND nodes is lower than its V_{CB}, a diode connected from V_{CB} to BST is turned on. The charging current path is from V_{IN}, V_{CB}, BST and then to SW. External circuit should provide enough voltage headroom to facilitate the charging.

When the power MOSFET is ON, V_{IN} is about equal to SW so the bootstrap capacitor cannot be charged. When the external freewheeling diode is on, V_{IN} to SW difference is the largest so it is the best period to charge. When there is no current in the inductor, SW equals to

the output voltage V_{OUT}, so the difference between V_{CB} and V_{OUT} can be used to charge the bootstrap capacitor. At higher duty cycle operation condition, the time period available to the bootstrap charging is less so the bootstrap capacitor may not be charged sufficiently.

In case the external circuit has not sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage in normal operation region.

The floating driver's UVLO is not communicated to the controller.

Current Comparator and Current Limit

The high side power MOSFET current is accurately sensed via a current sense MOSFET. It is then fed to the high-speed current comparator for the current mode control purpose. The current comparator takes this sensed current as one of its inputs. When the power MOSFET is turned on, the comparator is first blanked till the end of the turn- on transition to dodge the noise. Then, the comparator compares the power switch current with COMP voltage. When the sensed current is higher than COMP voltage, the comparator outputs low, turning off the power MOSFET. The maximum current of the internal power MOSFET is internally limited cycle by cycle.

Startup and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents and then the internal regulator is enabled. The regulator provides stable supply for the rest circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET OFF for about 16usec to blank the startup glitches. When the internal soft-start block is enabled, it first holds its SS output low to ensure the rest circuitries are ready and then slowly ramps up.

Three events shut down the chip: EN low, V_{IN} low, thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. COMP voltage and the internal supply rail are pulled down then. The floating driver is not subject to this shutdown command but its charging path is disabled.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT}\frac{R1}{R1 + R2}$$

Thus the output voltage is:

$$V_{OUT} = V_{FB}\frac{R1 + R2}{R1}$$

The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor.

Choose R2 around 124kΩ for optimal transient response. R1 is then given by:

$$R1 = \frac{R2}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1– Resistor Selection vs. V_{OUT}

V_{OUT} (V)	R2 (kΩ)	R1 (kΩ)
0.8	124 (1%)	NS
1.2	124 (1%)	249 (1%)
3.3	124 (1%)	40.2 (1%)
5	124 (1%)	23.7 (1%)

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. Generally, a good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L1 = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔIL is the peak-to-peak inductor ripple current.

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low and high efficiency.

Table 2 —Compensation Values for Typical Output Voltage/Capacitor Combinations

VOUT(V)	L1(μH)	C2(μF)	R1(kΩ)
3.3	4.7-10	10	40.2
5	10-15	10	23.7
12	15-22	10	8.87

Layout

Layout Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the V_{IN} and GND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin.
2. Minimize trace length to the FB pin net. Both feedback resistors, R1 and R2 should be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
3. Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
4. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

Layout Example

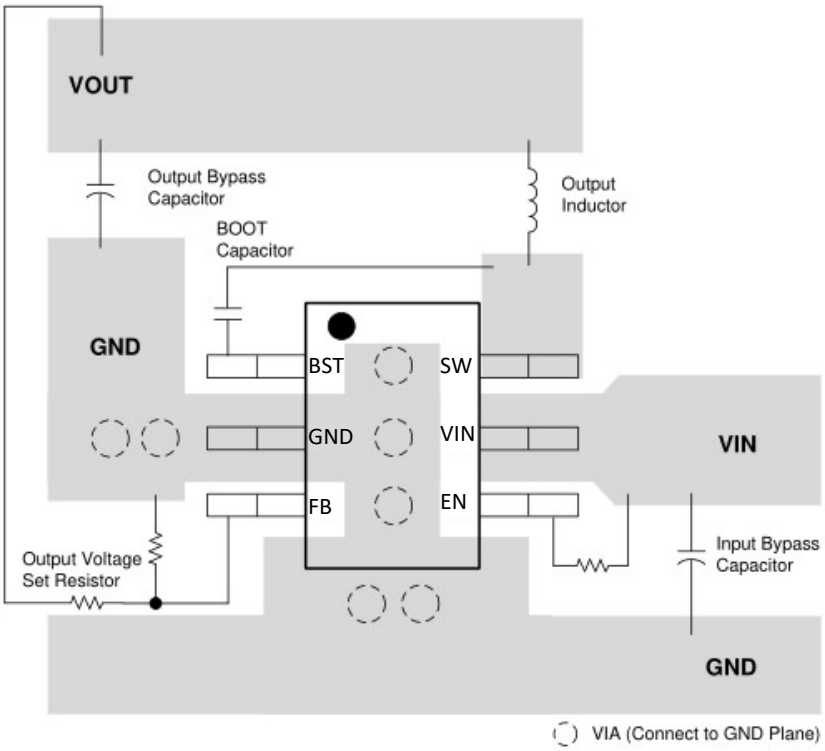
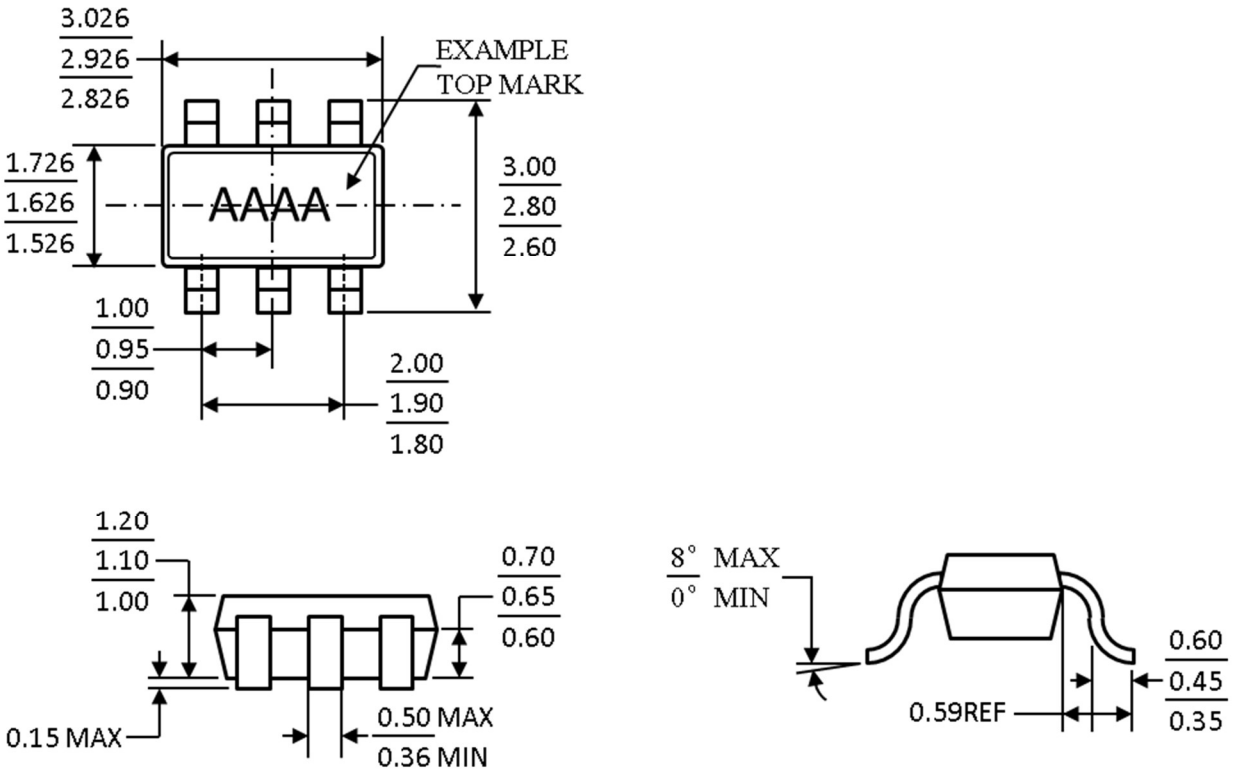


Figure 22 Layout Example

PACKAGE OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARD MO-178-AB

Figure 23 6-Lead Small Outline Transistor Package [SOT-23]

Dimensions shown in millimeters