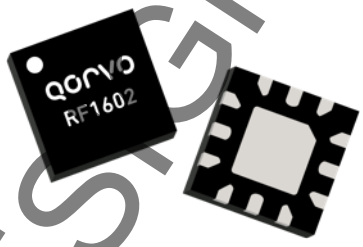
RF1602

Broadband SPDT Switch

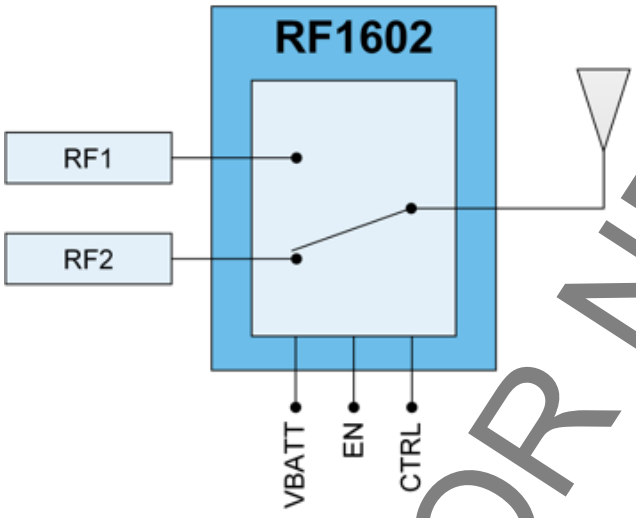
Product Overview

The RF1602 is a single-pole dual-throw (SPDT) switch designed for switching applications requiring very low insertion loss and high power handling capability coupled with minimal DC power consumption. The excellent linearity performance achieved by the RF1602 makes it ideal for use in SV-LTE, WCDMA, and CDMA applications. The RF1602 offers very high isolation between RF ports providing greater separation between transmit and receive paths. The RF1602 is packaged in a very compact 2 mm x 2 mm x 0.55 mm 12-Pin QFN package.



Package: QFN, 2 mm x 2 mm x 0.55 mm

Functional Block Diagram



Key Features

- Low Frequency to 3.8 GHz Operation
- Low Insertion Loss, Typ. 0.3 dB at 1 GHz
- Very High Isolation, Typ. 42 dB at 1 GHz
- High Linearity, IIP2 Typ. 129 dBm
- Direct Connection to V_{BATT}
- Compatible with Low Voltage Logic (V_{HIGH} Minimum = 1.3 V)
- No External DC Blocking Capacitors Required on RF Paths Unless DC is applied Externally
- 2 kV HBM Rating on All Ports

Applications

- SV-LTE, WCDMA, GSM
- Post PA Switching
- General Purpose Switching Application

Ordering Information

Part Number	Description
RF1602SB	5-Piece Sample Bag
RF1602SR	100-Piece Sample Reel
RF1602TR7	2500-Piece 7” Reel
RF1602PCK-410	Fully Assembled Evaluation Board and 5-Piece Sample Bag

Absolute Maximum Ratings

Parameter	Rating	Unit
Maximum V_{BATT}	6.0	V
Maximum EN	3.0	V
Maximum CTRL	3.0	V
Maximum Power Handling (6:1 VSWR, Temp. = 25 °C)	+36	dBm
Operating Temperature	-40 to +85	˚C
Storage Temperature	-40 to +125	˚C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					(All Nominal Test Conditions Unless Otherwise Stated) V_{BATT} = 3.5 V, Temperature = 25 °C, All RF ports terminated in 50 Ω
Insertion Loss					
RF1 to ANT, RF2 to ANT		0.30	0.40	dB	400 MHz to 1 GHz
		0.30	0.45	dB	1.0 GHz to 2.0 GHz
		0.35	0.50	dB	2.0 GHz to 2.5 GHz
		0.40	0.55	dB	2.5 GHz to 3.5 GHz
		0.40	0.60	dB	3.5 GHz to 3.8 GHz
Isolation					
RF1 to RF2, RF2 to RF1	37	42		dB	400 MHz to 1 GHz
	31	34		dB	1.0 GHz to 2.0 GHz
	30	32		dB	2.0 GHz to 2.5 GHz
	25	29		dB	2.5 GHz to 3.5 GHz
	24	29		dB	3.5 GHz to 3.8 GHz
RF Port Return Loss					
ANT, RF1, RF2	10	15		dB	400 MHz to 3.8 GHz
900 MHz Harmonics					
Second Harmonic		-95	-75	dBc	P_{IN} = 35 dBm
Third Harmonic		-90	-75	dBc	
1800 MHz Harmonics					
Second Harmonic		-95	-75	dBc	P_{IN} = 33 dBm
Third Harmonic		-90	-75	dBc	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					(All Nominal Test Conditions Unless Otherwise Stated) V_{BATT} = 3.5 V, Temperature = 25 °C, All RF ports terminated in 50 Ω
IIP2					
RF1, RF2, ANT (Cell)	122	129		dBm	Tone 1: 836.5 MHz at +26 dBm Tone 2: 1718 MHz at -20 dBm Receive Freq: 881.5 MHz
RF1, RF2, ANT (AWS)	122	129		dBm	Tone 1: 1732.5 MHz at +26 dBm Tone 2: 3865 MHz at -20 dBm Receive Freq: 2132.5 MHz
RF1, RF2, ANT (PCS)	122	129		dBm	Tone 1: 1880 MHz at +26 dBm Tone 2: 3840 MHz at -20 dBm Receive Freq: 1960 MHz
RF1, RF2, ANT (IMT)	122	129		dBm	Tone 1: 1950 MHz at +26 dBm Tone 2: 4090 MHz at -20 dBm Receive Freq: 2140 MHz
IIP3 SV – LTE					
RF1, RF2, ANT (Cell)	71	77		dBm	Tone 1: 786 MHz at +23 dBm Tone 2: 825 MHz at +14 dBm Receive Freq: 747 MHz
RF1, RF2, ANT (Cell)	76	83		dBm	Tone 1: 782 MHz at +23 dBm Tone 2: 827 MHz at +14 dBm Receive Freq: 872 MHz
IIP3					
RF1, RF2, ANT (Cell)	70	75		dBm	Tone 1: 836.5 MHz at +26 dBm Tone 2: 791.5 MHz at -20 dBm Receive Freq: 881.5 MHz
RF1, RF2, ANT (IMT)	70	75		dBm	Tone 1: 1950 MHz at +26 dBm Tone 2: 1760 MHz at -20 dBm Receive Freq: 2140 MHz
Max Operating Power					
			36	dBm	50 Ω, Temp. = 25 °C
			35	dBm	VSWR = 6:1, Temp. = -40 ° C to +85 °C
Supply and Control Signal Characteristics					
Supply Voltage, V_{BATT}	2.6	3.5	4.6	V	
Supply Current, V_{BATT}					
EN = HIGH		100	200	µA	
EN = LOW		14	20	µA	
Control Voltage (EN, CTRL)					V_{EN} & V_{ctrl} < V_{BATT}
V_{HIGH}	1.3	1.8	2.75	V	
V_{LOW}		0	0.45	V	
Control Current					
I_{HIGH}		2.5	5	µA	
I_{LOW}		1	3	µA	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					(All Nominal Test Conditions Unless Otherwise Stated) V_{BATT} = 3.5 V, Temperature = 25 °C, All RF ports terminated in 50 Ω
Switching Time					
Switching Speed ON		2	5	µs	All combinations; 50% control to 90% RF ON
Switching Speed RF OFF		2	5	µs	All combinations; 50% control to 10% RF OFF
Start Up Time from Shutdown			5	µs	Maximum set up time for the switch to reach fully compliant operation
Turn-on Time		5	20	µs	Time from V_{BATT} 50% of operational voltage to RF signal at 90%

Power – Up, Power – Down sequence and operation controls

Sequence for Power UP and Power DOWN from the phone battery or supply that is connected to RF1602 V_{BATT} pin.

Power – up Sequence:

1. Turn on V_{BATT} (supply)
2. Then EN
3. Then CTRL
4. Then (20 µs or greater)
5. Apply RF signal

Power – Down Sequence:

1. Turn off RF signal
2. Then CTRL
3. Then EN
4. Turn off V_{BATT} (supply)

Sequence for going in and out of a shutdown mode, keeping the V_{BATT} or supply on, but disabling/enabling the RF1602 by the EN pin.

Power – Up Sequence:

1. Turn-on EN (enable)
2. Then CTRL
3. Then (5 µs or greater)
4. Turn-on RF signal

Power – Down Sequence:

1. Turn-off RF signal
2. Then CTRL
3. Then EN (disable)

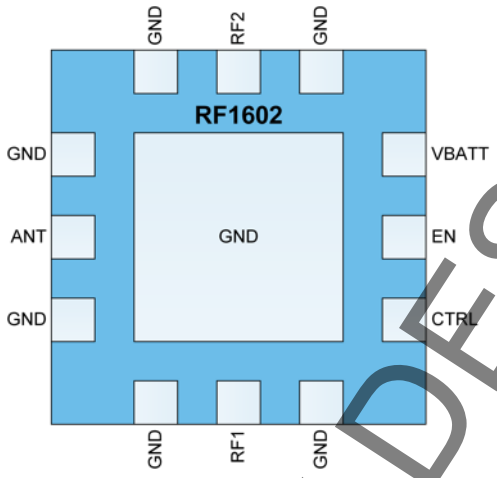
When changing switch positions between RF1 and RF2, no RF signal should be applied to any RF port while the CTRL is changing states

Switching Ports:

1. Turn-off RF signal
2. Then change CTRL state
3. Then (5 µs or greater)
4. Turn-on RF signal

Pin Out

Top View



Pin – Out Description

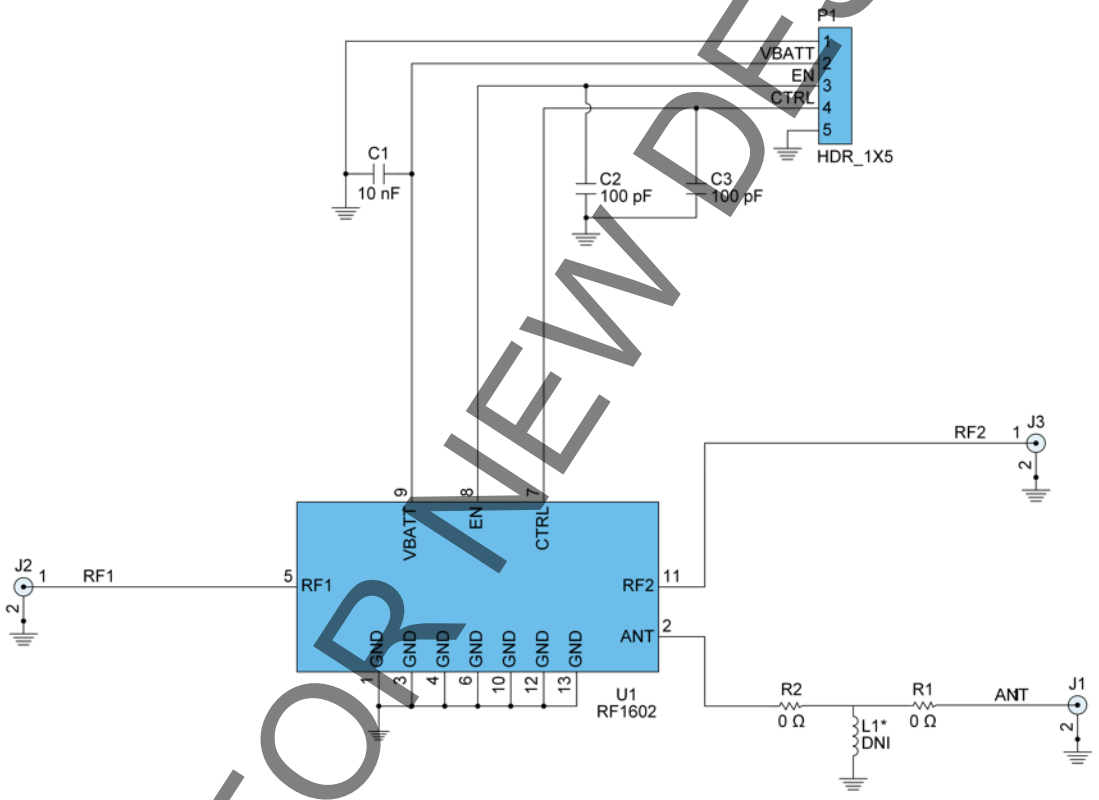
Pin	Function	Description
1	GND	Ground
2	ANT	Single ended RF port
3	GND	Ground
4	GND	Ground
5	RF1	Single ended RF port
6	GND	Ground
7	CTRL	Switch logic control input
8	EN	Switch logic control input, shutdown for low leakage current
9	V_{BATT}	Supply voltage from battery
10	GND	Ground
11	RF2	Single ended RF port
12	GND	Ground
13	Package Base	Ground

Control Logic

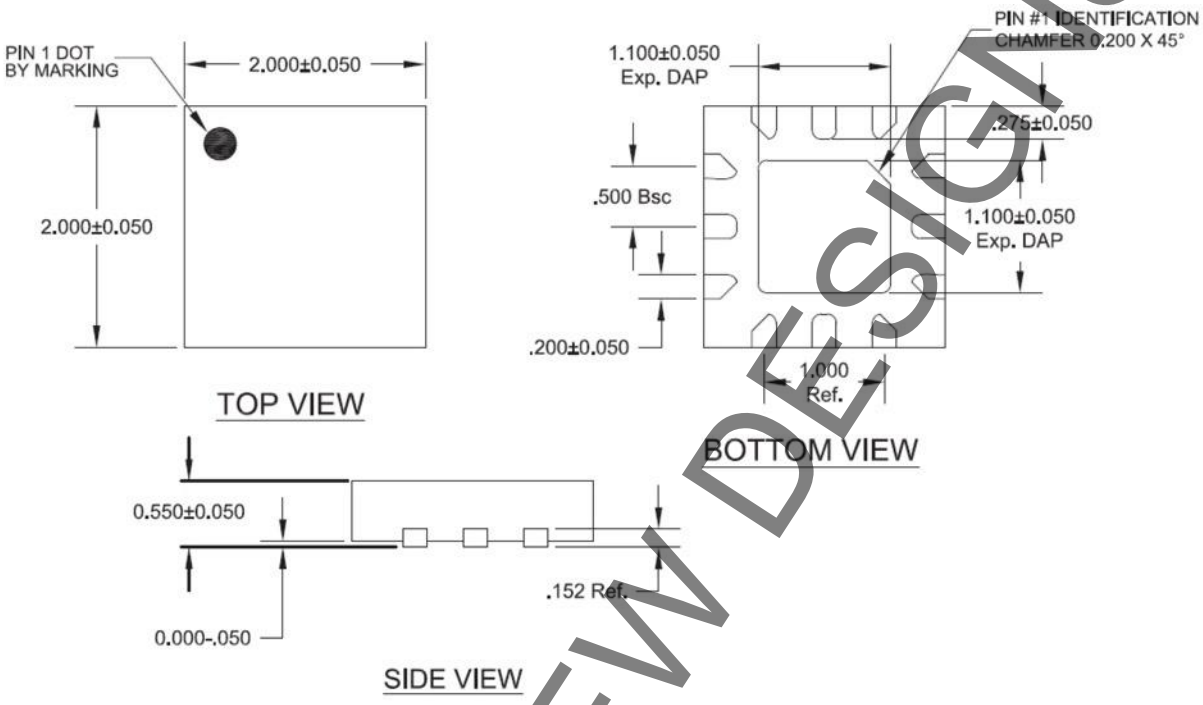
State	V_{BATT}	CTRL	EN	RF Path
1	2.7 V to 4.6 V	V_{HIGH}	V_{HIGH}	ANT – RF2
2	2.7 V to 4.6 V	V_{LOW}	V_{HIGH}	ANT – RF1
Shutdown	2.7 V to 4.6 V	Don't Care	V_{LOW}	Shutdown

The switch is operable in 3 states. The switch is designed for two modes: active and shutdown. Assuming V_{BATT} is always between 2.7 V and 4.6 V the switch is controlled by the EN voltage. When EN is HIGH the switch is active and when EN is LOW the switch is in standby mode.

Evaluation Board Schematic



Package Drawing



PCB Design Requirements

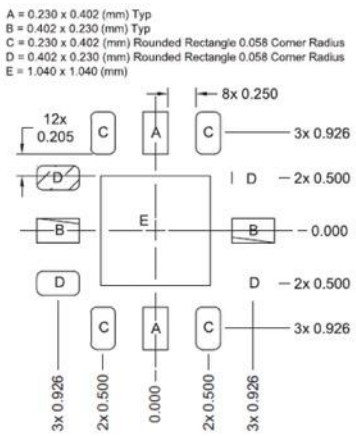
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 µ inch to 8 µ inch gold over 180 µ inch nickel.

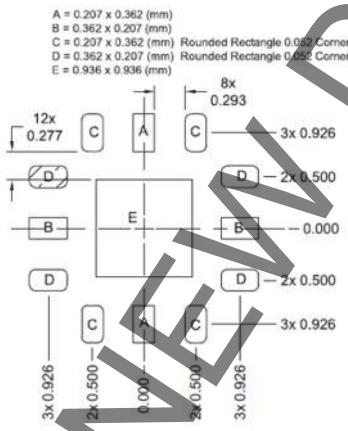
PCB Land Pattern Recommendation

PCB land pattern for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

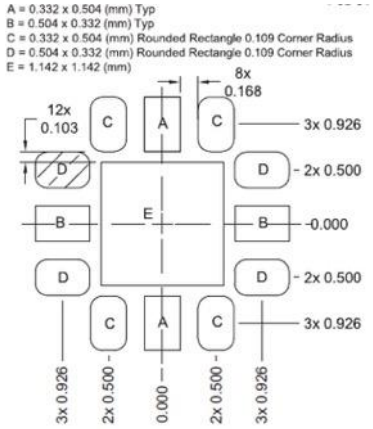
PCB Metal Land and Solder Mask Pattern



PCB Metal Pattern



PCB Stencil Pattern



PCB Solder mask Pattern

Shaded area represents Pin 1 location.

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: -Matte Sn

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

REVISION HISTORY

Revision	Description
Rev M	Update Supply Voltages.
DS140203	Update Ven from 2.7 to 2.75 V, Add comment "V_{EN} < V_{BATT} " to Control Voltage table.
DS20140812	Updated ordering information. Added minimums for SV-LTE IIP3 specs. Revised first SV-LTE IIP3 case typical value.
DS20170530	Updated from RFMD to Qorvo template
Q (20200219)	Added Not Recommended For New Designs marks

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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