

N- Channel 60V (D-S) MOSFET

GENERAL DESCRIPTION

The ME50N06A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

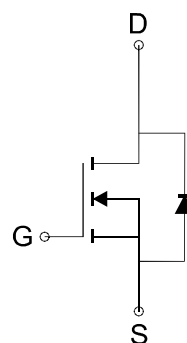
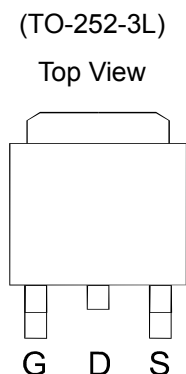
FEATURES

- $R_{DS(ON)} \leq 22m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- Secondary Synchronous Rectification

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME50N06A (Pb-free)

ME50N06A-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Steady	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current	I _D	T _C =25°C	35.1
		T _C =70°C	28.1
Pulsed Drain Current	I _{DM}	140	A
Maximum Power Dissipation	P _D	T _C =25°C	59.5
		T _C =70°C	38.1
Operating Junction Temperature	T _J	-55 to 150	°C
Thermal Resistance-Junction to Case*	R _{θJC}	2.1	°C/W

* Notes: The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

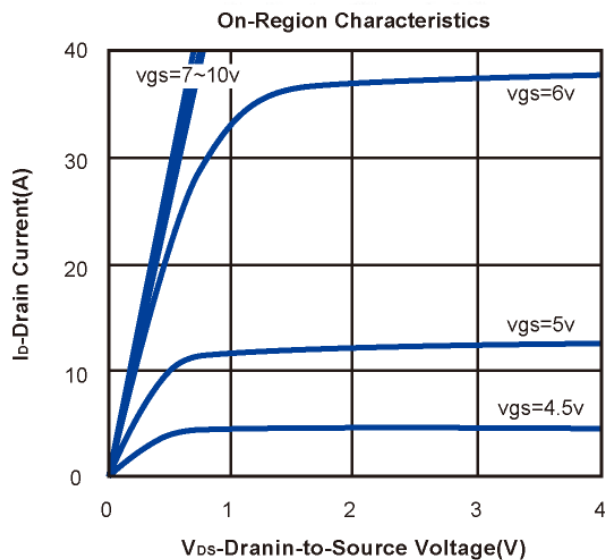
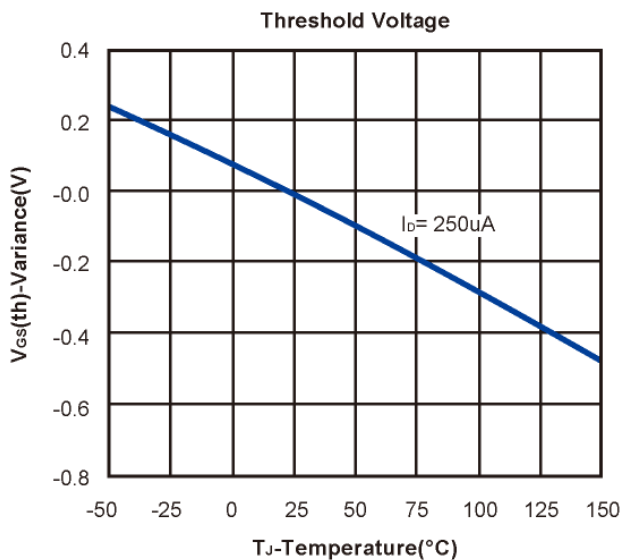
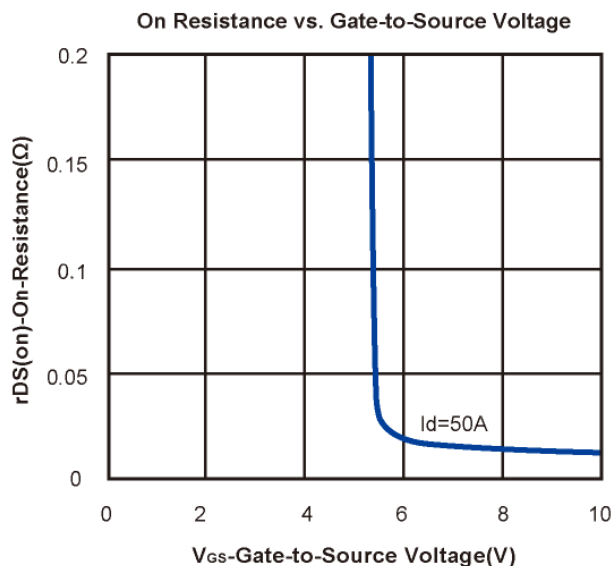
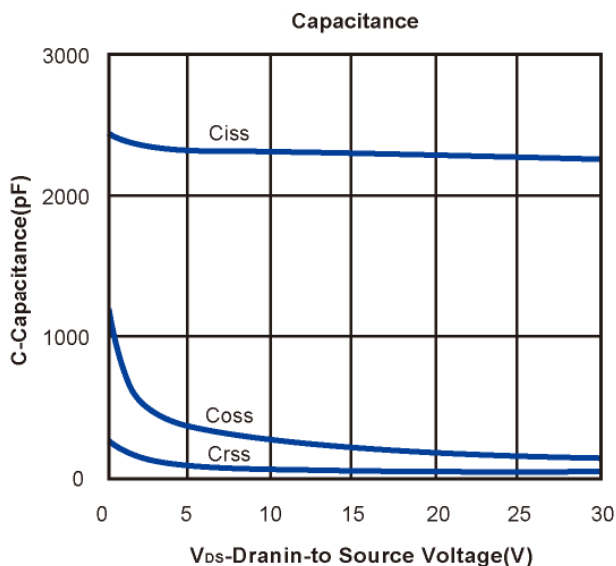
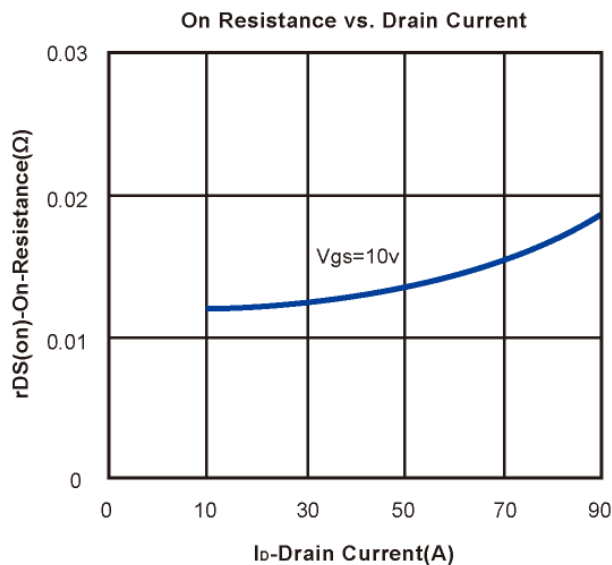
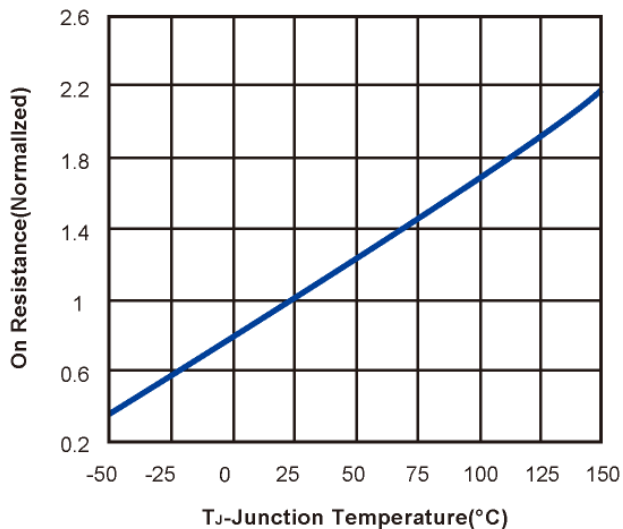
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2		4	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 50A		17	22	mΩ
V _{SD}	Diode Forward Voltage	I _S =50A, V _{GS} =0V		1.0	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =48V, V _{GS} =10V, I _D =50A		37.1		nC
Q _g	Total Gate Charge	V _{DD} =48V, V _{GS} =4.5V, I _D =50A		10.9		
Q _{gs}	Gate-Source Charge			14.3		
Q _{gd}	Gate-Drain Charge			8.3		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		2.1		Ω
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		2280		pF
C _{oss}	Output Capacitance			202		
C _{rss}	Reverse Transfer Capacitance			62		
t _{d(on)}	Turn-On Delay Time	V _{DS} =30V, V _{GS} =10V, R _G =3.6Ω, R _L =30Ω		27.7		ns
t _r	Turn-On Rise Time			5.1		
t _{d(off)}	Turn-Off Delay Time			54.2		
t _f	Turn-On Fall Time			5.5		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

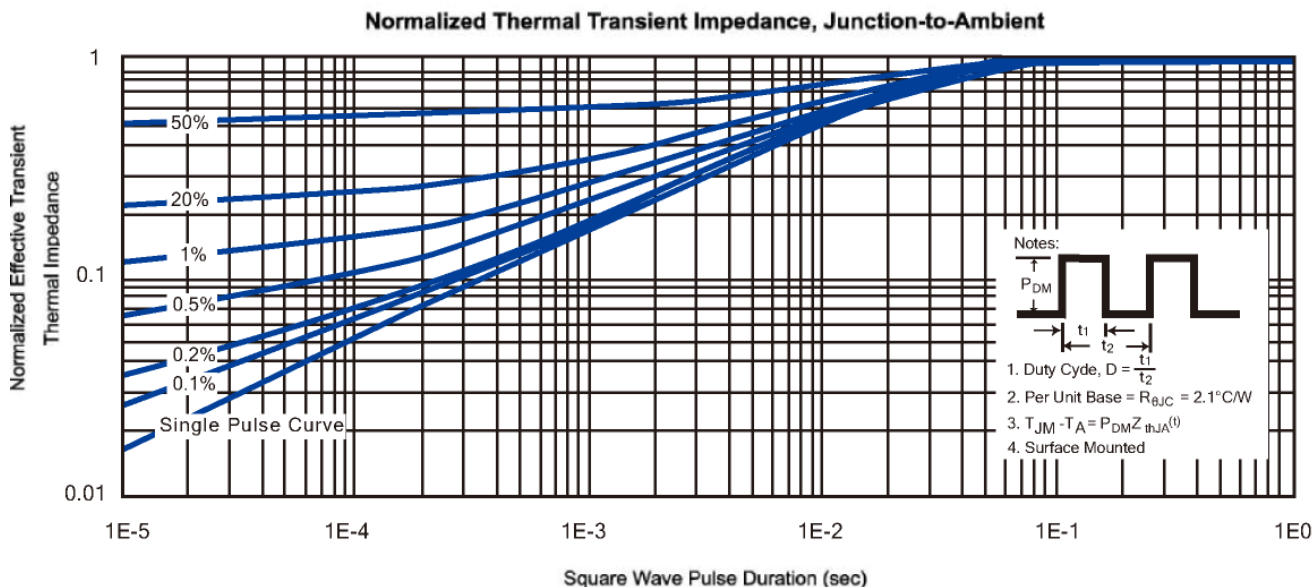
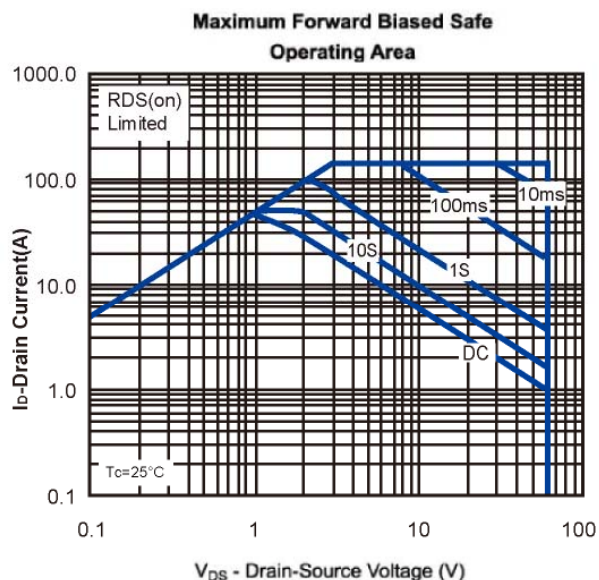
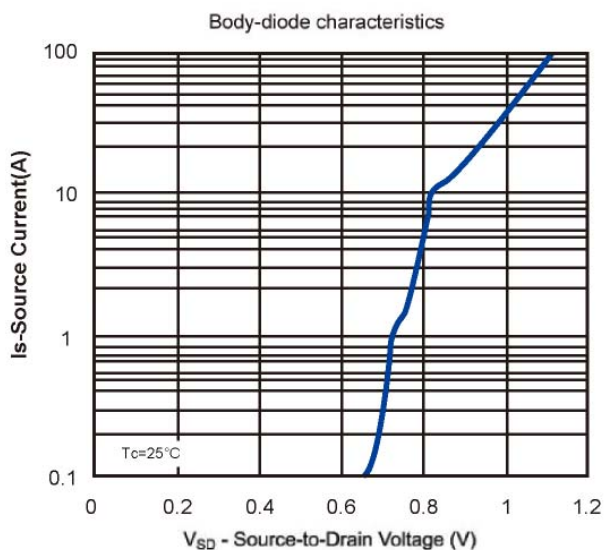
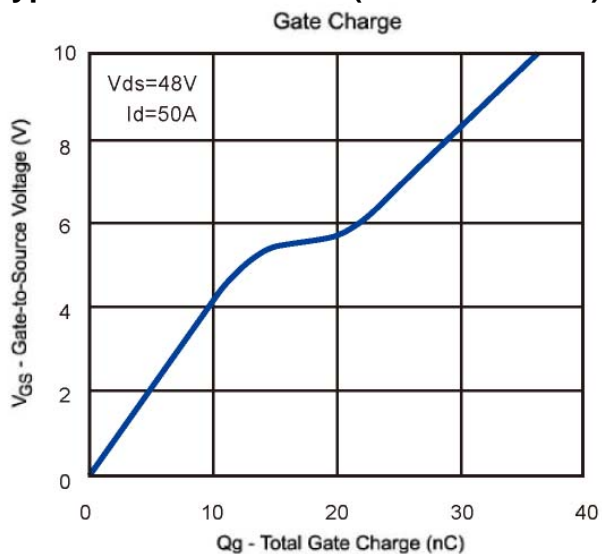
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Typical Characteristics (T_J = 25°C Noted)
 On Resistance vs. Junction Temperature

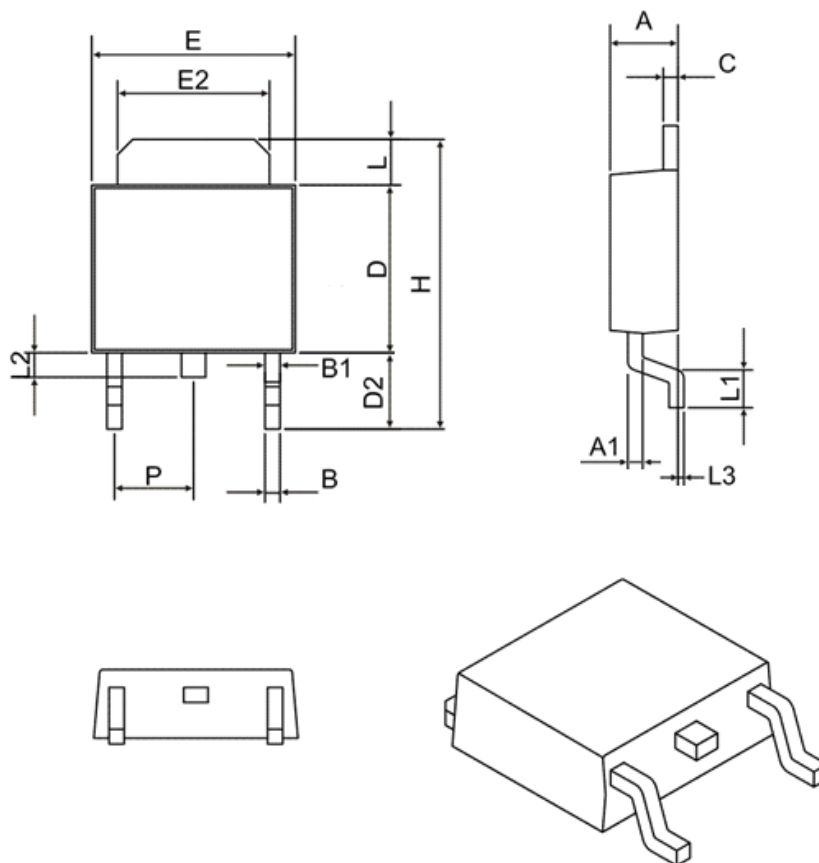


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Typical Characteristics (T_J =25°C Noted)



TO-252-3L Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.00	2.50
A1	0.45	0.60
B	0.50	0.88
B1	0.50	1.14
C	0.40	0.60
D	5.20	6.23
D2	2.743 REF	
H	9.40	10.50
E	6.30	6.80
E2	4.50	5.50
L	0.89	1.70
L1	0.90	1.77
L2	0.50	1.10
L3	0	0.30
P	2.286 BSC	