N-Channel 100-V(D-S) MOSFET

GENERAL DESCRIPTION

The MEE4294-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, EMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as synchronous rectification for AC/DC adapter or PC-power where load switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 12m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 15.5m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

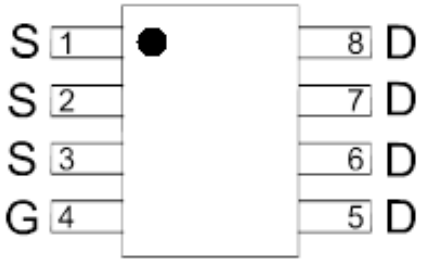
APPLICATIONS

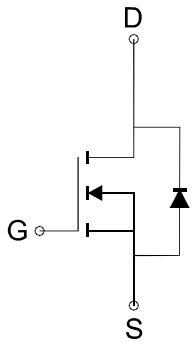
- Power Management
- Synchronous Rectification
- Load Switch

PIN CONFIGURATION

(SOP-8)

Top View





N-Channel MOSFET

Ordering Information:MEE4294-G (Green product- Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	11.3	A
	T_C=70℃		9	
Single pulse Avalanche Energy L=0.1mH		I_{AS}	20	A
		E_{AS}	20	mJ
Pulsed Drain Current		I_{DM}	45	A
Maximum Power Dissipation*	T_C=25℃	P_D	2.8	W
	T_C=70℃		1.8	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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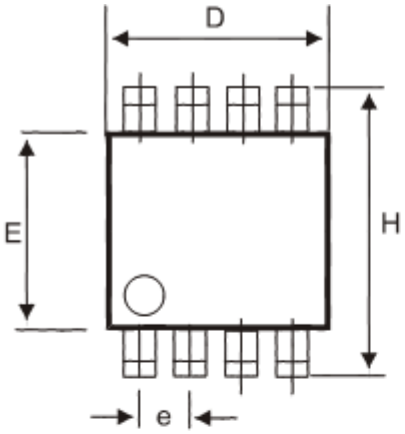
Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

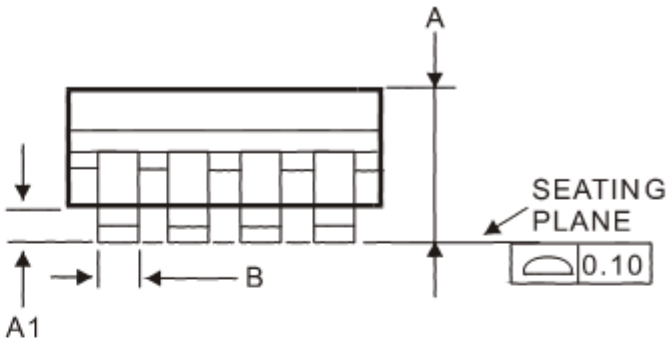
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250 μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250 μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 11.5A		10	12	mΩ
		V_{GS}=4.5V, I_D= 9.5A		13.5	15.5	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.6	1	V
DYNAMIC						
Ciss	Input capacitance	V_{DS}=30V,V_{GS}=0V, f=1.0MHz		2071		pF
Coss	Output Capacitance			704		
Crss	Reverse Transfer Capacitance			28		

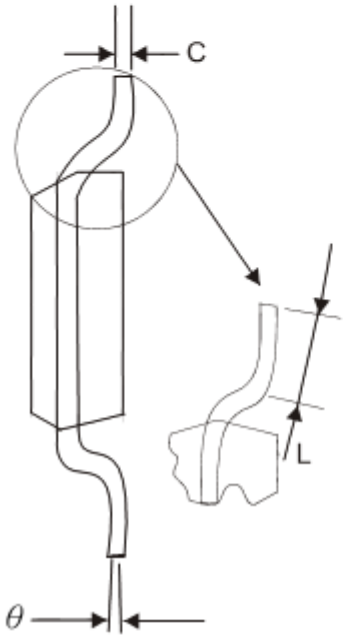
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.31	0.51
C	0.17	0.25
D	4.80	5.10
E	3.80	4.30
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.27
θ	0°	8°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.