16 Channel Automotive LED Driver with Bus Interface

E522.49

ADVANCED PRODUCT INFORMATION – Mar 8, 2019

Features

- Fast differential bus interface for dynamic LED control
- Device and LED supply voltage range from 5V up to 40V
- 16 PWM generators with 10bit resolution
- 16 programmable LED drivers up to 100mA
- LED driver current selection step size of 100uA
- 2 prioritized PWMIN interface pins
- PWMIN interface with fallback data
- Direct PWM input
- 10bit ADC for LED open, short and system diagnosis
- Single lamp mode behaviour option
- Advanced device power management by channel bundling option
- Automatic supply and temperature dependent LED current derating
- LED channel individual bin class brightness correction
- Optional external LED bin class resistor evaluation

Applications

- Automotive interior and exterior light systems
- General LED Applications
- High speed LED light animations

General Description

The E522.49 is a multi-channel PWM driver for e.g. light application. It provides 16 current sinks with integrated 10bit PWM generator for each channel. Each of the drivers can digitally be configured to drive up to 100mA with a selectable slew rate.

The device supports bus controlled operation to enable fast light animation sequences. For failsafe conditions the device provides internal non-volatile memory to store channel individual current and duty cycle information for highest flexibility.

An advanced device power management feature allows LED channel bundling with automatic current balancing to external resistors resulting in reduced device power dissipation.

Various diagnostic features, like LED open, short condition detection and temperature sensor, are provided to meet automotive requirements.

To protect the device from thermal damage, the device implements a configurable LED supply and device temperature dependent automatic LED current derating.

Ordering Information

Product ID	*Temperature Range*	*Package*
E52249A77B	-40°C to +125°C	QFN32L6

Typical Operating Circuit

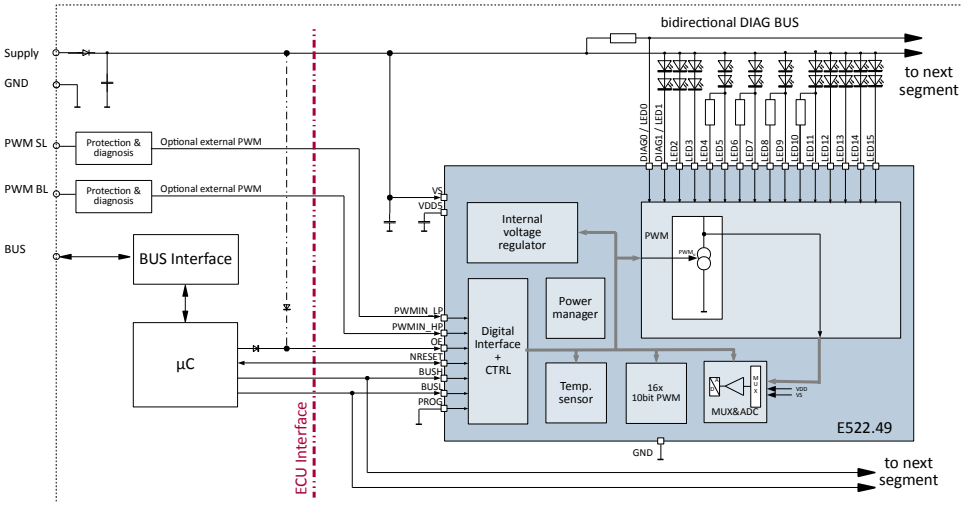

Figure 1: Typical application

Functional Diagram

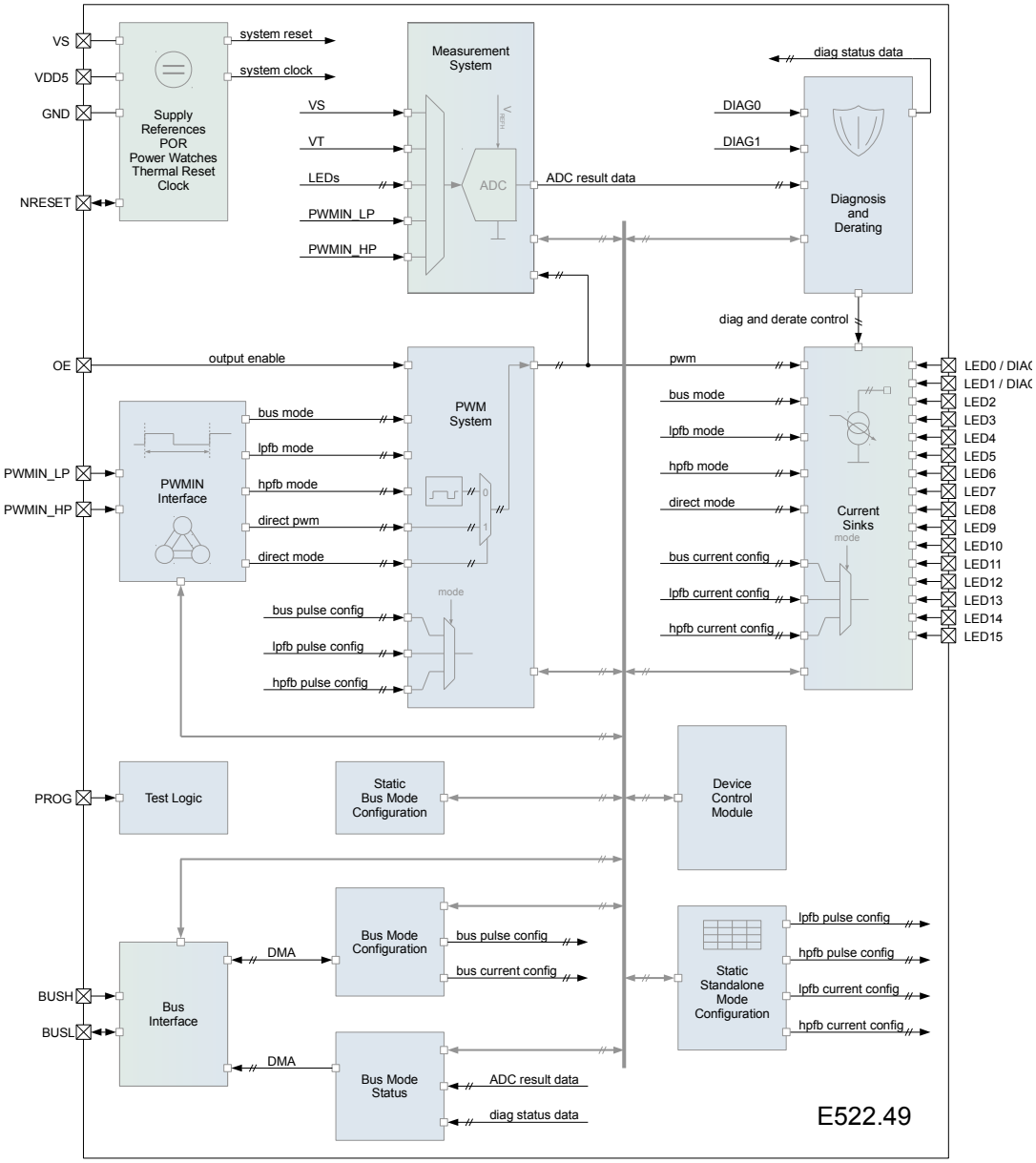

Figure 1: Functional Diagram

Pin Configuration QFN32L6

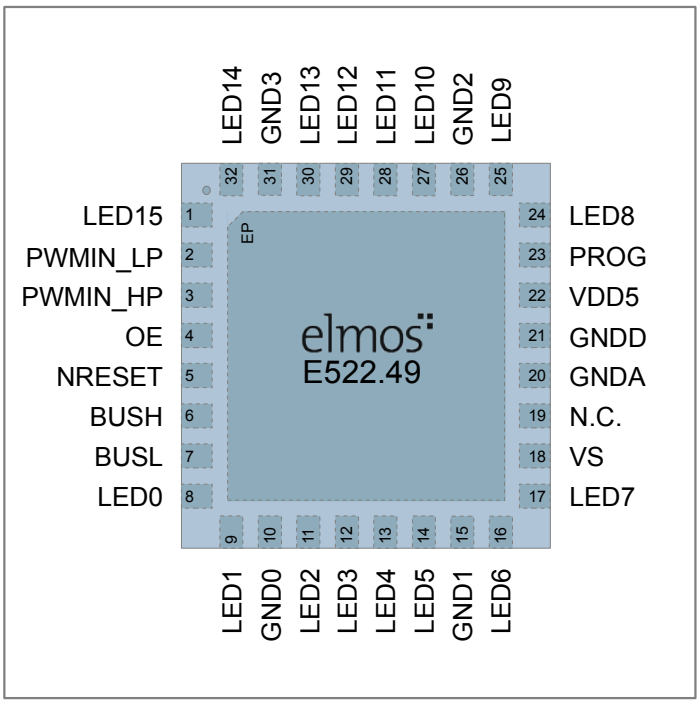

Figure 1: QFN32L6 pin configuration, transparent top view

Pin Description QFN32

No	*Name*	*Type*	*Description*
1	LED15	HV_A_O	LED15 current sink
2	PWMIN_LP	HV_D_I	low priority PWM control input used to select a data set for PWM generation or as direct PWM signal input pin
3	PWMIN_HP	HV_D_I	high priority PWM control input used to select a data set for PWM generation or as direct PWM signal input pin
4	OE	HV_D_I	PWM generator bus mode output enable pin
5	NRESET	HV_D_IO	device open-drain active low reset pin
6	BUS_H	HV_D_IO	UART bus H signal
7	BUS_L	HV_D_IO	UART bus L signal
8	LED0	HV_A_O	LED0 / DIAG0 current sink
9	LED1	HV_A_O	LED1 / DIAG1 current sink
10	GND0	S	LED group 0 ground, channels LED0 to LED3
11	LED2	HV_A_O	LED2 current sink
12	LED3	HV_A_O	LED3 current sink
13	LED4	HV_A_O	LED4 current sink
14	LED5	HV_A_O	LED5 current sink
15	GND1	S	LED group 1 ground, channels LED4 to LED7
16	LED6	HV_A_O	LED6 current sink

No	*Name*	*Type*	*Description*
17	LED7	HV_A_O	LED7 current sink
18	VS	HV_S	device supply pin
19	N.C.		not connected (unused)
20	GNDA	S	analog ground
21	GNDD	S	digital ground
22	VDD5	S	internal 5V supply, a decoupling capacitor has to be attached to this pin
23	PROG	HV_D_I	(terminate to GND in application) active high device program mode pin
24	LED8	HV_A_O	LED8 current sink
25	LED9	HV_A_O	LED9 current sink
26	GND2	S	LED group 2 ground, channels LED8 to LED11
27	LED10	HV_A_O	LED10 current sink
28	LED11	HV_A_O	LED11 current sink
29	LED12	HV_A_O	LED12 current sink
30	LED13	HV_A_O	LED13 current sink
31	GND3	S	LED group 3 ground, channels LED12 to LED15
32	LED14	HV_A_O	LED14 current sink
33	EP	S	Exposed die pad, connect to GND in application analog ground

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1 Functional Safety

The development of this product is based on a process according to ISO 26262 which has been certified to be compliant to ISO 26262 requirements and integrity levels up to ASIL D. Safety requirements for this product are rated ASIL B.

1.1 Technical Safety Requirements

Table 1.1-1: Technical Safety Requirements

Reference	*Description of Technical Safety Requirements*	*ASIL*
TSR1	**Control LED channels according to valid communication or control data** • The state of the LED output channels shall be controlled in accordance with the requests received via communication interface or direct control signals • Only valid communication and control information shall be used	ASIL B
TSR2	**Provide status and diagnosis information** • The IC shall provide functions which allow to read back the actual state of the LED output channels • The IC shall provide diagnosis information	ASIL B

1.2 Fault Tolerance Time Interval

The diagnosis/safety mechanisms implemented in the IC have been specified in such a way that the Fault Detection and Reaction Times (FDT/FRT) are compliant to the Fault Tolerant Time Interval requirements, which depend on the particular rear light function. Due to the fact that there is no allocation of IC channels to particular rear light functions, it has to be considered that any rear light function may be allocated to any channel of the IC. For that reason the most critical Fault Tolerant Time Interval requirement among all intended rear light functions, which amounts to 300ms, has been considered.

1.3 Safe State

The Safe State for the IC depends on the particular rear light function. Due to the fact that there is no allocation of IC channels to particular rear light functions, it has to be considered that any rear light function may be allocated to any channel of the IC. For that reason the IC implements a configurable fall-back concept for each channel, which allows to adapt the Safe State according to the requirements of the particular rear light function.

2 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only;
operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.
Exposure to conditions beyond those listed in the operational sections of this document for extended periods may affect device reliability.
All voltages with respect to ground. Currents flowing into terminals are signed as positive, those drawn out of a terminal are negative.

Table 2-1: Absolute Maximum Ratings

No.	*Description*	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
1	junction temperature		T_J	-40	150	°C
2	power dissipation		P_{DIS}		2	W
3	voltage at pin **VS**		V_{max_VS}	-0.3	40	V
4	voltage at pin **VDD5**[1)]		V_{max_VDD5}	-0.3	6	V
5	voltage Difference **VS** - **VDD5**[2)]		$V_{max\_VS\_VDD5}$	-0.3	40	V
6	voltage at pin **NRESET**		V_{max_NRESET}	-0.3	40	V
7	voltage at pin **PROG**		V_{max_PROG}	-0.3	40	V
8	voltage at pin **BUS**_x	x=H/L	$V_{max\_BUS\_x}$	-0.3	40	V
9	voltage at pin **PWMIN_LP**		$V_{max\_PWMIN\_LP}$	-0.3	40	V
10	voltage at pin **PWMIN_HP**		$V_{max\_PWMIN\_HP}$	-0.3	40	V
11	voltage at pin **OE**		V_{max_OE}	-0.3	40	V
12	voltage on pin **LED**n	n=0..15	V_{max_LEDn}	-0.3	40	V
13	power dissipation at pin LEDn	n=0..15	P_{LEDn}		800	mW

[1)] Device has internal voltage regulator to generate this supply.
[2)] This does not overrule V_{max_VS} and V_{max_VDD5}. They have the be respected in parallel.

3 ESD

Table 3-1: ESD Parameters

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
ESD HBM Protection at all Pins	[1)]	$V_{ESD(HBM)}$	-2	2	kV
ESD CDM Protection at all Pins	[2)]	$V_{ESD(CDM)}$	-500	500	V

[1)] According to AEC-Q100-002 (HBM) chip level test
[2)] According to AEC-Q100-011 (CDM) chip level test

4 Recommended Operating Conditions

Table 4-1: Recommended Operating Conditions

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	ambient temperature		T_A	-40		125	°C
2	voltage at pin **VS**	during startup, at least 1 ms	V_{start_VS}	5.5		32	V
3	voltage at pin **VS**	after startup	V_{func_VS}	5		32	V
4	voltage at pin **NRESET**		V_{func_NRESET}	0		32	V
5	voltage at pin **PROG**		V_{func_PROG}	0		32	V
6	full functionality VDD5 working range[1)]		V_{func_VDD5}	4.5		5.5	V
7	external capacitance at **VDD5** pin[2)]		C_{VDD5}	400			nF
8	tolerated voltage at pin **BUS**_x	x=H/L	$V_{tol\_BUS\_x}$	0		32	V
9	functional voltage range at pin **BUS**_x for RX module	x=H/L	$V_{func\_RX\_BUS\_x}$	0		5.5	V
10	bus data frame rate[3)]		$f_{BUS\_FRAME\_RATE}$			200	Hz
11	voltage at pin **PWMIN_LP**		$V_{func\_PWMIN\_LP}$	0		32	V
12	voltage at pin **PWMIN_HP**		$V_{func\_PWMIN\_HP}$	0		32	V
13	voltage at pin **OE**		V_{func_OE}	0		32	V
14	voltage at pin **LED**n, full functional working range	n=0..15	V_{func_LEDn}	1		32	V
15	tolerated voltage at pin **LED**n, reduced functionality working range[4)]	n=0..15	$V_{red\_func\_LEDn}$	0		1	V
16	voltage at PWMIN_LP, PWMIN_HP if used as LED supply during short diagnosis		$V_{PWMIN\_LED\_SUPPLY}$	4.5			V

[1)] VDD5 is intended to be driven by the integrated voltage regulator.
It should not be driven or loaded externally
[2)] Note: Ceramic capacitors derate over lifetime and bias voltage. It is therefore recommended to choose a part with higher nominal value to ensure the min requirement, e.g. 680nF.
[3)] device bus data update rate has to be limited to guaranty correct device function
[4)] Current sink works stable till resistive saturation. Saturation is below 1V for all currents below 100 mA. Some electrical parameters like settling time will be violated when the output voltage is below 1V

5 Thermal Characteristics

Table 5-1: Thermal Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	QFN32L6 package junction to case thermal resistance[*)]		$R_{TH\_JC\_QFN32L6}$			5	K/W
2	QFN32L6 package junction to ambient thermal resistance[*)]		$R_{TH\_JA\_QFN32L6}$		28		K/W

[*)] Not tested in production

6 Electrical Characteristics

(V_{VS} = 5V to 32V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VS} = 12.0V and T_A = +25°C. Positive currents flow into the device pins.)

6.1 Power Supply and Resets

6.1.1 Voltage Regulator 5V

Table 6.1.1-1: Electrical Parameters Voltage Regulator 5V

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	regulator output idle state	V_{VS} = 12V minimal internal current consumption	V_{VDD5_REG}	4.8	5.0	5.2	V
2	dropout voltage V_{VS} - V_{VDD5}	minimal internal current consumption, external: I_{VDD5} = 0 .. 20mA, V_{VS} = 4.9V	V_{VDD5_DROP}	0	200	500	mV
3	VDD5 reset threshold, rising supply		$V_{VDD5\_OK\_LH}$		4.75		V
4	VDD5 reset threshold, falling supply		$V_{VDD5\_OK\_HL}$		4		V
5	VDD5 reset threshold, hysteresis		$V_{VDD5\_OK\_HYST}$		0.75		V
6	total VS functional current consumption		$I_{VS\_TOT\_FUNC}$			15	mA

VS does not have a powerwatch, but VS reset levels can be derived from VDD5.
As they are only implicit given, they are not tested in production:
$V_{VS\_OK\_LH} = V_{VDD5\_OK\_LH} + V_{VDD5\_DROP}$ = 4.95 V (typ)
and:
$V_{VS\_OK\_HL} = V_{VDD5\_OK\_HL} + V_{VDD5\_DROP}$ = 4.2 V (typ)

6.1.2 Thermal Shutdown

Table 6.1.2-1: Thermal Shutdown

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	thermal shutdown threshold rising temperature*)		T_{THERM_LH}	155		175	°C
2	thermal shutdown threshold falling temperature*)		T_{THERM_HL}	135		155	°C
3	thermal shutdown hysteresis*)		T_{THERM_HYST}	10			K

*) Not tested in production

6.2 Device Startup

Table 6.2-1: Electrical Parameters Device Startup

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	device startup time*) 1)		$t_{DEVICE\_STARTUP}$			12	ms

*) Not tested in production

1) time needed by the device to enter active mode after power up or a device reset

6.3 UART Slave Bus Interface

Table 6.3-1: Electrical Parameters UART Receiver

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input threshold recessive		$V_{BUS\_RX\_DIFF\_R}$	500			mV
2	input threshold dominant		$V_{BUS\_RX\_DIFF\_D}$			900	mV
3	input hysteresis		$V_{BUS\_RX\_HYST}$	50			mV
4	internal common mode level		$V_{BUS\_RX\_VCM}$		2.5		V
5	propagation delay	0V -> 1.5V amplitude	$t_{BUS\_RX\_D\_LH}$			250	ns
6	propagation delay		$t_{BUS\_RX\_D\_HL}$			250	ns
7	input resistance		$R_{BUS\_RX\_IN}$	10		100	kΩ

Common condition: receiver is enabled.

Table 6.3-2: Electrical Parameters UART Transmitter

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	BUS_H voltage in dominant state	R_{TERM}=100Ω	$V_{BUS\_DRV\_H}$	3		4.5	V
2	BUS_L voltage in dominant state	R_{TERM}=100Ω	$V_{BUS\_DRV\_L}$	0.8		2.25	V
3	bus differential voltage in dominant state	R_{TERM}=100Ω	$V_{BUS\_DRV\_DIFF}$	1.5			V
4	rise time from 10% to 90%	R_{TERM}=100Ω, slew rate enabled	t_{BUS_RISE}	100	170	300	ns
5	fall time from 90% to 10%	R_{TERM}=100Ω, slew rate enabled	t_{BUS_FALL}	100	170	300	ns
6	peak to peak amplitude of common mode voltage when no stabilizing termination is used	R_{TERM}=100Ω directly connected to pin, no capacitive termination, data signal speed=250kHz	$V_{BUS\_CM\_RIPPLE}$			200	mV
7	current limitation at BUS_H	BUS_H shorted to device ground	$I_{BUS\_LIMIT\_H}$	-140	-100	-60	mA
8	current limitation at BUS_L	BUS_L shorted to device supply	$I_{BUS\_LIMIT\_L}$	60	100	140	mA

6.4 Digital IOs

Table 6.4-1: Electrical Parameters Digital IOs

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input voltage for digital "1"[1)]		V_{DIG_IH}	2			V
2	input voltage for digital "0"[1)]		V_{DIG_IL}			0.8	V
3	input hysteresis[1)]		V_{DIG_HYST}	0.3			V
4	positive supply of internal pull resistor[2)]		V_{DIG_PULL}		3.3		V
5	pull resistor[1)]		R_{DIG_PULL}	50			kΩ
6	PROG pin pull resistor		$R_{DIG\_PULL\_PROG}$	10			kΩ
7	output voltage for digital "0"[3)]	4mA load	V_{DIG_OL}			0.5	V
8	analog low-pulse debounce filter for pins NRESET and PROG		t_{DIG_DEB}		3		µs
9	digital low-pulse debounce filter for pins OE, DIAG0 and DIAG1		$t_{DIG\_DEB\_OE\_DIAG}$	50		100	µs

[1)] valid for DIAG0, DIAG1, PWMIN_LP, PWMIN_HP, OE, NRESET
[2)] please see pull current behavior figures 7.6-1 and 7.6-2 for details
[3)] valid for open-drain NRESET pin

6.5 PWM System

Table 6.5-1: Electrical Parameters PWM

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	device internal PWM frequency[*)]		f_{PWM}	50	300	500	Hz
2	PWMIN_LP, PWMIN_HP direct PWM frequency[*)]		f_{direct_PWM}		300	500	Hz

[*)] Not tested in production

6.6 LED Current Sinks

Table 6.6-1: Electrical Parameters Current Sinks

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	current below lower border[*)]	I_{LED} < 10 mA	$I_{SINK\_MIN\_SAT}$	-0.01		10.5	mA
2	overall accuracy of selected current	10mA < I_{LED} < 20 mA	$I_{SINK\_ACC\_OVA\_20}$	-5		5	%
3	overall accuracy of selected current	20mA < I_{LED} < 55 mA	$I_{SINK\_ACC\_OVA\_55}$	-3.5		3.5	%
4	overall accuracy of selected current	55mA < I_{LED} < 100 mA	$I_{SINK\_ACC\_OVA\_100}$	-3		3	%
5	channel matching accuracy	10mA < I_{LED} < 20 mA	$I_{SINK\_ACC\_CH\_20}$	-4		4	%
6	channel matching accuracy	20mA < I_{LED} < 55 mA	$I_{SINK\_ACC\_CH\_55}$	-2.5		2.5	%
7	channel matching accuracy	55mA < I_{LED} < 100 mA	$I_{SINK\_ACC\_CH\_100}$	-2		2	%

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
8	Current above upper border*)	100 mA < I_{LED} < 102.3 mA	I_{SINK_MAX}	97		106	mA
9	rise time 10% to 90%	slew = 0	$t_{SINK\_RISE\_0}$		0.1	0.75	us
10	fall time 90% to 10%	slew = 0	$t_{SINK\_FALL\_0}$		0.1	0.5	us
11	rise time 10% to 90%	slew = 1	$t_{SINK\_RISE\_1}$		5		us
12	fall time 90% to 10%	slew = 1	$t_{SINK\_FALL\_1}$		5		us
13	rise time 10% to 90%	slew = 2	$t_{SINK\_RISE\_2}$		10		us
14	fall time 90% to 10%	slew = 2	$t_{SINK\_FALL\_2}$		10		us
15	rise time 10% to 90%	slew = 3	$t_{SINK\_RISE\_3}$		20		us
16	fall time 90% to 10%	slew = 3	$t_{SINK\_FALL\_3}$		20		us
17	ADC MUX input resistance		R_{SINK_ADC}	500			kΩ
18	input current when OFF	current sink disabled or pwm dutycycle = 0	I_{SINK_LEAK}			5	uA

*) Not tested in production

Explanation:

- I_{LED} describes the current which is digitally requested (incl. derating and binning). The register has a size of 10 bit. This corresponds to a maximum value of 1023 LSB or 102.3 mA.
- Channel matching accuracy describes the matching of an individual channel against the average value of all channels programmed to same output current.
  Overall accuracy describes matching of an individual channel against absolute value selected by its register.

$$matchingaccuracy_n = \frac{I_{LEDn} - I_{LED\_average}}{I_{LED\_average}}$$

- All accuracy values are valid when lower range is selected for currents below 40mA and upper range is selected for currents above 40mA. When using analog channel bundling, the stated accuracy values are valid for current sums above 20mA of the two bundled channels.

6.7 Measurement System

Table 6.7-1: Electrical Parameters Measurement System

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	gain factor of ADC Mux, VS		A_{MEAS_VS}		25		LSB/V
2	gain factor of ADC Mux, PWMIN_LP and PWMIN_HP		A_{MEAS_PWMIN}		25		LSB/V
3	gain factor of ADC Mux, VS via sample and hold (S&H) buffer		$A_{MEAS\_VS\_SH}$		36		LSB/V
4	gain factor of ADC Mux, PWMIN_LP and PWMIN_HP via sample and hold (S&H) buffer		$A_{MEAS\_PWMIN\_SH}$		36		LSB/V
5	gain factor of ADC Mux, LED pin voltage		A_{MEAS_VLED}		36		LSB/V
6	gain factor of ADC Mux, LED pin current		A_{MEAS_ILED}		10		LSB/mA
7	gain factor of ADC Mux, VDD5		A_{MEAS_VDD5}		142		LSB/V
8	relative error fraction of measurement any channel except ILED		$E_{MEAS\_REL\_ANY}$			2	%

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
9	relative error fraction of measurement, channel ILED		$E_{MEAS\_REL\_ILED}$			5	%
10	uncertainty error fraction of measurement, channel VLED, VS (S&H), PWMIN_HP/LP (S&H)		$E_{MEAS\_UNC\_VLED\_SH}$			141	mV
11	uncertainty error fraction of measurement, channel VS, PWMIN_HP/LP		$E_{MEAS\_UNC\_VS\_PWM}$			203	mV
12	uncertainty error fraction of measurement, channel VDD5		$E_{MEAS\_UNC\_VDD5}$			35	mV
13	uncertainty error fraction of measurement, channel ILED		$E_{MEAS\_UNC\_ILED}$			5	mA
14	saturated region, channel VLED		$E_{MEAS\_SAT\_VLED}$			281	mV
15	saturated region, channel PWMIN_HP/LP		$E_{MEAS\_SAT\_PWM}$			404	mV
16	saturated region, channel ILED		$E_{MEAS\_SAT\_ILED}$			10	mA
17	error of temperature sensor measurement*)		E_{MEAS_TEMP}	-15		15	K

*) Not tested in production

See chapter 7.10.2 for correct interpretation of the accuracy specification.
Note that saturated region for VDD5 and VS measurement is not given, because it is below recommended operating voltage

6.7.1 SAR ADC

Table 6.7.1-1: Electrical Parameters SAR ADC

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	resolution*)		N_{ADC}	-	10	-	bit
2	differential non-linearity		DNL_{ADC}	-1	-	2	LSB
3	integral non-linearity		INL_{ADC}	-2	-	2	LSB
4	conversion rate*)	ADC clock = 8/3 MHz 1 cycle sample extension	f_{ADC_CONV}		205		kS/s

*) Not tested in production

7 Functional Description

7.1 System Introduction

The E522.49 is a multi-channel PWM driver for e.g. light application. It provides 16 current sinks with integrated 10bit PWM generator for each channel. Each driver can be used to drive external loads up to 100mA with a selectable LED current slew rate. All LED channels provide separate PWM duty cycle settings and high precision wide-range LED current configuration.
The device can be used with customer-pre-configured PWM, current sinks and diagnosis set-up in combination with the bus interface configuration and diagnosis status functionality. A PWMIN interface makes it possible to use the device with 3 fully independent sets of PWM duty cycle and LED current configuration value in addition to the possibility to drive a configurable subset of the device LED pins with an incoming PWM signal.
Various diagnostic features, like LED open and short condition detection, are provided to meet automotive requirements.
An advanced device power management feature makes it possible to bundle LED channels and use an automatic current balancing to reduce device power consumption.
To protect the device from thermal damage, the device implements a configurable LED supply and device temperature dependent automatic LED current derating.
The LED driver device can be used in a device group, configured to behave like a single lamp in case of an LED open or short condition. For this reason two diagnosis groups can be defined an used to connect the grouped LED driver devices.
The device offers a wide range of operating modes and covers different use cases.

7.2 Device Startup

7.2.1 Device States

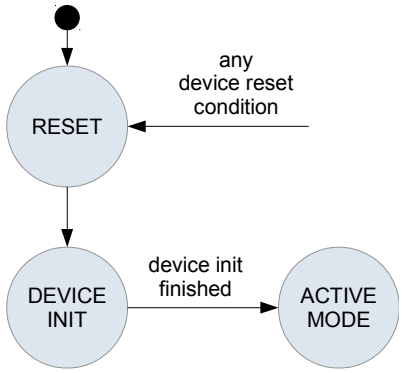

Figure 7.2.1-1: Device State Diagram

The device implements the following states as shown in the figure above:

- RESET
  - entered when any system reset source is active
  - when all reset sources are inactive system changes to DEVICE INIT

- DEVICE INIT
  - device configuration memory initialization from OTP
  - ADC sample data area initialization with 0-data
  - device internal initialization and functional set-up
  - the device initialization is handled by the Device Control Module
  - when device initialization has been finished, the device changes to ACTIVE MODE

- ACTIVE MODE
  - normal operating mode
  - the device internal data handling, as described later on, is done by the Device Control Module which handles the device internal data and adapts e.g. the LED current values regarding current derating and LED binning needs

The following table shows the device mode dependent state of the device components.

Table 7.2.1-1: Device Component Modes

system component	*RESET*	*DEVICE INIT*	*ACTIVE MODE*
communication bus interface	OFF	OFF	ON
system clock oscillator	-	running	running
LED current sinks	OFF	OFF	usable
PWM channels	cleared	cleared	usable
ADC	OFF	OFF	usable
over-temperature comparator	ON	ON	ON

7.3 UART Slave Bus Interface

7.3.1 UART Transmitter

The UART transmitter generates a differential voltage for communication. The generated voltage levels are oriented to standard CAN bus voltage levels. The bus is high-voltage protected, but does not support voltage levels far below local ground. Therefore, the minimal voltage driven at BUS_L ($V_{BUS\_DRV\_L}$) is higher than ground to allow more ground shift between communication nodes.
For short-circuit-protection, a current limiter for both lines is implemented.
To minimize radiation, a slew rate limit is implemented. Additionally, the maximum common mode ripple ($V_{BUS\_CM\_RIPPLE}$) generated by a single driver is limited, even if only a single resistor is used as termination. Figure 7.3.1-1 shows this termination. Optionally, the termination scheme shown at figure 7.3.1-2 can be used to stabilize the common mode more than $V_{BUS\_CM\_RIPPLE}$.

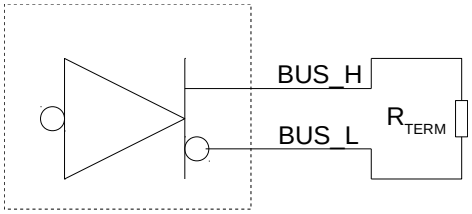

Figure 7.3.1-1: Recommended Bus Termination

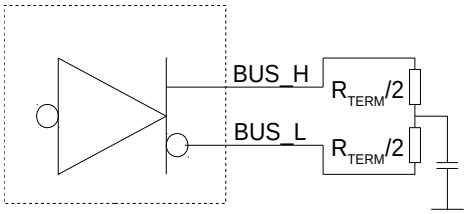

Figure 7.3.1-2: Bus Termination with Additional Common Mode Stabilization

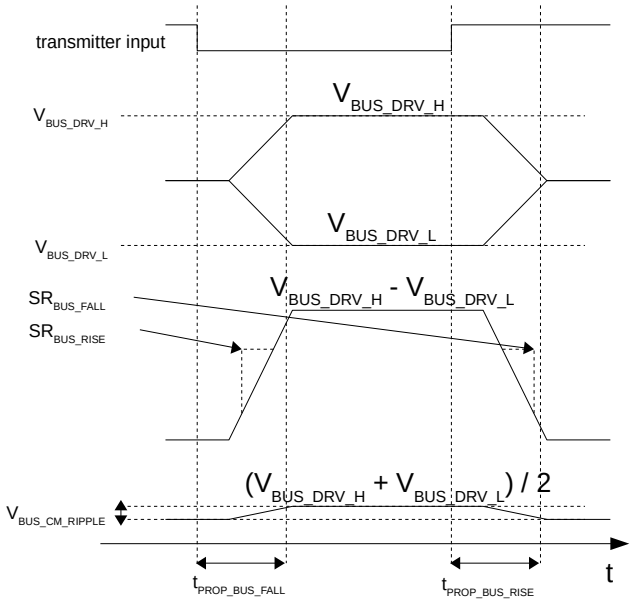

Figure 7.3.1-3: Bus Voltage Levels and Timing Diagram

7.3.2 UART Interface Features

- Data rate of 57600 Bit/s up to 500k Bit/s
- 8N1 data format, standard mark/space NRZ format
- LSB first communication
- Parity bit (even, odd, zero, none)
- Programmable stop bit length (1,2)
- Programmable break detection threshold (9.5xTBit, 11xTBit)
- Break measurement counter (baud clock based) to detect concurrent break events
  - Sync-byte baud measurement results are used to auto-adjust the baud rate
- Bus short detection with auto transmit shut down
- Overcurrent detection with auto transmit shut down

The UART provides a baud rate clock recovery to be able to communicate at data rates up to 500kBit/s without clock reference or quartz.

7.3.3 UART Protocol

Protocol Features:

- CRC protected communication
  - avoid misconfiguration of one or multiple bus slave devices
- frame based communication
  - unambiguous communication restart by using a frame starting break
- bus slave device auto baud rate adaption
  - determine communication baud rate by using sync byte measurement
- fixed frame header size
  - allows header content independent slave device error response even if any header content field is corrupted during transmission
- broadcast access to all bus slave devices

Protocol Frame Header Formats:

The device implements 2 different frame header formats which can be selected via UART configuration.

- 3 byte header format:
  - 1 to 31 bus slave devices and broadcast access: 5 bit
  - 1 to 16 data words (num_words): 4 bit
  - 8 bit device internal memory address space: 8 bit
  - read / write: 1 bit
  - Hamming Distance 4 CRC: 6 bit

- 4 byte header format:
  - 1 to 31 bus slave devices and broadcast access: 5 bit
  - 1 to 16 data words (num_words): 4 bit
  - 8 bit device internal memory address space: 8 bit
  - read / write: 1 bit
  - live count value: 6 bit
  - Hamming Distance 4 CRC: 8 bit

In the following frame format figures some abbreviations are used:

- ST : start bit
- PY : parity bit (optional)
- SP : stop bit(s)
- SW : switching between master and slave activity
- w : write bit = '1'
- r : read bit = '0'

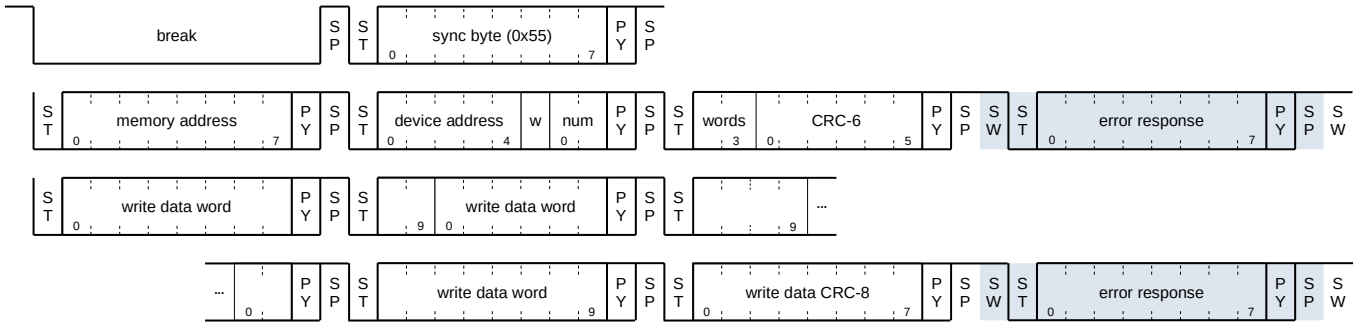

Figure 7.3.3-1: Write Frame Format (3 Byte Header Variant)

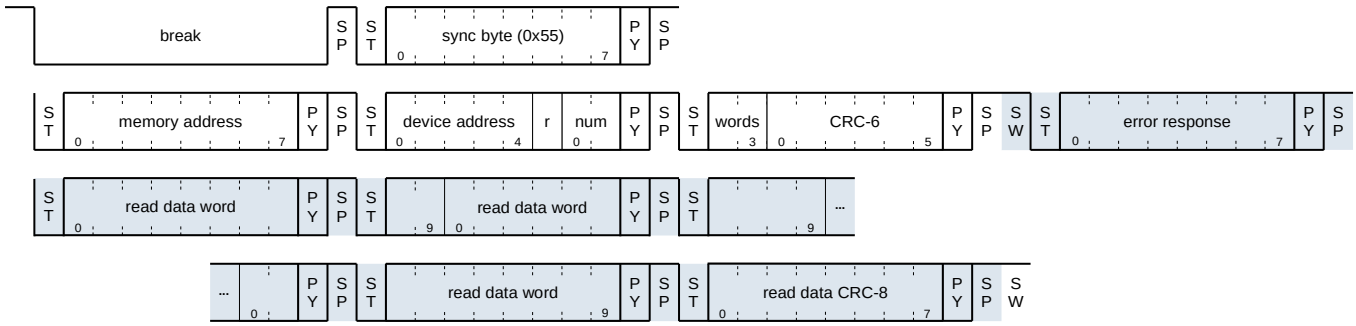

Figure 7.3.3-2: Read Frame Format (3 Byte Header Variant)

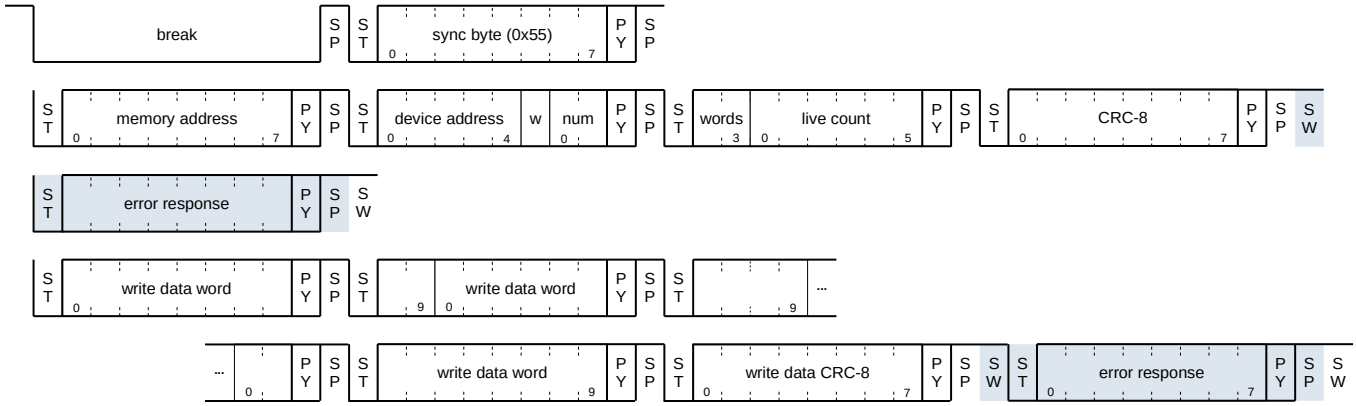

Figure 7.3.3-3: Write Frame Format (4 Byte Header Variant)

Figure 7.3.3-4: Read Frame Format (4 Byte Header Variant)

The following figures show the UART protocol flow of the bus master and slave devices.

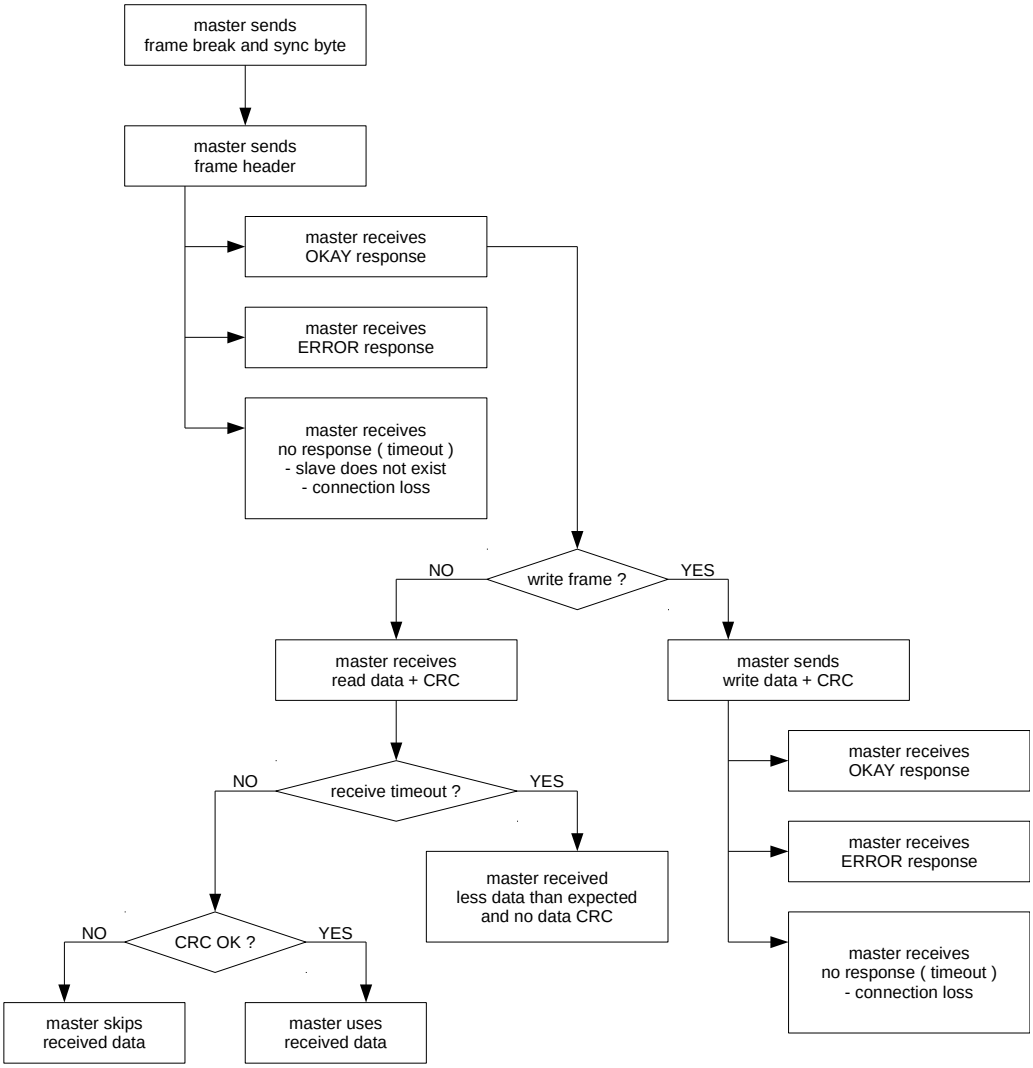

Figure 7.3.3-5: Bus Master Flow

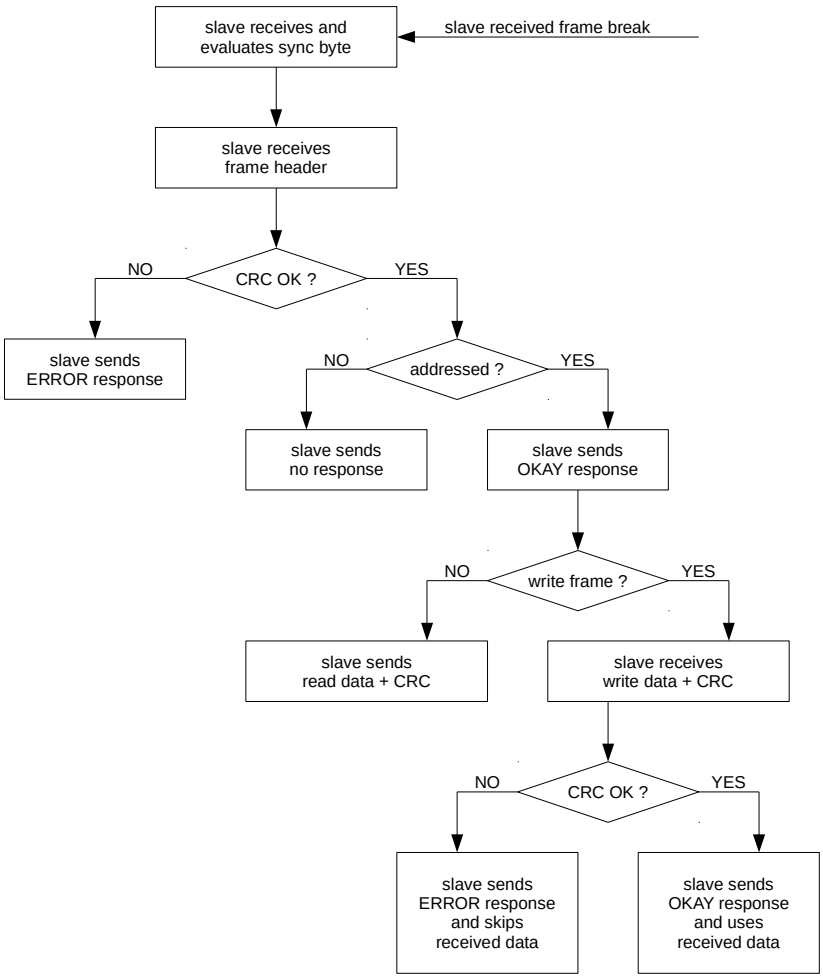

Figure 7.3.3-6: Bus Slave Flow

Protocol Handling:

Independent of the frame access mode (read / write) the frame header has a fixed length.
When a bus slave device receives a frame header it checks the header CRC.
If the header CRC is correct and the bus slave device is addressed by the header - in case of a broadcast address or explicit device address match - the bus slave device sends a frame header OKAY response.
If the header CRC is correct and the bus slave device is not addressed by the header, the bus slave device sends no response.
If the header CRC is incorrect - even if the bus slave device is addressed or not - the bus slave device sends an ERROR response.

If frame header CRC is correct and the device is addressed, the data part of the frame will be handled. Data is always handled as 10 bit word values.
In case of a read frame, the addressed bus slave device sends the requested number of data words (10 bit words) in a compact byte manner followed by a data CRC byte.
If the number of 10 bit data word stream bits is not a multiple of 8, the slave will fill up the last send byte with zero bits before sending the data CRC byte.
In case of a write frame, an addressed bus slave device receives the given number of data words including the additional write data CRC byte.

If the bus master sends a number of data word stream bits which is not a multiple of 8, the additional fill bits at the end of the data stream will be ignored by the bus slave device.
If the write data CRC is correct, the bus slave device sends a data OKAY response and uses the received data, otherwise a data ERROR response and skips the received data.

In case of a broadcast write frame, all bus slave devices will respond simultaneously. These responses will be combined by superposition on the bus and in case of mixed OKAY and ERROR responses this superposition will result in an ERROR response because of the dominant zero level. A bus one-level equals the resistive bus state.
In case of a broadcast write frame all bus slave devices have to evaluate this response to know if all bus slave devices have correctly received the broadcast data. In case of an ERROR response, the bus slave devices will skip the received data even if their own data CRC evaluation was correct. This guarantees the system data consistency.

Protocol Error Response Bytes:

The following figure shows the two possible error response bytes generated by a bus slave device.
A bus slave device will signal an OKAY response with 0xFC (2 zero-bits), an ERROR response with 0xC0 (6 zero-bits).
The master has to evaluate a response byte with less or equal than 4 zero-bits as an OKAY response, and a response byte with more than 4 zero-bits as an ERROR response.
In case of a broadcast response, the response byte parity bit can be corrupted because of the non-exact superposition timing of all bus slave response bytes on the bus. For this reason the response byte parity bit has not to be evaluated by the master and bus slave devices.

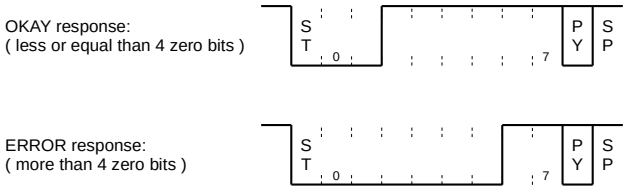

Figure 7.3.3-7: Bus slave error response

Break:

A Break is a long transmission pulse with low level. The Break pulse must be longer than the longest low level transmission in a valid data word.

For a 9 bit transmission per data bytes (without parity) CONFIG.break_sel = '0' can be set. A break length send from UART master to UART slaves of 13*TBit is recommended and must be minimal 9.5xTBit.

For a 10 bit transmission per data bytes (with parity) set CONFIG.break_sel = '1'. A break length send from UART master to UART slaves of 13*TBit is recommended and must be minimal 11xTBit.

Break Timeout:

A Break longer than 16xTBit leads to a Break timeout and a Break is not detected.

SYNC Byte:

The SYNC Byte value is always 0x55.

Broadcast:

Use device address 0x00 to broadcast all bus slave devices.

Universal Device Address:

A slave with device address configured to 0x00 can be addressed with any device address.

Live Count:

The Live Count is used in header 4 format only.
The 6 bit live count value must be unequal from last used live count value at this bus.
Additionally the live count value must not be 0x00.

If the live count value is wrong, then the addressed slave sends an ERROR response. Additionally all slaves reinitialize the live count value with 0x00. So the next correct transmitted live count value is valid for all slaves.

Number of 10 bit data words

The number of 10 bit data words is transmitted in header frame in num_words[3:0]. This value is split over two consecutive bytes. 1 to 16 data words (10 bit) can be transmitted.
In which num_words[3:0]=0x0 means 1 data word and num_words[3:0]=0xF means 16 data words.

CRC-Polynoms:

Three different CRC-Polynoms are implemented and automatical selected.
- 6 bit polynom 0x2C (HD4 for up to 25 bit) when 3 byte header
- 8 bit polynom 0x97 (HD4 for up to 119 bit) when 4 byte header or num_words < 11
- 8 bit polynom 0xA6 (HD3 for up to 247 bit) when num_words ≥ 11

For the CRC calculations the reverse CRC-polynoms are used.

CRC-Calculation:

All CRC calculations in used protocol are bytewise and LSB first.
BREAK and SYNC byte are not part of the CRC calculation.

Following CRC calculation sequence for a data byte is used (C style):

```
// calculate CRC for a data byte
uint8_t crc_calc(uint8_t crc, uint8_t rev_poly, uint8_t byte) {
        uint8_t n;
        for(n = 0; n < 8; n++) {
                if ((crc ^ byte) & 1) {
                        crc = (crc >> 1) ^ rev_poly;
                } else {
                        crc = (crc >> 1);
                }
                byte >>= 1;
        }
        return crc;
}
```

For generation of the reverse polynom, the following sequence is used:

```
// build reverse polynom
// example:
// polynomial 0xA6 => 1010.0110.1 (including bit 0 which is 1) => 1.0100.1101 = 0x14D
// => reversed 1.0110.0101 = 0x165 => 1011.0010.1 => 0xB2 (LSB skipped)
uint8_t calc_rev_poly(uint8_t poly) {
        uint8_t rev_poly = 1;
        while (poly > 1) {
                rev_poly = (rev_poly << 1) | (poly & 1);
                poly >>= 1;
        }
        return rev_poly;
}
```

CRC-6 Calculation:

The 6 bit CRC is only used for the transmission of 3 byte header frame.

CRC-6 Calculation Sequence:
- use 6 bit polynom 0x2C (HD4 for up to 25 bit)
  - calculate reverse polynom to 0x2C => 0x26
    - rev_poly = calc_rev_poly(0x2C)
- initialize crc variable with 0x3F
  - crc = 0x3F
- calculate crc with byte_1
  - crc = calc_crc(crc, rev_poly, byte_1)
- calculate crc with byte_2
  - crc = calc_crc(crc, rev_poly, byte_2)
- calculate crc with the two LSBs of byte_3 (6 MSBs must set to zero)
  - crc = calc_crc(crc, rev_poly, byte_3 & 0x03)
- concatenate the 6 bit CRC-6 result with the two LSBs of byte_3 to get the 3rd header byte
  - byte_3_crc = (crc << 2) | (byte_3 & 0x03)

CRC-8 Calculation:

The 8 bit CRC is used for transmittion of 4 byte header frame and for all data word transmissions. The polynom depends on the length of the transmission.

CRC-8 Calculation Sequence:
- use 8 bit polynom 0x97 (HD4 for up to 119 bit) when 4 byte header or num_words < 11
  - calculate reverse polynom to 0x97 => 0xF4
    - rev_poly = calc_rev_poly(0x97)
- use 8 bit polynom 0xA6 (HD3 for up to 247 bit) when num_words ≥ 11
  - calculate reverse polynom to 0xA6 => 0xB2
    - rev_poly = calc_rev_poly(0xA6)
- initialize crc variable with 0xFF
  - crc = 0xFF
- calculate crc with byte_1 (first byte)
  - crc = calc_crc(crc, rev_poly, byte_1)
- ...
- calculate crc with byte_N (last byte) to get the CRC-8 result
  - crc = calc_crc(crc, rev_poly, byte_N)

7.4 Device Access via the Bus Interface

7.4.1 Bus Interface Memory Map

The device configuration and status values can be accessed through the communication bus interface.
The following table defines the bus memory view map. The base address and area size values reflect the internal 16 bit organisation of the values. When transferred via the communication interface, the unused (always 0) address LSB is skipped. For this reason, only 8 address bits need to be transferred to access the complete area of 256 values.

The following table lists the 4 main access areas accessible via the bus interface.

Table 7.4.1-1: Bus Base Address Table

base address	*area size*	*name*	*type*	*description*
0x0000	0x80	BUS_CONFIG	CMD_UPDATE	area accessible via bus interface with update by command behavior
0x0080	0x80	BUS_CONFIG	IMM_UPDATE	area accessible via bus interface with immediate update behavior
0x0100	0x80	BUS_STATUS		area accessible via bus interface used for ADC result and system status data
0x0180	0x80	PAGING		page mapping area which makes STANDALONE and BUS_DEF_CONFIG areas accessible via bus interface

To access different parts of the device OTP configuration memory, the device implements a paging mechanism.
The following figure shows the memory view blocks visible via the bus interface.
There are three fixed areas, which are always visible. Two of these areas implement the same value mapping and are used as device control value area (BUS_CONFIG). One area (BUS_STATUS) implements access to ADC result values and other device status values.
The upper quarter of the bus interface memory view can be mapped to different memory areas (using the PAGE_BASE_ADDR register PAGE_BASE_ADDR) to e.g. access OTP area for device OTP configuration value programming.
All values necessary for application mode device usage (bus configuration and status values) are always accessible via the bus interface. For this reason it's not necessary to change memory mapping in application mode.

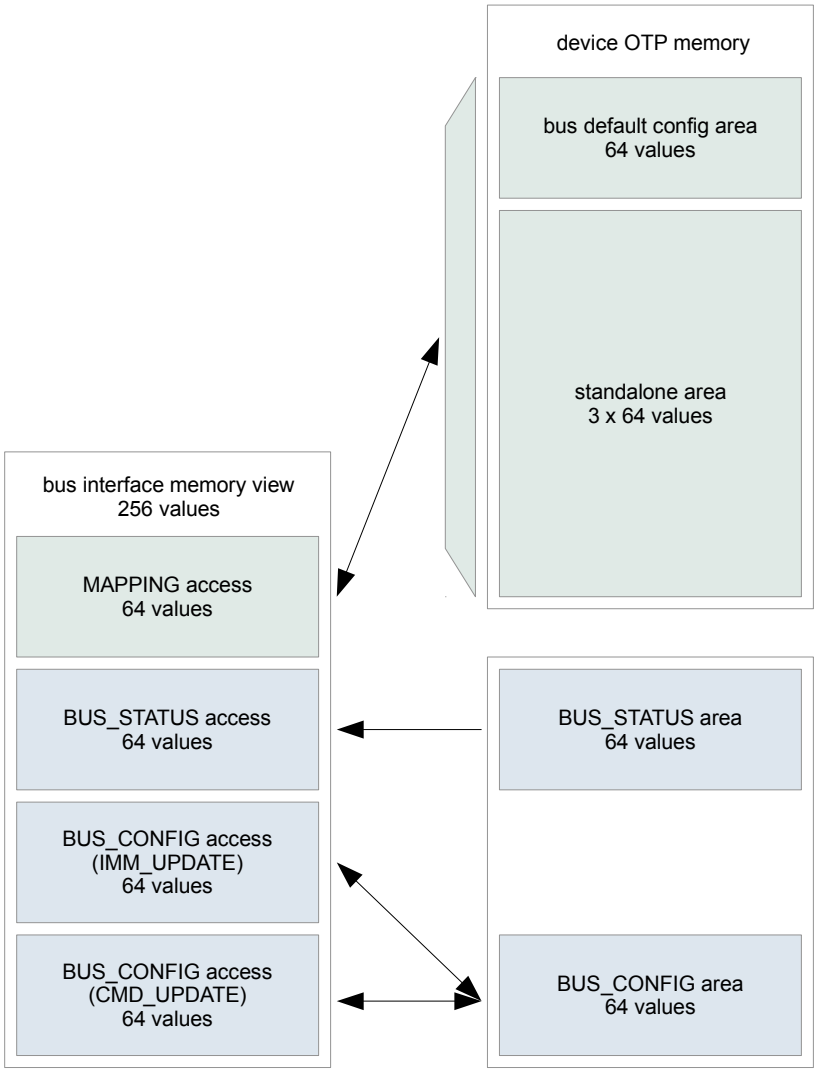

Figure 7.4.1-1: Bus Memory Mapping

In general:

- When writing BUS_CONFIG area values via bus interface, unused bitfields have to be written as zero.
- When programming BUS_DEF_CONFIG or STANDALONE area values via bus interface, unused bitfields have to be programmed as zero.
- When reading values from the device via bus interface, unused bitfields may contain non-zero values and therefore have to be ignored on evaluation.

7.4.2 Data Handling Structure

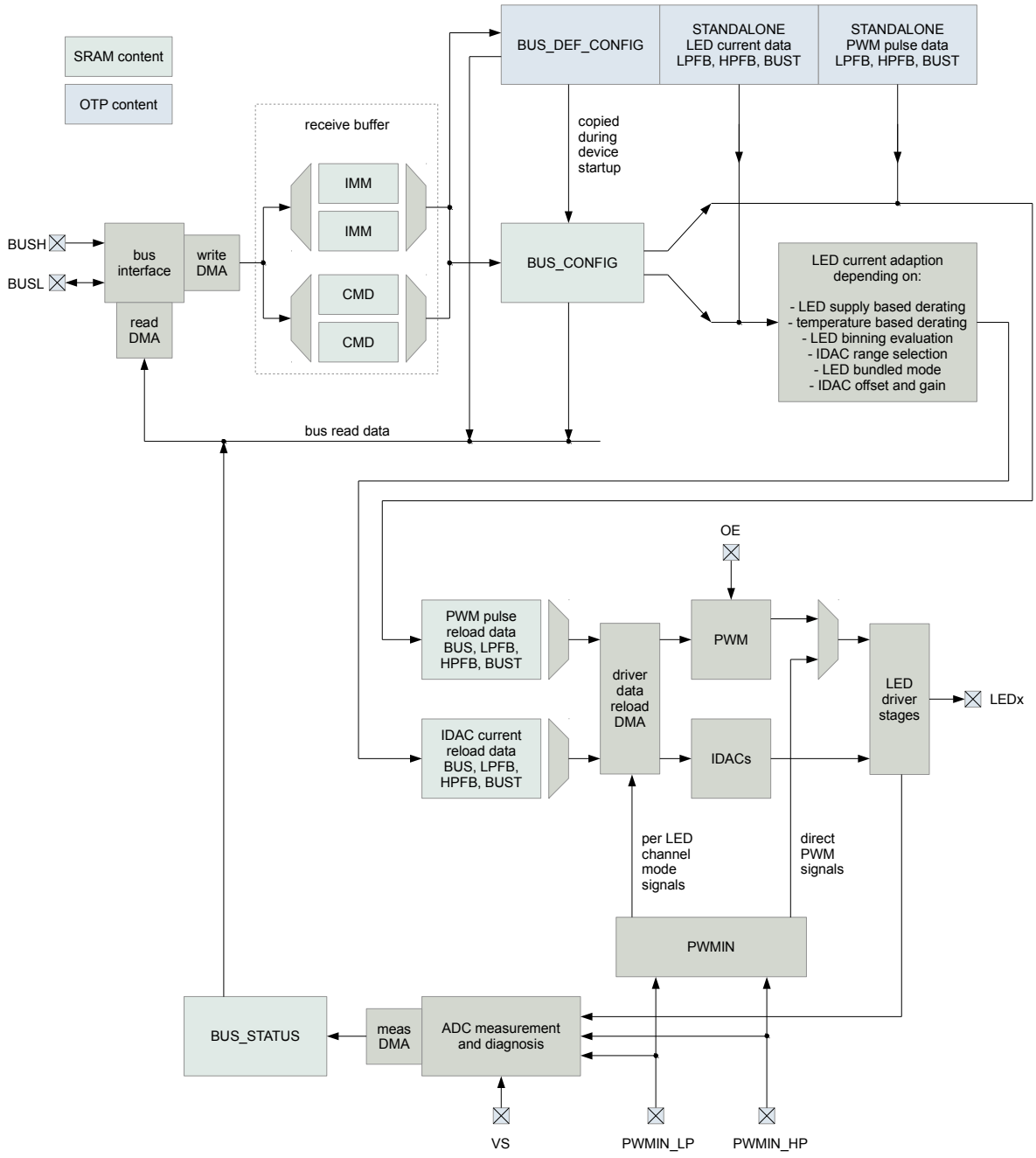

Figure 7.4.2-1: Device Data Handling

The Figure above shows the device internal PWM pulse length and LED current configuration data handling.
This data handling is done using DMA functionality and the Device Control Module.

Data comming in through the bus interface are first put into the receive buffers. This is needed to be able to evaluate the frame data CRC before writing the data to the actual BUS_CONFIG area, which is only done in case of a correct data CRC sum.

If the received data CRC sum does not match the received data, the data will be skipped and not be copied to the BUS_CONFIG area.

During device startup:
- The BUS_CONFIG area is initialized using OTP BUS_DEF_CONFIG data including BUS mode PWM pulse length and LED current configuration data.
- LPFB, HPFB and BUST mode related PWM pulse length data is copied from the OTP STANDALONE area to the device internal PWM pulse length reload data area.

Every time BUS_CONFIG PWM pulse length configuration data, derating factor or LED binning factor changes:
- BUS mode related LED current data is read from BUS_CONFIG area, adapted using derating, LED binning, IDAC range and LED bundled mode factors, and then written to the IDAC current reload data area.

Every time derating factor or LED binning factor changes:
- LPFB, HPFB and BUST mode related LED current data is read from OTP STANDALONE area, adapted using derating, LED binning, IDAC range and LED bundled mode factors, and then written to the IDAC current reload data area.

Depending on the PWMIN_LP and PWMIN_HP pin states and the PWMIN pin usage configuration (STANDALONE area PWMIN_ENABLE_x_x values), device internal mode signals are generated to select the correct PWM pulse length and LED current reload data set for each LED. Every PWMIN mode signal change triggers the common PWM and IDACs reload DMA to load the corresponding data set. It's also possible to feed a direct PWM signal, received through the PWMIN_LP or PWMIN_HP pin, to some or all LED driver stages instead of the internal PWM signal. In this case the used LED current configuration data can be selected using an ISINK_CONFIG 2 bit select value.

Active LED driver stages will be measured for diagnosis and the ADC result data is written to the BUS_STATUS area, readable via the bus interface. The BUS_CONFIG area can also be read via the bus interface e.g. to verify configuration data written via the bus interface.

The bus interface allows the programming and a read of the OTP STANDALONE and BUS_DEF_CONFIG (bus default configuration) areas using the page mapping area. Please see description below for more details.

7.4.3 Receive Buffers

The device implements 2 receive switch-buffers:

- one for the CMD update area,
- one for the IMM update area.

Each switch buffer consists of two parts:

- one part used by the communication interface to write the receive data to,
- the other used by the device control module to copy the data to their destination.

When the communication interface has received a complete write frame without errors, it switches the corresponding buffer and signals the new data available to the device control module using an interrupt. This mechanism makes it possible to receive write data frames without time gap between them.

An update command send via the IMM update area, causes the copy/evaluation of the switch buffer data by the device control module.
When no update command is received by the device, the CMD update area switch buffer data will not be evaluated by the device control module and will be overwritten by subsequent CMD area data frames.

The bus configuration and status areas are implemented as 10 bit value areas.
The CMD and IMM bus configuration areas share the same 64 word destination area (BUS_CONFIG).

7.4.4 Standalone Area

Table 7.4.4-1: STANDALONE

Register Name	*Address*	*Description*
UART_CONFIG	0x0FA	
UART_BAUDRATE	0x0FC	

Table 7.4.4-2: Register **UART_CONFIG** (0x0FA)

Bit	*Name*	*Default*	*Access*	*Description*
9	-	0	R	
8	auto_baud	0	R	sync byte related auto baud adaption enable 0: auto baud adaption disabled (default) 1: auto baud adaption enable
7	break_sel	0	R	break time configuration 0: 9.5*Tbit (default) 1: 11*Tbit Note: When a parity bit is configured then the break time configuration is internal set to 11*Tbit automatically.
6	stop	0	R	stop bit configuration 0: 1 stop bit (default) 1: 2 stop bits
5:4	parity	0	R	parity configuration 0: even (default) 1: odd 2: zero (parity bit is always '0') 3: none (no parity bit)
3:1	turn_around	0	R	additional turn around time at change of transmit direction from master transmit to slave transmit [half Tbit]
0	format	0	R	UART frame header format 0: 3 byte header format (CRC-6 variant) (default) 1: 4 byte header format (CRC-8 variant)

Table 7.4.4-3: Register **UART_BAUDRATE** (0x0FC)

Bit	*Name*	*Default*	*Access*	*Description*
9	-	0	R	
8:0	div	0	R	baud rate divider Note: baud_rate = uart_clock_frequency / div -> div = uart_clock frequency / baud_rate uart_clock_frequency = 24MHz Example : baud_rate = 500k Baud div = 24000000 / 500000 div = 48 (0x30) (default) Example : baud rate = 57600 Baud div = 24000000 / 57600 div = 417 (0x1A1) Note: Will be initialized from OTP during power up. Note: If this value is not configured, a default value of 48 will be used.

7.4.5 Bus Communication Timeout

A communication timeout can be configured to make sure, the device uses a valid set of data when communication stops for a longer time or CRC valid communication is not possible.
The timeout is active after device start up, if the bus standalone area timeout mode configuration COM_TIMEOUT.val is programmed to a non-zero value. A timeout up to 1s can be configured using COM_TIMEOUT inside the standalone area value.
When a bus communication timeout occurs, all LEDs in bus mode (PWMIN defined mode), will change to the bus timeout PWM pulse length and LED current configuration data usage.
The communication timeout counter is reset, every time a valid bus interface frame header is received in case of write and read frames. At this moment the device also changes back to bus mode configuration data usage.
Bus timeout mode can only be entered from bus mode. LED channels which are in LPFB, HPFB or direct PWM mode will not be affected when a bus timeout occurs.

7.4.6 Empty Device Behavior

If no communication device address has been programmed before to the device STANDALONE area COM_DEV_ADDR value, the bus interface is inactive and will not receive or interpret bus frames. To switch such a device to an active bus interface mode, the PROG pin has to be set to active high level during device startup. The device will then be accessible using device address 31 and device group 1.

To assign unique device addresses to all LED driver devices connected to a common bus, the following procedure can be used:

1. Set one device PROG pin to active high level and restart at least this device via it's reset pin or a power cycle.
2. Access the device using the device address value 31 and device group 1.
3. Program a unique device address value (larger than 0, smaller than 31) to STANDALONE COM_DEV_ADDR.
4. Remove the PROG pin active high level and repeat these steps with all other devices.

Note: The last assigned device address can also be a 31.

7.4.7 OTP Programming via Bus Interface

Programming of the STANDALONE and bus default configuration (BUS_DEF_CONFIG) areas is possible via the bus interface. For this, the PROG pin has to be set to active high level to allow programming.

The programming can be done as follows:

1. The target page has to be selected using the BUS_CONFIG area PAGE_BASE_ADDR value.
2. The data to be programmed have to be written via a single bus interface frame.
3. The programming busy status has to be polled reading the BUS_STATUS area PROG_STATUS value.
4. When the programming busy status changes to non-busy, the PROG_STATUS error flag has to be evaluated.
5. If more data has to be programmed, continue with step 1 or 2.

7.4.8 Bus Configuration Area

Table 7.4.8-1: BUS_CONFIG

Register Name	*Address*	*Description*
PAGE_BASE_ADDR	0x60	
CMD_RESET	0x7C	
CMD_UPDATE	0x7E	

Table 7.4.8-2: Register **PAGE_BASE_ADDR** (0x60)

Bit	*Name*	*Default*	*Access*	*Description*
9:3	-	0	R	
2:0	sel	0	R/W	standalone and bus default config page selection 0 : selects standalone page 0 for access (0x000 ... 0x07E) 1 : selects standalone page 1 for access (0x080 ... 0x0FE) 2 : selects standalone page 2 for access (0x100 ... 0x17E) 3 : selects bus default config page for access 4 .. 7 : reserved, do not write in application

Table 7.4.8-3: Register **CMD_RESET** (0x7C)

Bit	*Name*	*Default*	*Access*	*Description*
9:0	cmd	0	W	writing the value 0x0259 asserts a device reset

Table 7.4.8-4: Register **CMD_UPDATE** (0x7E)

Bit	*Name*	*Default*	*Access*	*Description*
9:0	cmd	0	W	writing the value 0x026A updates received bus command area data to the system

7.4.9 Bus Status Area

Table 7.4.9-1: BUS_STATUS

Register Name	*Address*	*Description*
PROG_STATUS	0x7E	OTP programming status

Table 7.4.9-2: Register **PROG_STATUS** (0x7E) OTP programming status

Bit	*Name*	*Default*	*Access*	*Description*
9:4	-	0	R	
3:2	base_addr_sel	0	R	read-back value of selected mapping area page This value can be used to be sure that mapping area page base address value set via BUS_CONFIG PAGE_BASE_ADDR is active, because after setting the PAGE_BASE_ADDR.sel value it takes some time to switch to the requested page. Without checking this value until it has the same value as requested, mapping area read requests may read from the previous active (wrong) mapping area !
1	error	0	R	0 : programming successful 1 : programming failed
0	busy	0	R	1 : programming in progress

7.4.10 Standalone Area

Table 7.4.10-1: STANDALONE

Register Name	*Address*	*Description*
COM_DEV_ADDR	0x0F6	communication interface device address value
COM_TIMEOUT	0x0F8	communication timeout configuration value
DEVICE_INFO	0x17A	device version information
FOR_CUSTOMER_USE_0	0x17C	reserved for customer specific use
FOR_CUSTOMER_USE_1	0x17E	reserved for customer specific use

Table 7.4.10-2: Register **COM_DEV_ADDR** (0x0F6) communication interface device address value

Bit	*Name*	*Default*	*Access*	*Description*
9:5	-	0	R	
4:0	addr	0	R	bus slave device address address value 0 is used as broadcast address value address values 1 to 31 are used for explicit device access Note: If this register is not configured, a default value of 31 will be used.

Table 7.4.10-3: Register **COM_TIMEOUT** (0x0F8) communication timeout configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9	diag1_e	0	R	0 : a bus communication timeout has no effect on DIAG1 1 : a bus communication timeout asserts DIAG1
8	diag0_e	0	R	0 : a bus communication timeout has no effect on DIAG0 1 : a bus communication timeout asserts DIAG0
7	timebase	0	R	selects the timeout timebase 0 : 1ms 1 : 8ms
6:0	val	0	R	communication interface timeout before the device LEDs in bus mode change to bus timeout mode timeout = (val + 1) * timebase example (timebase = 8ms, val = 127): timeout = 128 * 8ms = 1s example (timebase = 1ms, val = 3): timeout = 4 * 1ms = 4ms Note: val = 0 disables the bus timeout.

Table 7.4.10-4: Register **DEVICE_INFO** (0x17A) device version information

Bit	*Name*	*Default*	*Access*	*Description*
9:5	ic_version	1	R	Silicon version of IC
4:0	fw_version	1	R	Firmware version of IC

Table 7.4.10-5: Register **FOR_CUSTOMER_USE_0** (0x17C) reserved for customer specific use

Bit	*Name*	*Default*	*Access*	*Description*
9:0	val_customer	0	R	

Table 7.4.10-6: Register **FOR_CUSTOMER_USE_1** (0x17E) reserved for customer specific use

Bit	*Name*	*Default*	*Access*	*Description*
9:0	val_customer	0	R	

7.5 PWMIN Interface

The device implements two PWMIN inputs, a low priority (PWMIN_LP) and a high priority (PWMIN_HP) input. The PWMIN signals evaluation is used to implement prioritized fallback modes, which use pre-defined PWM pulse length and LED current data, and a direct PWM signal feed-through mode.
The following figure shows the PWMIN state diagram. State changes are driven by the PWMIN signal level and a detection of a valid PWM input signal. The PWM detection timing parameter can be configured.

Each PWMIN input (PWMIN_LP, PWMIN_HP) implements the following states:

- bus configuration usage
  - when related PWMIN pin input level is static 0
- PWM direct mode
  - when related PWMIN pin receives a valid PWM signal
- fallback configuration mode
  - when related PWMIN pin input level is static 1

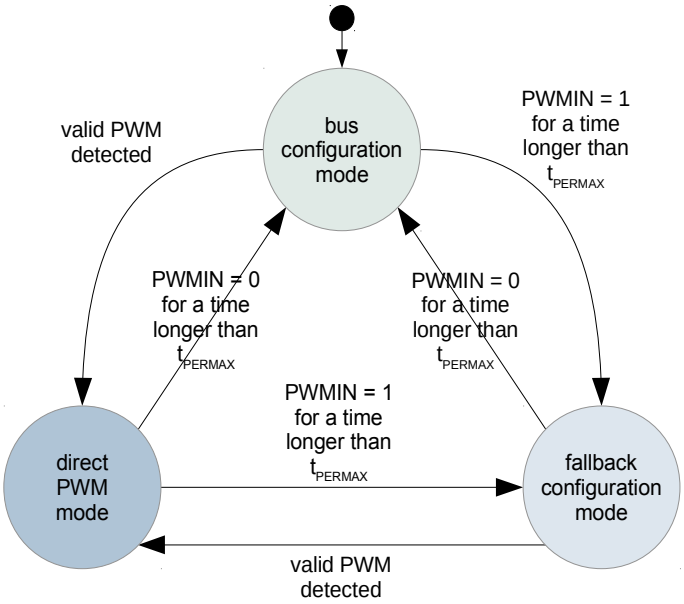

Figure 7.5-1: PWMIN Pin State Diagram

The following figures and tables describe the modes generated by the PWMIN Interface depending on the two PWMIN pin states and their influence to the PWM System and current sinks configuration data usage.
The mode signals are generate per LED channel. The device implements a 2 bit PWMIN usage configuration per LED channel, which allows to enable the usage of the PWMIN_LP and PWMIN_HP input signals per LED channel. Please see standalone area PWMIN_ENABLE_x_x values description for details.

Received PWM signals will be considered to be valid when its period is:

- larger as or equal to t_{PERMIN}
- smaller as or equal to t_{PERMAX}

Period length measurement starts at each edge of PWMIN input signal. There are independent length measurement units, one for the rising PWMIN signal edge, one for the falling PWMIN signal edge.

t_{PERMIN} can be configured using the PWMIN_TIMING.TPERMIN value

- PWMIN_TIMING.TPERMIN configuration range = 0 .. 30
- t_{PERMIN} = (PWMIN_TIMING.TPERMIN + 1) * 256us
- t_{PERMIN} configuration range: 256us .. 7936us (3906Hz down to 126Hz)

t_{PERMAX} can be configured using the PWMIN_TIMING.TPERMAX value

- PWMIN_TIMING.TPERMAX configuration range = (PWMIN_TIMING.TPERMIN + 1) .. 31
- t_{PERMAX} = (PWMIN_TIMING.TPERMAX + 1) * 256us
- t_{PERMAX} configuration range: 512us .. 8192us (1953Hz down to 122Hz)

When the PWMIN period is considered to be too small, PWMIN state stays the same, when too large, PWMIN state changes to:

- "bus configuration mode", when a static 0 level is detected
- "fallback configuration mode", when a static 1 level is detected

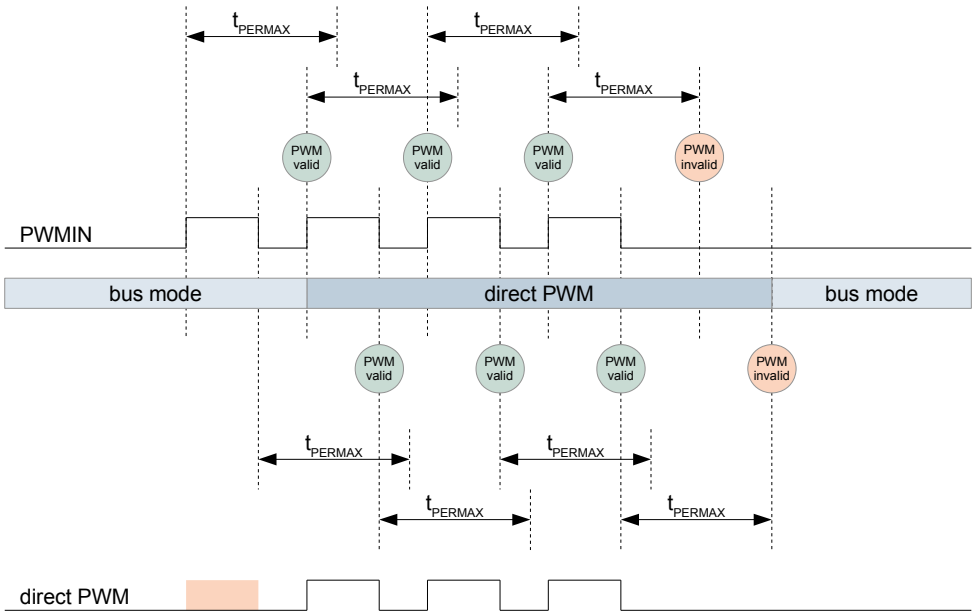

Figure 7.5-2: Change Between Bus Mode and Direct PWM

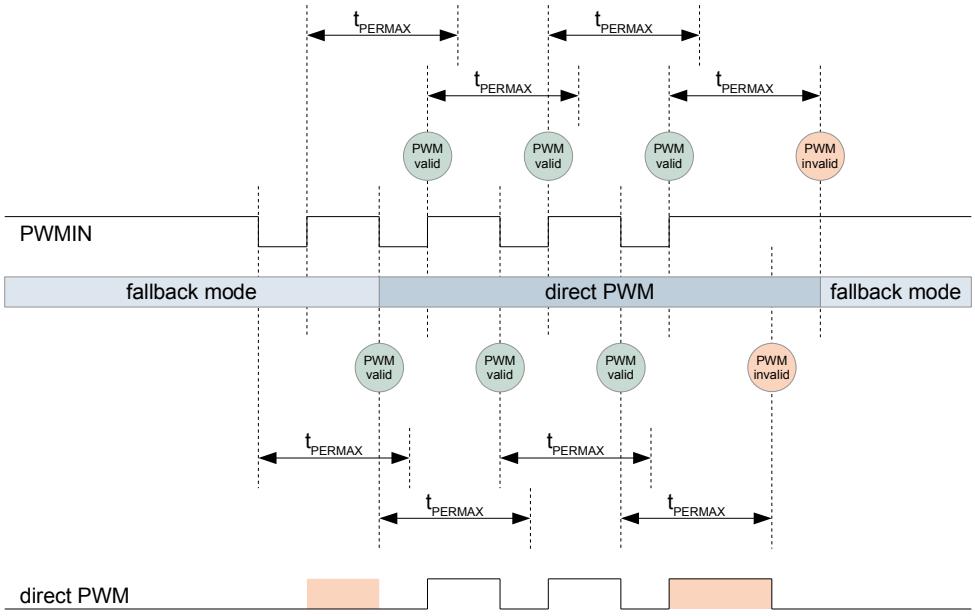

Figure 7.5-3: Change Between Fallback Mode and Direct PWM

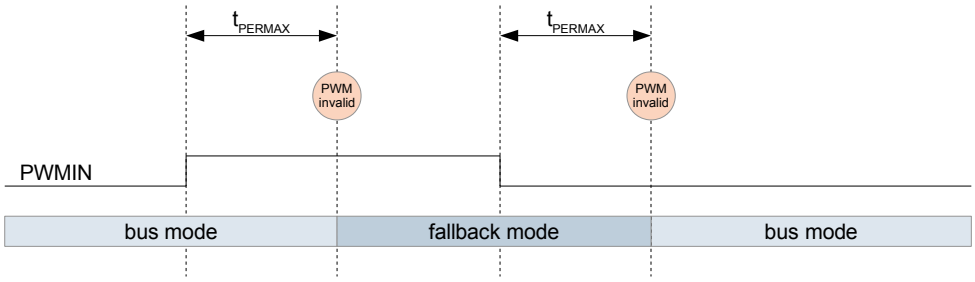

Figure 7.5-4: Change Between Bus Mode and Fallback Mode

Table 7.5-1: PWMIN Interface Generated Modes

bus timeout	*PWMIN_LP state*	*PWMIN_HP state*	*PWMIN mode*
1	0	0	bus timeout mode
0	0	0	bus mode
-	1	0	low priority fallback (LPFB) mode
-	valid PWM	0	low priority direct PWM mode
-	-	1	high priority fallback (HPFB) mode
-	-	valid PWM	high priority direct PWM mode

When LED data mode changes, related PWM pulse length and LED current values are loaded and get active immediately at the driver stages.
The currently generated PWM pulse will be extended, shorted or re-activated depending on the previously used and currently loaded values and the current time stamp inside the PWM channel virtual period.

For a description of the PWMIN mode dependent data usage, please see 7.4.2.

7.5.1 Standalone Area

Table 7.5.1-1: STANDALONE

Register Name	*Address*	*Description*
PWMIN_TIMING	0x0C2	PWMIN pins timing configuration value
PWMIN_ENABLE_0_3	0x0C4	LED channels 0 to 3, PWMIN usage enable value
PWMIN_ENABLE_4_7	0x0C6	LED channels 4 to 7, PWMIN usage enable value
PWMIN_ENABLE_8_11	0x0C8	LED channels 8 to 11, PWMIN usage enable value
PWMIN_ENABLE_12_15	0x0CA	LED channels 12 to 15, PWMIN usage enable value

Table 7.5.1-2: Register **PWMIN_TIMING** (0x0C2) PWMIN pins timing configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:5	max	0	R	valid period max value (TPERMAX) resulting value = (max + 1) * 256us
4:0	min	0	R	valid period min value (TPERMIN) resulting value = (min + 1) * 256us

Table 7.5.1-3: Register **PWMIN_ENABLE_0_3** (0x0C4) LED channels 0 to 3, PWMIN usage enable value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7	led3_hp_e	0	R	PWMIN_HP signal usage for LED channel 3 enable
6	led3_lp_e	0	R	PWMIN_LP signal usage for LED channel 3 enable
5	led2_hp_e	0	R	PWMIN_HP signal usage for LED channel 2 enable
4	led2_lp_e	0	R	PWMIN_LP signal usage for LED channel 2 enable
3	led1_hp_e	0	R	PWMIN_HP signal usage for LED channel 1 enable
2	led1_lp_e	0	R	PWMIN_LP signal usage for LED channel 1 enable
1	led0_hp_e	0	R	PWMIN_HP signal usage for LED channel 0 enable
0	led0_lp_e	0	R	PWMIN_LP signal usage for LED channel 0 enable

Table 7.5.1-4: Register **PWMIN_ENABLE_4_7** (0x0C6) LED channels 4 to 7, PWMIN usage enable value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7	led7_hp_e	0	R	PWMIN_HP signal usage for LED channel 7 enable
6	led7_lp_e	0	R	PWMIN_LP signal usage for LED channel 7 enable
5	led6_hp_e	0	R	PWMIN_HP signal usage for LED channel 6 enable
4	led6_lp_e	0	R	PWMIN_LP signal usage for LED channel 6 enable
3	led5_hp_e	0	R	PWMIN_HP signal usage for LED channel 5 enable
2	led5_lp_e	0	R	PWMIN_LP signal usage for LED channel 5 enable
1	led4_hp_e	0	R	PWMIN_HP signal usage for LED channel 4 enable
0	led4_lp_e	0	R	PWMIN_LP signal usage for LED channel 4 enable

Table 7.5.1-5: Register **PWMIN_ENABLE_8_11** (0x0C8) LED channels 8 to 11, PWMIN usage enable value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7	led11_hp_e	0	R	PWMIN_HP signal usage for LED channel 11 enable
6	led11_lp_e	0	R	PWMIN_LP signal usage for LED channel 11 enable
5	led10_hp_e	0	R	PWMIN_HP signal usage for LED channel 10 enable
4	led10_lp_e	0	R	PWMIN_LP signal usage for LED channel 10 enable
3	led9_hp_e	0	R	PWMIN_HP signal usage for LED channel 9 enable
2	led9_lp_e	0	R	PWMIN_LP signal usage for LED channel 9 enable
1	led8_hp_e	0	R	PWMIN_HP signal usage for LED channel 8 enable
0	led8_lp_e	0	R	PWMIN_LP signal usage for LED channel 8 enable

Table 7.5.1-6: Register **PWMIN_ENABLE_12_15** (0x0CA) LED channels 12 to 15, PWMIN usage enable value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7	led15_hp_e	0	R	PWMIN_HP signal usage for LED channel 15 enable
6	led15_lp_e	0	R	PWMIN_LP signal usage for LED channel 15 enable
5	led14_hp_e	0	R	PWMIN_HP signal usage for LED channel 14 enable
4	led14_lp_e	0	R	PWMIN_LP signal usage for LED channel 14 enable
3	led13_hp_e	0	R	PWMIN_HP signal usage for LED channel 13 enable
2	led13_lp_e	0	R	PWMIN_LP signal usage for LED channel 13 enable
1	led12_hp_e	0	R	PWMIN_HP signal usage for LED channel 12 enable
0	led12_lp_e	0	R	PWMIN_LP signal usage for LED channel 12 enable

7.6 Digital IOs

The signal polarity of some device digital input pins can be configured using the IO_CONFIG value. These pins are: OE, PWMIN_LP and PWMIN_HP.
This makes it possible to connect inverted control signals to the device and enable the device internal inversion and behave like the device where supplied with non-inverted control signals.
The description in the following chapters refers to the internal signal states, which represent the "normal" control signal polarity.
OE, PWMIN_LP and PWMIN_HP show a pull-down behavior if inversion is disabled. The pull direction changes with the selected polarity and for this changes to pull-up if the invert option is selected.
The following figures show the pull-up and pull-down IO typical current behavior of the digital IOs. The internal pull resistor voltage will be limited to approximately V_{DIG_PULL}+0.2V. For this reason the pull current saturates above V_{DIG_PULL}+0.2V IO input voltage.

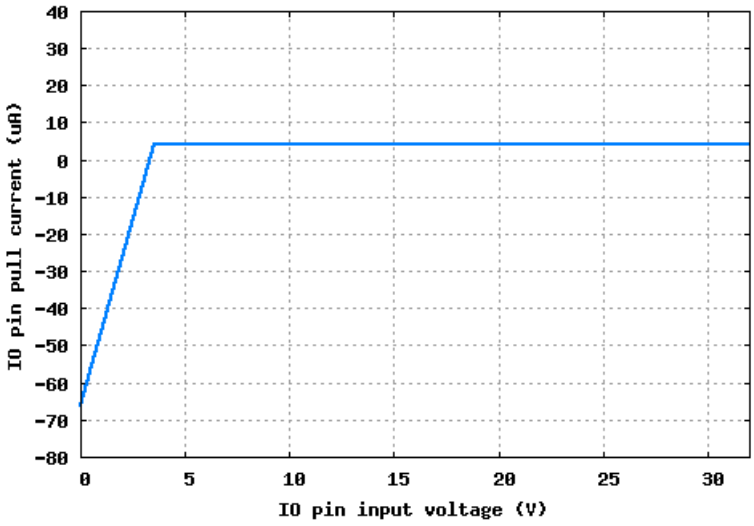

Figure 7.6-1: Digital IO Pull-up Typical Current Behavior

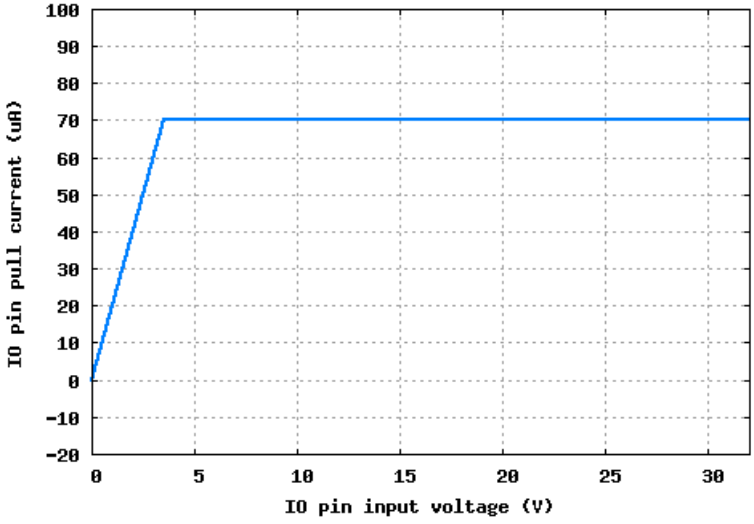

Figure 7.6-2: Digital IO Pull-down Typical Current Behavior

7.6.1 Standalone Area

Table 7.6.1-1: STANDALONE

Register Name	*Address*	*Description*
IO_CONFIG	0x14E	IO configuration value

Table 7.6.1-2: Register **IO_CONFIG** (0x14E) IO configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:4	-	0	R	
3	reserved	0	R	Reserved, write default value
2	pwmin_hp_inv	0	R	PWMIN_HP pin invert selection 0 : not inverted and pull-down 1 : inverted and pull-up
1	pwmin_lp_inv	0	R	PWMIN_LP pin invert selection 0 : not inverted and pull-down 1 : inverted and pull-up
0	oe_inv	0	R	OE pin invert selection 0 : not inverted and pull-down 1 : inverted and pull-up

7.7 PWM System

The PWM system generates the PWM pulse signals needed to control the LED driver stages. It consists of a common PWM period generator (configured using PWM_PRESCALER and PWM_PERIOD values) and 16 independent PWM generator channels (configured using the PULSE_x values).

The figure below shows the PWM generator structure.

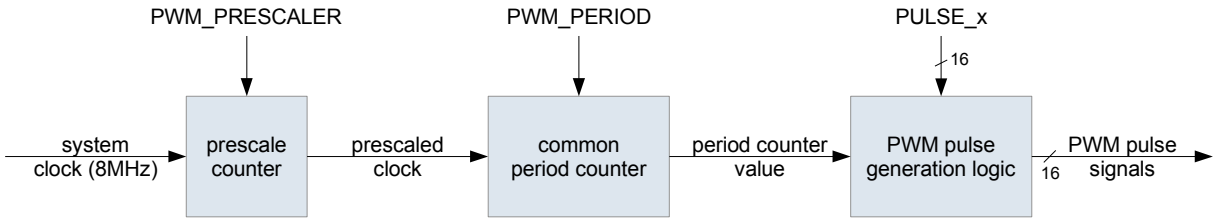

Figure 7.7-1: PWM Generator Structure

The timing figure below shows an example timing of the prescaler counter, the period counter and different pulse lengths shown as LED channels a, b and c. In this example the prescaler is configured with a value of 5, resulting in a prescaler dividing factor of 6 system clock cycles. The period counter in this example is configured with a value of 4 which results in counting from 0 to 3. The period counter is incremented every time the prescaler counter is reset to 0 when reaching it's configuration value. The period counter itself is reset to 0 every time it reaches it's period configuration value minus one. This results in a PWM period length equal to the PWM_PERIOD configuration value, based on a prescaled increment clock. In the example timing below, the pulse starting time stamps are equal and correspond to the period counter re-start event time stamp. The channel a is configured to generate a 2 PWM cycle pulse, the channel b is configured to generate a 3 PWM cycle pulse and the channels c generates a 100% duty cycle pulse. A channel PWM pulse length configured to be longer than the PWM period will result in 100% duty cycle for this channel.

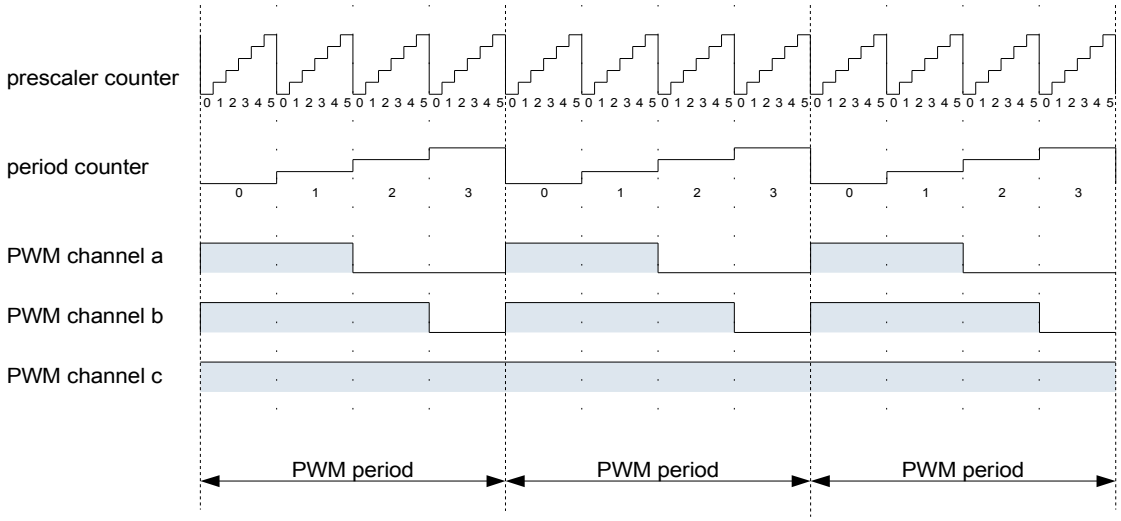

Figure 7.7-2: PWM Prescaler, Period and Pulse Timing

Please keep in mind, that the PWM_PERIOD configuration value is supposed to be set to 1023, else the generated PWM pulse signals will not have the full 10 bit resolution.

Each PWM pulse generation logic channel uses its own virtual PWM period and can be set up to generate a PWM signal with duty cycles from 0% up to 100%. The PWM pulse starting points of the 16 channels can be configured using the PWM_CONFIG value as follows:

- all PWM pulses start at the same time stamp
  - adjacent PWM channel pulse starting point distance = 0
- all PWM pulse starting points are distributed equidistantly over the PWM period
  - adjacent PWM channel pulse starting point distance = PWM period / 16

The following figure shows an example of equidistantly distributed PWM channel starting time stamps with all PWM channels set up with 75% duty cycle. The coloured parts mark the virtual PWM period of the different PWM channels.

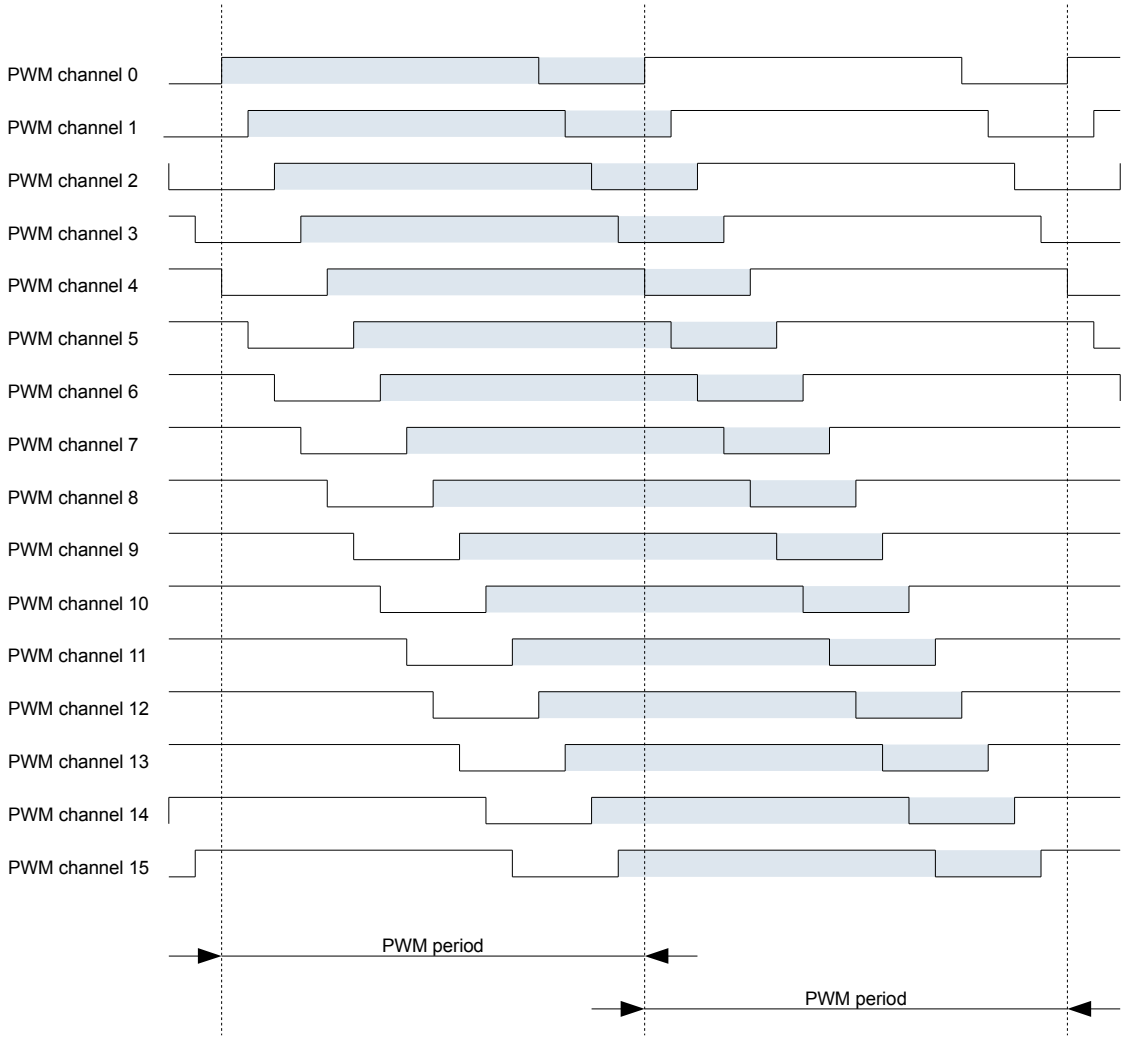

Figure 7.7-3: Equidistantly Distributed Timing Example

If LED PWM channels are combined (using the PWM_COMBINE_x values), these PWM channels are supplied with the same PWM pulse length value (taken from the first channel inside the combined channel group) and will start at the same time stamp, which means these PWM channels are active during exactly the same time period.

The following figure shows an example of a combined PWM channel timing. In this example 8 groups of 2 adjacent LED PWM channels are combined.

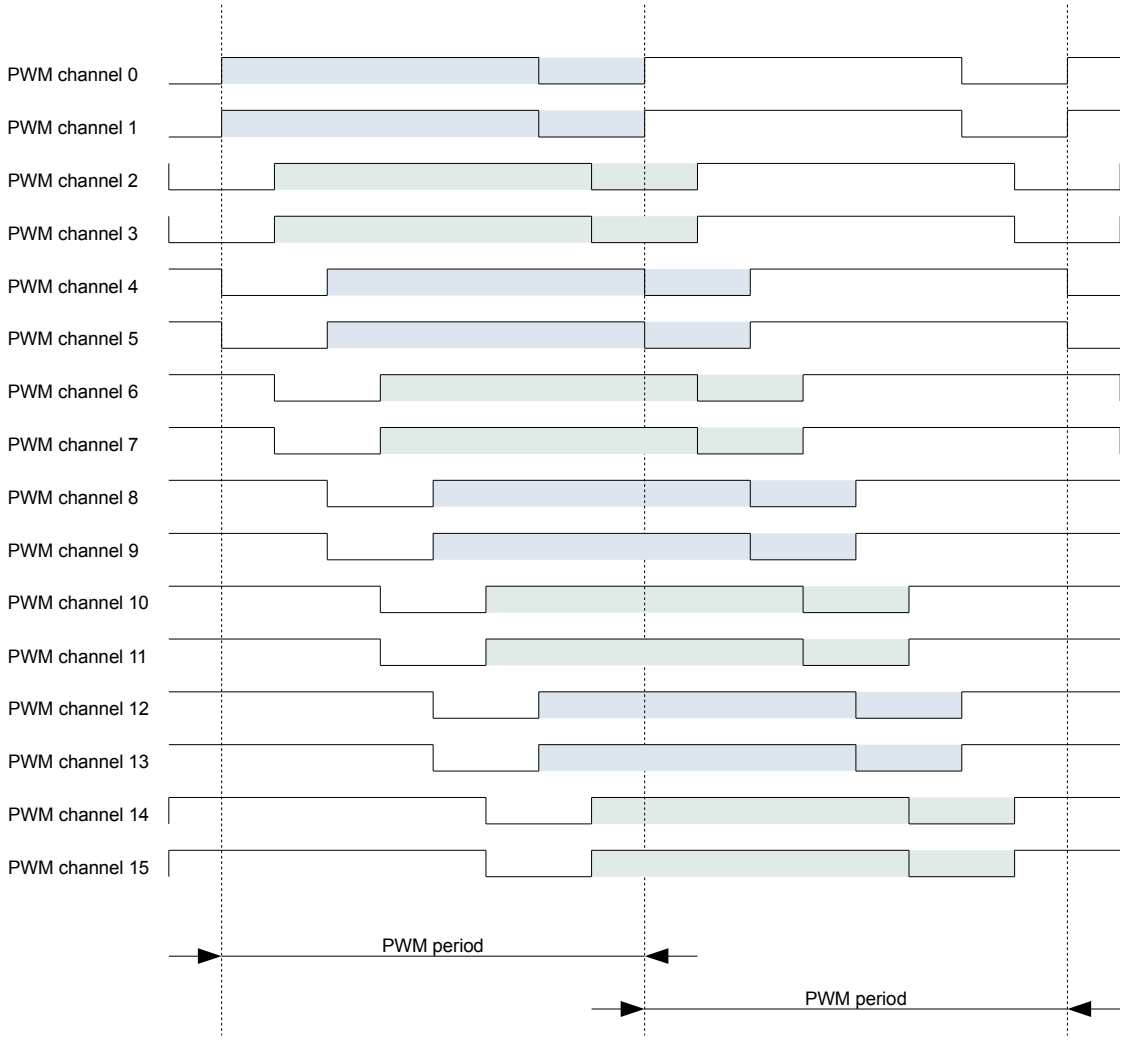

Figure 7.7-4: Combined PWM Channels Example

7.7.1 OE PWM Masking

The OE pin can be used to mask PWM signals generated by the PWM system generator.
When the OE pin is inactive (low level in case of non-inverted OE usage), the PWM pulses of all LED channels in bus mode are suppressed, which sets the related LED channel driver stages to an off state. When the OE pin is active (high level in case of non-inverted OE usage), this mask is removed and PWM signals of LED channels in bus mode are fed from the PWM generator to the related LED driver stages.
There is an option (via STANDALONE PWM_CONFIG value) to apply the same masking behavior also to LED channels in bus timeout mode.

The OE pin state does not influence the PWMIN direct PWM, which is directly fed to the configured LED driver stages, when a valid PWM at the PWMIN pins was recognized. All LED channels in a fallback mode are not masked and the PWM system generator signals are fed to these LED channel driver stages and are not influenced by the OE pin state.

7.7.2 Bus Configuration Area

Table 7.7.2-1: BUS_CONFIG

Register Name	*Address*	*Description*
BUS_PULSE_0	0x00	LED0 PWM pulse length configuration value
BUS_PULSE_1	0x02	LED1 PWM pulse length configuration value
BUS_PULSE_2	0x04	LED2 PWM pulse length configuration value
BUS_PULSE_3	0x06	LED3 PWM pulse length configuration value
BUS_PULSE_4	0x08	LED4 PWM pulse length configuration value
BUS_PULSE_5	0x0A	LED5 PWM pulse length configuration value
BUS_PULSE_6	0x0C	LED6 PWM pulse length configuration value
BUS_PULSE_7	0x0E	LED7 PWM pulse length configuration value
BUS_PULSE_8	0x10	LED8 PWM pulse length configuration value
BUS_PULSE_9	0x12	LED9 PWM pulse length configuration value
BUS_PULSE_10	0x14	LED10 PWM pulse length configuration value
BUS_PULSE_11	0x16	LED11 PWM pulse length configuration value
BUS_PULSE_12	0x18	LED12 PWM pulse length configuration value
BUS_PULSE_13	0x1A	LED13 PWM pulse length configuration value
BUS_PULSE_14	0x1C	LED14 PWM pulse length configuration value
BUS_PULSE_15	0x1E	LED15 PWM pulse length configuration value
BUS_PULSE_ALL	0x78	all LED channels PWM pulse length configuration command

Table 7.7.2-2: Register **BUS_PULSE_0** (0x00) LED0 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-3: Register **BUS_PULSE_1** (0x02) LED1 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-4: Register **BUS_PULSE_2** (0x04) LED2 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-5: Register **BUS_PULSE_3** (0x06) LED3 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-6: Register **BUS_PULSE_4** (0x08) LED4 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-7: Register **BUS_PULSE_5** (0x0A) LED5 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-8: Register **BUS_PULSE_6** (0x0C) LED6 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-9: Register **BUS_PULSE_7** (0x0E) LED7 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-10: Register **BUS_PULSE_8** (0x10) LED8 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-11: Register **BUS_PULSE_9** (0x12) LED9 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-12: Register **BUS_PULSE_10** (0x14) LED10 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-13: Register **BUS_PULSE_11** (0x16) LED11 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-14: Register **BUS_PULSE_12** (0x18) LED12 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-15: Register **BUS_PULSE_13** (0x1A) LED13 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-16: Register **BUS_PULSE_14** (0x1C) LED14 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-17: Register **BUS_PULSE_15** (0x1E) LED15 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R/W	bus mode PWM channel pulse length [PWM cycles]

Table 7.7.2-18: Register **BUS_PULSE_ALL** (0x78) all LED channels PWM pulse length configuration command

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	W	bus mode PWM channel pulse length for all LED channels [PWM cycles]

7.7.3 Standalone Area

Table 7.7.3-1: STANDALONE

Register Name	*Address*	*Description*
LPFB_PULSE_0	0x000	low priority fallback mode LED0 PWM pulse length configuration value
LPFB_PULSE_1	0x002	low priority fallback mode LED1 PWM pulse length configuration value
LPFB_PULSE_2	0x004	low priority fallback mode LED2 PWM pulse length configuration value
LPFB_PULSE_3	0x006	low priority fallback mode LED3 PWM pulse length configuration value
LPFB_PULSE_4	0x008	low priority fallback mode LED4 PWM pulse length configuration value
LPFB_PULSE_5	0x00A	low priority fallback mode LED5 PWM pulse length configuration value
LPFB_PULSE_6	0x00C	low priority fallback mode LED6 PWM pulse length configuration value
LPFB_PULSE_7	0x00E	low priority fallback mode LED7 PWM pulse length configuration value
LPFB_PULSE_8	0x010	low priority fallback mode LED8 PWM pulse length configuration value
LPFB_PULSE_9	0x012	low priority fallback mode LED9 PWM pulse length configuration value
LPFB_PULSE_10	0x014	low priority fallback mode LED10 PWM pulse length configuration value
LPFB_PULSE_11	0x016	low priority fallback mode LED11 PWM pulse length configuration value
LPFB_PULSE_12	0x018	low priority fallback mode LED12 PWM pulse length configuration value
LPFB_PULSE_13	0x01A	low priority fallback mode LED13 PWM pulse length configuration value
LPFB_PULSE_14	0x01C	low priority fallback mode LED14 PWM pulse length configuration value
LPFB_PULSE_15	0x01E	low priority fallback mode LED15 PWM pulse length configuration value
HPFB_PULSE_0	0x020	high priority fallback mode LED0 PWM pulse length configuration value

Register Name	*Address*	*Description*
HPFB_PULSE_1	0x022	high priority fallback mode LED1 PWM pulse length configuration value
HPFB_PULSE_2	0x024	high priority fallback mode LED2 PWM pulse length configuration value
HPFB_PULSE_3	0x026	high priority fallback mode LED3 PWM pulse length configuration value
HPFB_PULSE_4	0x028	high priority fallback mode LED4 PWM pulse length configuration value
HPFB_PULSE_5	0x02A	high priority fallback mode LED5 PWM pulse length configuration value
HPFB_PULSE_6	0x02C	high priority fallback mode LED6 PWM pulse length configuration value
HPFB_PULSE_7	0x02E	high priority fallback mode LED7 PWM pulse length configuration value
HPFB_PULSE_8	0x030	high priority fallback mode LED8 PWM pulse length configuration value
HPFB_PULSE_9	0x032	high priority fallback mode LED9 PWM pulse length configuration value
HPFB_PULSE_10	0x034	high priority fallback mode LED10 PWM pulse length configuration value
HPFB_PULSE_11	0x036	high priority fallback mode LED11 PWM pulse length configuration value
HPFB_PULSE_12	0x038	high priority fallback mode LED12 PWM pulse length configuration value
HPFB_PULSE_13	0x03A	high priority fallback mode LED13 PWM pulse length configuration value
HPFB_PULSE_14	0x03C	high priority fallback mode LED14 PWM pulse length configuration value
HPFB_PULSE_15	0x03E	high priority fallback mode LED15 PWM pulse length configuration value
PWM_PRESCALER	0x0B8	PWM generator prescaler configuration value
PWM_PERIOD	0x0BA	PWM generator period configuration value
PWM_CONFIG	0x0BC	PWM generator configuration value
PWM_COMBINE_PRI	0x0BE	primary PWM channel combine configuration value
PWM_COMBINE_SEC	0x0C0	secondary PWM channel combine configuration value
BUST_PULSE_0	0x100	bus timeout mode LED0 PWM pulse length configuration value
BUST_PULSE_1	0x102	bus timeout mode LED1 PWM pulse length configuration value
BUST_PULSE_2	0x104	bus timeout mode LED2 PWM pulse length configuration value
BUST_PULSE_3	0x106	bus timeout mode LED3 PWM pulse length configuration value
BUST_PULSE_4	0x108	bus timeout mode LED4 PWM pulse length configuration value
BUST_PULSE_5	0x10A	bus timeout mode LED5 PWM pulse length configuration value
BUST_PULSE_6	0x10C	bus timeout mode LED6 PWM pulse length configuration value
BUST_PULSE_7	0x10E	bus timeout mode LED7 PWM pulse length configuration value
BUST_PULSE_8	0x110	bus timeout mode LED8 PWM pulse length configuration value
BUST_PULSE_9	0x112	bus timeout mode LED9 PWM pulse length configuration value
BUST_PULSE_10	0x114	bus timeout mode LED10 PWM pulse length configuration value
BUST_PULSE_11	0x116	bus timeout mode LED11 PWM pulse length configuration value
BUST_PULSE_12	0x118	bus timeout mode LED12 PWM pulse length configuration value
BUST_PULSE_13	0x11A	bus timeout mode LED13 PWM pulse length configuration value
BUST_PULSE_14	0x11C	bus timeout mode LED14 PWM pulse length configuration value
BUST_PULSE_15	0x11E	bus timeout mode LED15 PWM pulse length configuration value

Table 7.7.3-2: Register **LPFB_PULSE_0** (0x000) low priority fallback mode LED0 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-3: Register **LPFB_PULSE_1** (0x002) low priority fallback mode LED1 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-4: Register **LPFB_PULSE_2** (0x004) low priority fallback mode LED2 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-5: Register **LPFB_PULSE_3** (0x006) low priority fallback mode LED3 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-6: Register **LPFB_PULSE_4** (0x008) low priority fallback mode LED4 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-7: Register **LPFB_PULSE_5** (0x00A) low priority fallback mode LED5 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-8: Register **LPFB_PULSE_6** (0x00C) low priority fallback mode LED6 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-9: Register **LPFB_PULSE_7** (0x00E) low priority fallback mode LED7 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-10: Register **LPFB_PULSE_8** (0x010) low priority fallback mode LED8 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-11: Register **LPFB_PULSE_9** (0x012) low priority fallback mode LED9 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-12: Register **LPFB_PULSE_10** (0x014) low priority fallback mode LED10 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-13: Register **LPFB_PULSE_11** (0x016) low priority fallback mode LED11 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-14: Register **LPFB_PULSE_12** (0x018) low priority fallback mode LED12 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-15: Register **LPFB_PULSE_13** (0x01A) low priority fallback mode LED13 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-16: Register **LPFB_PULSE_14** (0x01C) low priority fallback mode LED14 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-17: Register **LPFB_PULSE_15** (0x01E) low priority fallback mode LED15 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	low priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-18: Register **HPFB_PULSE_0** (0x020) high priority fallback mode LED0 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-19: Register **HPFB_PULSE_1** (0x022) high priority fallback mode LED1 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-20: Register **HPFB_PULSE_2** (0x024) high priority fallback mode LED2 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-21: Register **HPFB_PULSE_3** (0x026) high priority fallback mode LED3 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-22: Register **HPFB_PULSE_4** (0x028) high priority fallback mode LED4 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-23: Register **HPFB_PULSE_5** (0x02A) high priority fallback mode LED5 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-24: Register **HPFB_PULSE_6** (0x02C) high priority fallback mode LED6 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-25: Register **HPFB_PULSE_7** (0x02E) high priority fallback mode LED7 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-26: Register **HPFB_PULSE_8** (0x030) high priority fallback mode LED8 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-27: Register **HPFB_PULSE_9** (0x032) high priority fallback mode LED9 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-28: Register **HPFB_PULSE_10** (0x034) high priority fallback mode LED10 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-29: Register **HPFB_PULSE_11** (0x036) high priority fallback mode LED11 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-30: Register **HPFB_PULSE_12** (0x038) high priority fallback mode LED12 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-31: Register **HPFB_PULSE_13** (0x03A) high priority fallback mode LED13 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-32: Register **HPFB_PULSE_14** (0x03C) high priority fallback mode LED14 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-33: Register **HPFB_PULSE_15** (0x03E) high priority fallback mode LED15 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	high priority fallback mode PWM channel pulse length [PWM cycles]

Table 7.7.3-34: Register **PWM_PRESCALER** (0x0B8) PWM generator prescaler configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:7	-	0	R	
6:0	div	0	R	PWM period prescaler This value is used by the PWM prescale counter to create the PWM period counter increment clock. PWM period frequency = system clock frequency / (PWM_PERIOD.length * (div + 1)) Example: 8MHz / (1023 * (25+1)) = 300.8Hz Note: If this value is not configured, a default value of 25 will be used.

Table 7.7.3-35: Register **PWM_PERIOD** (0x0BA) PWM generator period configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	PWM period length [PWM cycles] Note: If a value smaller than 1023 is configured, the PWM resolution will be less than 10 bit ! Note: If this value is not configured, a default value of 1023 will be used.

Table 7.7.3-36: Register **PWM_CONFIG** (0x0BC) PWM generator configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:3	-	0	R	
2	oe_mask_bust	0	R	configuration, which selects, if OE signal masks bus timeout mode LED channels PWM 0 : OE has no influence in bus timeout mode LED channels 1 : OE masks LED channels, which are in bus timeout mode
1	-	0	R	
0	timing	0	R	PWM pulse start timing configuration 0 : no PWM inter channel start delay i.e. all channel pulses start at the same time at PWM period start 1 : equidistant distribution of PWM channel starting point over PWM period

Table 7.7.3-37: Register **PWM_COMBINE_PRI** (0x0BE) primary PWM channel combine configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	primary PWM channel combination selection bit 0 : combines channels 0 and 1 bit 1 : combines channels 2 and 3 ... bit 6 : combines channels 12 and 13 bit 7 : combines channels 14 and 15 0 : the two corresponding channels are independent (PWM_CONFIG defines inter-channel delay) 1 : the two corresponding channels are combined (start delay between these channels is forced to 0)

Table 7.7.3-38: Register **PWM_COMBINE_SEC** (0x0C0) secondary PWM channel combine configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:7	-	0	R	
6:0	enable	0	R	secondary PWM channel combination selection bit 0 : combines channels 1 and 2 bit 1 : combines channels 3 and 4 ... bit 6 : combines channels 13 and 14 0 : the two corresponding channels are independent (PWM_CONFIG defines inter-channel delay) 1 : the two corresponding channels are combined (start delay between these channels is forced to 0)

Table 7.7.3-39: Register **BUST_PULSE_0** (0x100) bus timeout mode LED0 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-40: Register **BUST_PULSE_1** (0x102) bus timeout mode LED1 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-41: Register **BUST_PULSE_2** (0x104) bus timeout mode LED2 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-42: Register **BUST_PULSE_3** (0x106) bus timeout mode LED3 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-43: Register **BUST_PULSE_4** (0x108) bus timeout mode LED4 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-44: Register **BUST_PULSE_5** (0x10A) bus timeout mode LED5 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-45: Register **BUST_PULSE_6** (0x10C) bus timeout mode LED6 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-46: Register **BUST_PULSE_7** (0x10E) bus timeout mode LED7 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-47: Register **BUST_PULSE_8** (0x110) bus timeout mode LED8 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-48: Register **BUST_PULSE_9** (0x112) bus timeout mode LED9 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-49: Register **BUST_PULSE_10** (0x114) bus timeout mode LED10 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-50: Register **BUST_PULSE_11** (0x116) bus timeout mode LED11 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-51: Register **BUST_PULSE_12** (0x118) bus timeout mode LED12 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-52: Register **BUST_PULSE_13** (0x11A) bus timeout mode LED13 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-53: Register **BUST_PULSE_14** (0x11C) bus timeout mode LED14 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

Table 7.7.3-54: Register **BUST_PULSE_15** (0x11E) bus timeout mode LED15 PWM pulse length configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	length	0	R	bus timeout mode PWM channel pulse length [PWM cycles]

7.8 LED Current Sinks

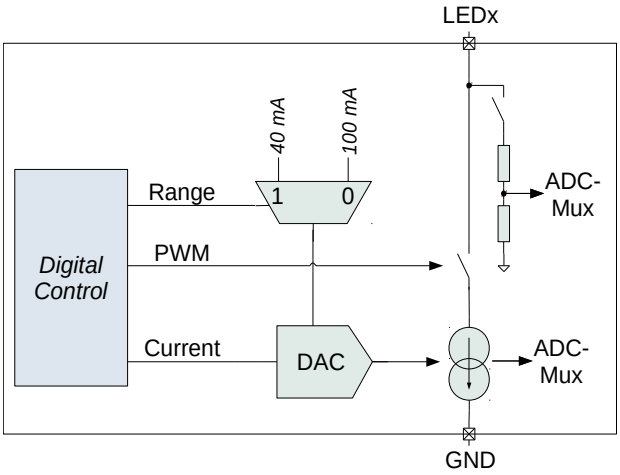

Figure 7.8-1: ISINK Block Diagram

Each current sink is based on a DAC with selectable full scale range. The range can be selected per LED using the IDAC_REF_SEL_x values.
The current sink gets current strength information and the PWM duty cycle from the digital part.
The output switch offers various slew rate settings, configurable using the ISINK_CONFIG.slew value, to improve EMC performance.
An internal ADC can be connected to monitor pad-voltage and actual current value for diagnosis purpose.
Unused LED driver stages can be left OFF inside the LED_ENABLE_x values to save power.
When a PWMIN pin direct PWM is fed to an LED driver, the LED current configuration values used in this mode can be selected with the ISINK_CONFIG value bit fields.

The following figures show the relation between the current configuration value (digital set value) and the resulting LED current. The LED current can saturate above the selected range maximum current value. Below the selected range minimum current value the LED current behavior can be non-linear including a possible saturation of the driven LED current. For this reason it's not recommended to select an LED current outside the selected range.

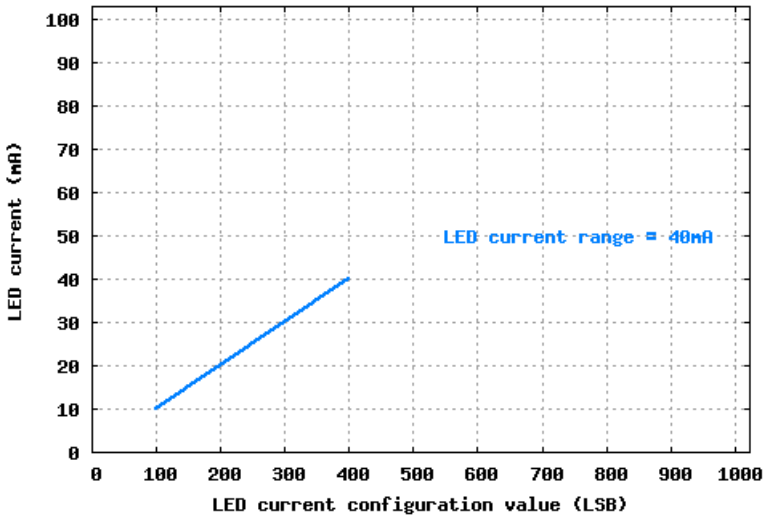

Figure 7.8-2: LED Current Sink 40mA Range Behavior

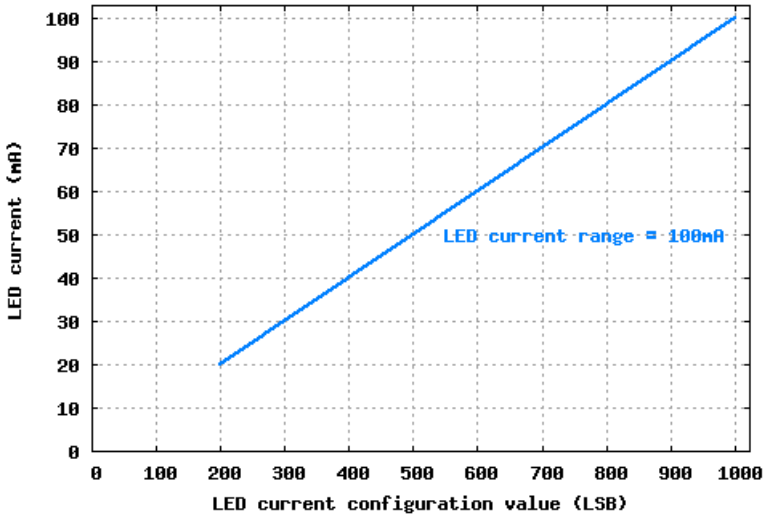

Figure 7.8-3: LED Current Sink 100mA Range Behavior

7.8.1 Advanced Power Management

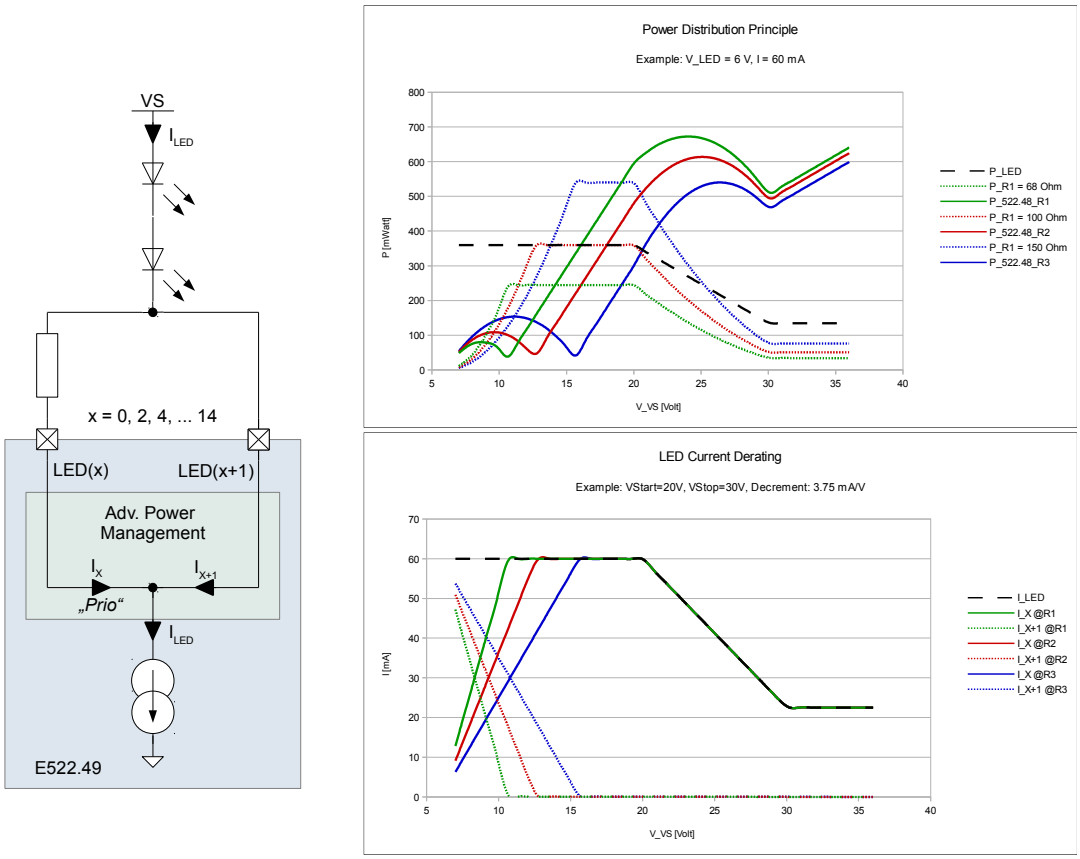

Figure 7.8.1-1: Advanced Power Management

Eight pairs of LED pins offer the option to be configured in channel bundling mode (LED0 & LED1, LED2 & LED3, ... LED14 & LED15). This bundling option is intended for advanced thermal management (please see figure 7.8.1-1), shifting power dissipation to an external power sink resistor, which reduces the driver power consumption.
The channel current is regulated as a sum of currents in LED(x) and LED(x+1). The priority output LED(x) drives the current as long as the voltage headroom allows to. The bypass output LED(x+1) is used to deliver the remaining current flow. In any case the bypass output LED(x+1) drives at least 5% of the sum of currents preventing the LED(x+1) from regulation performance lost. This implies, that the priority output LED(x) will drive at maximum 95% of the sum of currents.

The analog current sink channel bundling with prioritized current sum regulation can be enabled per LED driver pair using the STANDALONE ISINK_BUNDLE configuration value. In case, an LED driver pair is configured to be bundled like described before, the PWM channel combine has to be set up according to this to obtain phase-aligned PWM pulses with equal pulse lengths for bundled LED channels.
For LED channels in analog bundling mode, the LED current, DAC range and PWM pulse length configuration will only be taken from the lower channel configuration and will also be applied to the upper channel to provide a consistent behavior of analog bundled LED channel pairs. The upper channel LED current, DAC range and PWM pulse length configuration is ignored in this special case.

The described distribution of current allows to share some of the linear regulator power with the external power-shunt. Figure 7.8.1-1 shows the basic power dissipation per channel as a function of the LED supply voltage at:

- the driven LEDs (I_{LED} = 60mA in this example)
- the external power shunt, given for exemplary values R1 = 68Ω, R2 = 100Ω, R3 = 150Ω
- and the remaining on-chip power dissipation of the bundled driver channels.

For further power-budget optimization, the chip offers the option to enable supply-voltage based derating of the LED currents, as well as core-temperature based derating. LED current derating is described in to following sub-chapter.

- Supply voltage based derating is displayed, starting at 20V, and decreasing the output current with 3.75mA/V up to 30V.
- Depending on ambient temperature and power dissipation in other channels, temperature derating can decrease the current further. This is not displayed in this figure above.

7.8.2 LED Current Derating

To protect the device from thermal damage, an automatic LED current derating is implemented. Two independent types of device internal (LED supply and device temperature) measurement based derating functions can be configured to derate the LED current between a start and stop value as shown in the following figures. The derating is implemented as a nominal LED current dependent percental function, which means that larger currents are more derated than smaller currents from an absolute point of view. The LED supply and VT (device temperature) derating configuration values found below can be used to configure the desired range and gain values. The LED supply measurement is done using the direct amplification AMEAS_VS and AMEAS_PWMIN paths and the derating start and stop values have to be set according to this amplification factor.
The external micro controller also has the possibility to derate the LED current using the BUS_DERATE_GAIN value. The overall LED current derating factor is defined as the product of the 3 derating factors mentioned above.

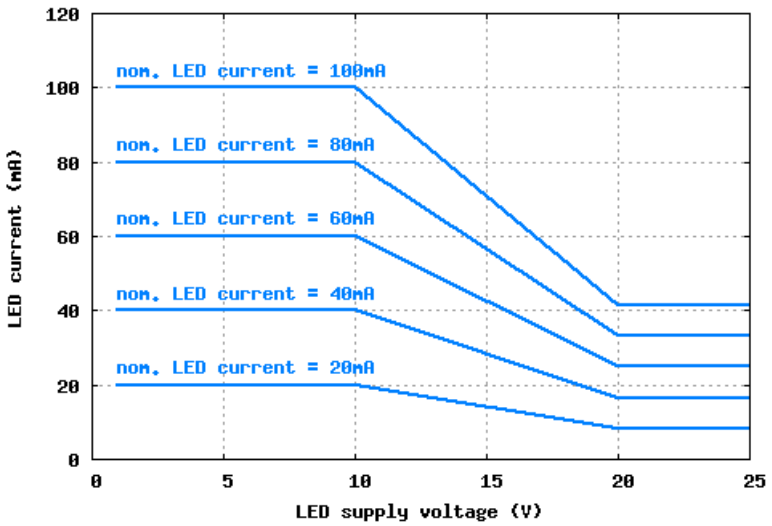

Figure 7.8.2-1: LED Supply Voltage Based Derating Example

The figure above shows the LED supply voltage dependent LED current derating with the following example configuration values:

- derating start LED supply value = 10V
- derating stop LED supply value = 20V
- derating gain select value = 15

This results in a percental LED derating by:

- 10V * 15 * 0.25%/V = 37.5%

Considering a nominal LED current of 100mA, the stop LED current will be at:

- 100mA * 62.5% = 62.5mA

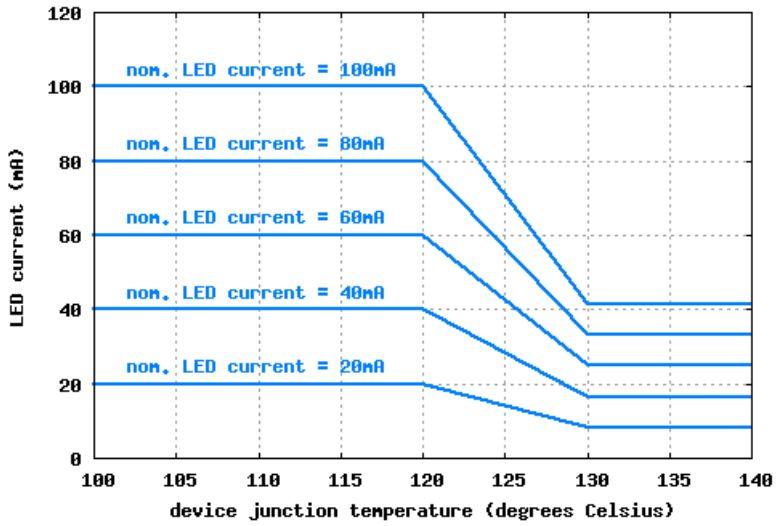

Figure 7.8.2-2: Device Junction Temperature Based Derating Example

The figure above shows the device junction temperature dependent LED current derating with the following example configuration values:

- derating start VT value = 120°C
- derating stop VT value = 130°C
- derating gain select value = 15

This results in a percental LED derating by:

- 10K * 15 * 0.39%/K = 58.5%

Considering a nominal LED current of 100mA, the stop LED current will be at:

- 100mA * 41.5% = 41.5mA

7.8.3 LED Binning

To support different LED bin classes per device, a general LED bin factor can be configured per LED using the BIN_GAIN_X values.

Separate to this fixed bin configuration, the voltage drop over an external resistor connected to an LED pin can be evaluated for LED binning. The pin used for this evaluation can be selected using the BIN_CLASS_CONFIG.pin_sel value. A 100 percent PWM duty cycle and a sink current configuration value regarding BIN_CLASS_CONFIG.current_sel is used to drive this pin if bin class evaluation is enabled using BIN_CLASS_CONFIG.enable bit.
A table of 4 bin class levels (BIN_CLASS_LEVEL_x values) can be used to distinct between 5 bin classes with separate bin gain values (BIN_CLASS_GAIN_x values). The ADC measurement value of the pin to be evaluated is compared to the specified levels, the resistor value related bin class gain is determined and applied to the LEDs selected using the BIN_CLASS_ENABLE_x values.
When the BIN_CLASS_ENABLE_x bit of an LED channel is configured as 1, the related general LED bin factor is not used and only the evaluated bin class gain is applied.

The following figure shows an example bin class table with resistor values selected from the E12 series.
In this example the external resistor is supplied with a current of 20mA.
The external resistor is evaluated once every LED PWM period and 5 adjacent sample values are filtered using a median filter algorithm (the last 5 values including the current value are sorted and the middle value is taken) before bin class gain selection.

The bin adoption is implemented as a LED current factor to reduce or raise the LED current depending on the LED bin class to achieve a uniform LED luminance of LEDs connected to a single driver device and between LEDs connected to different LED driver devices.

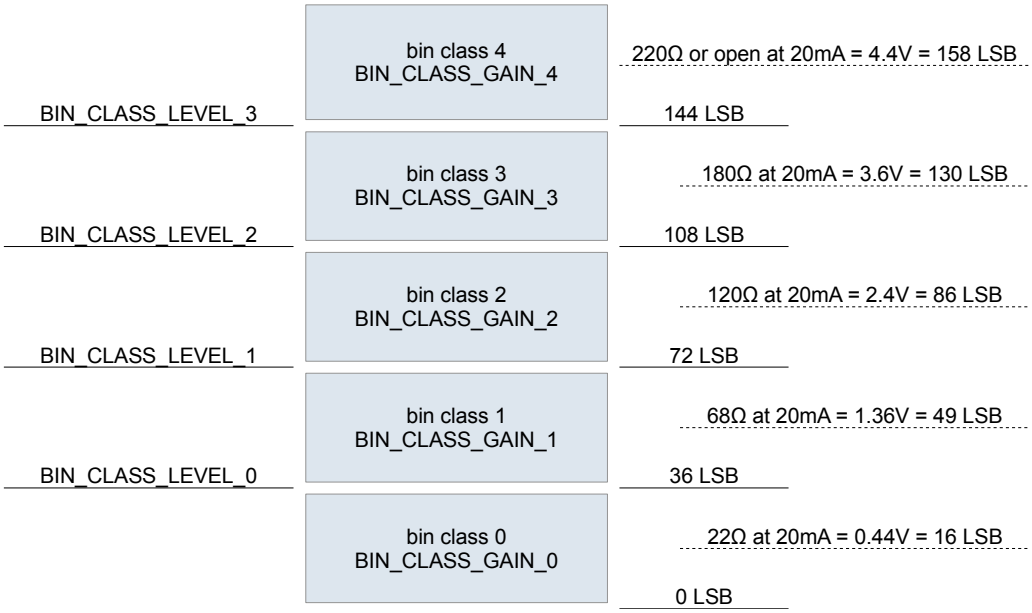

Figure 7.8.3-1: Example Bin Class Table

The following figure shows an LED binning example of the following parameter set:

- BIN_CLASS_LEVEL_0 = 1V
- BIN_CLASS_LEVEL_1 = 2V
- BIN_CLASS_LEVEL_2 = 3V
- BIN_CLASS_LEVEL_3 = 4V
- BIN_CLASS_GAIN_0 = -25%
- BIN_CLASS_GAIN_1 = -12.5%
- BIN_CLASS_GAIN_2 = +0%
- BIN_CLASS_GAIN_3 = +12.5%
- BIN_CLASS_GAIN_4 = +25%

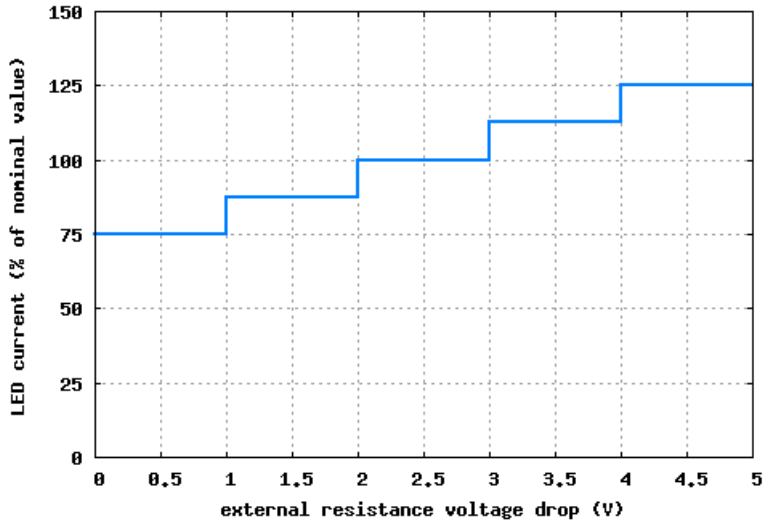

Figure 7.8.3-2: LED Binning Example

7.8.4 Bus Configuration Area

Table 7.8.4-1: BUS_CONFIG

Register Name	*Address*	*Description*
BUS_CURRENT_0	0x20	bus mode LED0 sink current configuration value
BUS_CURRENT_1	0x22	bus mode LED1 sink current configuration value
BUS_CURRENT_2	0x24	bus mode LED2 sink current configuration value
BUS_CURRENT_3	0x26	bus mode LED3 sink current configuration value
BUS_CURRENT_4	0x28	bus mode LED4 sink current configuration value
BUS_CURRENT_5	0x2A	bus mode LED5 sink current configuration value
BUS_CURRENT_6	0x2C	bus mode LED6 sink current configuration value
BUS_CURRENT_7	0x2E	bus mode LED7 sink current configuration value
BUS_CURRENT_8	0x30	bus mode LED8 sink current configuration value
BUS_CURRENT_9	0x32	bus mode LED9 sink current configuration value
BUS_CURRENT_10	0x34	bus mode LED10 sink current configuration value
BUS_CURRENT_11	0x36	bus mode LED11 sink current configuration value

Register Name	*Address*	*Description*
BUS_CURRENT_12	0x38	bus mode LED12 sink current configuration value
BUS_CURRENT_13	0x3A	bus mode LED13 sink current configuration value
BUS_CURRENT_14	0x3C	bus mode LED14 sink current configuration value
BUS_CURRENT_15	0x3E	bus mode LED15 sink current configuration value
LED_ENABLE_0_7	0x44	LED driver channels 0 to 7 enable value
LED_ENABLE_8_15	0x46	LED driver channels 8 to 15 enable value
BUS_DERATE_GAIN	0x70	bus based derating value
BUS_CURRENT_ALL	0x7A	all LED channels current configuration command

Table 7.8.4-2: Register **BUS_CURRENT_0** (0x20) bus mode LED0 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-3: Register **BUS_CURRENT_1** (0x22) bus mode LED1 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-4: Register **BUS_CURRENT_2** (0x24) bus mode LED2 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-5: Register **BUS_CURRENT_3** (0x26) bus mode LED3 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-6: Register **BUS_CURRENT_4** (0x28) bus mode LED4 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-7: Register **BUS_CURRENT_5** (0x2A) bus mode LED5 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-8: Register **BUS_CURRENT_6** (0x2C) bus mode LED6 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-9: Register **BUS_CURRENT_7** (0x2E) bus mode LED7 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-10: Register **BUS_CURRENT_8** (0x30) bus mode LED8 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-11: Register **BUS_CURRENT_9** (0x32) bus mode LED9 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-12: Register **BUS_CURRENT_10** (0x34) bus mode LED10 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-13: Register **BUS_CURRENT_11** (0x36) bus mode LED11 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-14: Register **BUS_CURRENT_12** (0x38) bus mode LED12 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-15: Register **BUS_CURRENT_13** (0x3A) bus mode LED13 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-16: Register **BUS_CURRENT_14** (0x3C) bus mode LED14 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-17: Register **BUS_CURRENT_15** (0x3E) bus mode LED15 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R/W	bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.4-18: Register **LED_ENABLE_0_7** (0x44) LED driver channels 0 to 7 enable value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R/W	enable for driver channels 0 to 7 bit 0: enable for driver channel 0 ... bit 7: enable for driver channel 7 an enable bit value of 0 disables channel driver analog part an enable bit value of 1 enables channel driver analog part Note: Used to save current when channel drivers are OFF.

Table 7.8.4-19: Register **LED_ENABLE_8_15** (0x46) LED driver channels 8 to 15 enable value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R/W	enable for driver channels 8 to 15 bit 0: enable for driver channel 8 ... bit 7: enable for driver channel 15 an enable bit value of 0 disables channel driver analog part an enable bit value of 1 enables channel driver analog part Note: Used to save current when channel drivers are OFF.

Table 7.8.4-20: Register **BUS_DERATE_GAIN** (0x70) bus based derating value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	gain	0	R/W	defines reduction of nominal LED current by a value settable via bus communication (derating by master controller) derating multiplier: M_{BUS_derate} = 1 - (gain / 256)

Table 7.8.4-21: Register **BUS_CURRENT_ALL** (0x7A) all LED channels current configuration command

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	W	bus mode driver channel current selection for all LED channels driver current [100uA] The driver current will be limited to the channel related IDAC selected range maximum current.

7.8.5 Standalone Area

Table 7.8.5-1: STANDALONE

Register Name	*Address*	*Description*
LPFB_CURRENT_0	0x040	low priority fallback mode LED0 sink current configuration value
LPFB_CURRENT_1	0x042	low priority fallback mode LED1 sink current configuration value
LPFB_CURRENT_2	0x044	low priority fallback mode LED2 sink current configuration value
LPFB_CURRENT_3	0x046	low priority fallback mode LED3 sink current configuration value
LPFB_CURRENT_4	0x048	low priority fallback mode LED4 sink current configuration value
LPFB_CURRENT_5	0x04A	low priority fallback mode LED5 sink current configuration value
LPFB_CURRENT_6	0x04C	low priority fallback mode LED60 sink current configuration value
LPFB_CURRENT_7	0x04E	low priority fallback mode LED7 sink current configuration value
LPFB_CURRENT_8	0x050	low priority fallback mode LED8 sink current configuration value
LPFB_CURRENT_9	0x052	low priority fallback mode LED9 sink current configuration value
LPFB_CURRENT_10	0x054	low priority fallback mode LED10 sink current configuration value
LPFB_CURRENT_11	0x056	low priority fallback mode LED11 sink current configuration value
LPFB_CURRENT_12	0x058	low priority fallback mode LED12 sink current configuration value
LPFB_CURRENT_13	0x05A	low priority fallback mode LED13 sink current configuration value
LPFB_CURRENT_14	0x05C	low priority fallback mode LED14 sink current configuration value
LPFB_CURRENT_15	0x05E	low priority fallback mode LED15 sink current configuration value
HPFB_CURRENT_0	0x060	high priority fallback mode LED0 sink current configuration value
HPFB_CURRENT_1	0x062	high priority fallback mode LED1 sink current configuration value
HPFB_CURRENT_2	0x064	high priority fallback mode LED2 sink current configuration value
HPFB_CURRENT_3	0x066	high priority fallback mode LED3 sink current configuration value
HPFB_CURRENT_4	0x068	high priority fallback mode LED4 sink current configuration value
HPFB_CURRENT_5	0x06A	high priority fallback mode LED5 sink current configuration value

Register Name	*Address*	*Description*
HPFB_CURRENT_6	0x06C	high priority fallback mode LED6 sink current configuration value
HPFB_CURRENT_7	0x06E	high priority fallback mode LED7 sink current configuration value
HPFB_CURRENT_8	0x070	high priority fallback mode LED8 sink current configuration value
HPFB_CURRENT_9	0x072	high priority fallback mode LED9 sink current configuration value
HPFB_CURRENT_10	0x074	high priority fallback mode LED10 sink current configuration value
HPFB_CURRENT_11	0x076	high priority fallback mode LED11 sink current configuration value
HPFB_CURRENT_12	0x078	high priority fallback mode LED12 sink current configuration value
HPFB_CURRENT_13	0x07A	high priority fallback mode LED13 sink current configuration value
HPFB_CURRENT_14	0x07C	high priority fallback mode LED14 sink current configuration value
HPFB_CURRENT_15	0x07E	high priority fallback mode LED15 sink current configuration value
BIN_GAIN_0	0x080	LED0 bin class adoption gain configuration value
BIN_GAIN_1	0x082	LED1 bin class adoption gain configuration value
BIN_GAIN_2	0x084	LED2 bin class adoption gain configuration value
BIN_GAIN_3	0x086	LED3 bin class adoption gain configuration value
BIN_GAIN_4	0x088	LED4 bin class adoption gain configuration value
BIN_GAIN_5	0x08A	LED5 bin class adoption gain configuration value
BIN_GAIN_6	0x08C	LED6 bin class adoption gain configuration value
BIN_GAIN_7	0x08E	LED7 bin class adoption gain configuration value
BIN_GAIN_8	0x090	LED8 bin class adoption gain configuration value
BIN_GAIN_9	0x092	LED9 bin class adoption gain configuration value
BIN_GAIN_10	0x094	LED10 bin class adoption gain configuration value
BIN_GAIN_11	0x096	LED11 bin class adoption gain configuration value
BIN_GAIN_12	0x098	LED12 bin class adoption gain configuration value
BIN_GAIN_13	0x09A	LED13 bin class adoption gain configuration value
BIN_GAIN_14	0x09C	LED14 bin class adoption gain configuration value
BIN_GAIN_15	0x09E	LED15 bin class adoption gain configuration value
BIN_CLASS_CONFIG	0x0A0	evaluated LED bin class configuration value
BIN_CLASS_ENABLE_0_7	0x0A2	evaluated LED bin class assignment configuration value
BIN_CLASS_ENABLE_8_15	0x0A4	evaluated LED bin class assignment configuration value
BIN_CLASS_LEVEL_0	0x0A6	LED bin class evaluation level value
BIN_CLASS_LEVEL_1	0x0A8	LED bin class evaluation level value
BIN_CLASS_LEVEL_2	0x0AA	LED bin class evaluation level value
BIN_CLASS_LEVEL_3	0x0AC	LED bin class evaluation level value
BIN_CLASS_GAIN_0	0x0AE	evaluated LED bin class 0 gain value
BIN_CLASS_GAIN_1	0x0B0	evaluated LED bin class 1 gain value
BIN_CLASS_GAIN_2	0x0B2	evaluated LED bin class 2 gain value
BIN_CLASS_GAIN_3	0x0B4	evaluated LED bin class 3 gain value
BIN_CLASS_GAIN_4	0x0B6	evaluated LED bin class 4 gain value
BUST_CURRENT_0	0x120	bus timeout mode LED0 sink current configuration value
BUST_CURRENT_1	0x122	bus timeout mode LED1 sink current configuration value
BUST_CURRENT_2	0x124	bus timeout mode LED2 sink current configuration value

Register Name	*Address*	*Description*
BUST_CURRENT_3	0x126	bus timeout mode LED3 sink current configuration value
BUST_CURRENT_4	0x128	bus timeout mode LED4 sink current configuration value
BUST_CURRENT_5	0x12A	bus timeout mode LED5 sink current configuration value
BUST_CURRENT_6	0x12C	bus timeout mode LED6 sink current configuration value
BUST_CURRENT_7	0x12E	bus timeout mode LED7 sink current configuration value
BUST_CURRENT_8	0x130	bus timeout mode LED8 sink current configuration value
BUST_CURRENT_9	0x132	bus timeout mode LED9 sink current configuration value
BUST_CURRENT_10	0x134	bus timeout mode LED10 sink current configuration value
BUST_CURRENT_11	0x136	bus timeout mode LED11 sink current configuration value
BUST_CURRENT_12	0x138	bus timeout mode LED12 sink current configuration value
BUST_CURRENT_13	0x13A	bus timeout mode LED13 sink current configuration value
BUST_CURRENT_14	0x13C	bus timeout mode LED14 sink current configuration value
BUST_CURRENT_15	0x13E	bus timeout mode LED15 sink current configuration value
IDAC_REF_SEL_0_7	0x140	LED channels 0 to 7 IDAC reference selection value
IDAC_REF_SEL_8_15	0x142	LED channels 8 to 15 IDAC reference selection value
ISINK_CONFIG	0x144	LED current sinks configuration value
VS_DERATE_RANGE	0x146	LED supply based derating range configuration value
VT_DERATE_START	0x148	device temperature based derating start configuration value
VT_DERATE_STOP	0x14A	device temperature based derating stop configuration value
DERATE_GAIN	0x14C	derating gain configuration value
ISINK_BUNDLE	0x15C	analog current sink bundling configuration value

Table 7.8.5-2: Register **LPFB_CURRENT_0** (0x040) low priority fallback mode LED0 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-3: Register **LPFB_CURRENT_1** (0x042) low priority fallback mode LED1 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-4: Register **LPFB_CURRENT_2** (0x044) low priority fallback mode LED2 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-5: Register **LPFB_CURRENT_3** (0x046) low priority fallback mode LED3 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-6: Register **LPFB_CURRENT_4** (0x048) low priority fallback mode LED4 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-7: Register **LPFB_CURRENT_5** (0x04A) low priority fallback mode LED5 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-8: Register **LPFB_CURRENT_6** (0x04C) low priority fallback mode LED60 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-9: Register **LPFB_CURRENT_7** (0x04E) low priority fallback mode LED7 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-10: Register **LPFB_CURRENT_8** (0x050) low priority fallback mode LED8 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-11: Register **LPFB_CURRENT_9** (0x052) low priority fallback mode LED9 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-12: Register **LPFB_CURRENT_10** (0x054) low priority fallback mode LED10 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-13: Register **LPFB_CURRENT_11** (0x056) low priority fallback mode LED11 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-14: Register **LPFB_CURRENT_12** (0x058) low priority fallback mode LED12 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-15: Register **LPFB_CURRENT_13** (0x05A) low priority fallback mode LED13 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-16: Register **LPFB_CURRENT_14** (0x05C) low priority fallback mode LED14 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-17: Register **LPFB_CURRENT_15** (0x05E) low priority fallback mode LED15 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	low priority fallback mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-18: Register **HPFB_CURRENT_0** (0x060) high priority fallback mode LED0 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-19: Register **HPFB_CURRENT_1** (0x062) high priority fallback mode LED1 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-20: Register **HPFB_CURRENT_2** (0x064) high priority fallback mode LED2 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-21: Register **HPFB_CURRENT_3** (0x066) high priority fallback mode LED3 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-22: Register **HPFB_CURRENT_4** (0x068) high priority fallback mode LED4 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-23: Register **HPFB_CURRENT_5** (0x06A) high priority fallback mode LED5 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-24: Register **HPFB_CURRENT_6** (0x06C) high priority fallback mode LED6 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-25: Register **HPFB_CURRENT_7** (0x06E) high priority fallback mode LED7 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-26: Register **HPFB_CURRENT_8** (0x070) high priority fallback mode LED8 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-27: Register **HPFB_CURRENT_9** (0x072) high priority fallback mode LED9 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-28: Register **HPFB_CURRENT_10** (0x074) high priority fallback mode LED10 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-29: Register **HPFB_CURRENT_11** (0x076) high priority fallback mode LED11 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-30: Register **HPFB_CURRENT_12** (0x078) high priority fallback mode LED12 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-31: Register **HPFB_CURRENT_13** (0x07A) high priority fallback mode LED13 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-32: Register **HPFB_CURRENT_14** (0x07C) high priority fallback mode LED14 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-33: Register **HPFB_CURRENT_15** (0x07E) high priority fallback mode LED15 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	high priority mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-34: Register **BIN_GAIN_0** (0x080) LED0 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-35: Register **BIN_GAIN_1** (0x082) LED1 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-36: Register **BIN_GAIN_2** (0x084) LED2 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-37: Register **BIN_GAIN_3** (0x086) LED3 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-38: Register **BIN_GAIN_4** (0x088) LED4 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-39: Register **BIN_GAIN_5** (0x08A) LED5 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-40: Register **BIN_GAIN_6** (0x08C) LED6 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-41: Register **BIN_GAIN_7** (0x08E) LED7 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-42: Register **BIN_GAIN_8** (0x090) LED8 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-43: Register **BIN_GAIN_9** (0x092) LED9 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-44: Register **BIN_GAIN_10** (0x094) LED10 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-45: Register **BIN_GAIN_11** (0x096) LED11 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-46: Register **BIN_GAIN_12** (0x098) LED12 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-47: Register **BIN_GAIN_13** (0x09A) LED13 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-48: Register **BIN_GAIN_14** (0x09C) LED14 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-49: Register **BIN_GAIN_15** (0x09E) LED15 bin class adoption gain configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	LED channel binning gain gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 7.8.5-50: Register **BIN_CLASS_CONFIG** (0x0A0) evaluated LED bin class configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:5	current_sel	0	R	LED pin bin class evaluation current current [mA] = current_sel * 3.2mA
4	enable	0	R	enable LED pin bin class evaluation
3:0	pin_sel	0	R	selects LED pin used to determine bin class 0 : selects pin LED0 1 : selects pin LED1 ... 15 : selects pin LED15

Table 7.8.5-51: Register **BIN_CLASS_ENABLE_0_7** (0x0A2) evaluated LED bin class assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	selects which LED pins (0 to 7) are supplied with determined bin class gain

Table 7.8.5-52: Register **BIN_CLASS_ENABLE_8_15** (0x0A4) evaluated LED bin class assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	selects which LED pins (8 to 15) are supplied with determined bin class gain

Table 7.8.5-53: Register **BIN_CLASS_LEVEL_0** (0x0A6) LED bin class evaluation level value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	bin class compare level definition

Table 7.8.5-54: Register **BIN_CLASS_LEVEL_1** (0x0A8) LED bin class evaluation level value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	bin class compare level definition

Table 7.8.5-55: Register **BIN_CLASS_LEVEL_2** (0x0AA) LED bin class evaluation level value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	bin class compare level definition

Table 7.8.5-56: Register **BIN_CLASS_LEVEL_3** (0x0AC) LED bin class evaluation level value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	bin class compare level definition

Table 7.8.5-57: Register **BIN_CLASS_GAIN_0** (0x0AE) evaluated LED bin class 0 gain value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	bin class gain value definition gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation.

Table 7.8.5-58: Register **BIN_CLASS_GAIN_1** (0x0B0) evaluated LED bin class 1 gain value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	bin class gain value definition gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation.

Table 7.8.5-59: Register **BIN_CLASS_GAIN_2** (0x0B2) evaluated LED bin class 2 gain value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	bin class gain value definition gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation.

Table 7.8.5-60: Register **BIN_CLASS_GAIN_3** (0x0B4) evaluated LED bin class 3 gain value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	bin class gain value definition gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation.

Table 7.8.5-61: Register **BIN_CLASS_GAIN_4** (0x0B6) evaluated LED bin class 4 gain value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	gain	0	R	bin class gain value definition gain 0,50 = 0x100 gain 1,00 = 0x200 gain 1,99 = 0x3FF Note: Gain will be applied with saturation.

Table 7.8.5-62: Register **BUST_CURRENT_0** (0x120) bus timeout mode LED0 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-63: Register **BUST_CURRENT_1** (0x122) bus timeout mode LED1 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-64: Register **BUST_CURRENT_2** (0x124) bus timeout mode LED2 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-65: Register **BUST_CURRENT_3** (0x126) bus timeout mode LED3 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-66: Register **BUST_CURRENT_4** (0x128) bus timeout mode LED4 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-67: Register **BUST_CURRENT_5** (0x12A) bus timeout mode LED5 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-68: Register **BUST_CURRENT_6** (0x12C) bus timeout mode LED6 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-69: Register **BUST_CURRENT_7** (0x12E) bus timeout mode LED7 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-70: Register **BUST_CURRENT_8** (0x130) bus timeout mode LED8 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-71: Register **BUST_CURRENT_9** (0x132) bus timeout mode LED9 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-72: Register **BUST_CURRENT_10** (0x134) bus timeout mode LED10 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-73: Register **BUST_CURRENT_11** (0x136) bus timeout mode LED11 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-74: Register **BUST_CURRENT_12** (0x138) bus timeout mode LED12 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-75: Register **BUST_CURRENT_13** (0x13A) bus timeout mode LED13 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-76: Register **BUST_CURRENT_14** (0x13C) bus timeout mode LED14 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-77: Register **BUST_CURRENT_15** (0x13E) bus timeout mode LED15 sink current configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	bus timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 7.8.5-78: Register **IDAC_REF_SEL_0_7** (0x140) LED channels 0 to 7 IDAC reference selection value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	sel	0	R	IDAC reference (range) selection for driver channels 0 to 7 bit 0: select IDAC reference for driver channel 0 ... bit 7: select IDAC reference for driver channel 7 a sel bit value of 0 selects IDAC upper range a sel bit value of 1 selects IDAC lower range

Table 7.8.5-79: Register **IDAC_REF_SEL_8_15** (0x142) LED channels 8 to 15 IDAC reference selection value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	sel	0	R	IDAC reference (range) selection for driver channels 8 to 15 bit 0: select IDAC reference for driver channel 8 ... bit 7: select IDAC reference for driver channel 15 a sel bit value of 0 selects IDAC upper range a sel bit value of 1 selects IDAC lower range

Table 7.8.5-80: Register **ISINK_CONFIG** (0x144) LED current sinks configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	derate_sup	0	R	LED supply (25 LSB/V channel) used for derating functionality selection 0, 1 : VS 2 : PWMIN_LP 3 : PWMIN_HP
7:6	lpfb_hpfb	0	R	selects the PWM pulse and ISINK current data set used when both PWMIN_LP and PWMIN_HP signal fallback default : HPFB data set 0 : high priority fallback (HPFB) data set 1 : low priority fallback (LPFB) data set 2 : bus configuration data set 3 : bus timeout configuration data set
5:4	hp_direct	0	R	selects the LED current data set to use in high priority direct PWM mode default: HPFB LED current configuration 0 : high priority fallback (HPFB) data set 1 : low priority fallback (LPFB) data set 2 : bus configuration data set 3 : bus timeout configuration data set
3:2	lp_direct	0	R	selects the LED current data set to use in low priority direct PWM mode default: LPFB LED current configuration 0 : low priority fallback (LPFB) data set 1 : high priority fallback (HPFB) data set 2 : bus configuration data set 3 : bus timeout configuration data set
1:0	slew	0	R	driver slew rate configuration 0 : please see $t_{SINK\_RISE\_0}$ and $t_{SINK\_FALL\_0}$ parameters 1 : please see $t_{SINK\_RISE\_1}$ and $t_{SINK\_FALL\_1}$ parameters 2 : please see $t_{SINK\_RISE\_2}$ and $t_{SINK\_FALL\_2}$ parameters 3 : please see $t_{SINK\_RISE\_3}$ and $t_{SINK\_FALL\_3}$ parameters

Table 7.8.5-81: Register **VS_DERATE_RANGE** (0x146) LED supply based derating range configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:5	stop	0	R	LED supply voltage level at which derating stops [V] 0 : derating stop disabled n (n != 0) : derating stops at LED supply = n V
4:0	start	0	R	LED supply voltage level at which derating starts [V] 0 : derating disabled n (n != 0) : derating starts at LED supply = n V

Table 7.8.5-82: Register **VT_DERATE_START** (0x148) device temperature based derating start configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	start	0	R	temperature level at which derating starts [K] Note: start = 0 disables temperature derating

Table 7.8.5-83: Register **VT_DERATE_STOP** (0x14A) device temperature based derating stop configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	stop	0	R	temperature level at which derating stops [K]

Table 7.8.5-84: Register **DERATE_GAIN** (0x14C) derating gain configuration value

Bit	Name	Default	Access	Description
9:5	vt_gain	0	R	defines reduction of nominal LED current per Kelvin between VT_{start} and VT_{stop} VT derating multiplier (M_{VT_derate}) in case VT derating is enabled: • if VT <= VT_{start} : M_{VT_derate} = 1 • if VT_{start} < VT < VT_{stop} : M_{VT_derate} = 1 - (vt_gain * (VT - VT_{start}) / 256) • this equals a derating by vt_gain * 0.39% of nominal LED current per Kelvin • if VT >= VT_{stop} : M_{VT_derate} = 1 - (vt_gain * (VT_{stop} - VT_{start}) / 256) Note: If calculation of M_{VT_derate} gives a negative value, M_{VT_derate} will be set to 0.
4:0	vs_gain	0	R	defines reduction of nominal LED current per Volt between VS_{start} and VS_{stop} VS derating multiplier (M_{VS_derate}) in case VS derating is enabled: • if VS <= VS_{start} : M_{VS_derate} = 1 • if VS_{start} < VS < VS_{stop} : M_{VS_derate} = 1 - (vs_gain * (VS - VS_{start}) / (16 * 25)) • this equals a derating by vs_gain * 0.25% of nominal LED current per Volt • if VS >= VS_{stop} : M_{VS_derate} = 1 - (vs_gain * (VS_{stop} - VS_{start}) / (16 * 25)) Note: If calculation of M_{VS_derate} gives a negative value, M_{VS_derate} will be set to 0.

Table 7.8.5-85: Register **ISINK_BUNDLE** (0x15C) analog current sink bundling configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R	analog channel bundling for LED current balancing bit 0 : bundles channels 0 and 1 bit 1 : bundles channels 2 and 3 ... bit 6 : bundles channels 12 and 13 bit 7 : bundles channels 14 and 15 Note: Please note, that usually the corresponding PWM_COMBINE_PRI bits have also to be set when analog bundle bits are configured, to guarranty the correct analog bundling mode behavior.

7.9 Measurement System

7.9.1 Description

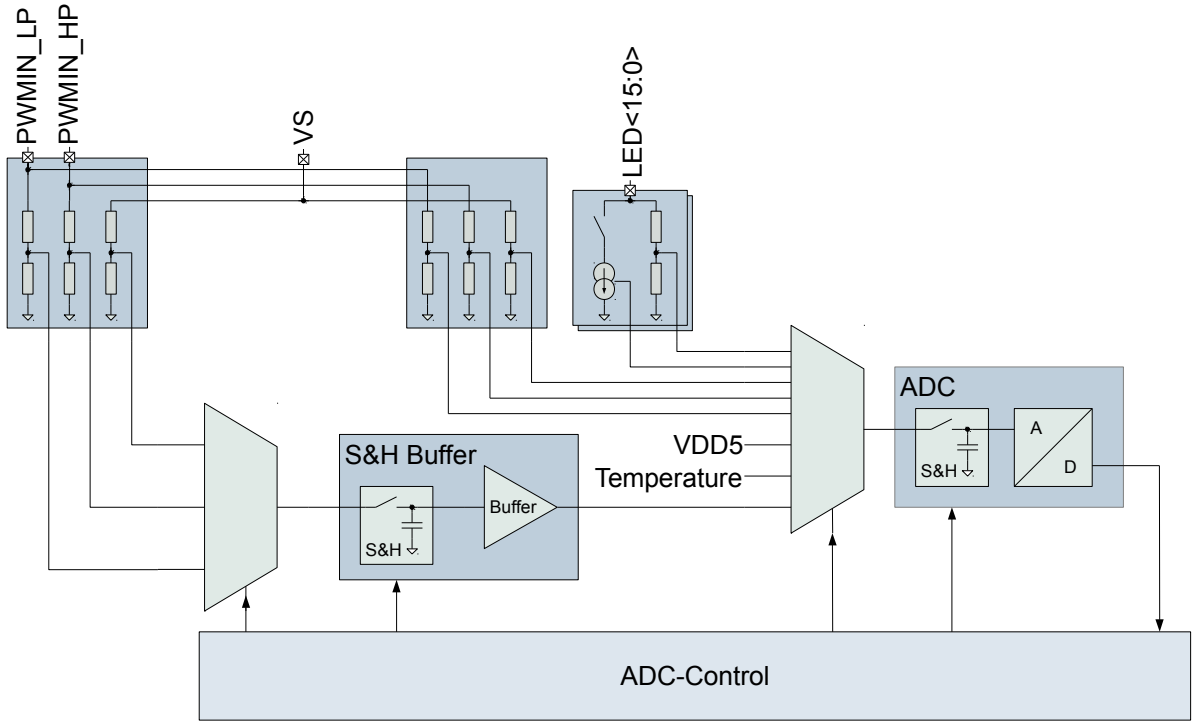

Figure 7.9.1-1: Measurement System

The centre of the measurement system is a 10 Bit SAR ADC.
With the ADC, it is possible to convert:

- LED voltage of each channel (prescaled and saturated)
- LED current of each channel
- Internal temperature-sensor voltage
- VDD5 voltage
- VS voltage (full range)
- PMWIN_HP voltage (full range)
- PMWIN_LP voltage (full range)
- A sample and hold (S&H) buffer voltage

3 inputs to the measurement system can be send to a sample and hold buffer. These are:

- VS voltage (prescaled and saturated)
- PMWIN_HP voltage (prescaled and saturated)
- PMWIN_LP voltage (prescaled and saturated)

LED(x) voltage and its supply can be sampled at the same time, and conversion of them can be done afterwards in series.
The diagnosis module will do a digital subtraction of the two results and compare it against the short detection threshold.

For better resolution in normal supply scenarios, the LED resistor dividers will reach ADC full scale at approximately 28V (see electrical parameter A_{MEAS_VLED}). VS and PWMIN resistor dividers use the same gain factors (see electrical parameters $A_{MEAS\_VS\_SH}$ and $A_{MEAS\_PWMIN\_SH}$).
To implement a full scale VS derating up to 40V, another resistor divider for VS is added to the measurement system (see electrical parameter A_{MEAS_VS}).

7.9.2 Accuracy of Measurement System

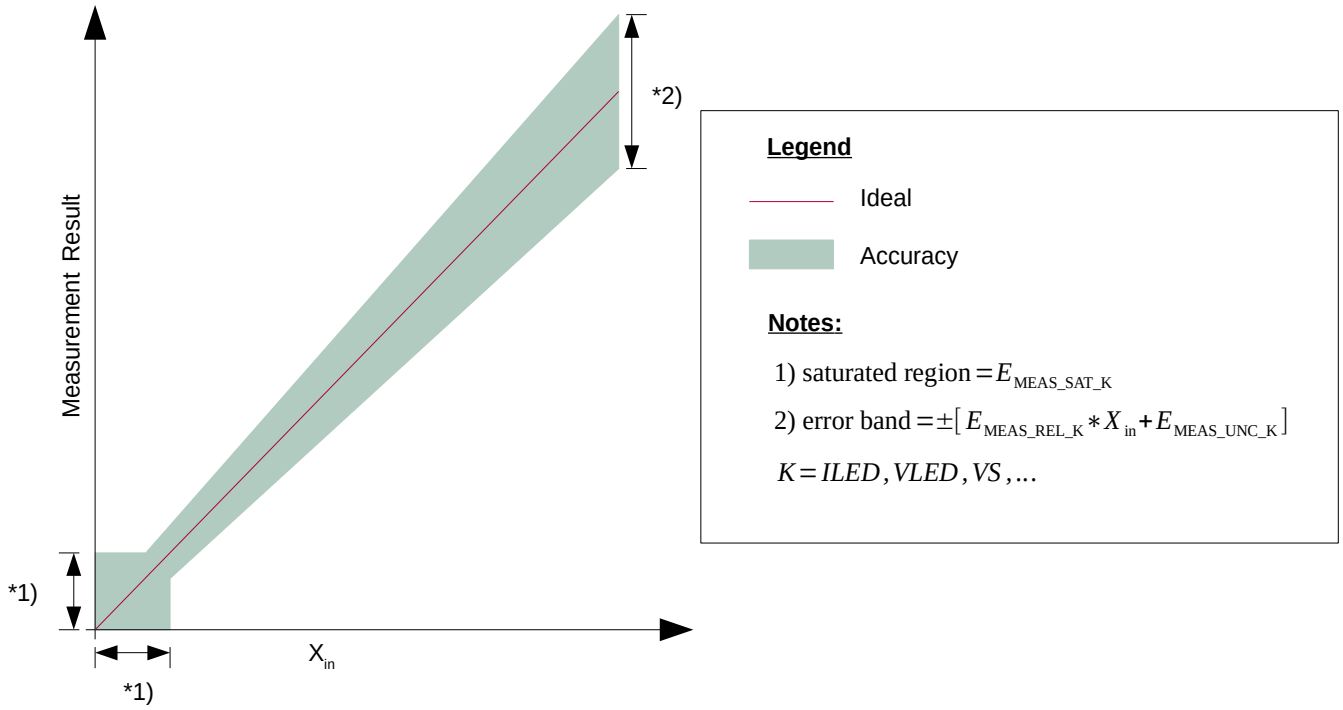

Figure 7.9.2-1: Accuracy Diagram

Explanation of Electrical Parameters for Accuracy Estimation:

The figure above shows exemplary the tolerances of each measurement:
There are mainly two effects:
1) Very low input values may saturate.
2) Normal input values suffer a combination of linear errors, which are a percentage value of the input plus some uncertainty. This sum includes temperature effects, non-linearities of the ADC and also noise.

7.10 Diagnosis

The device implements diagnosis features to detect open or short conditions of the connected LEDs.
An LED short condition means, that the LED driver pin is shorted with the LED supply net. An LED open condition means, that the LED driver pin is open and does not sink a significant current, e.g. caused by a broken LED or LED connection.

This diagnosis is implemented using once per PWM period ADC measurements of all LED channel voltages and their related supply voltages, measured using the sample and hold path amplification AMEAS_VS_SH and AMEAS_PWMIN_SH.

Every diagnosis result compare operation generates an event which is fed into an LED error filter.
Each LED channel implements it's own error filter using a counter and a common error level value (DIAG_CONFIG.level).

In case of an LED error condition, the filter counter value is incremented by 1 if the counter values is smaller than the DIAG_CONFIG.level value. In case of an LED OK condition, the filter counter value is decremented by 1 if the error counter is larger than 0.
When the filter counter value reaches the DIAG_CONFIG.level value, an LED channel error flag is set and kept until the filter counter value reaches 0 again. When the filter counter value reaches 0, the LED channel error flag is cleared.

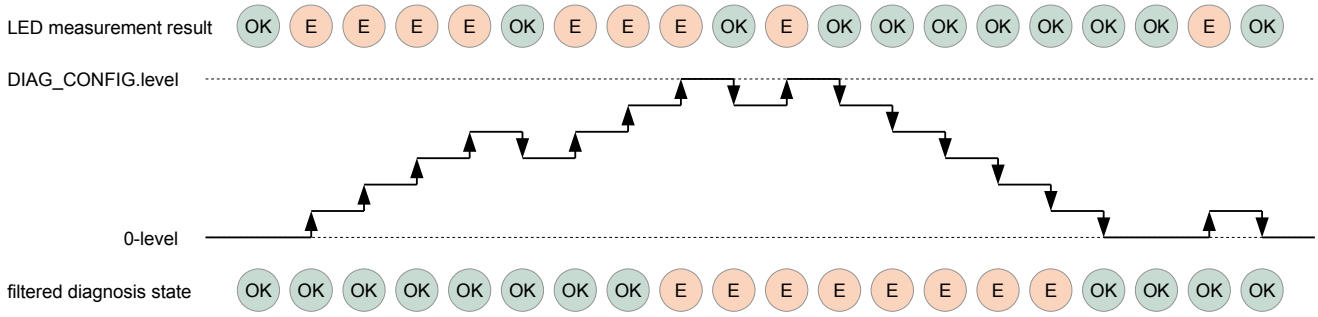

Figure 7.10-1: Open and Short Diagnosis Filter Behavior

If the related LEDx/DIAGx pin is selected to behave as a diagnosis pin (DIAG_CONFIG.diagx_sel = 1), LED channel error flag states are output at this diagnosis pin depending on the DIAGx_CONFIG.enable settings.
The device implements two independent DIAG pins (diagnosis groups) with their related evaluation logic shown in the figure below.

An LED pin short condition evaluation is only done and signalled in case of:

- LED related raw (non-offset-gain corrected) LED supply ADC measurement value is not saturated
  - LED supply is selected using the LED_SUPPLY_SEL_x (VS, PWMIN_LP or PWMIN_HP) values
- Short detection for the pin is enabled
- PWM was active and valid (LED current slewing has finished) during ADC measurement

An LED pin voltage based open condition evaluation is only done and signalled in case of:

- LED supply is larger than the minimum LED supply level configured using VS_TOO_LOW
- Voltage based Open detection for the pin is enabled
- PWM was active and valid (LED current slewing has finished) during ADC measurement

The device implements different modes of behaviour depending on the DIAG pin configuration:

- diag_enable = 1, diag_sel = 0, slm = 0:
  - Device internal only diagnosis information evaluation
  - The related LED/DIAG pin will not drive diagnosis state and can be used as LED driver pin
  - In case of an active diagnosis error flag:
    - The corresponding LED driver is switched to a retry measurement state
- diag_enable = 1, diag_sel = 0, slm = 1:
  - Device internal only diagnosis information evaluation
  - The related LED/DIAG pin will not drive diagnosis state and can be used as LED driver pin
  - In case of an active diagnosis error flag:
    - The corresponding LED driver is switched to a retry measurement state
    - All LED drivers of the related diagnosis group will be switched off (Device Single Lamp Mode)

- diag_enable = 1, diag_sel = 1, slm = 0:
  - The related LED/DIAG pin will drive diagnosis state (used as DIAG pin)
  - In case of an active diagnosis error flag:
    - The corresponding LED driver is switched to a retry measurement state
  - In case of an incoming active diagosis state:
    - This information will be ignored
- diag_enable = 1, diag_sel = 1, slm = 1:
  - The related LED/DIAG pin will drive diagnosis state (used as DIAG pin)
  - In case of an active diagnosis error flag:
    - The corresponding LED driver is switched to a retry measurement state
    - All LED drivers of the related diagnosis group will be switched off (System Single Lamp Mode)
  - In case of an incoming active diagosis state:
    - All LED drivers of the related diagnosis group will be switched off (System Single Lamp Mode)

The LED channel retry measurement state is used to recover LED channels from active error state. In this state the LED channel is switched ON for the minimum time needed to do LED channel retry ADC measurement.

Note: Diagnosis groups can be configured using the DIAGx_CONFIG.enable values.
Note: diag_ie is generated inside the device from diag_sel and slm: diag_ie = diag_sel & slm

The diagnosis evaluation logic shown in the figure below, behaves as follows:

- In case slm is 0, the LED error flag states are fed through the SLM logic.
- In case slm is 1, the output vector of the SLM logic has only two states:
  - When any LED error flag is active, all bits of the vector are set to 1.
  - When no LED error flag is active, all bits of the vector are set to 0.

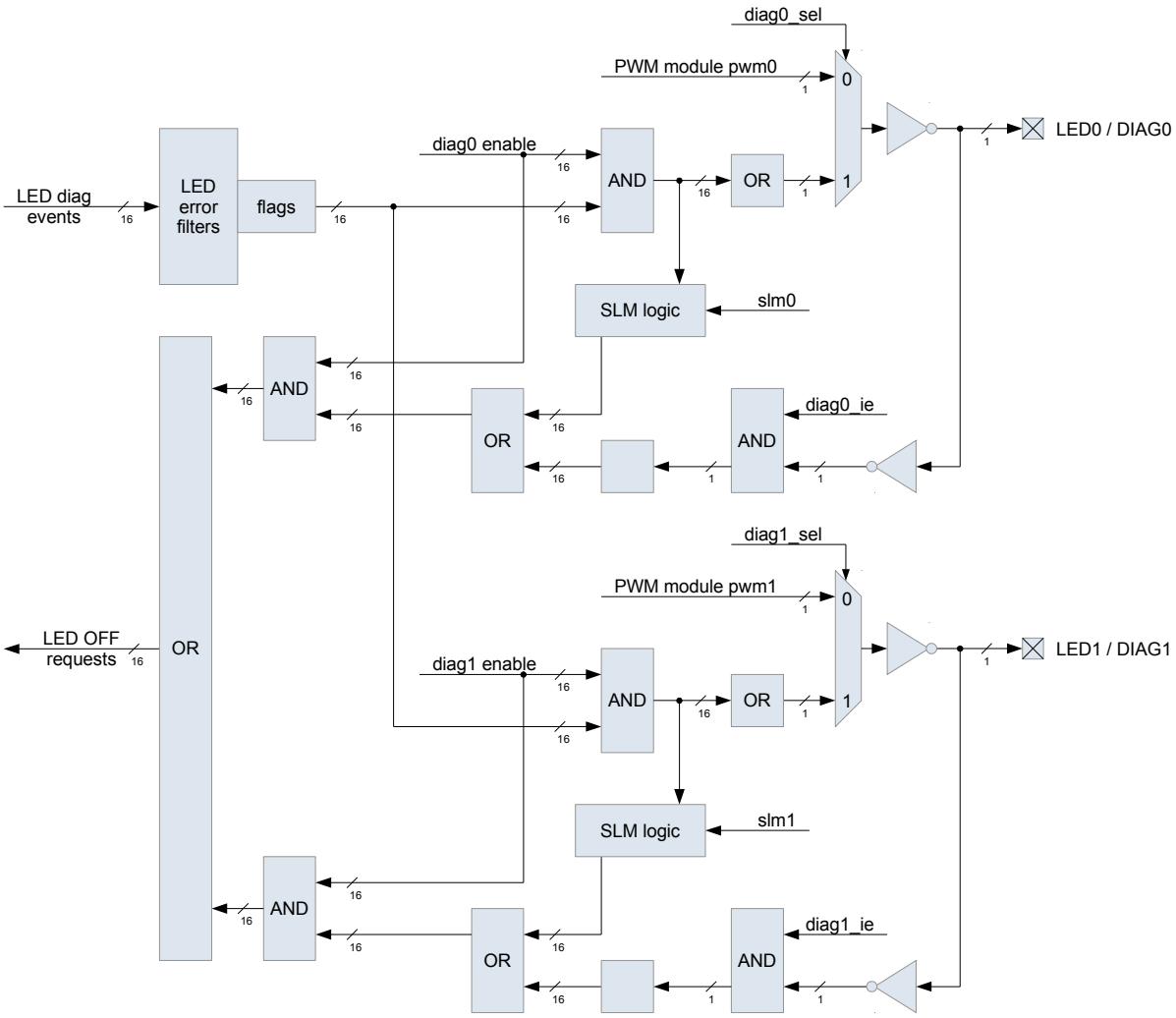

Figure 7.10-2: DIAG Evaluation Structure

Analog Bundled Mode Diagnosis

In analog bundled mode, the ILED diagnosis is not possible. This means, that the ILED open evaluation will be disabled by the device for all analog bundled channels. In case the device also drives non-bundled LED channels, the ILED open evaluation for these channels will be done regarding the ILED open threshold configuration value.

7.10.1 Standalone Area

Depending on the application, different LED supply concepts are possible to implement. To do a correct open and short diagnosis, the device needs to know the LED supply relation. This can be configured using the LED_SUPPLY_SEL_x values.
For open diagnosis, three different voltage levels can be configured using the LED_OPEN_THR_x values, and assigned to LED channels using the LED_OPEN_SEL_x values.
For short diagnosis, three different voltage levels can be configured using the LED_SHORT_THR_x values, and assigned to LED channels using the LED_SHORT_SEL_x values.

An LED open condition is detected if the LED pin voltage is below it's related LED_OPEN_THR_x level. In case of at least one enabled open condition, a common open error flag is set in the EVENT_STATUS value.
An LED short condition is detected if the LED related supply voltage minus the LED pin voltage is below it's related LED_SHORT_THR_x level. In case of at least one enabled short condition, a common short error flag is set in the EVENT_STATUS value.
An LED short condition is only signalized in case the sampled ADC supply and LED pin values are not saturated.

The device power supply can be observed using level values, which can be configured using the VS_TOO_LOW and VS_CRITICAL values.

- When VS voltage falls below the VS_TOO_LOW level, an error flag is set in the EVENT_STATUS value.
- When VS voltage is larger than the VS_CRITICAL level, an error flag is set in the EVENT_STATUS value.
- When VT temperate value is larger than the VT_CRITICAL level, an error flag is set in the EVENT_STATUS value.

Table 7.10.1-1: Device Event Effects

event	*realisation*	*DEVICE INIT*	*ACTIVE MODE*	*effect*
power-ON reset	analog comparator	-	-	reset
5V under-voltage	analog comparator	YES	YES	reset
over-temperature	analog comparator	YES	YES	reset
communication timeout	digital signal	NO	YES	DIAG + status bit
active LED current derating	ADC measurement	NO	YES	status bit
VS too low	ADC measurement	NO	YES	status bit
critical VS (too high)	ADC measurement	NO	YES	status bit
critical temperature (too high)	ADC measurement	NO	YES	status bit
LED short condition	ADC measurement	NO	YES	DIAG + status bit
LED open condition	ADC measurement	NO	YES	DIAG + status bit

Table 7.10.1-2: STANDALONE

Register Name	*Address*	*Description*
LED_OPEN_THR_1	0x0D0	LED open detection threshold level 1 configuration value
LED_OPEN_THR_2	0x0D2	LED open detection threshold level 2 configuration value
LED_OPEN_THR_3	0x0D4	LED open detection threshold level 3 configuration value
LED_OPEN_SEL_0_3	0x0D6	LED open threshold level to LED channels 0 to 3 assignment configuration value
LED_OPEN_SEL_4_7	0x0D8	LED open threshold level to LED channels 4 to 7 assignment configuration value
LED_OPEN_SEL_8_11	0x0DA	LED open threshold level to LED channels 8 to 11 assignment configuration value
LED_OPEN_SEL_12_15	0x0DC	LED open threshold level to LED channels 12 to 15 assignment configuration value
LED_SHORT_THR_1	0x0DE	LED short detection threshold level 1 configuration value
LED_SHORT_THR_2	0x0E0	LED short detection threshold level 2 configuration value
LED_SHORT_THR_3	0x0E2	LED short detection threshold level 3 configuration value

Register Name	*Address*	*Description*
LED_SHORT_SEL_0_3	0x0E4	LED short threshold level to LED channels 0 to 3 assignment configuration value
LED_SHORT_SEL_4_7	0x0E6	LED short threshold level to LED channels 4 to 7 assignment configuration value
LED_SHORT_SEL_8_11	0x0E8	LED short threshold level to LED channels 8 to 11 assignment configuration value
LED_SHORT_SEL_12_15	0x0EA	LED short threshold level to LED channels 12 to 15 assignment configuration value
ILED_OPEN_THR	0x0EE	LED current based open detection threshold configuration value
VS_TOO_LOW	0x0F0	VS too low watch configuration value
VS_CRITICAL	0x0F2	VS too high watch configuration value
VT_CRITICAL	0x0F4	VT too high watch configuration value
DIAG_CONFIG	0x150	diagnosis pins configuration
DIAG0_CONFIG_0_7	0x152	diagnosis group 0 configuration for LED channels 0 to 7
DIAG0_CONFIG_8_15	0x154	diagnosis group 0 configuration for LED channels 8 to 15
DIAG1_CONFIG_0_7	0x156	diagnosis group 1 configuration for LED channels 0 to 7
DIAG1_CONFIG_8_15	0x158	diagnosis group 1 configuration for LED channels 8 to 15
DIAG_CURRENT	0x15A	DIAG pins current configuration
LED_SUPPLY_SEL_0_3	0x160	LED related supply selection configuration value
LED_SUPPLY_SEL_4_7	0x162	LED related supply selection configuration value
LED_SUPPLY_SEL_8_11	0x164	LED related supply selection configuration value
LED_SUPPLY_SEL_12_15	0x166	LED related supply selection configuration value

Table 7.10.1-3: Register **LED_SUPPLY_SEL_0_3** (0x160) LED related supply selection configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led3	0	R	LED channel 3 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
5:4	led2	0	R	LED channel 2 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
3:2	led1	0	R	LED channel 1 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
1:0	led0	0	R	LED channel 0 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !

Table 7.10.1-4: Register **LED_SUPPLY_SEL_4_7** (0x162) LED related supply selection configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led7	0	R	LED channel 7 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
5:4	led6	0	R	LED channel 6 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
3:2	led5	0	R	LED channel 5 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
1:0	led4	0	R	LED channel 4 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !

Table 7.10.1-5: Register **LED_SUPPLY_SEL_8_11** (0x164) LED related supply selection configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led11	0	R	LED channel 11 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
5:4	led10	0	R	LED channel 10 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
3:2	led9	0	R	LED channel 9 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
1:0	led8	0	R	LED channel 8 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !

Table 7.10.1-6: Register **LED_SUPPLY_SEL_12_15** (0x166) LED related supply selection configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led15	0	R	LED channel 15 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
5:4	led14	0	R	LED channel 14 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
3:2	led13	0	R	LED channel 13 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !
1:0	led12	0	R	LED channel 12 supply selection 0 : VS 1 : PWMIN_LP 2 : PWMIN_HP 3 : reserved, do not use !

Table 7.10.1-7: Register **LED_OPEN_THR_1** (0x0D0) LED open detection threshold level 1 configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	LED OPEN detection threshold level [36 LSB/V] Note: OPEN condition, if the LED pin voltage sample value is smaller than the selected detection threshold level.

Table 7.10.1-8: Register **LED_OPEN_THR_2** (0x0D2) LED open detection threshold level 2 configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	LED OPEN detection threshold level [36 LSB/V] Note: OPEN condition, if the LED pin voltage sample value is smaller than the selected detection threshold level.

Table 7.10.1-9: Register **LED_OPEN_THR_3** (0x0D4) LED open detection threshold level 3 configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	LED OPEN detection threshold level [36 LSB/V] Note: OPEN condition, if the LED pin voltage sample value is smaller than the selected detection threshold level.

Table 7.10.1-10: Register **LED_OPEN_SEL_0_3** (0x0D6) LED open threshold level to LED channels 0 to 3 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led3	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led2	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led1	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led0	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 7.10.1-11: Register **LED_OPEN_SEL_4_7** (0x0D8) LED open threshold level to LED channels 4 to 7 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led7	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led6	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led5	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led4	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 7.10.1-12: Register **LED_OPEN_SEL_8_11** (0x0DA) LED open threshold level to LED channels 8 to 11 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led11	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led10	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led9	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led8	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 7.10.1-13: Register **LED_OPEN_SEL_12_15** (0x0DC) LED open threshold level to LED channels 12 to 15 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led15	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led14	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led13	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led12	0	R	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 7.10.1-14: Register **LED_SHORT_THR_1** (0x0DE) LED short detection threshold level 1 configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	LED SHORT detection threshold level [36 LSB/V] Note: SHORT condition, if the difference between LED supply sample and LED pin voltage sample is smaller than the detection threshold level.

Table 7.10.1-15: Register **LED_SHORT_THR_2** (0x0E0) LED short detection threshold level 2 configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	LED SHORT detection threshold level [36 LSB/V] Note: SHORT condition, if the difference between LED supply sample and LED pin voltage sample is smaller than the detection threshold level.

Table 7.10.1-16: Register **LED_SHORT_THR_3** (0x0E2) LED short detection threshold level 3 configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	LED SHORT detection threshold level [36 LSB/V] Note: SHORT condition, if the difference between LED supply sample and LED pin voltage sample is smaller than the detection threshold level.

Table 7.10.1-17: Register **LED_SHORT_SEL_0_3** (0x0E4) LED short threshold level to LED channels 0 to 3 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led3	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led2	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led1	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led0	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 7.10.1-18: Register **LED_SHORT_SEL_4_7** (0x0E6) LED short threshold level to LED channels 4 to 7 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led7	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led6	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led5	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led4	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 7.10.1-19: Register **LED_SHORT_SEL_8_11** (0x0E8) LED short threshold level to LED channels 8 to 11 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led11	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led10	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led9	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led8	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 7.10.1-20: Register **LED_SHORT_SEL_12_15** (0x0EA) LED short threshold level to LED channels 12 to 15 assignment configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:6	led15	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led14	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led13	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led12	0	R	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 7.10.1-21: Register **ILED_OPEN_THR** (0x0EE) LED current based open detection threshold configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	When the ADC result of LED current measurement is smaller than this [10 LSB/mA] level value, an "LED open" will be signalled. Note: A level value of 0 disables LED current value evaluation for LED open detection. Note: If device uses analog channel bundling, LED open detection via LED current measurement is disabled for analog bundled channels.

Table 7.10.1-22: Register **VS_TOO_LOW** (0x0F0) VS too low watch configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	When the ADC result of VS measurement is smaller than this [25 LSB/V] level value, a "VS too low" will be signalled. Note: LED open and short evaluation of all LED channels will be disabled in case of "VS too low". Note: A level value of 0 prevents the device from disabling the LED open/short evaluation.

Table 7.10.1-23: Register **VS_CRITICAL** (0x0F2) VS too high watch configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	When the ADC result of VS measurement is larger than this [25 LSB/V] level value, a "VS critical" will be signalled. Note: A level value of 0 disables VS value evaluation for "VS critical".

Table 7.10.1-24: Register **VT_CRITICAL** (0x0F4) VT too high watch configuration value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	level	0	R	When the ADC result of VT measurement is larger than this [1 LSB/K] level value, a "VT critical" will be signalled. Note: A level value of 0 disables VT value evaluation for "VT critical".

Table 7.10.1-25: Register **DIAG_CONFIG** (0x150) diagnosis pins configuration

Bit	*Name*	*Default*	*Access*	*Description*
9	slm1	0	R	diagnosis group 1 single lamp mode selection 0 : multi-lamp-mode (MLM) 1 : single-lamp-mode (SLM)
8	slm0	0	R	diagnosis group 0 single lamp mode selection 0 : multi-lamp-mode (MLM) 1 : single-lamp-mode (SLM)
7	diag1_sel	0	R	LED1 pin usage selection 0 : pin used as LED pin 1 : pin used as DIAG1 pin
6	diag0_sel	0	R	LED0 pin usage selection 0 : pin used as LED pin 1 : pin used as DIAG0 pin
5	-	0	R	
4:0	level	0	R	DIAG counter level DIAG error counter level which has to be reached before asserting a diagnosis error Note: If level is 0, the filter will block all diagnosis events received from the measurement system and it's output will not show a diagnosis error. Set level at least to 1 to enable the filter.

Table 7.10.1-26: Register **DIAG0_CONFIG_0_7** (0x152) diagnosis group 0 configuration for LED channels 0 to 7

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	DIAG0 diagnosis enable for driver channels 0 to 7

Table 7.10.1-27: Register **DIAG0_CONFIG_8_15** (0x154) diagnosis group 0 configuration for LED channels 8 to 15

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	DIAG0 diagnosis enable for driver channels 8 to 15

Table 7.10.1-28: Register **DIAG1_CONFIG_0_7** (0x156) diagnosis group 1 configuration for LED channels 0 to 7

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	DIAG1 diagnosis enable for driver channels 0 to 7

Table 7.10.1-29: Register **DIAG1_CONFIG_8_15** (0x158) diagnosis group 1 configuration for LED channels 8 to 15

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	enable	0	R	DIAG1 diagnosis enable for driver channels 8 to 15

Table 7.10.1-30: Register **DIAG_CURRENT** (0x15A) DIAG pins current configuration

Bit	*Name*	*Default*	*Access*	*Description*
9:0	sel	0	R	DIAG pin driver current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

7.10.2 Bus Config Area

Table 7.10.2-1: BUS_CONFIG

Register Name	*Address*	*Description*
ASSERT_DIAG	0x62	DIAG pin assertion via bus

Table 7.10.2-2: Register **ASSERT_DIAG** (0x62) DIAG pin assertion via bus

Bit	*Name*	*Default*	*Access*	*Description*
9:4	pass	0	R/W	write password This bitfield has to be written as 0x26 to enable the evaluation of bits 0 .. 3, else the written value will be ignored.
3	mask_diag1_in	0	R/W	0 : DIAG1 pin input path behaves like set up by STANDALONE configuration 1 : DIAG1 pin input path disabled
2	mask_diag0_in	0	R/W	0 : DIAG0 pin input path behaves like set up by STANDALONE configuration 1 : DIAG0 pin input path disabled
1	assert_diag1	0	R/W	0 : device internal DIAG pin functionality only 1 : DIAG1 pin is asserted, when DIAG is selected for pin LED1
0	assert_diag0	0	R/W	0 : device internal DIAG pin functionality only 1 : DIAG0 pin is asserted, when DIAG is selected for pin LED0

7.10.3 Bus Status Area

The ADC measurement result values are stored by the device in the following data structure even like the open, short and device event status flags.
The EVENT_STATUS flags are captured and held until the value is read via the bus communication interface. At this moment the event flags are cleared automatically.

ADC open and short measurements

The ADC will perform VLED, VDIF and ILED measurements independent of the open and short thresholds and analog bundling configuration and provide the data in the BUS_STATUS area. This makes it possible to implement a bus master driven open and short evaluation without using the device internal open and short evaluation logic.

Table 7.10.3-1: BUS_STATUS

Register Name	*Address*	*Description*
RESULT_VLED_0	0x00	LED0 pin voltage ADC measurement result value
RESULT_VLED_1	0x02	LED1 pin voltage ADC measurement result value
RESULT_VLED_2	0x04	LED2 pin voltage ADC measurement result value
RESULT_VLED_3	0x06	LED3 pin voltage ADC measurement result value
RESULT_VLED_4	0x08	LED4 pin voltage ADC measurement result value
RESULT_VLED_5	0x0A	LED5 pin voltage ADC measurement result value
RESULT_VLED_6	0x0C	LED6 pin voltage ADC measurement result value
RESULT_VLED_7	0x0E	LED7 pin voltage ADC measurement result value
RESULT_VLED_8	0x10	LED8 pin voltage ADC measurement result value
RESULT_VLED_9	0x12	LED9 pin voltage ADC measurement result value
RESULT_VLED_10	0x14	LED10 pin voltage ADC measurement result value
RESULT_VLED_11	0x16	LED11 pin voltage ADC measurement result value
RESULT_VLED_12	0x18	LED12 pin voltage ADC measurement result value
RESULT_VLED_13	0x1A	LED13 pin voltage ADC measurement result value
RESULT_VLED_14	0x1C	LED14 pin voltage ADC measurement result value
RESULT_VLED_15	0x1E	LED15 pin voltage ADC measurement result value
RESULT_VDIF_0	0x20	LED0 related external load voltage drop value
RESULT_VDIF_1	0x22	LED1 related external load voltage drop value
RESULT_VDIF_2	0x24	LED2 related external load voltage drop value
RESULT_VDIF_3	0x26	LED3 related external load voltage drop value
RESULT_VDIF_4	0x28	LED4 related external load voltage drop value
RESULT_VDIF_5	0x2A	LED5 related external load voltage drop value
RESULT_VDIF_6	0x2C	LED6 related external load voltage drop value
RESULT_VDIF_7	0x2E	LED7 related external load voltage drop value
RESULT_VDIF_8	0x30	LED8 related external load voltage drop value
RESULT_VDIF_9	0x32	LED9 related external load voltage drop value
RESULT_VDIF_10	0x34	LED10 related external load voltage drop value
RESULT_VDIF_11	0x36	LED11 related external load voltage drop value
RESULT_VDIF_12	0x38	LED12 related external load voltage drop value
RESULT_VDIF_13	0x3A	LED13 related external load voltage drop value
RESULT_VDIF_14	0x3C	LED14 related external load voltage drop value
RESULT_VDIF_15	0x3E	LED15 related external load voltage drop value
RESULT_ILED_0	0x40	LED0 current ADC measurement result value
RESULT_ILED_1	0x42	LED1 current ADC measurement result value
RESULT_ILED_2	0x44	LED2 current ADC measurement result value
RESULT_ILED_3	0x46	LED3 current ADC measurement result value
RESULT_ILED_4	0x48	LED4 current ADC measurement result value
RESULT_ILED_5	0x4A	LED5 current ADC measurement result value
RESULT_ILED_6	0x4C	LED6 current ADC measurement result value
RESULT_ILED_7	0x4E	LED7 current ADC measurement result value

Register Name	*Address*	*Description*
RESULT_ILED_8	0x50	LED8 current ADC measurement result value
RESULT_ILED_9	0x52	LED9 current ADC measurement result value
RESULT_ILED_10	0x54	LED10 current ADC measurement result value
RESULT_ILED_11	0x56	LED11 current ADC measurement result value
RESULT_ILED_12	0x58	LED12 current ADC measurement result value
RESULT_ILED_13	0x5A	LED13 current ADC measurement result value
RESULT_ILED_14	0x5C	LED14 current ADC measurement result value
RESULT_ILED_15	0x5E	LED15 current ADC measurement result value
RESULT_VT	0x60	device temperature ADC measurement result value
RESULT_VSUP	0x62	selected derating supply ADC meas result value
RESULT_VDD5	0x64	VDD5 voltage ADC measurement result value
LED_OPEN_0_7	0x70	LED channels 0 to 7 open detection status value
LED_OPEN_8_15	0x72	LED channels 8 to 15 open detection status value
LED_SHORT_0_7	0x74	LED channels 0 to 7 short detection status value
LED_SHORT_8_15	0x76	LED channels 8 to 15 short detection status value
EVENT_STATUS	0x78	device events status value
PWMIN_STATUS	0x7A	PWMIN interface state value
DIAG_STATUS	0x7C	diagnosis groups status

Table 7.10.3-2: Register **RESULT_VLED_0** (0x00) LED0 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-3: Register **RESULT_VLED_1** (0x02) LED1 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-4: Register **RESULT_VLED_2** (0x04) LED2 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-5: Register **RESULT_VLED_3** (0x06) LED3 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-6: Register **RESULT_VLED_4** (0x08) LED4 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-7: Register **RESULT_VLED_5** (0x0A) LED5 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-8: Register **RESULT_VLED_6** (0x0C) LED6 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-9: Register **RESULT_VLED_7** (0x0E) LED7 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-10: Register **RESULT_VLED_8** (0x10) LED8 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-11: Register **RESULT_VLED_9** (0x12) LED9 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-12: Register **RESULT_VLED_10** (0x14) LED10 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-13: Register **RESULT_VLED_11** (0x16) LED11 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-14: Register **RESULT_VLED_12** (0x18) LED12 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-15: Register **RESULT_VLED_13** (0x1A) LED13 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-16: Register **RESULT_VLED_14** (0x1C) LED14 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-17: Register **RESULT_VLED_15** (0x1E) LED15 pin voltage ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin voltage ADC result data value [36 LSB/V]

Table 7.10.3-18: Register **RESULT_VDIF_0** (0x20) LED0 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-19: Register **RESULT_VDIF_1** (0x22) LED1 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-20: Register **RESULT_VDIF_2** (0x24) LED2 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-21: Register **RESULT_VDIF_3** (0x26) LED3 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-22: Register **RESULT_VDIF_4** (0x28) LED4 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-23: Register **RESULT_VDIF_5** (0x2A) LED5 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-24: Register **RESULT_VDIF_6** (0x2C) LED6 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-25: Register **RESULT_VDIF_7** (0x2E) LED7 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-26: Register **RESULT_VDIF_8** (0x30) LED8 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-27: Register **RESULT_VDIF_9** (0x32) LED9 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-28: Register **RESULT_VDIF_10** (0x34) LED10 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-29: Register **RESULT_VDIF_11** (0x36) LED11 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-30: Register **RESULT_VDIF_12** (0x38) LED12 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-31: Register **RESULT_VDIF_13** (0x3A) LED13 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-32: Register **RESULT_VDIF_14** (0x3C) LED14 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-33: Register **RESULT_VDIF_15** (0x3E) LED15 related external load voltage drop value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED channel related LED supply ADC result data value minus LED pin voltage ADC result value [36 LSB/V]

Table 7.10.3-34: Register **RESULT_ILED_0** (0x40) LED0 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-35: Register **RESULT_ILED_1** (0x42) LED1 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-36: Register **RESULT_ILED_2** (0x44) LED2 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-37: Register **RESULT_ILED_3** (0x46) LED3 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-38: Register **RESULT_ILED_4** (0x48) LED4 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-39: Register **RESULT_ILED_5** (0x4A) LED5 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-40: Register **RESULT_ILED_6** (0x4C) LED6 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-41: Register **RESULT_ILED_7** (0x4E) LED7 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-42: Register **RESULT_ILED_8** (0x50) LED8 current ADC measurement result value

Bit	*Name*	*Default*	*Access*	*Description*
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-43: Register **RESULT_ILED_9** (0x52) LED9 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-44: Register **RESULT_ILED_10** (0x54) LED10 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-45: Register **RESULT_ILED_11** (0x56) LED11 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-46: Register **RESULT_ILED_12** (0x58) LED12 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-47: Register **RESULT_ILED_13** (0x5A) LED13 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-48: Register **RESULT_ILED_14** (0x5C) LED14 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-49: Register **RESULT_ILED_15** (0x5E) LED15 current ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin current ADC result data value [100uA]

Table 7.10.3-50: Register **RESULT_VT** (0x60) device temperature ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	VT (temperature) ADC channel result data value in Kelvin Example: T = 25°C -> data = 273 + 25 = 298

Table 7.10.3-51: Register **RESULT_VSUP** (0x62) selected derating supply ADC meas result value

Bit	Name	Default	Access	Description
9:0	data	0	R	selected derating supply ADC measurement result value [25 LSB/V]

Table 7.10.3-52: Register **RESULT_VDD5** (0x64) VDD5 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	VDD5 voltage ADC measurement result value [142 LSB/V]

Table 7.10.3-53: Register **LED_OPEN_0_7** (0x70) LED channels 0 to 7 open detection status value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	status	0	R	LED channels 0 to 7 OPEN status

Table 7.10.3-54: Register **LED_OPEN_8_15** (0x72) LED channels 8 to 15 open detection status value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	status	0	R	LED channels 8 to 15 OPEN status

Table 7.10.3-55: Register **LED_SHORT_0_7** (0x74) LED channels 0 to 7 short detection status value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	status	0	R	LED channels 0 to 7 SHORT status

Table 7.10.3-56: Register **LED_SHORT_8_15** (0x76) LED channels 8 to 15 short detection status value

Bit	*Name*	*Default*	*Access*	*Description*
9:8	-	0	R	
7:0	status	0	R	LED channels 8 to 15 SHORT status

Table 7.10.3-57: Register **EVENT_STATUS** (0x78) device events status value

Bit	*Name*	*Default*	*Access*	*Description*
9	bus_crc_error	0	R	communication CRC error flag
8	meas_error	0	R	wrong ADC reference measurement result occurred
7	led_open	0	R	LED open condition flag
6	led_short	0	R	LED short condition flag
5	vt_too_high	0	R	critical temperature (too high) flag
4	vs_too_high	0	R	critical VS (too high) flag
3	vs_too_low	0	R	VS too low flag
2	derating	0	R	LED current derating active flag
1	timeout	0	R	communication timeout flag
0	reset	1	R	reset flag

Table 7.10.3-58: Register **PWMIN_STATUS** (0x7A) PWMIN interface state value

Bit	*Name*	*Default*	*Access*	*Description*
9	oe_state	0	R	OE pin state
8	reserved	0	R	reserved
7	hp_state_direct	0	R	PWMIN_HP evaluated state is "direct PWM state"
6	lp_state_direct	0	R	PWMIN_LP evaluated state is "direct PWM state"
5	hp_state_fallback	0	R	PWMIN_HP evaluated state is "fallback state"
4	lp_state_fallback	0	R	PWMIN_LP evaluated state is "fallback state"
3	hp_state_bus	1	R	PWMIN_HP evaluated state is "bus state"
2	lp_state_bus	1	R	PWMIN_LP evaluated state is "bus state"
1	pwmin_hp	0	R	PWMIN_HP pin state (CONFIG.pwmin_hp_inv dependent)
0	pwmin_lp	0	R	PWMIN_LP pin state (CONFIG.pwmin_lp_inv dependent)

Table 7.10.3-59: Register **DIAG_STATUS** (0x7C) diagnosis groups status

Bit	*Name*	*Default*	*Access*	*Description*
9:4	-	0	R	
3	diag1_in	0	R	DIAG1 input (incoming) state 1 : if DIAG1 pin is active and DIAG1 input path is enabled
2	diag0_in	0	R	DIAG0 input (incoming) state 1 : if DIAG0 pin is active and DIAG0 input path is enabled
1	diag1_out	0	R	DIAG1 internal (outgoing) state 1 : if an LED of device diagnosis group 1 shows an error
0	diag0_out	0	R	DIAG0 internal (outgoing) state 1 : if an LED of device diagnosis group 0 shows an error

8 Typical Applications

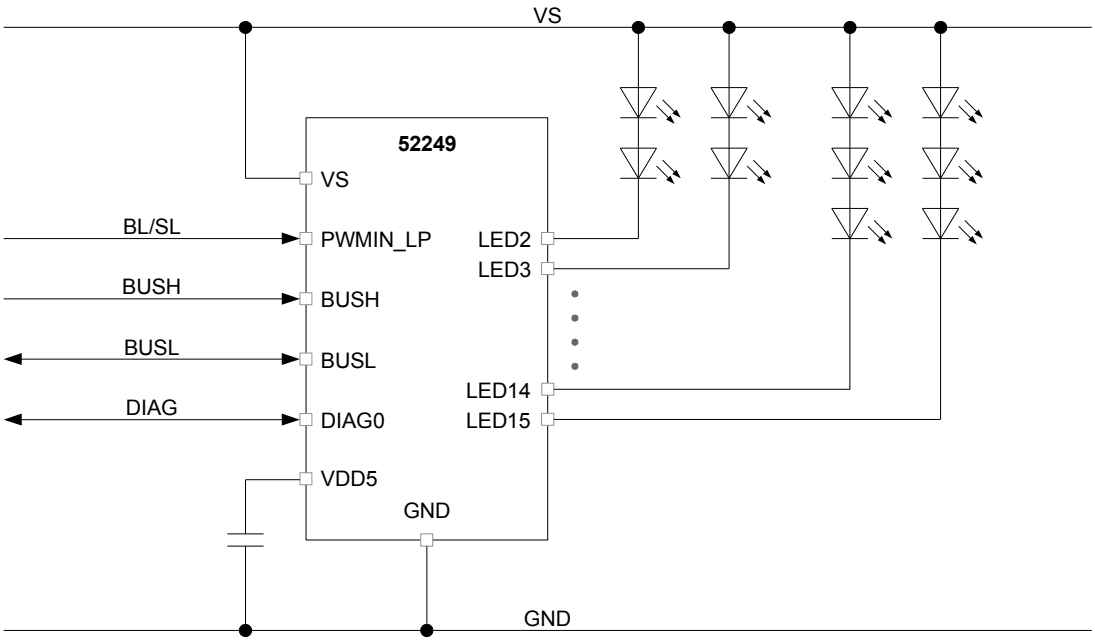

Figure 8-1: VS Supplied LEDs with Bus Interface

Device and connected LEDs are supplied by VS.
Device is controlled by external uC via bus and PWMIN interface.
Device is connected with other devices via diagnosis (DIAG) network.
Device can be configured to drive mixed LED structures.

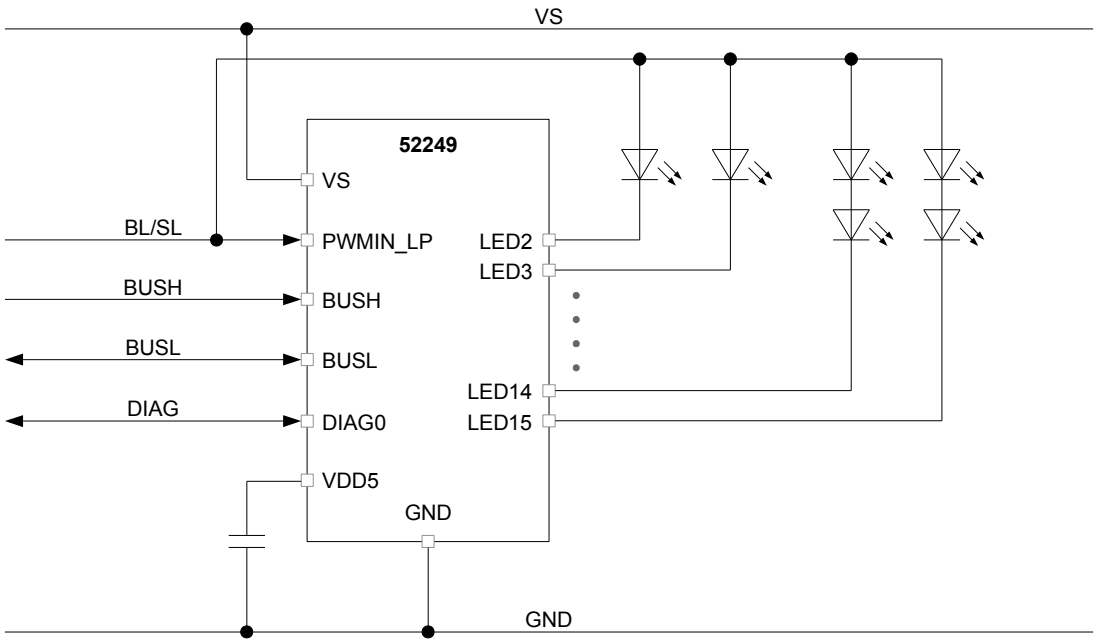

Figure 8-2: PWMIN Supplied LEDs with Bus Interface

Device is supplied by VS and connected LEDs are supplied by PWMIN interface signal.
Device is controlled by external uC via bus and PWMIN interface.
Device is connected with other devices via diagnosis (DIAG) network.
Device can be configured to drive mixed LED structures.

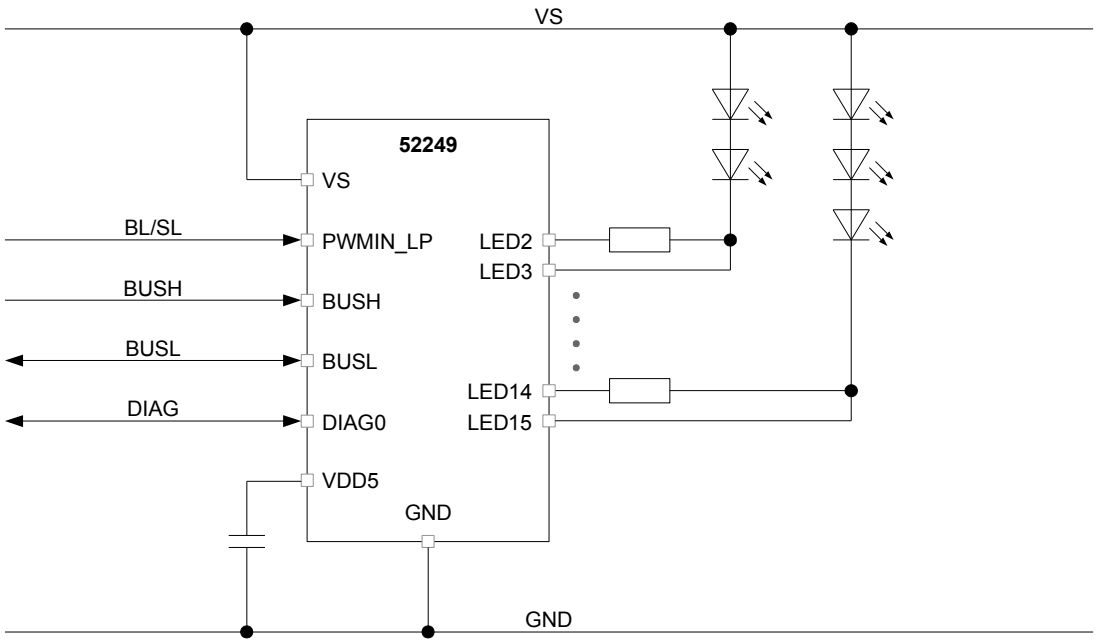

Figure 8-3: LED Channel Bundling and Current Balancing

Device and connected LEDs are supplied by VS.
Device is controlled by external uC via bus and PWMIN interface.
Device is connected with other devices via diagnosis (DIAG) network.
Device can be configured to drive bundled LED with LED current balancing to reduce device power dissipation.

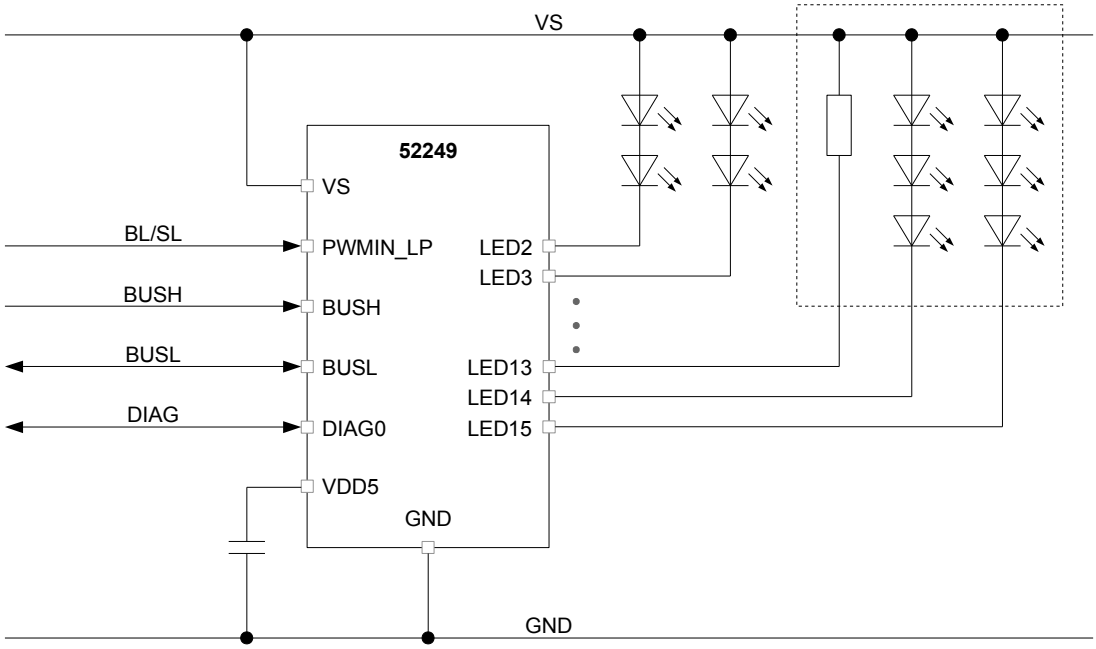

Figure 8-4: LED Bin Resistor Evaluation Example

Device and connected LEDs are supplied by VS.
Device is controlled by external uC via bus and PWMIN interface.
Device is connected with other devices via diagnosis (DIAG) network.
An external resistor value can be evaluated to adjust the LED bin class dependent brightness of a configurable LED group.

9 Package Reference

The E522.49 is available in a Pb free, RoHs compliant, QFN32L6 plastic package according to JEDEC MO-220-K VJJC-2, except the dimensions of the exposed pad. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of 260°C.

Note: Thermal resistance junction to ambient $R_{th,ja}$ is typ. 28 °C/W, based on JEDEC standard JESD-51-6 and JESD.

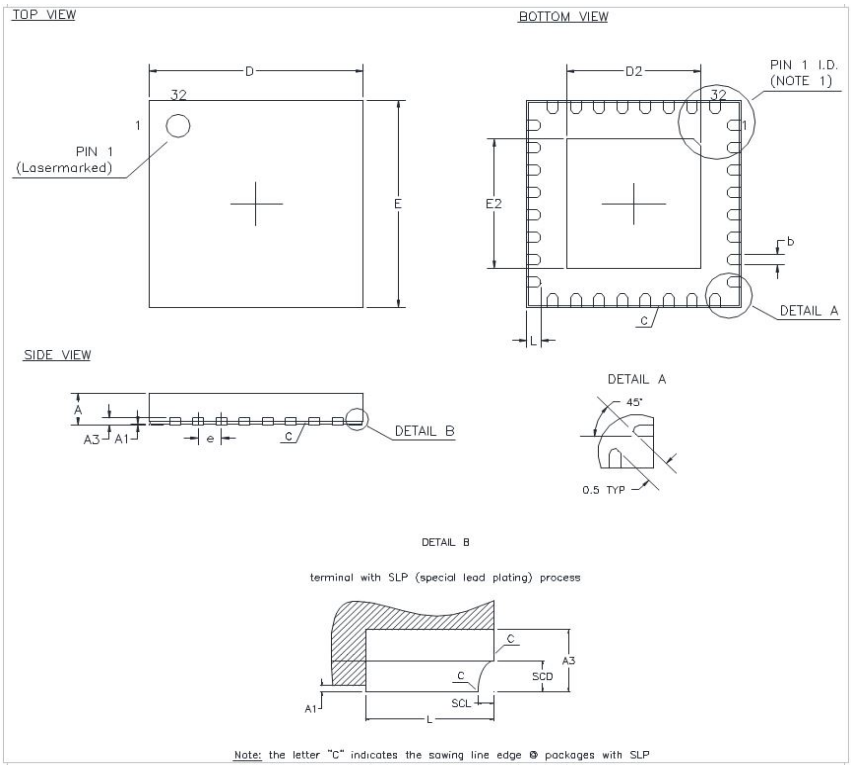

Figure 9-1: Package Outline QFN32L6

Table 9-1: Package Characteristics QFN32L6

Description	*Symbol*		*mm*			*inch*	
		min	**typ**	**max**	**min**	**typ**	**max**
Package height	A	0.8	0.9	1	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.0	0.00079	0.002
Thickness of terminal leads, including lead finish	A3		0.2 REF			0.0079 REF	
Width of terminal leads	b	0.25	0.3	0.35	0.01	0.012	0.014
Package length / width	D / E		6.00 BSC			0.237 BSC	
Length /width of exposed pad	D2 / E2	3.6	3.75	3.9	0.142	0.148	0.154
Lead pitch	e		0.65 BSC			0.026 BSC	
Length of terminal for soldering to substrate	L	0.35	0.4	0.45	0.014	0.016	0.018
Step cut depth (incl. plating layer)	SCD	0.075	0.1	0.125	0.003	0.004	0.005
Step cut length (incl. plating layer)	SCL	0.025	0.05	0.075	0.001	0.002	0.003
Number of terminal positions	N		32			32	

Note: The mm values are valid, the inch values contain rounding errors.

10 General

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11 Contact Info

Table 11-1: Contact Information

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