STK554U392C-E

Intelligent Power Module (IPM)

600 V, 15 A

The STK554U392C−E is a fully−integrated inverter power stage consisting of a high−voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless−DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3−phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has a full range of protection functions including cross−conduction protection, external shutdown and under−voltage lockout functions. Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Features

- Three−phase 15 A/600 V IGBT Module with Integrated Drivers
- Typical Values: $V_{CE}(sat)$ = 1.7 V, V_F = 1.9 V
- 62.0 mm × 21.8 mm Single In−line Package with Vertical LF Type
- Cross−conduction Protection
- Integrated Bootstrap Diodes and Resistors
- These Devices are Pb−Free and are RoHS Compliant

Certification

- UL1557 (File number : E339285)

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Heat Pumps, Home Appliances

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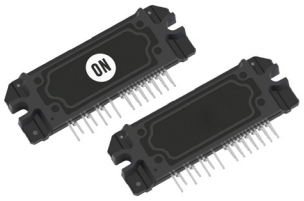
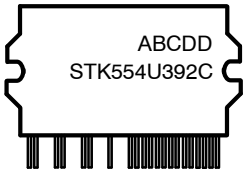


SIP29 62 x 21.8FP−1
CASE 127EZ

MARKING DIAGRAM



STK554U392C = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot code
Device marking is on package underside

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

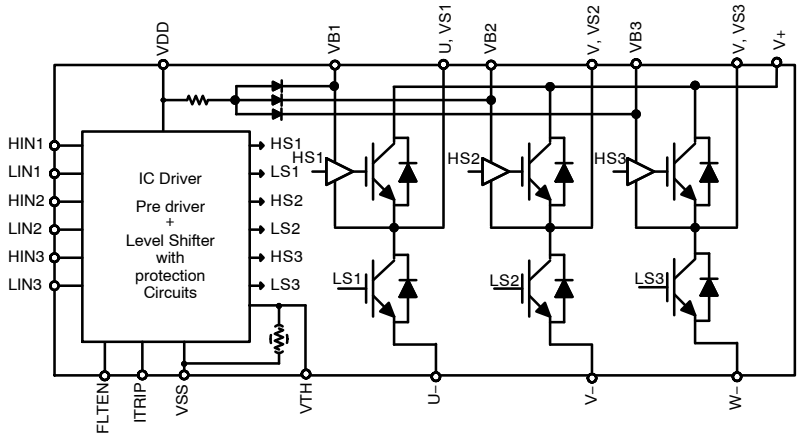


Figure 1. Functional Diagram

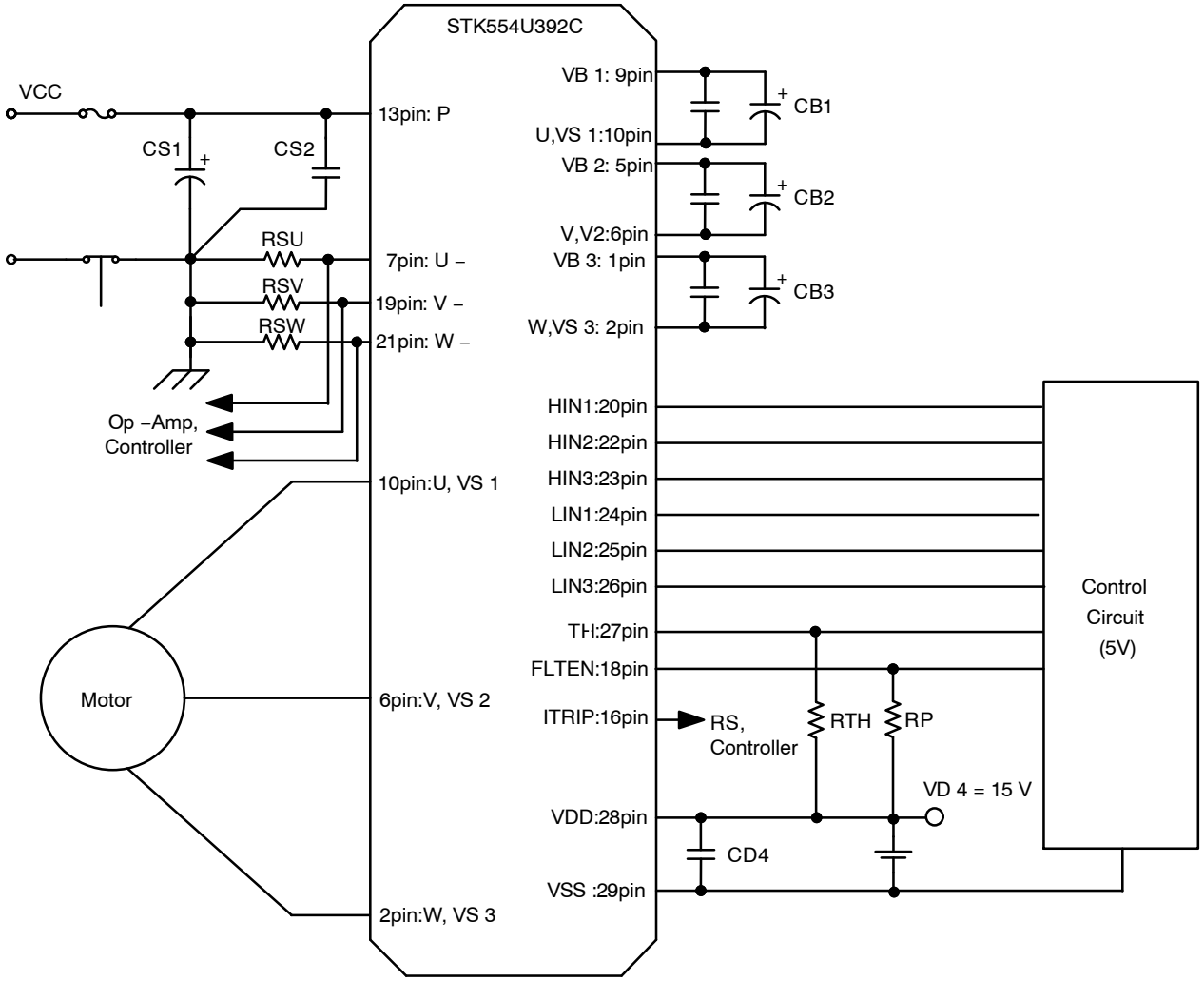


Figure 2. Application Schematic

Usage Precaution

1. It is essential that warning length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10 μF
2. The “FLTEN” terminal (Pin 18) is I/O terminal; Fault output / Enable input. It is used to indicate an internal fault condition of the module and also can be used to disable the module operation
3. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used
4. The pull−down resistor (:33 kΩ(typ)) is connected with the inside of the signal input terminal, but please connect the pull−down resistor(about 2.2 to 3.3 kΩ) outside to decrease the influence of the noise by wiring etc
5. As protection of IPM to the unusual current by a short circuit etc. it recommends installing shunt resistors and an over−current protection circuit outside. Moreover, for safety, a fuse on Vcc line is recommended
6. Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection
7. When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

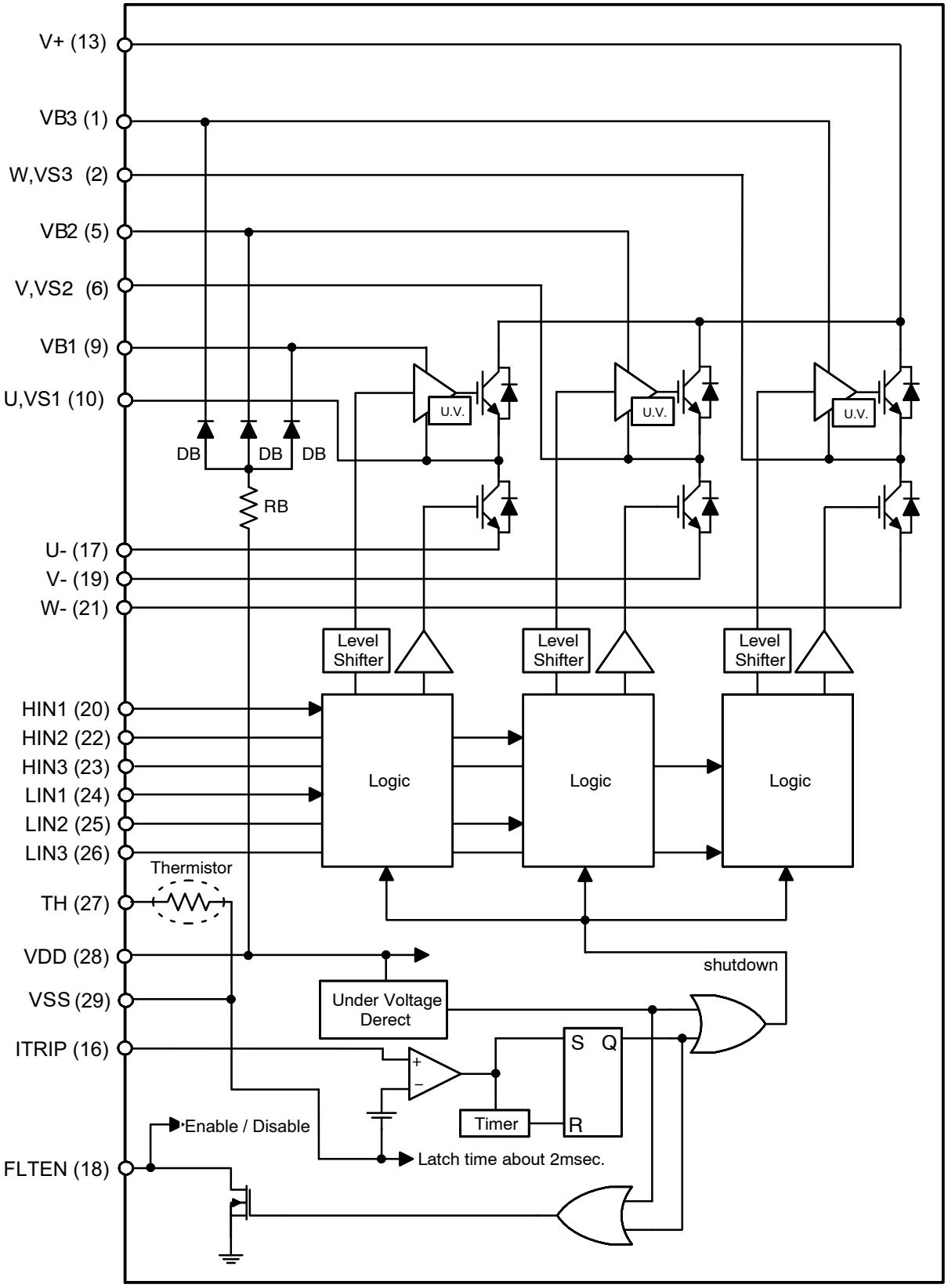


Figure 3. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3 − High Side Floating Supply Offset Voltage
5	VB2	High Side Floating Supply voltage 2
6	V,VS2	Output 2 − High Side Floating Supply Offset Voltage
9	VB1	High Side Floating Supply voltage 1
10	U,VS1	Output 1 − High Side Floating Supply Offset Voltage
13	V+	Positive Bus Input Voltage
16	ITRIP	Current protection pin
17	U−	Low Side Emitter Connection − Phase U
18	FLTEN	Enable input / Fault output
19	V−	Low Side Emitter Connection − Phase V
20	HIN1	Logic Input High Side Gate Driver − Phase U
21	W−	Low Side Emitter Connection − Phase W
22	HIN2	Logic Input High Side Gate Driver − Phase V
23	HIN3	Logic Input High Side Gate Driver − Phase W
24	LIN1	Logic Input Low Side Gate Driver − Phase U
25	LIN2	Logic Input Low Side Gate Driver − Phase V
26	LIN3	Logic Input Low Side Gate Driver − Phase W
27	TH	Thermistor output
28	VDD	+15 V Main Supply
29	VSS	Negative Main Supply

NOTE: Pins 3, 4, 7, 8, 11, 12, 14, 15 are not present.

Table 2. ABSOLUTE MAXIMUM RATINGS at T_C = 25°C (Note 1, 2)

Rating	Symbol	Conditions	Value	Unit
Supply Voltage	VCC	V+ to U−, V−, W−, surge < 500 V (Note 3)	450	V
Collector−emitter Voltage	VCE	V+ to U, V, W or U, V, W, to U−, V−, W−	600	V
Output Current	Io	V+, U−, V−, W−, U, V, W terminal current	+15	A
		V+, U−, V−, W−, U, V, W terminal current, Tc = 100°C	±8	A
Output Peak Current	Iop	V+, U−, V−, W−, U, V, W terminal current, P.W. = 1 ms	+30	A
Pre−driver Voltage	VD1, 2, 3, 4	VB1 to U, VB2 to V, VB3 to W, VDD to VSS (Note 4)	20	V
Input Signal Voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	−0.3 to VDD	V
FLTEN Terminal Voltage	VFLTEN	FLTEN terminal	−0.3 to VDD	V
Maximum Power Dissipation	Pd	IGBT per 1 channel	35	W
Junction Temperature	Tj	IGBT, FRD, Pre−Driver IC	150	°C
Storage Temperature	Tstg		−40 to +125	°C
Operating Case Temperature	Tc	IPM case	−40 to +100	°C
Tightening Torque		A screw part (Note 5)	0.9	Nm
Withstand Voltage	Vis	50 Hz sine wave AC 1 minute (Note 6)	2000	VRMS

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. Surge voltage developed by the switching operation due to the wiring inductance between + and U−(V−, W−) terminal.
4. VD1 = VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = VDD to VSS terminal voltage.
5. Flatness of the heat−sink should be less than −50 μm to +100 μm.
6. Test conditions : AC2500V, 1 second

Table 3. RECOMMENDED OPERATING RANGES at Tc = 25°C (Note 7)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	V+ to U−(V−,W−)	0	280	450	V
Pre−driver Supply Voltage	VD1, 2, 3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} (Note 7)	13.5	15	16.5	V
ON−state Input Voltage	VIN(ON)	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3	3.0	−	5.0	V
OFF−state Input Voltage	VIN(OFF)		0	−	0.3	
PWM Frequency	fPWM		1.0	−	20	kHz
Dead Time	DT	Turn−off to turn−on (external)	0.5	−	−	μs
Allowable Input Pulse Width	PWIN	ON and OFF	1.0	−	−	μs
Package Mounting Torque		'M3' type screw	0.6	−	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Pre−drive power supply (VD4 = 15 ±1.5 V) must have the capacity of Io = 20 mA (DC), 0.5 A (Peak).

Table 4. ELECTRICAL CHARACTERISTICS at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POWER OUTPUT SECTION						
Collector−emitter Leakage Current	V_{CE} = 600 V	I_{CE}	−	−	100	μA
Bootstrap Diode Reverse Current	VR(BD) = 600 V	IR(BD)	−	−	100	μA
Collector to Emitter Saturation Voltage	Ic = 15 A, Tj = 25°C	V_{CE}(sat)	−	1.7	2.4	V
	Ic = 8 A, Tj = 100°C		−	1.4	−	V
Diode Forward Voltage	IF = −15 A, Tj = 25°C	VF	−	1.9	2.6	V
	IF = −8 A, Tj = 100°C		−	1.4	−	V
Junction to Case Thermal Resistance	IGBT	θj−c(T)	−	−	3.5	°C/W
	FRD	θj−c(D)	−	−	5.0	
SWITCHING CHARACTER						
Switching Time	Io = 15 A Inductive load	t ON	−	0.45	−	μs
		t OFF	−	0.55	−	μs
Turn−on Switching Loss	Ic = 15 A, V^+ = 300 V, V_{DD} = 15 V, L=3.9 mH Tc = 25°C	Eon	−	410	−	μJ
Turn−off Switching Loss		Eoff	−	390	−	μJ
Total Switching Loss		Etot	−	800	−	μJ
Turn−on Switching Loss	Ic = 8 A, V^+ = 300 V, V_{DD} = 15 V, L = 3.9 mH Tc = 100°C	Eon	−	270	−	μJ
Turn−off Switching Loss		Eoff	−	280	−	μJ
Total Switching Loss		Etot	−	550	−	μJ
Diode Reverse Recovery Energy	I_F = 8 A, V^+ = 400 V, V_{DD} = 15 V, L = 3.9 mH, Tc = 100°C	Erec	−	12	−	μJ
Diode Reverse Recovery Time		Trr	−	54	−	ns
Reverse Bias Safe Operating Area	Io = 20°, VCE = 450 V	RBSOA	Full Square			
Short Circuit Safe Operating Area	VCE = 400 V, Tc = 100°C	SCSOA	4.0	−	−	μs
Allowable Offset Voltage Slew Rate	Between U(V,W) to U−(V−,W−)	dv/dt	−50	−	50	V/ns
CONTROL (PRE−DRIVER) SECTION						
Pre−driver Power Dissipation	VD1, 2, 3 = 15 V	ID	−	0.08	0.4	mA
	VD4 = 15 V		−	1.6	4.0	
High level Input Voltage	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to VSS	Vin H	2.5	−	−	V
Low level Input Voltage		Vin L	−	−	0.8	V
Logic 1 input Leakage Current	VIN = +3.3 V	I_{IN+}	−	100	143	μA

Table 4. ELECTRICAL CHARACTERISTICS at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V (continued)

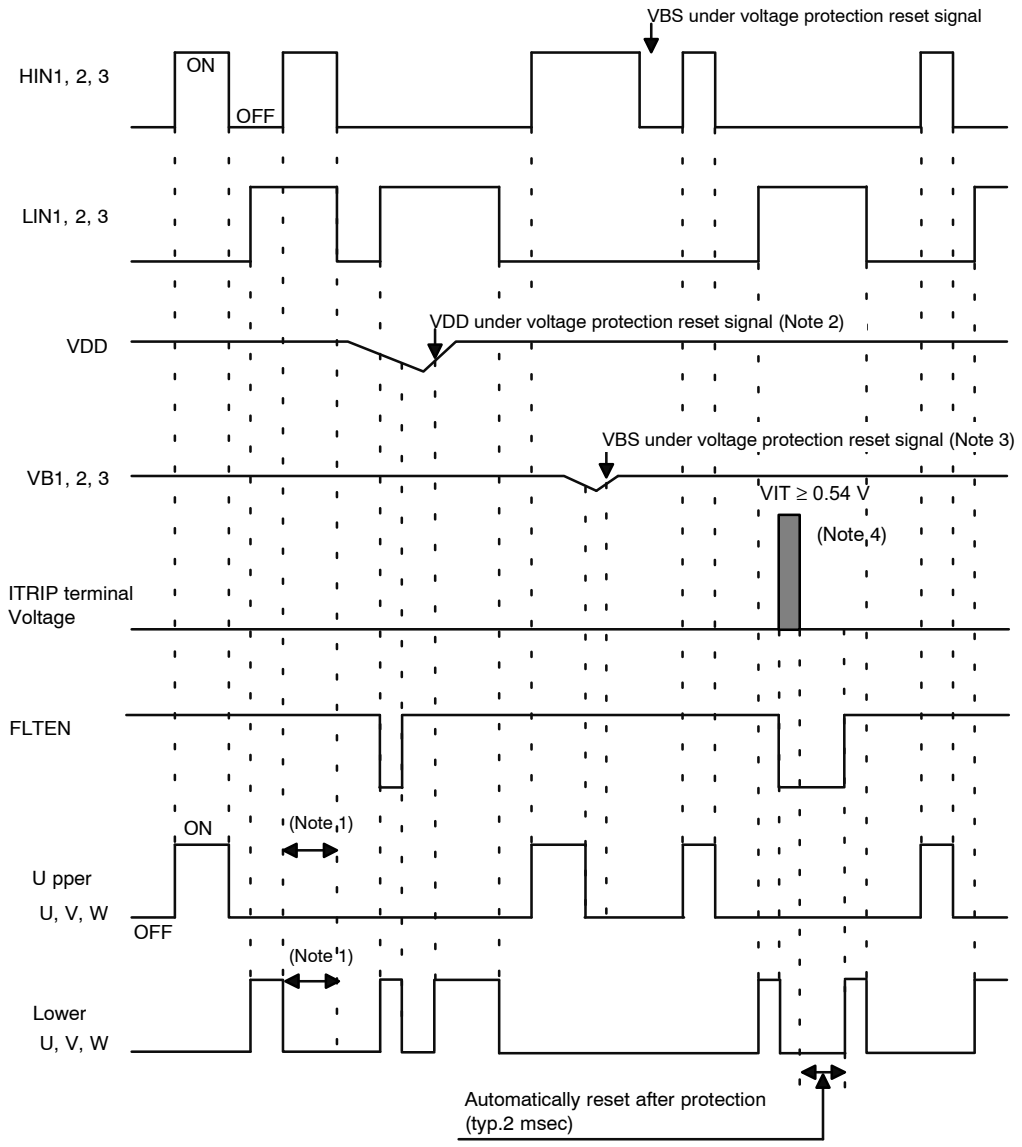
Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Logic 0 input Leakage Current	VIN = 0 V	I_{IN-}	−	−	2.0	μA
FLTEN Terminal Sink Current	FAULT: ON / VFLTEN = 0.1 V	IoSD	−	2.0	−	mA
FLTEN Clearance Delay Time	From time fault condition clear	FLTCLR	1.55	1.9	2.25	ms
FLTEN Threshold	VEN rising	VEN+	−	−	2.5	V
	VEN falling	VEN−	0.8	−	−	V
ITRIP Threshold Voltage	ITRIP(16) to VSS(29)	VITRIP	0.44	0.49	0.54	V
ITRIP to Shutdown Propagation Delay		t_{ITRIP}	340	550	800	ns
ITRIP Blanking Time		$t_{ITRIPBL}$	250	350		ns
V_{CC} and V_{BS} Supply Undervoltage Protection Reset		V_{CCUV+} V_{BSUV+}	10.5	11.1	11.7	V
V_{CC} and V_{BS} Supply Undervoltage Protection set		V_{CCUV-} V_{BSUV-}	10.3	10.9	11.5	V
V_{CC} and V_{BS} Supply Undervoltage Hysteresis		V_{CCUVH} V_{BSUVH}	0.14	0.2	−	V
Thermistor for Substrate Temperature Monitor	Resistance between TH(27) and VSS(29)	Rt	42.3	47	51.7	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Reference voltage is “VSS” terminal voltage unless otherwise specified.

APPLICATIONS INFORMATION

Input / Output Timing Chart



NOTES:
1. Shows the prevention of shoot−thru via control logic, however, more dead time must be added to account for switching delay externally.
2. When VDD decreases all gate output signals will go low and cut off all 6 IGBT outputs. When VDD rises the operation will resume immediately.
3. When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
4. When VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes 2 ms (typ) after over current condition is removed.

Figure 4. Input / Output Timing Chart

Table 5. LOGIC LEVEL TABLE

INPUT			OUTPUT			
HIN	**LIN**	**Itrip**	**High side IGBT**	**Low side IGBT**	**U,V,W**	**FLTEN**
H	L	L	ON	OFF	VP	OFF
L	H	L	OFF	ON	NU, NV, NW	OFF
L	L	L	OFF	OFF	High Impedance	OFF
H	H	L	OFF	OFF	High Impedance	OFF
X	X	H	OFF	OFF	High Impedance	ON

Table 6. THERMISTOR CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	44.6	47.0	49.4	kΩ
	R_{125}	Tc = 125°C	1.28	1.41	1.53	kΩ
B−Constant (25 to 50°C)	B	−	4010	4050	4091	K
Temperature Range	−	−	−40	−	+125	°C

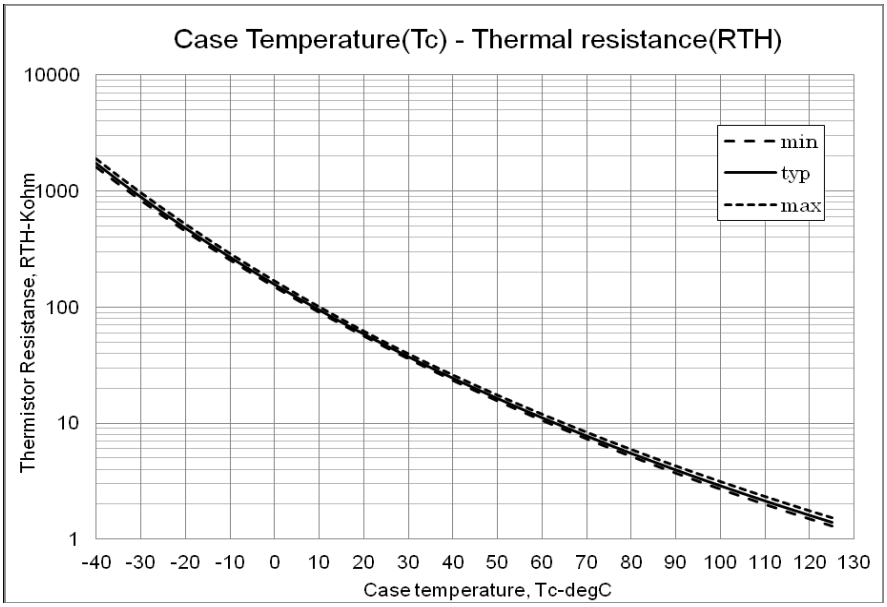
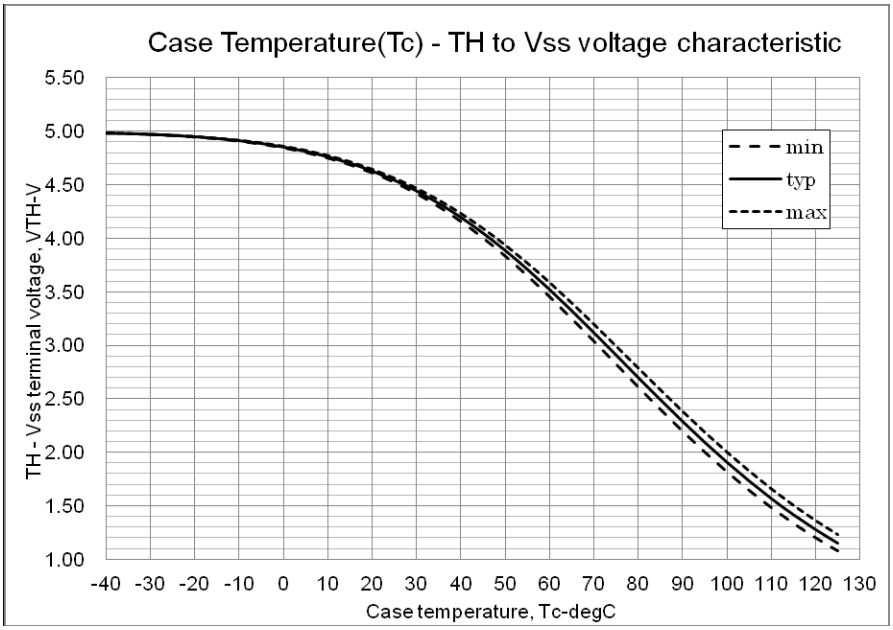


Figure 5. Thermistor Resistance versus Case Temperature



Condition:Pull−up resistor = 4.7 kphm, Pull−up voltage of TH = 5 V

Figure 6. Thermistor Voltage versus Case Temperature

FAULT Output

The FLTEN terminal is an open drain output requiring a pull−up resistor. If the pull−up voltage is 5 V, use a pull−up resistor with a value of 6.8 kΩ or higher. If the pull−up voltage is 15 V, use a pull−up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a VDD undervoltage or an overcurrent condition.

The terminal has a function of enable output, this pin is used to enable or shut down the built−in driver. If the voltage on the FLTEN pin rises above the ENABLE ON−state voltage, the output drivers are enabled. If the voltage on the ELTEN pin falls below the ENABLE OFF−state voltage, the drivers are disabled.

UnderVoltage Lockout Protection

If VDD goes below the VDD supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply undervoltage lockout rising threshold. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Overcurrent Protection

An over−current condition is detected if the voltage on the ITRIP pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 550ns, the FAULT output is switched on.

The over−current protection threshold should be set to be equal or lower to 2 times the module rated current (IO).

An additional fuse is recommended to protect against system level or abnormal over−current fault conditions.

Capacitors on High Voltage and V_{DD} Supplies

Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor.

Minimum Input Pulse Width

When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of bootstrap capacitor value.

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS : Bootstrap power supply.
  15 V is recommended
- QG : Total gate charge of IGBT at VBS = 15 V.
  132 nC
- UVLO : Falling threshold for UVLO.
  Specified as 12 V
- ID_{MAX} : High side drive consumption current.
  Specified as 400 μA
- t_{ONMAX} : Maximum ON pulse width of high side IGBT

Capacitance calculation formula

$CB = (QG + IDMAX \times tONMAX) / (VBS - UVLO)$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

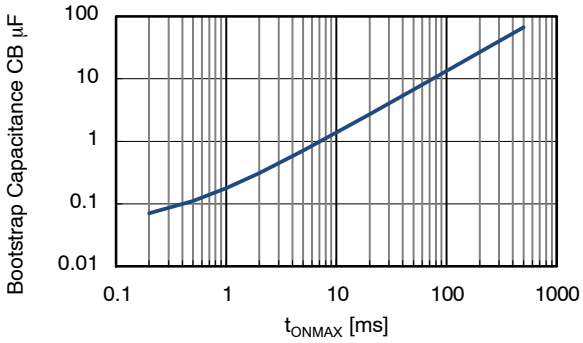


Figure 7. Bootstrap Capacitance versus t_{ONMAX}

Table 7. MOUNTING INSTRUCTIONS

Item	Recommended Condition
Pitch	56.0 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer The size is D : 7 mm, d : 3.2 mm and t : 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to +100 μm Screw holes must be countersunk No contamination on the heat sink surface that contacts IPM
Torque	Final tightening : 0.6 to 0.9 Nm Temporary tightening : 20 to 30 % of final tightening
Grease	Silicone grease Thickness : 100 to 200 μm Uniformly apply silicone grease to whole back

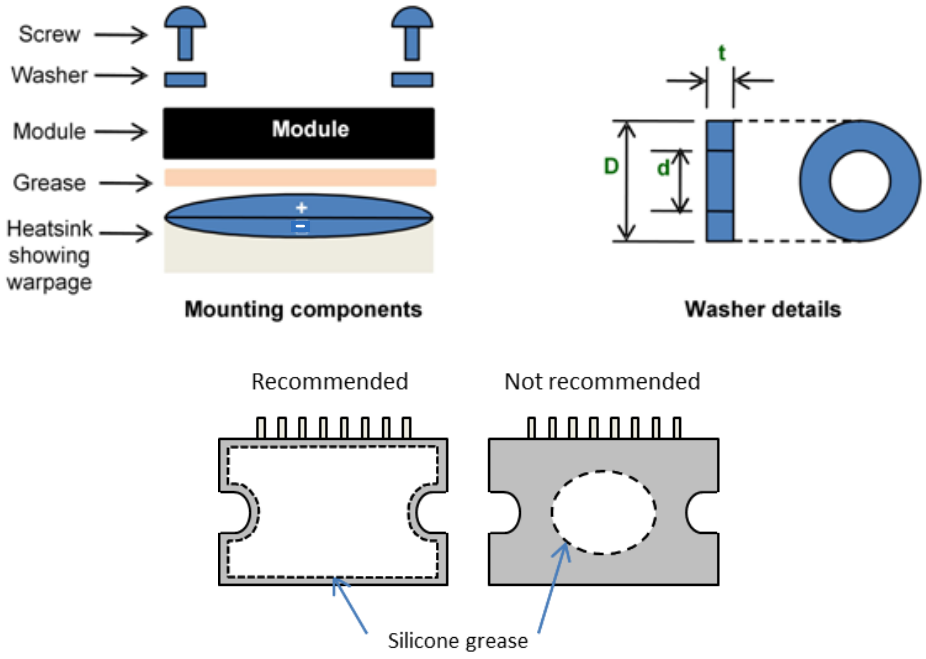


Figure 8. Module Mounting Details: Components; Washer Drawing; Need for Even Spreading of Thermal Grease

TEST CIRCUITS

- I_{CE}

	U+	V+	W+	U−	V−	W−
M	13	13	13	10	6	2
N	10	6	2	17	19	21

	U(DB)	V(DB)	W(DB)
M	9	5	1
N	29	29	29

NOTE: U+, V+, W+ : High side phase
U−, V−, W− : Low side phase

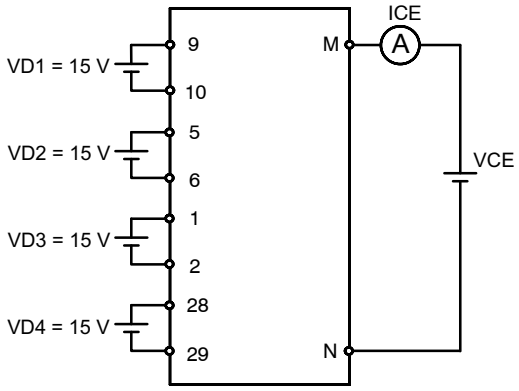


Figure 9. Test Circuit for I_{CE}

- V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	13	13	13	10	6	2
N	10	6	2	17	19	21
m	20	22	23	24	25	26

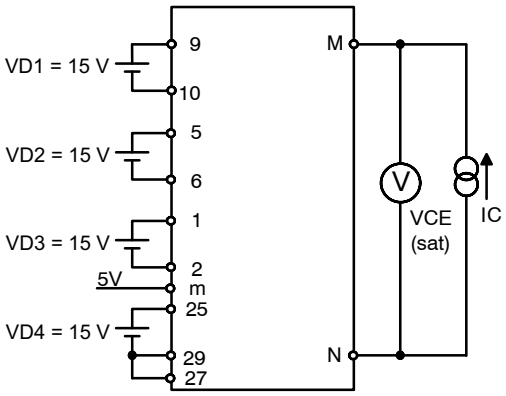


Figure 10. Test Circuit for V_{CE}(sat)

- V_F (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	13	13	13	10	6	2
N	10	6	2	17	19	21

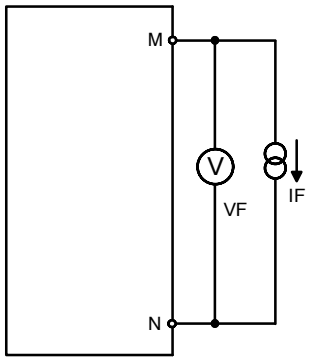


Figure 11. Test Circuit for V_F

- ID

	VD1	VD2	VD3	VD4
M	9	5	1	28
N	10	6	2	29

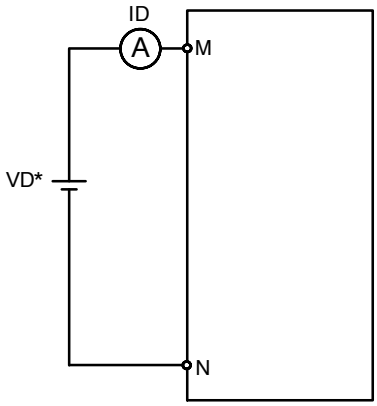
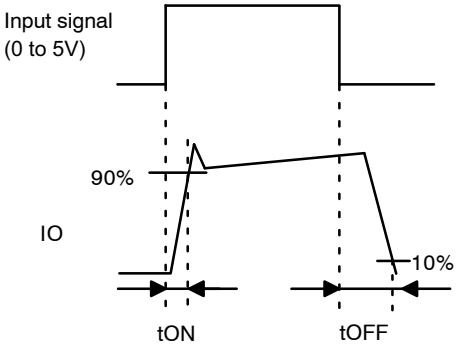


Figure 12. Test Circuit for ID

- Switching time (The circuit is a representative example of the low side U phase.)



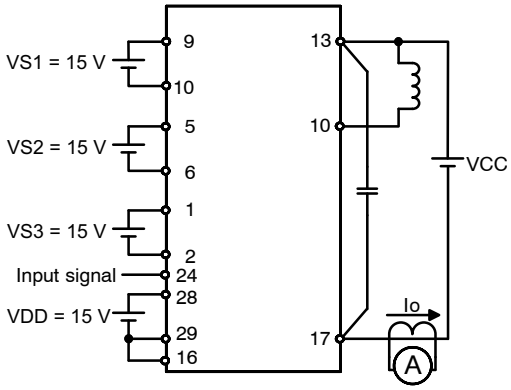
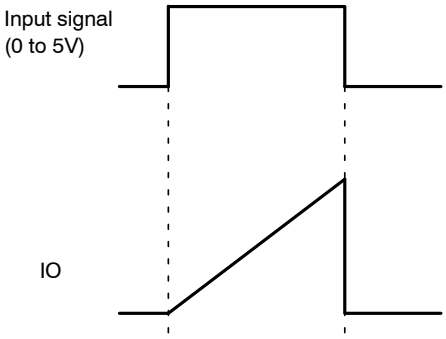


Figure 13. Switching Time Test Circuit

- RB−SOA (The circuit is a representative example of the lower side U phase.)



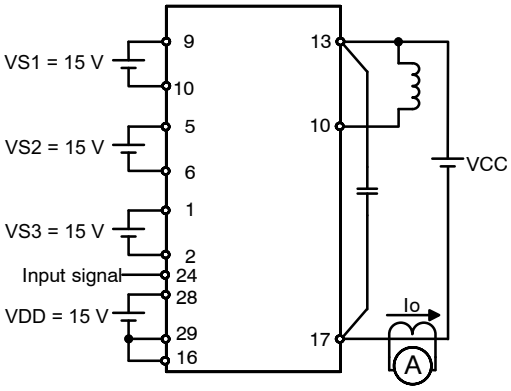


Figure 14. RB−SOA Test Circuit

ORDERING INFORMATION

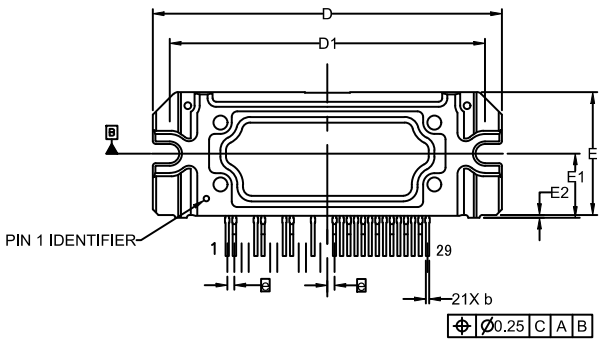
Device	Package	Shipping
STK554U392C−E	MODULE SIP29 62x21.8FP−1 Vertical Type (Pb−Free)	8 Units / Tube

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

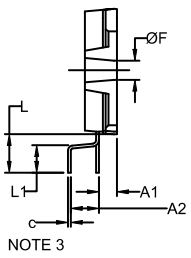
ON Semiconductor®

SIP29 62x21.8FP−1
CASE 127EZ
ISSUE O

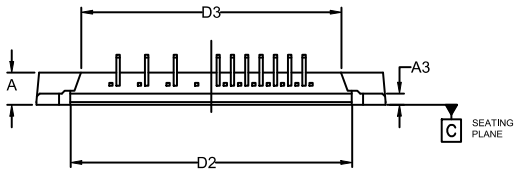
DATE 07 MAY 2018



TOP VIEW



END VIEW



SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. MISSING PINS ARE 3,4,7,8,11,12,14 AND 15.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	5.20	5.70	6.20
A1	2.70	3.20	3.70
A2	4.50	5.00	5.50
A3	1.50	2.00	2.50
b	0.55	0.60	0.80
c	0.45	0.50	0.70
D	61.50	62.00	62.50
D1	55.50	56.00	56.50
D2	49.50	50.00	50.50
D3	45.70	46.20	46.70
E	21.8 REF		
E1	11.4 REF		
E2	0.00	0.50	1.00
e	1.27 BSC		
F	2.90	3.40	3.90
L	6.30	6.80	7.30
L1	3.80	4.30	4.80

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