Nineteen Output Differential Buffer for PCIe Gen3 9DB1933

Recommended Application

19 output PCIe Gen3 zero-delay/fanout buffer

General Description

The 9DB1933 zero-delay buffer supports PCIe Gen3 requirements, while being backwards compatible to PCIe Gen2 and Gen1. The 9DB1933 is driven by a differential SRC output pair from an IDT 932S421, 932SQ420, or equivalent, main clock generator. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without Spread-Spectrum clocking.

Output Features

- 19 - 0.7V current mode differential HCSL output pairs

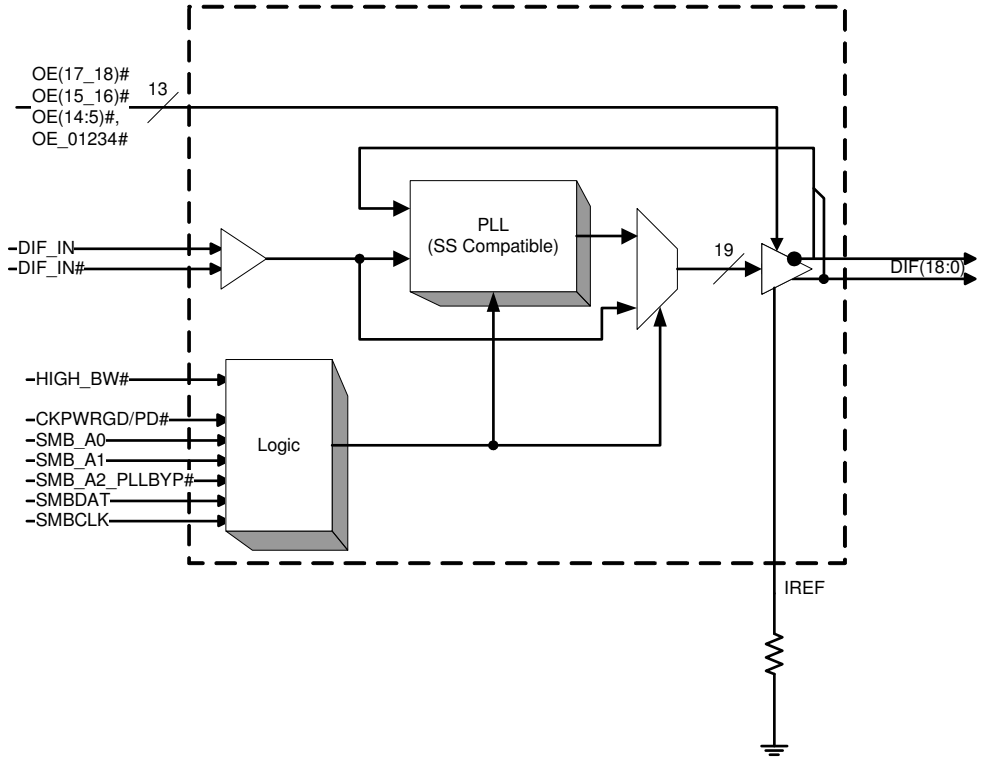
Features/Benefits

- 8 Selectable SMBus Addresses/Mulitple devices can share the same SMBus Segment
- 11 dedicated and 3 group OE# pins/Hardware control of the outputs
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled
- Supports undriven differential outputs in Power Down mode for power management

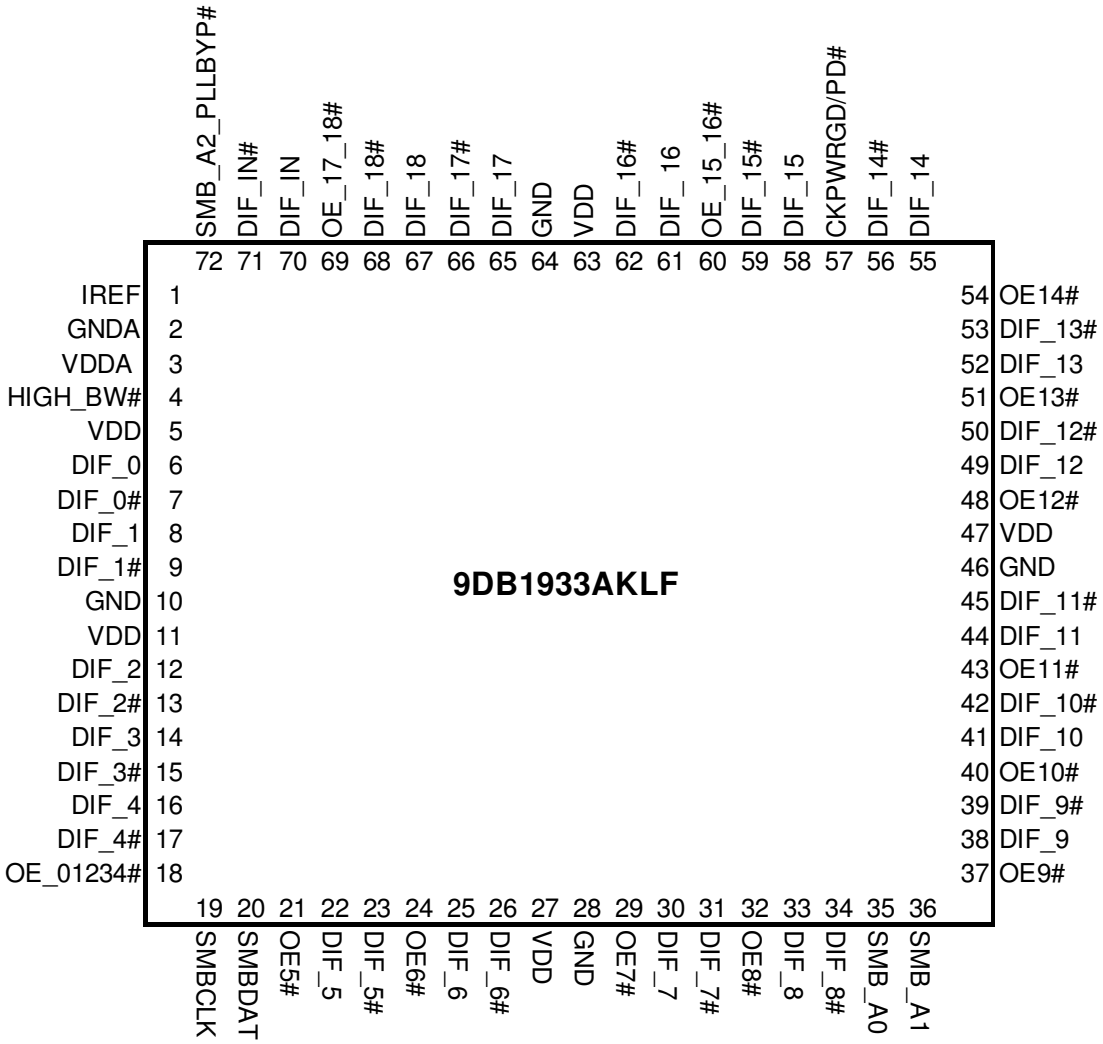
Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew < 150 ps
- PCIe Gen3 phase jitter < 1.0ps RMS

Functional Block Diagram



Pin Configuration



Power Down Functionality

INPUTS		OUTPUTS	PLL State
CKPWRGD/ PD#	DIF_IN/ DIF_IN#	DIF/DIF#	
1	Running	Running	ON
0	X	Hi-Z	OFF

Power Groups

Pin Number		Description
VDD	GND	
3	2	PLL, Analog
5,11,27,47,63	10,28,46,64	DIF clocks

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
2	GNDA	PWR	Ground pin for the PLL core.
3	VDDA	PWR	3.3V power for the PLL core.
4	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
5	VDD	PWR	Power supply, nominal 3.3V
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential Complementary clock output
8	DIF_1	OUT	0.7V differential true clock output
9	DIF_1#	OUT	0.7V differential Complementary clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_2	OUT	0.7V differential true clock output
13	DIF_2#	OUT	0.7V differential Complementary clock output
14	DIF_3	OUT	0.7V differential true clock output
15	DIF_3#	OUT	0.7V differential Complementary clock output
16	DIF_4	OUT	0.7V differential true clock output
17	DIF_4#	OUT	0.7V differential Complementary clock output
18	OE_01234#	IN	Active low input for enabling DIF pairs 0, 1, 2, 3 and 4. 1 =disable outputs, 0 = enable outputs
19	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
20	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
21	OE5#	IN	Active low input for enabling DIF pair 5. 1 =disable outputs, 0 = enable outputs
22	DIF_5	OUT	0.7V differential true clock output
23	DIF_5#	OUT	0.7V differential Complementary clock output
24	OE6#	IN	Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs
25	DIF_6	OUT	0.7V differential true clock output
26	DIF_6#	OUT	0.7V differential Complementary clock output
27	VDD	PWR	Power supply, nominal 3.3V
28	GND	PWR	Ground pin.
29	OE7#	IN	Active low input for enabling DIF pair 7. 1 =disable outputs, 0 = enable outputs
30	DIF_7	OUT	0.7V differential true clock output
31	DIF_7#	OUT	0.7V differential Complementary clock output
32	OE8#	IN	Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs
33	DIF_8	OUT	0.7V differential true clock output
34	DIF_8#	OUT	0.7V differential Complementary clock output
35	SMB_A0	IN	SMBus address bit 0 (LSB)
36	SMB_A1	IN	SMBus address bit 1

Pin Description (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	OE9#	IN	Active low input for enabling DIF pair 9. 1 =disable outputs, 0 = enable outputs
38	DIF_9	OUT	0.7V differential true clock output
39	DIF_9#	OUT	0.7V differential Complementary clock output
40	OE10#	IN	Active low input for enabling DIF pair 10. 1 =disable outputs, 0 = enable outputs
41	DIF_10	OUT	0.7V differential true clock output
42	DIF_10#	OUT	0.7V differential Complementary clock output
43	OE11#	IN	Active low input for enabling DIF pair 11. 1 =disable outputs, 0 = enable outputs
44	DIF_11	OUT	0.7V differential true clock output
45	DIF_11#	OUT	0.7V differential Complementary clock output
46	GND	PWR	Ground pin.
47	VDD	PWR	Power supply, nominal 3.3V
48	OE12#	IN	Active low input for enabling DIF pair 12. 1 =disable outputs, 0 = enable outputs
49	DIF_12	OUT	0.7V differential true clock output
50	DIF_12#	OUT	0.7V differential Complementary clock output
51	OE13#	IN	Active low input for enabling DIF pair 13. 1 =disable outputs, 0 = enable outputs
52	DIF_13	OUT	0.7V differential true clock output
53	DIF_13#	OUT	0.7V differential Complementary clock output
54	OE14#	IN	Active low input for enabling DIF pair 14. 1 =disable outputs, 0 = enable outputs
55	DIF_14	OUT	0.7V differential true clock output
56	DIF_14#	OUT	0.7V differential Complementary clock output
57	CKPWRGD/PD#	IN	A rising edge samples latched inputs and release Power Down Mode, a low puts the part into power down mode and tristates all outputs.
58	DIF_15	OUT	0.7V differential true clock output
59	DIF_15#	OUT	0.7V differential Complementary clock output
60	OE_15_16#	IN	Active low input for enabling DIF pair 15 and 16. 1 = tri-state outputs, 0 = enable outputs
61	DIF_ 16	OUT	0.7V differential true clock output
62	DIF_16#	OUT	0.7V differential Complementary clock output
63	VDD	PWR	Power supply, nominal 3.3V
64	GND	PWR	Ground pin.
65	DIF_17	OUT	0.7V differential true clock output
66	DIF_17#	OUT	0.7V differential Complementary clock output
67	DIF_18	OUT	0.7V differential true clock output
68	DIF_18#	OUT	0.7V differential Complementary clock output
69	OE_17_18#	IN	Active low input for enabling DIF pair 17, 18. 1 = tri-state outputs, 0 = enable outputs
70	DIF_IN	IN	0.7 V Differential TRUE input
71	DIF_IN#	IN	0.7 V Differential Complementary Input
72	SMB_A2_PLLBYP#	IN	SMBus address bit 2. When Low, the part operates as a fanout buffer with the PLL bypassed. When High, the part operates as a zero-delay buffer (ZDB) with the PLL operating. 0 = fanout mode (PLL bypassed), 1 = ZDB mode (PLL used)

Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Parameters

TA = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	10		166	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	90	100	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance		2.5	6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		1.000	1.8	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

Electrical Characteristics - Clock Input Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	2	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on			20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	789	850	mV	1
Voltage Low	VLow		-150	45	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		834	1150	mV	1
Min Voltage	Vmin		-300	17			1
Vswing	Vswing	Scope averaging off	300	744		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	380	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		24	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics - Current Consumption

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, C_L = Full load;		427	500	mA	1
Powerdown Current	$I_{DD3.3PDZ}$	All differential pairs tri-stated		32	40	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Output Duty Cycle, Jitter, Skew and PLL Characterisitics

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	3	4	MHz	1
		-3dB point in Low BW Mode	0.7	1	1.4	MHz	1
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain		1.4	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	49.5	55	%	1,2
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-2	1	2	%	1,2,5
Skew, Input to Output	t_{pdBYP}	Bypass Mode, nominal value @ 25°C, 3.3V, V_T = 50%	2500	3700	4500	ps	1,2,4
	t_{pdPLL}	PLL Mode, nominal value @ 25°C, 3.3V, V_T = 50%	100	300	500	ps	1,2,3
DIF_IN, DIF [x:0]	Δt_{pd_BYP}	Input-to-Output Skew Variation in Bypass mode (over specified voltage / temperature operating ranges)		|500|	|600|	ps	1,2,4,6, 7,8,9, 13
DIF_IN, DIF [x:0]	Δt_{pd_PLL}	Input-to-Output Skew Variation in PLL mode (over specified voltage / temperature operating ranges)		|250|	|350|	ps	1,2,3,6, 7,8,9, 13
DIF[X:0]	t_{JPH}	Differential Phase Jitter (RMS Value)		2	10	ps	1,7,10
DIF[X:0]	$t_{SSTERROR}$	Differential Spread Spectrum Tracking Error (peak to peak)		40	80	ps	1,7,12
Skew, Output to Output	t_{sk3}	V_T = 50%		100	150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		40	50	ps	1,2
		Additive Jitter in Bypass Mode		25	50	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production. C_{LOAD} = 2pF

[2] Measured from differential cross-point to differential cross-point

[3] PLL mode Input-to-Output skew is measured at the first output edge following the corresponding input.

[4] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[5] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[6] VT = 50% of Vout

[7] This parameter is deterministic for a given device

[8] Measured with scope averaging on to find mean value.

[9] Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.

[10] This parameter is measured at the outputs of two separate 9DB1933 devices driven by a single main clock. The 9DB1933's must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the

[11] t is the period of the input clock

[12] Differential spread spectrum tracking error is the difference in spread spectrum tracking between two 9DB1933 devices This parameter is measured at the outputs of two separate 9DB1933 devices driven by a single main clock in Spread Spectrum mode. The 9DB1933's must be set to high bandwidth. The spread spectrum characteristics are: maximum of 0.5%, 30-33KHz modulation frequency, linear

[13] This parameter is an absolute value. It is not a double-sided figure.

Electrical Characteristics - PCIe Phase Jitter Parameters

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1		44	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.4	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.5	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.6	1	ps (rms)	1,2,4
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1}$	PCIe Gen 1		3	5	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.02	0.1	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.2	0.3	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.04	0.1	ps (rms)	1,2,4

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
DIF	DIF 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2,3

Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
DIF	DIF 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The 9DB1933 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, PLL or Bypass mode

DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

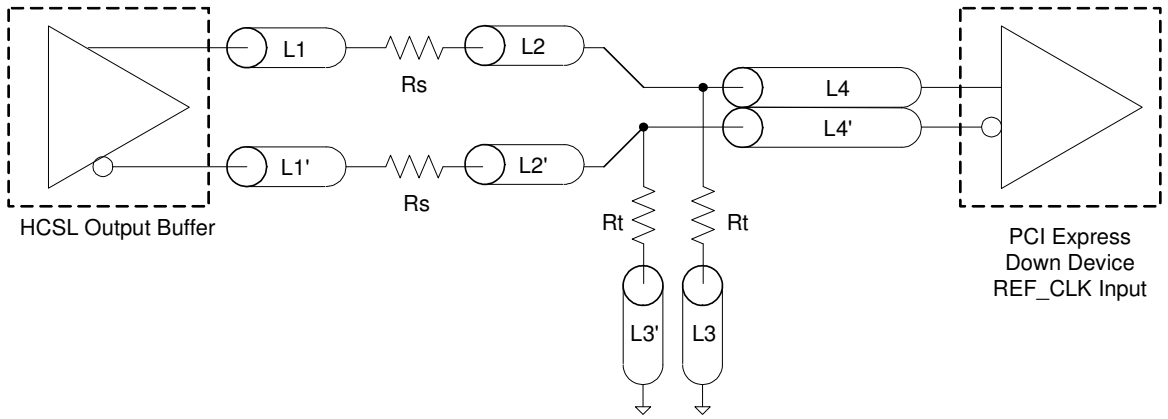
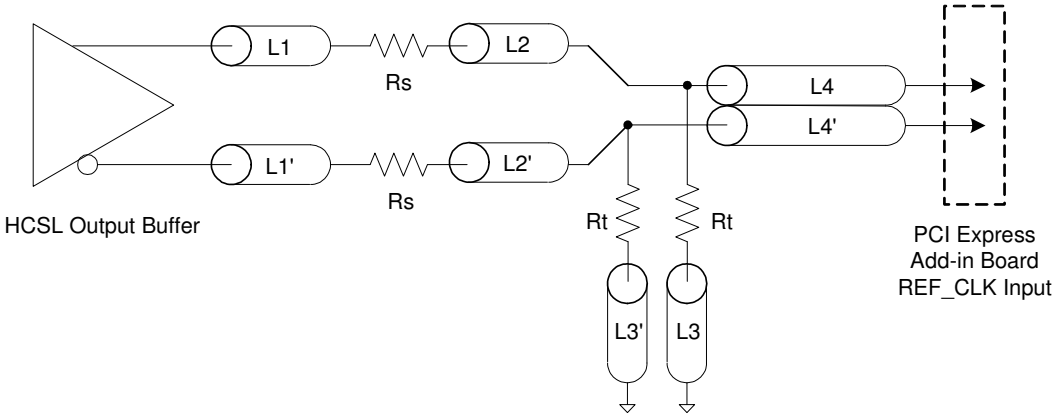


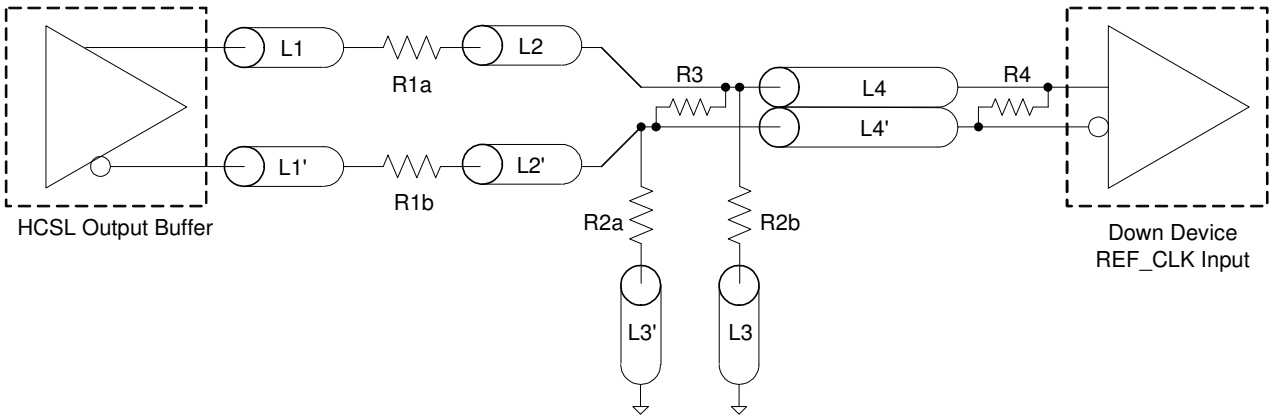
Figure 2: PCI Express Connector Routing



Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

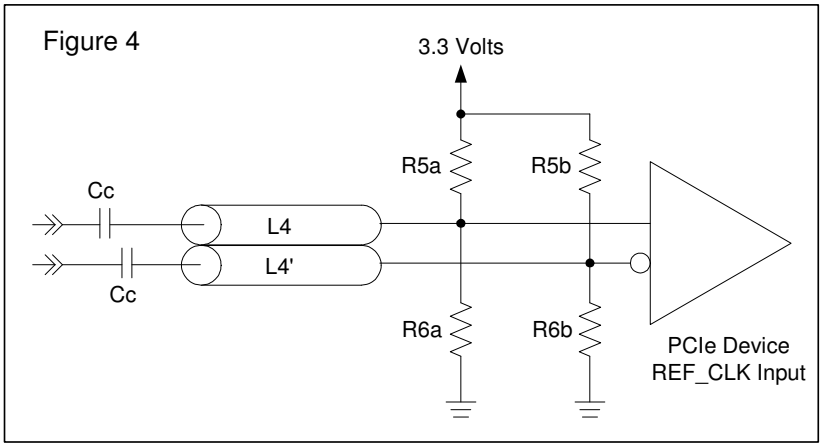
R1a = R1b = R1
R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



General SMBus serial interface information for the 9DB1933

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD (h)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(h)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $DC_{(h)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $DC_{(h)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $DD_{(h)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Note: Addresses show assumes pin 29 is low.

SMBusTable: Reserved Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Reserved		R			1
Bit 6	-	Reserved		R			1
Bit 5	-	Reserved		R			1
Bit 4	-	Reserved		R			1
Bit 3	-	Reserved		R			1
Bit 2	-	Reserved		R			0
Bit 1	-	Reserved		R			1
Bit 0	-	Reserved		R			1

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DIF_7	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_6	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_5	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_4	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_3	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_2	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_1	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_0	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output and PLL BW Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	see note	PLL_BW# adjust		RW	High BW	Low BW	**1**
Bit 6	see note	BYPASS# test mode / PLL		RW	Bypass	PLL	**1**
Bit 5		DIF_13	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_12	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_11	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_10	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_9	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_8	Output Control	RW	Hi-Z	Enable	1

Note: Bit 7 is wired OR to the HIGH_BW# input, any 0 selects High BW

Note: Bit 6 is wired OR to the SMB_A2_PLLBYP# input, any 0 selects Fanout Bypass mode

SMBusTable: Output Enable Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Readback - OE9# Input		R	Readback		X
Bit 6		Readback - OE8# Input		R	Readback		X
Bit 5		Readback - OE7# Input		R	Readback		X
Bit 4		Readback - OE6# Input		R	Readback		X
Bit 3		Readback - OE5# Input		R	Readback		X
Bit 2		Readback - OE_01234# Input		R	Readback		X
Bit 1	8	Readback - HIGH_BW# In		R	Readback		X
Bit 0	72	Readback - SMB_A2_PLLBYP# In		R	Readback		X

SMBusTable: Output Enable Readback Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	69	Readback - OE17_18# Input		R	Readback		X
Bit 6	60	Readback - OE15_16# Input		R	Readback		X
Bit 5	Reserved						0
Bit 4	54	Readback - OE14# Input		R	Readback		X
Bit 3	51	Readback - OE13# Input		R	Readback		X
Bit 2	48	Readback - OE12# Input		R	Readback		X
Bit 1	43	Readback - OE11# Input		R	Readback		X
Bit 0	40	Readback - OE10# Input		R	Readback		X

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID (194 Decimal or C2 Hex)

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		RW	Reserved		1
Bit 6	-	Device ID 6		RW	Reserved		1
Bit 5	-	Device ID 5		RW	Reserved		0
Bit 4	-	Device ID 4		RW	Reserved		0
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		0
Bit 1	-	Device ID 1		RW	Reserved		1
Bit 0	-	Device ID 0		RW	Reserved		0

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

SMBusTable: Output Control Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					1
Bit 6		RESERVED					X
Bit 5		RESERVED					X
Bit 4		DIF_18	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_17	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_16	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_15	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_14	Output Control	RW	Hi-Z	Enable	1

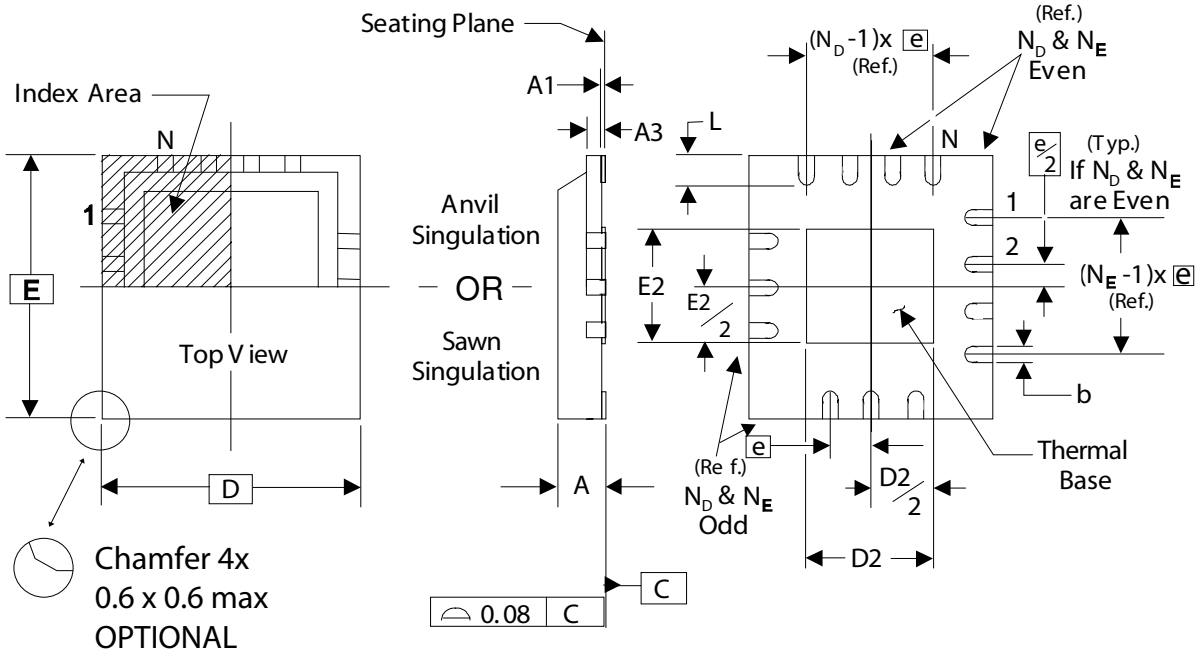
SMBusTable: Reserved Register

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					1
Bit 1		RESERVED					0
Bit 0		RESERVED					1

SMBus Address Mapping

SMBus Address (Hex)	Main Clock (CKxxx)	9DB233	9DB433	9DB633	9DB833	9DB1233	9DB1933
D0							✓
D2	✓						✓
D4		✓		✓		✓	✓
D6						✓	✓
D8			✓		✓		✓
DA			✓		✓		✓
DC			✓		✓	✓	✓
DE							✓

Note: ✓ Indicates Bypass Mode. PLL is OFF.



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	72L
N	72
N_D	18
N_E	18

DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	10.00 x 10.00	
D2 MIN. / MAX.	5.75	6.15
E2 MIN. / MAX.	5.75	6.15
L MIN. / MAX.	0.3	0.5

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DB1933AKLF	Tubes	72-pin MLF	0 to +70°C
9DB1933AKLFT	Tape and Reel	72-pin MLF	0 to +70°C

"LF" after the package code denotes the Pb-Free configuration, RoHS compliant.
"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Who	Description	Page #
0.1	7/7/2010	RDW	Initial release	-
A	7/12/2010	RDW	1. Updated 'PWD' to 'Default' in SMBus column headings 2. Updated electrical tables with char data 3. Added SMBusAddressing Table to page 15	5-8,13-15

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