Description

The F1490 is a high gain, two-stage RF Amplifier designed to operate within the 1.8GHz to 5.0GHz frequency range. Using a single 5V power supply, the F1490 provides two selectable gain modes (35.5dB and 39.5dB), 2.5dB of Noise Figure and 24dBm OP1dB at 2.6GHz.

The F1490 is packaged in a 3 × 3 mm, 16-pin QFN package, with matched 50Ω input and output impedances for ease of integration into the signal path.

Competitive Advantage

- Combines a two-stage RF amplifier in a single, compact 3 × 3 mm QFN package
- Excellent performance over exceptionally wide bandwidths
- Two selectable gain modes
- Low current consumption

Typical Applications

- 5G Sub-6GHz massive MIMO
- Wireless infrastructure base stations
- FDD or TDD systems
- Point-to-point infrastructure
- Public safety infrastructure
- Military handhelds
- Repeaters and DAS
- General purpose RF

Features

- RF range: 1.8GHz to 5.0GHz
- 39.5dB typical gain at 2.6GHz in high gain mode
- 35.5dB typical gain at 2.6GHz in low gain mode
- 2.5dB NF at 2.6GHz
- 50Ω single-ended input and output impedances
- 5V power supply
- 75mA quiescent current consumption
- 1.8V logic compatible Standby Mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +115°C
- 3 × 3 mm 16-VFQFPN package

Block Diagram

Figure 1. Block Diagram

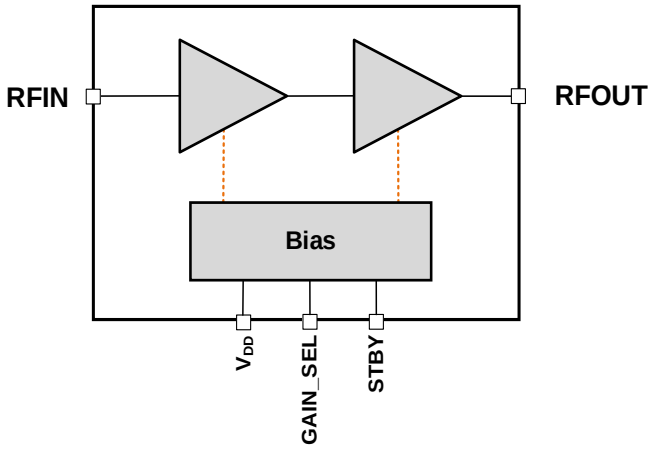

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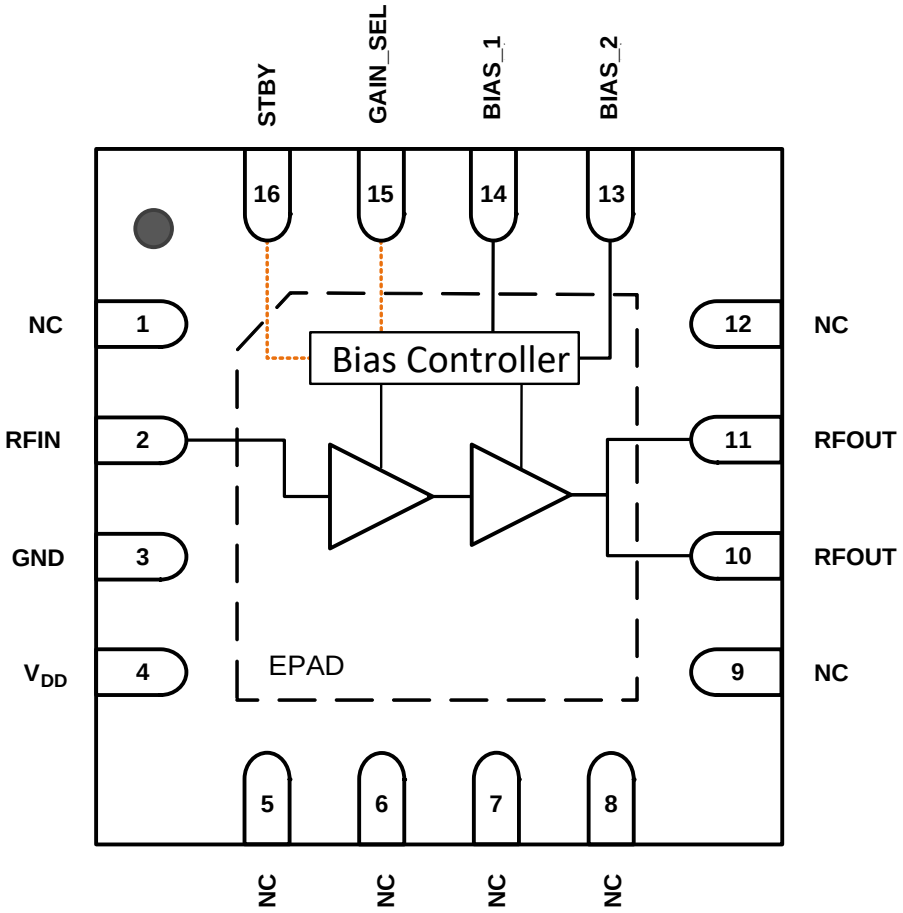
Figure 2. Pin Assignments – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 5, 6, 7, 8, 9, 12	NC	No internal connection. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.
2	RFIN	RF input internally matched to 50Ω. Must use an external DC block.
3	GND	Internally grounded. This pin can be left unconnected, or it can be connected to ground (recommended).
4	VDD	Pull up to V_{DD} through inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the device with a DC voltage, there is also an RF signal present.
10, 11	RFOUT	RF output. Pull up to V_{DD} through inductor. Must use external DC block.
13	BIAS_2	Connect via resistor to a common V_{DD} and use bypass capacitors. Place network as close to the pin as possible.
14	BIAS_1	Connect via resistor to a common V_{DD} and use bypass. Place network as close to the pin as possible.
15	GAIN_SEL	Gain Selection pin. Logic HIGH selects High Gain Mode operation. Logic LOW (or if the pin is left unconnected or grounded) selects Low Gain Mode operation. Pin is 1.8V logic compatible.
16	STBY	Standby pin. With Logic LOW applied to this pin, the amplifier is powered off. With Logic HIGH applied to this pin (or if the pin is left unconnected), the part is in full operation mode. Pin is 1.8V logic compatible.
	— EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
V_{DD} to GND	V_{DD}	-0.3	+6.0	V
STBY	V_{CTL}	-0.3	Lower of (5.0, V_{CC} + 0.25)	V
BIAS_1 (into pin)	I_{BIAS_1}		1.5	mA
BIAS_2 (out of pin)	I_{BIAS_2}		3	mA
RFIN externally applied DC voltage	V_{RFIN}	-0.5	+0.5	V
RFOUT externally applied DC voltage	V_{RFOUT}	-0.5	+8	V
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 115˚C, input / output VSWR < 2:1 based on a 50Ω system. Standby = logic HIGH: ON state. [a]	$P_{MAX\_IN\_ON}$		22	dBm
Maximum CW Input Power applied for 24 hour. V_{CC} = 5V, T_{EPAD} = 115˚C, input / output VSWR < 2:1 based on a 50Ω system. Standby = logic LOW: OFF state.[a]	$P_{MAX\_IN\_OFF}$		22	
Junction Temperature	T_{JMAX}		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		1000	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		500	V

[a] Exposure to these maximum RF levels can result in significantly higher I_{cc} current draw due to overdriving the amplifier stages.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage	V_{DD}		4.75	5	5.25	V
Operating Temperature Range	T_{EPAD}	Exposed Paddle	-40		+115	°C
RF Frequency Range [a]	f_{RF}	2GHz Tuning Set	1.8		2.2	GHz
		2.5GHz Tuning Set	2.3		2.7	
		3.55GHz Tuning Set	3.3		3.8	
		4.0GHz Tuning Set	3.8		4.2	
		4.7GHz Tuning Set	4.4		5.0	
RFIN Port Impedance	Z_{RFI}	Single Ended		50		Ω
RFOUT Port Impedance	Z_{RFO}	Single Ended		50		Ω

[a] Using external matching, gain flatness is optimized from 1.8GHz to 2.2GHz (2GHz Tuning Set), 2.3GHz to 2.7GHz (2.5GHz Tuning Set), 3.3GHz to 3.8GHz (3.55GHz Tuning Set), 3.8GHz to 4.2GHz (4.0GHz Tuning Set), and 4.4GHz to 5.0GHz (4.7GHz Tuning Set).

Electrical Characteristics – General

Specifications apply when operated as a TX amplifier with tuning optimized for desired band of interest, V_{DD} = +5.0V, T_{EPAD} = +25°C, STBY = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics – General

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High	V_{IH}		*1.17* [a]		V_{DD}	V
Logic Input Low	V_{IL}		-0.3		*0.63*	V
Logic Current	I_{IH}, I_{IL}	STBY pin. V_{CTL} = 1.8 V		40		µA
Quiescent Current [b]	I_{DD_QH}	High Gain Mode		75	98	mA
	I_{DD_QL}	Low Gain Mode		75	*98*	
Standby Current	I_{CC_STBY}	STBY = LOW		2.5		mA
Standby Switching Time	t_{ON}	50% STBY control to within 0.5dB of the on-state final gain value		250		ns
	t_{OFF}	50% STBY control to I_{CC} < 10mA		250		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] I_{DD} refers to the nominal small signal bias current.

Electrical Characteristics – 2.3GHz to 2.7GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 2.3GHz to 2.7GHz band, V_{DD} = +5.0V, f_{RF} = 2.6GHz, T_{EPAD} = +25°C, GAIN_SEL = LOW, STBY = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 5. Electrical Characteristics – 2.3GHz to 2.7GHz (Low Gain Mode unless Otherwise Specified)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Gain	G	Low Gain Mode	*33*[a]	35.5		dB
		High Gain Mode		39.5		
Gain Flatness	G_{FLAT}	f_{RF} = 2.3GHz to 2.7GHz		0.7		dB
Gain Variation Over Temperature	G_{TEMP}	T_{EPAD} = -40°C to +115°C, referenced to T_{EPAD} = 25°C		+1.5 / -1.0		dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW $P_{IN} \leq$ -15dBm f_{RF} = 2.3GHz to 2.7GHz		-39		dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 2.3GHz to 2.7GHz		18		dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 2.3GHz to 2.7GHz		12		dB
Reverse Isolation	ISO_{REV}			55		dB
Noise Figure	NF			2.5		dB
Output Third Order Intercept Point	OIP3	P_{OUT} = +4dBm / tone 1MHz tone separation		38		dBm
		P_{OUT} = +4dBm / tone 1MHz tone separation V_{DD} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	30			
Output 1dB Compression Point	OP1dB			24		dBm
		V_{DD} = 4.75V to 5.25V T_{EPAD} = -40°C to +115°C	21			

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Electrical Characteristics – 3.3GHz to 3.8GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 3.3GHz to 3.8GHz band, V_{DD} = +5.0V, f_{RF} = 3.55GHz, T_{EPAD} = +25°C, GAIN_SEL = LOW, STBY = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 6. Electrical Characteristics – 3.3GHz to 3.8GHz (Low Gain Mode unless Otherwise Specified)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Gain	G	Low Gain Mode		36		dB
		High Gain Mode		40		
Gain Flatness	G_{FLAT}	f_{RF} = 3.3GHz to 3.8GHz		0.7		dB
Gain Variation Over Temperature	G_{TEMP}	T_{EPAD} = -40°C to +115°C, referenced to T_{EPAD} = 25°C		+1.9 / -1.7		dB
STBY Mode Gain	G_{STBY}	STBY = logic LOW $P_{IN} \leq$ -15dBm f_{RF} = 3.3GHz to 3.8GHz		-43		dB
RF Input Return Loss	RL_{RFIN}	f_{RF} = 3.3GHz to 3.8GHz		11		dB
RF Output Return Loss	RL_{RFOUT}	f_{RF} = 3.3GHz to 3.8GHz		10		dB
Reverse Isolation	ISO_{REV}			55		dB
Noise Figure	NF			2.8		dB
Output Third Order Intercept Point	OIP3	P_{OUT} = +4dBm / tone 1MHz tone separation		34		dBm
Output 1dB Compression Point	OP1dB			23		dBm

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	55.2	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC_BOT}	8.175	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions

Unless otherwise stated the typical operating graphs were measured under the following conditions:

- V_{DD} = 5.0V
- STBY = HIGH
- GAIN_SEL = LOW
- T_{EPAD} = +25°C
- f_{RF} = 2.0GHz
- f_{RF} = 2.6GHz
- f_{RF} = 3.55GHz
- f_{RF} = 4.0GHz
- f_{RF} = 4.7GHz
- Z_S = Z_L = 50Ω Single Ended
- Pout = 4dBm/tone and 1MHz Tone Spacing for OIP3

Typical Performance Characteristics (Band 2p5 – 2.3GHz to 2.7GHz)

Figure 3. Gain - Low Gain Mode

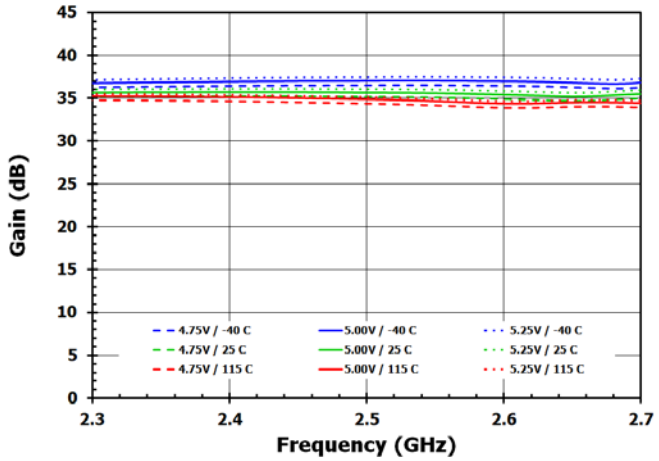


Figure 4. Gain - High Gain Mode

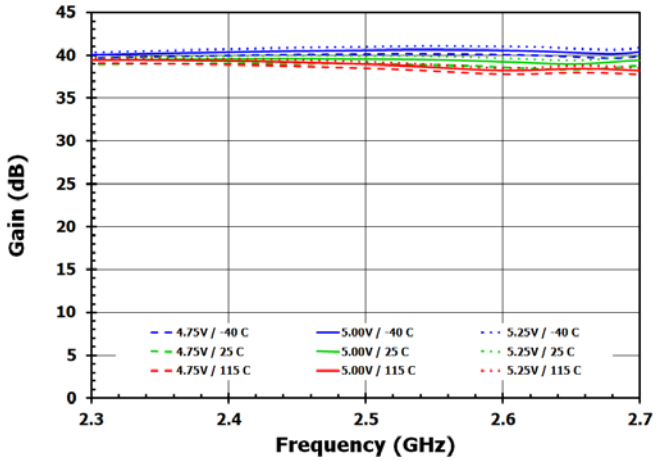


Figure 5. Input Return Loss - Low Gain Mode

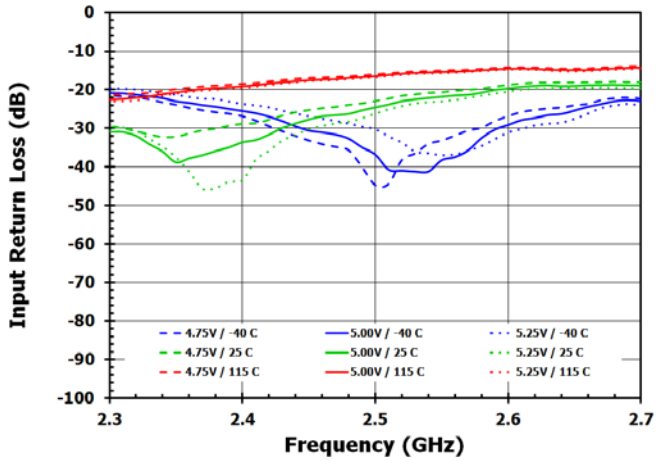


Figure 6. Input Return Loss - High Gain Mode

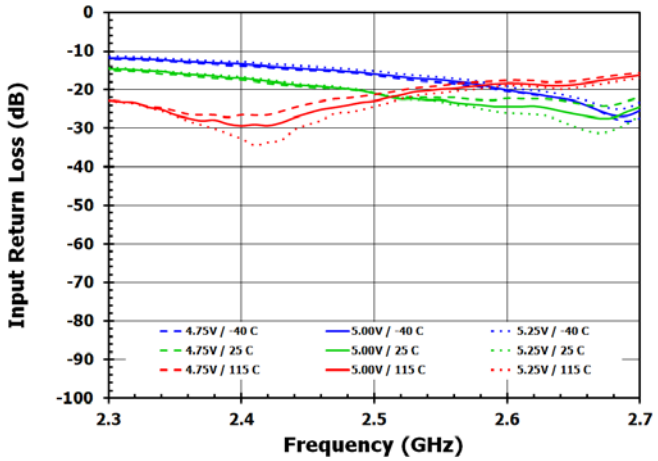


Figure 7. Output Return Loss - Low Gain Mode

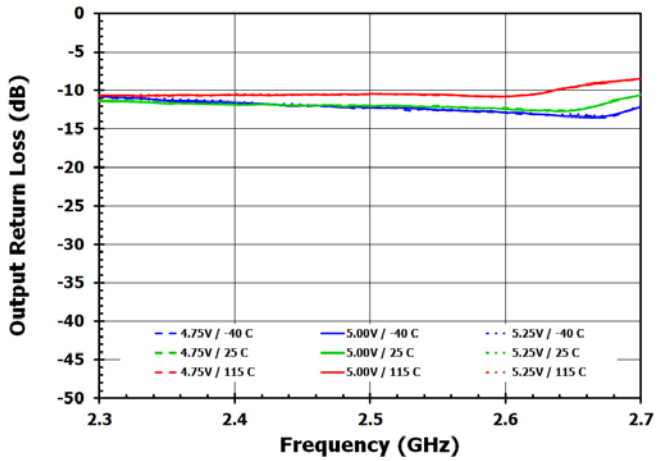


Figure 8. Output Return Loss - High Gain Mode

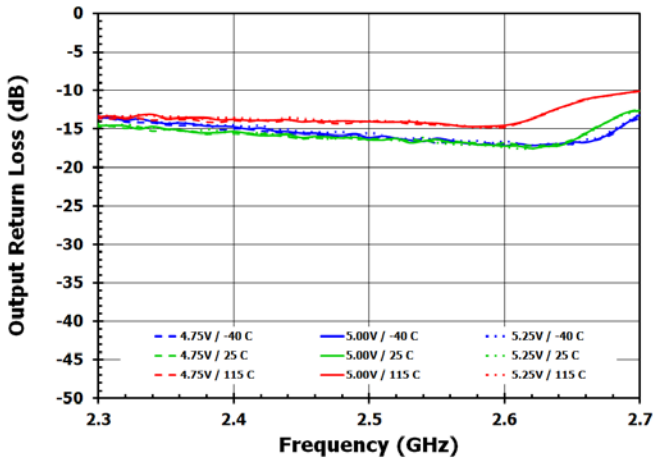


Figure 9. Reverse Isolation - Low Gain Mode

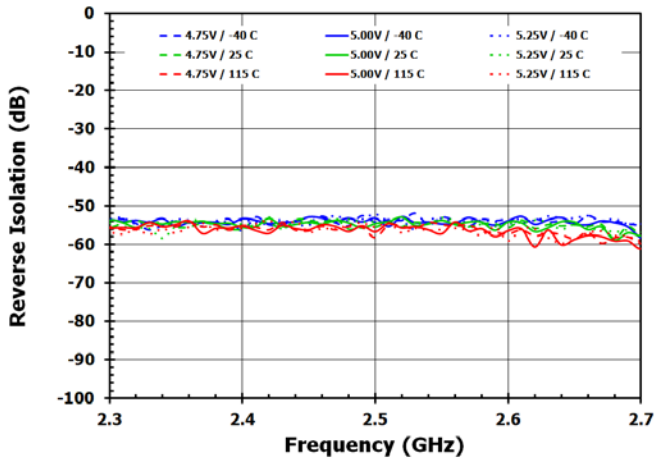


Figure 10. Reverse Isolation - High Gain Mode

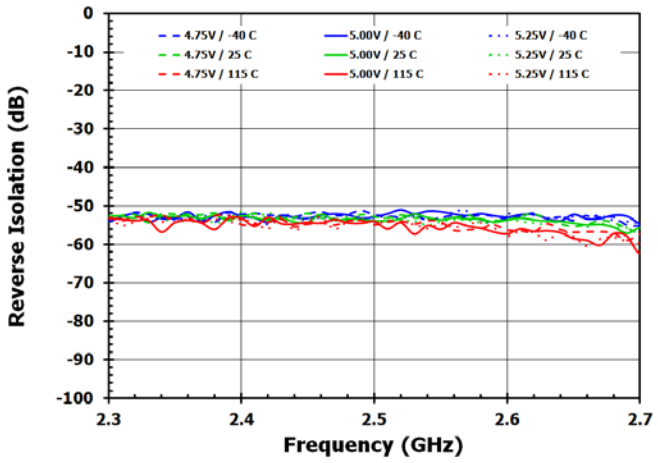


Figure 11. Standby Mode Gain

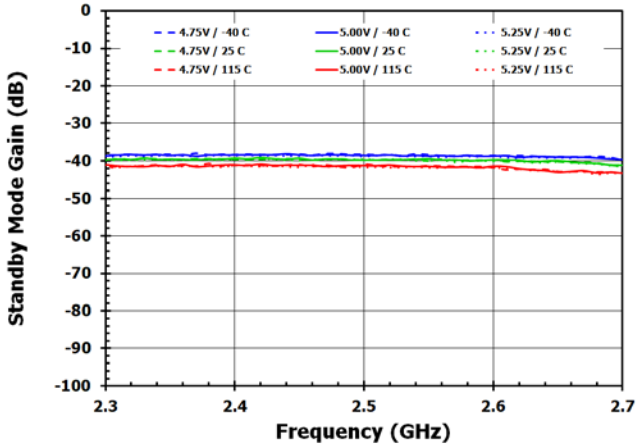


Figure 12. Current versus Power Supply Voltage

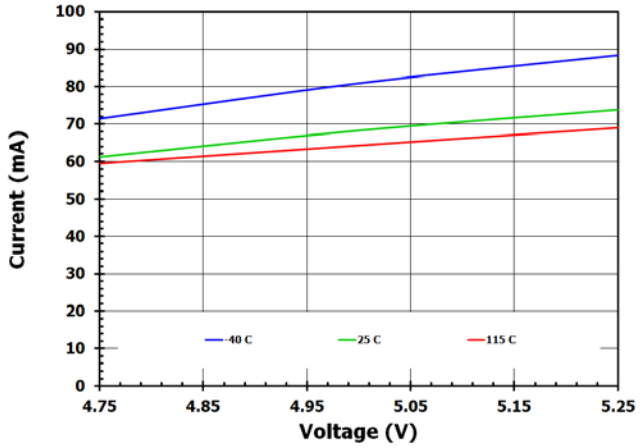


Figure 13. Noise Figure - Low Gain Mode

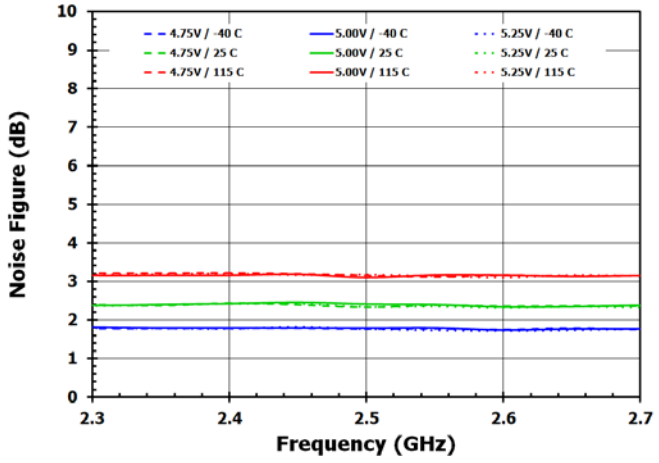


Figure 14. Noise Figure - High Gain Mode

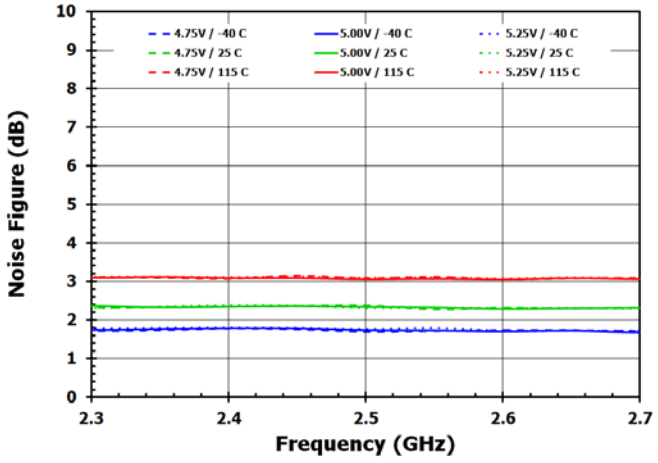


Figure 15. Output IP3 - Low Gain Mode

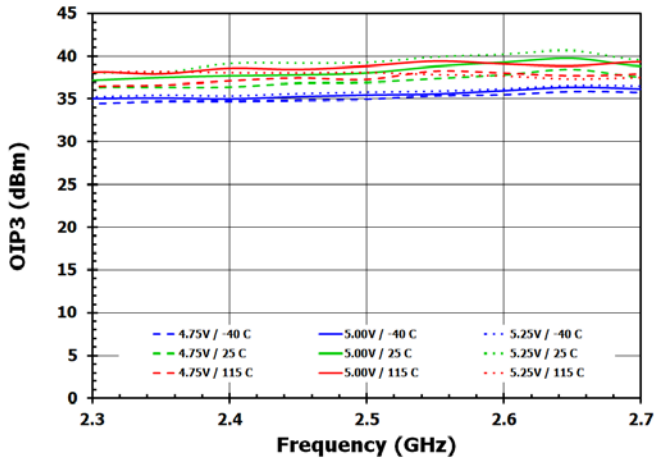


Figure 16. Output IP3 - High Gain Mode

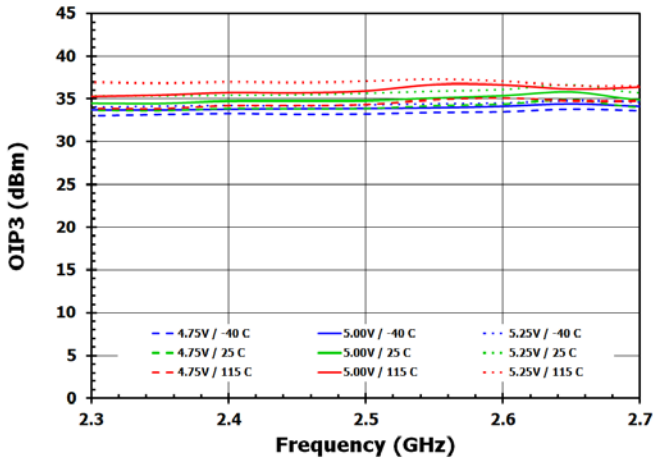


Figure 17. Output P1dB - Low Gain Mode

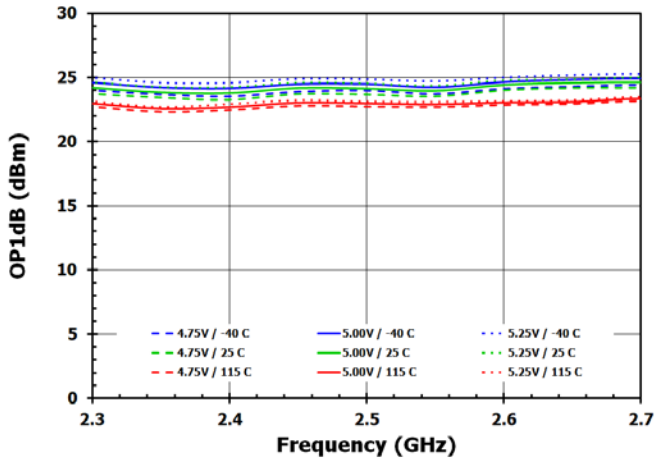
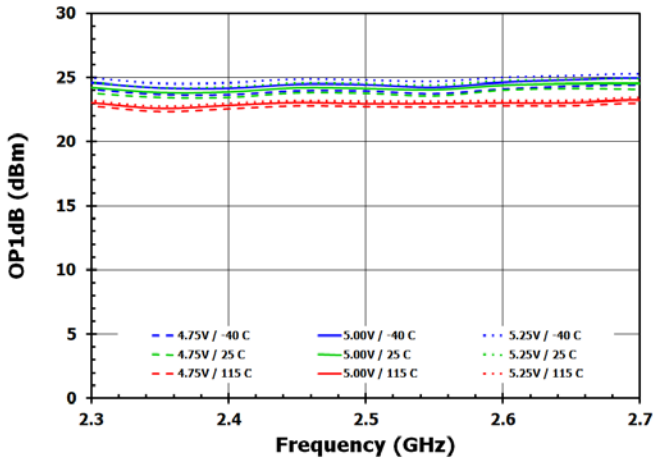


Figure 18. Output P1dB - High Gain Mode



Typical Performance Characteristics (Band 3p55 – 3.3GHz to 3.8GHz)

Figure 19. Gain - Low Gain Mode

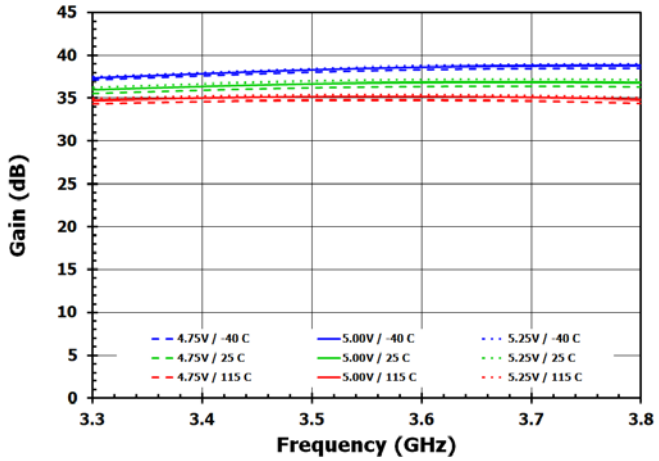


Figure 20. Gain - High Gain Mode

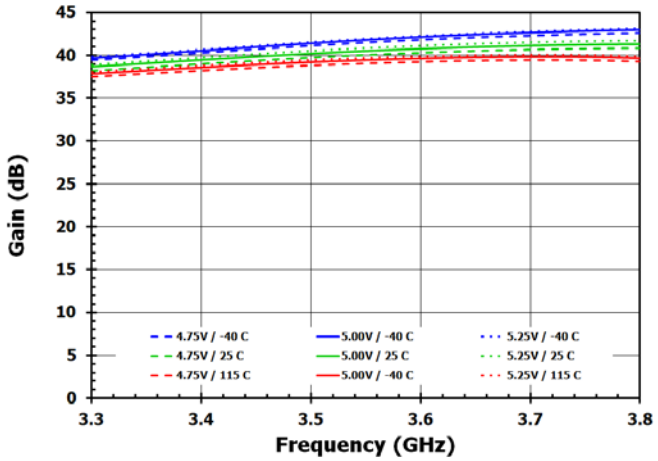


Figure 21. Input Return Loss - Low Gain Mode

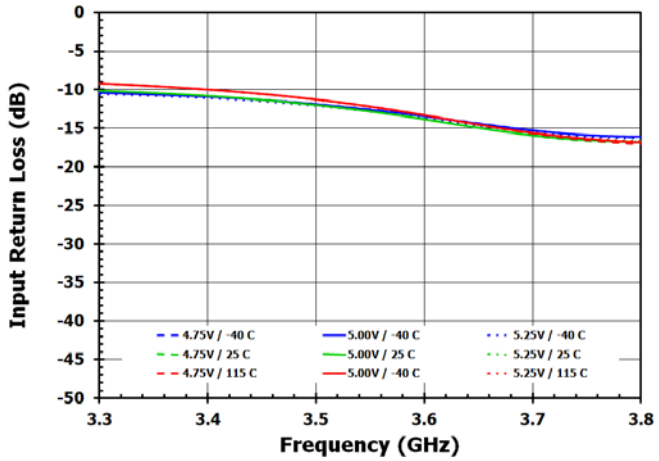


Figure 22. Input Return Loss - High Gain Mode

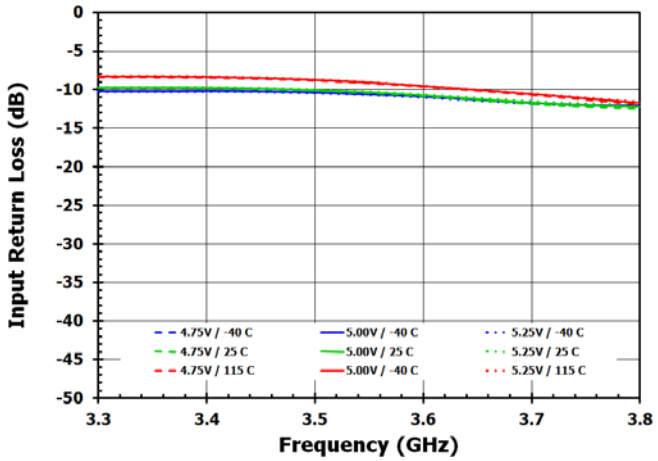


Figure 23. Output Return Loss - Low Gain Mode

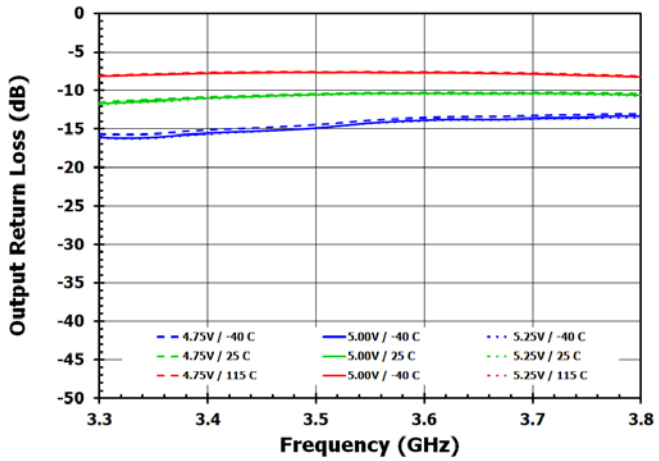


Figure 24. Output Return Loss – High Gain Mode

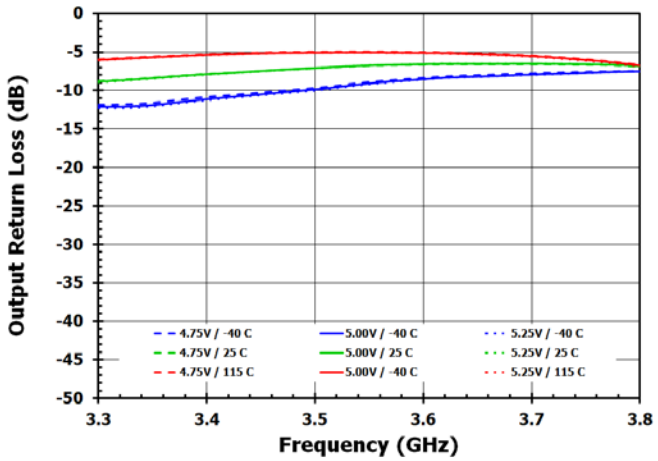


Figure 25. Reverse Isolation - Low Gain Mode

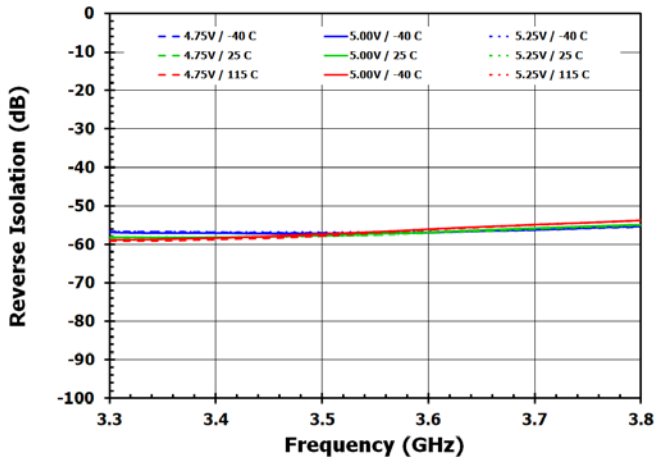


Figure 26. Reverse Isolation - High Gain Mode

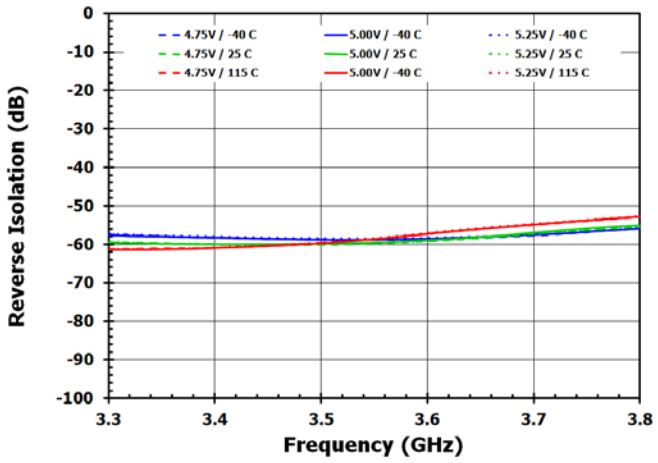


Figure 27. Standby Mode Gain

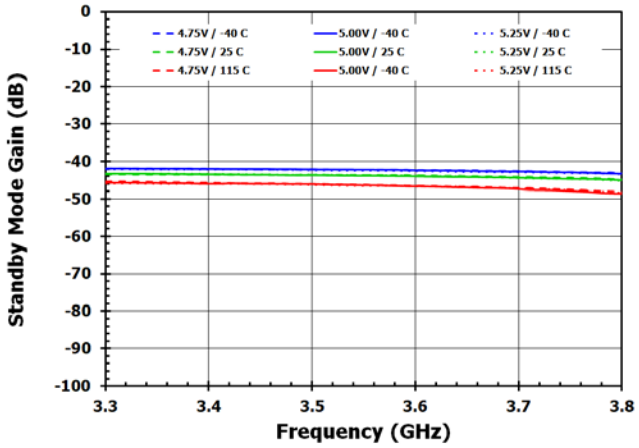


Figure 28. Current versus Power Supply Voltage

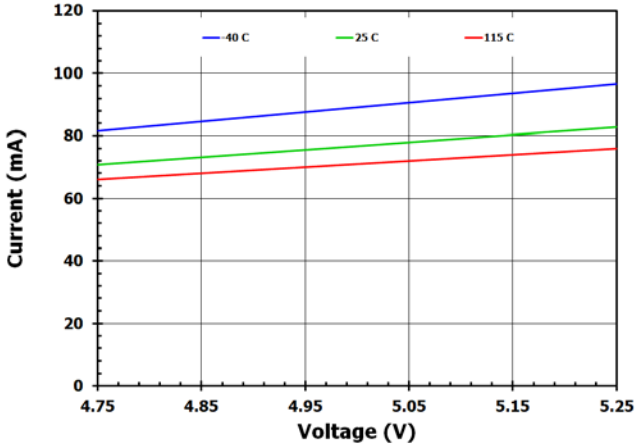


Figure 29. Noise Figure - Low Gain Mode

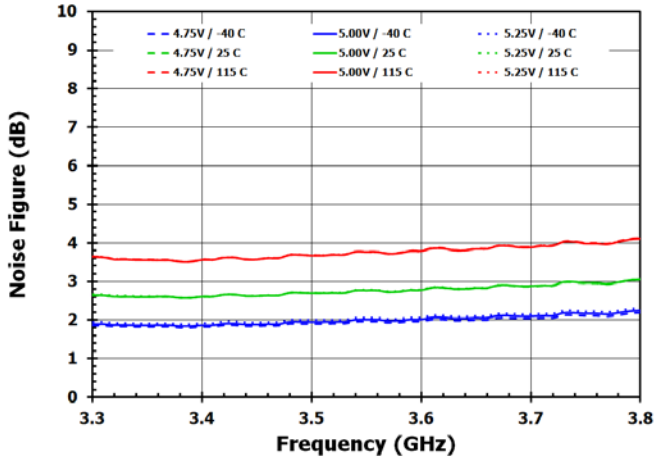


Figure 30. Noise Figure - High Gain Mode

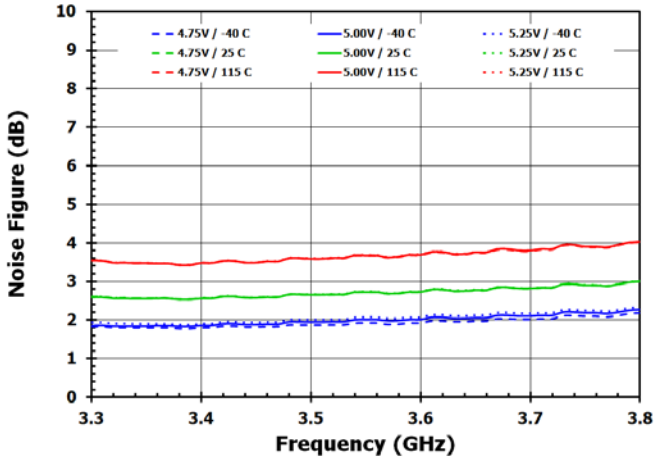


Figure 31. Output IP3 - Low Gain Mode

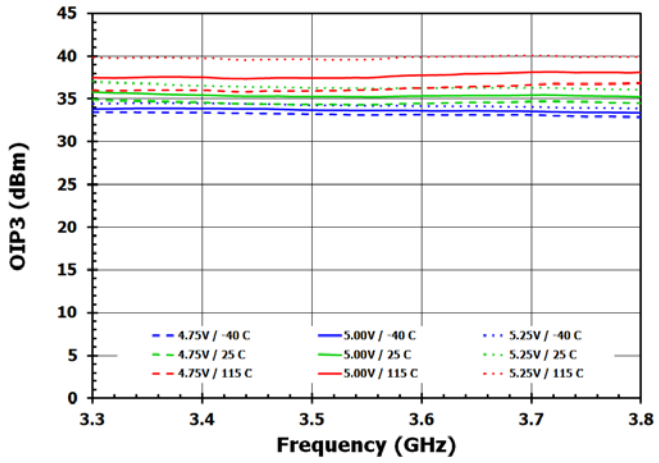


Figure 32. Output IP3 - High Gain Mode

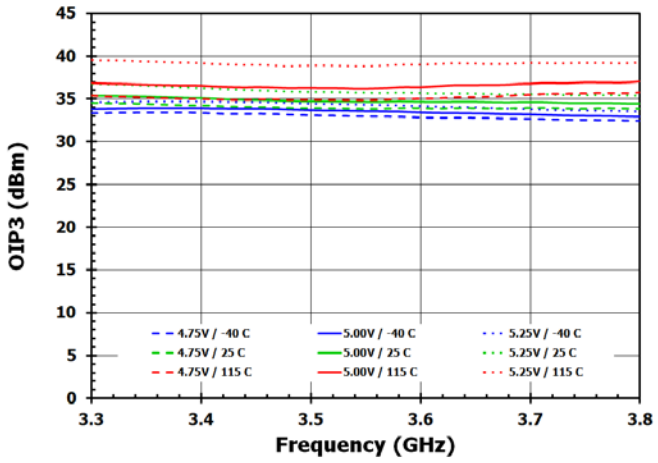


Figure 33. Output P1dB - Low Gain Mode

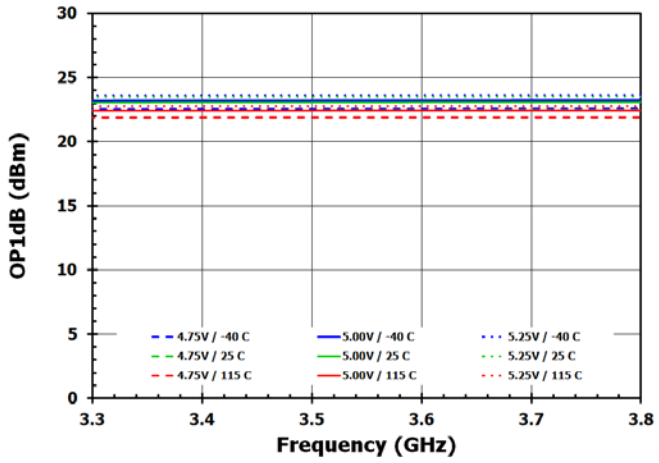
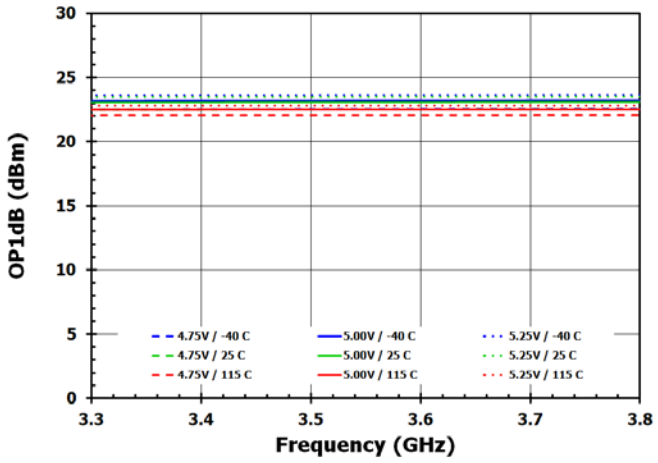


Figure 34. Output P1dB - High Gain Mode



Functional Description

Standby

The F1490 can be turned off for low current consumption. This is done by applying a logic voltage to pin 16 using the following table.

Table 8. Standby Truth Table

STBY	Condition
Logic HIGH / NC	Full operation
Logic LOW	Amplifier OFF

Gain Selection

The F1490 can be selected to be in a High Gain Mode or Low Gain Mode operation. This is done by applying a logic voltage to pin 15 using the following table.

Table 9. Gain Selection Truth Table

GAIN_SEL	Condition
Logic HIGH	High Gain Mode
Logic LOW / NC	Low Gain Mode

Evaluation Kit Picture

Figure 35. Evaluation Kit: Top View

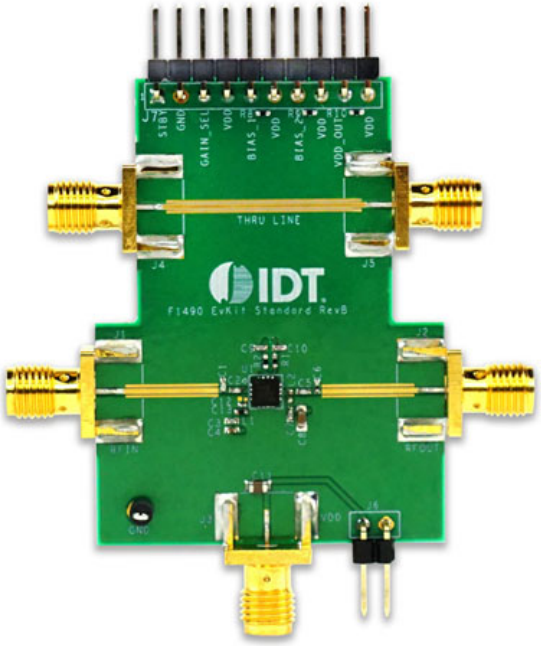
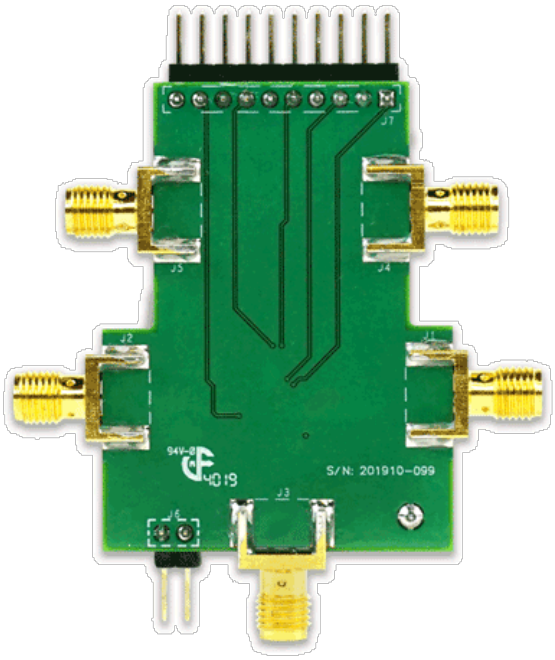
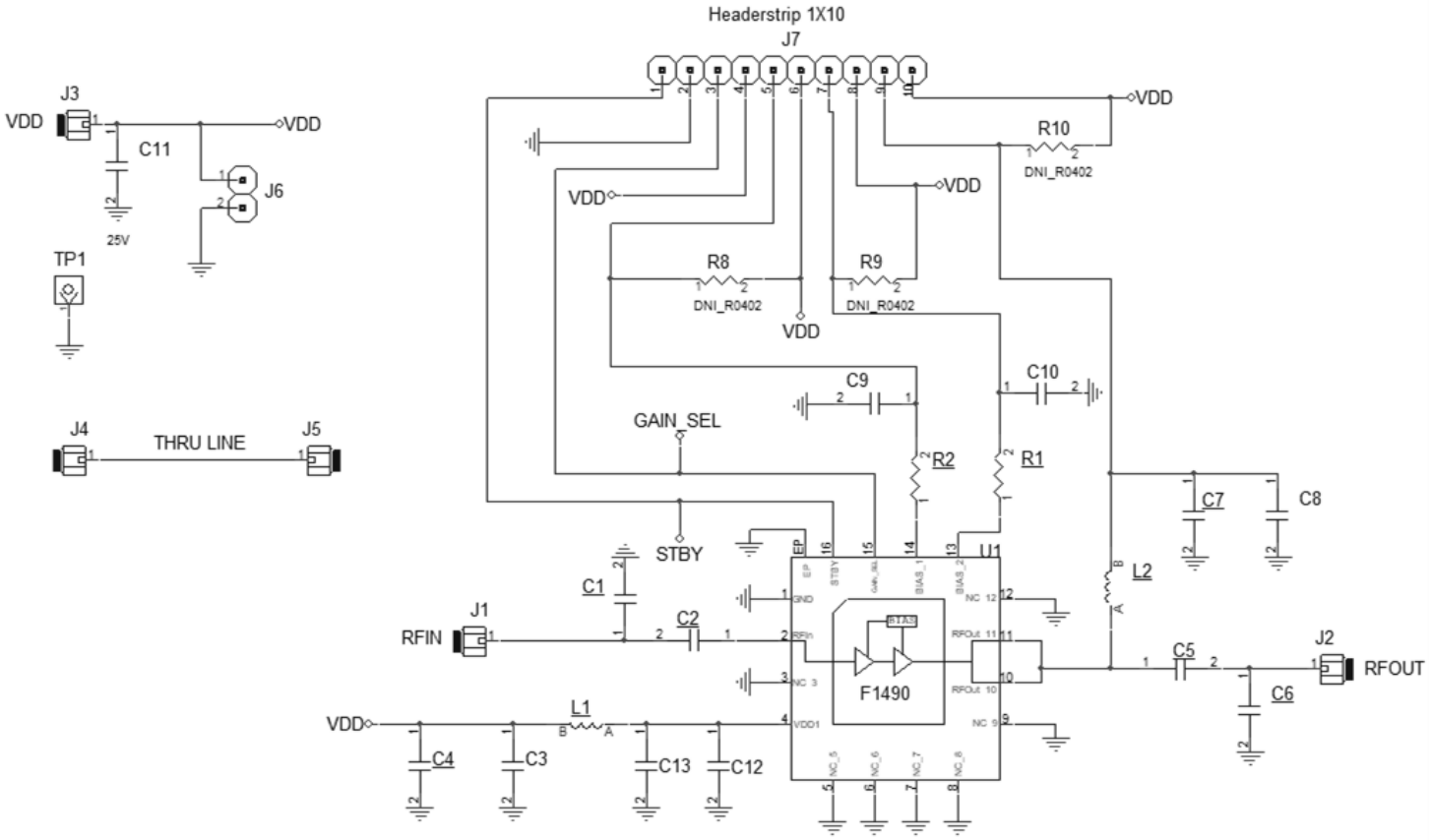


Figure 36. Evaluation Kit: Bottom View



Evaluation Board Schematic

Figure 37. Electrical Schematic



Evaluation Kit BOM – 2.3GHz to 2.7GHz

Table 10. 2.3GHz to 2.7GHz Evaluation Kit Bill of Materials (BOM)[a]

Part Reference	Qty.	Description	Mfr. Part #	Mfr.
C1	1	0.8pF ±0.1pF, 50V ,COG Surface Mount Capacitor	GJM1555C1HR80BB01D	Murata
C6	1	0.7pF ±0.1pF, 50V ,COG Surface Mount Capacitor	GJM1555C1HR70BB01D	Murata
C2	1	10pF ±0.25pF, 50V ,COG Surface Mount Capacitor	GJM1555C1H100JB01	Murata
C3, C7, C10, C9	4	33pF ±5%, 25V, COG Surface Mount Capacitor	GRM1555C1H330J	Murata
C4	1	0.1uF ±10%, 16V ,X7R Surface Mount Capacitor	GRM155R71C104KA88D	Murata
C8	1	0.1uF ±10%, 50V ,H8L Surface Mount Capacitor	GCM188L81H104KA57D	Murata
C11	1	1uF ±10%, 25V, X5R Surface Mount Capacitor	GRM188R61E105KA12	Murata
C5	1	22pF ±5%, 50V , COG Surface Mount Capacitor	GRM1555C1H220J	Murata
C12, C13	2	DNI		
R1	1	1.5kΩ ±5%, 1/10W	ERJ2GEJJ152	Panasonic
R2	1	1kΩ ±5%, 1/16W	ERJ2GEJJ102	Panasonic
R8, R9, R10	3	0Ω, 1/10W	ERJ2GE0R00X	Panasonic
L2	1	2.2nH ±0.3nH, 300mA, Surface Mount Inductor	LQG15HS2N2S02	Murata
L1	1	1.5nH ±0.3nH, 1A 100mΩ, Surface Mount Inductor	LQG15HN1N5S02D	Murata
J1, J2, J3, J4, J5	5	Connector SMA Jack STR 50ohm Edge Mount	142-0701-851	Cinch Connectivity
J6	1	DNI Headerstrip 1x2		
J7	1	Headerstrip 1x10	0022284103	Molex
TP1	1	Loop, Black, Phosphor Bronze Wire Loop	5001	Keystone electronics
U1	1	F1490, GaAs Pre-Driver Amplifier	F1490	IDT

[a] This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.

Evaluation Kit BOM – 3.3GHz to 3.8GHz

Table 11. 3.3GHz to 3.8GHz Evaluation Kit Bill of Materials (BOM)[a]

Part Reference	Qty.	Description	Mfr. Part #	Mfr.
C1	1	0.8pF ±0.1pF, 50V ,COG Surface Mount Capacitor	GJM1555C1HR80BB01D	Murata
C6 (inductor)	1	4.3nH ±0.3nH,COG Surface Mount Capacitor	LQG15HS4N3S02D	Murata
C2	1	6pF ±5%, 50V ,COG Surface Mount Capacitor	GJM1555C1H6R0BB01	Murata
C3, C7, C10, C9	4	33pF ±5%, 25V, COG Surface Mount Capacitor	GRM1555C1H330J	Murata
C4	1	0.1uF ±10%, 16V ,X7R Surface Mount Capacitor	GRM155R71C104KA88D	Murata
C8	1	0.1uF ±10%, 25V ,X5R Surface Mount Capacitor	GCM188R71C104KA37D	Murata
C11	1	1uF ±10%, 25V, X5R Surface Mount Capacitor	GRM188R61E105KA12D	Murata
C5	1	1.1pF ±0.1pF, 16V , COG Surface Mount Capacitor	GJM1555C1H1R1BB01D	Murata
C12	1	DNI		
C13	1	33pF ±5%, 25V , COG Surface Mount Capacitor	GRM0335C1E330JA01D	Murata
R1	1	1.8kΩ ±5%, 1/10W	ERJ2GEJ182	Panasonic
R2	1	150Ω ±5%, 1/16W	ERJ2GEJ151	Panasonic
R8, R9, R10, L1	3	0Ω, 1/10W	ERJ2GE0R00X	Panasonic
L2	1	1.8nH ±0.3nH, 300mA, Surface Mount Inductor	LQG15HS1N8S02	Murata
J1, J2, J3	3	Connector SMA Jack STR 50ohm Edge Mount	142-0701-851	Cinch Connectivity
J4, J5	2	DNI		
J6	1	DNI Headerstrip 1x2		
J7	1	Headerstrip 1x10	0022284103	Molex
TP1	1	Loop, Black, Phosphor Bronze Wire Loop	5001	Keystone electronics
U1	1	F1490, GaAs Pre-Driver Amplifier	F1490	IDT

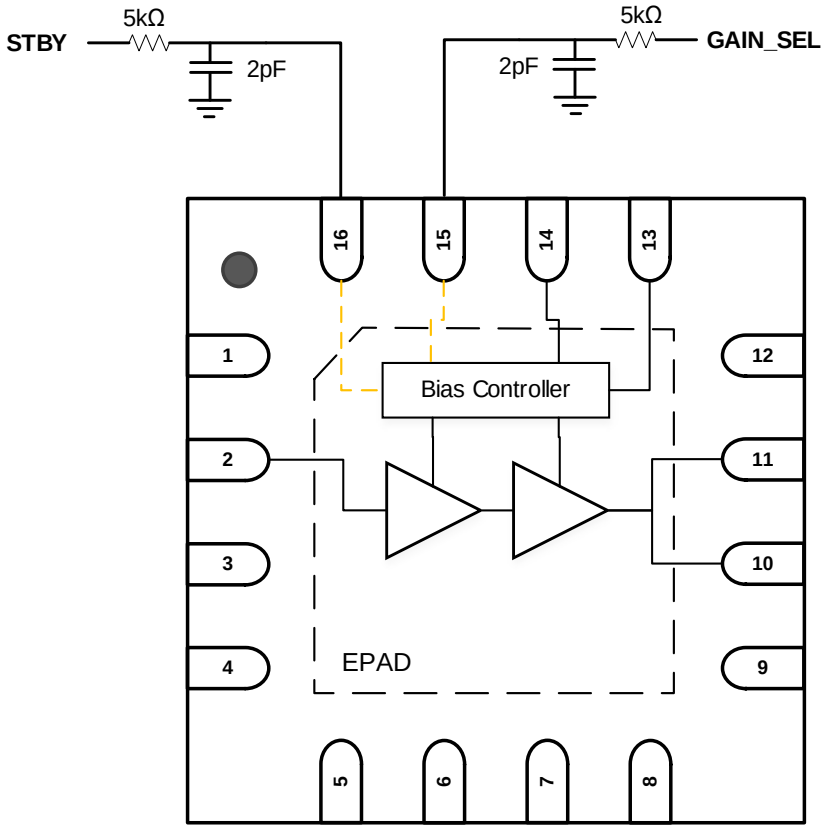
[a] This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.

Power Supplies

A common V_{CC} power supply should be used for all power supply pins. To minimize noise and fast transients, add de-coupling capacitors to all supply pins. Supply noise can degrade noise figure. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit is recommended at the input of each control pin. This applies to the GAIN_SEL pin (15) and STBY pin (16) as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV Kit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

Figure 38. Control Pin Interface for Signal Integrity



Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-090-mm-050mm-pitch-160-x-160-mm-epad-nlg16p3

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F1490NLGA	3 × 3 × 0.9 mm 16-VFQFPN	MSL 1	Tray	-40° to +115°C
F1490NLGA8	3 × 3 × 0.9 mm 16- VFQFPN	MSL 1	Tape and Reel	-40° to +115°C
F1490EVB-2P5	Evaluation Board for 2.3GHz to 2.7GHz Band			
F1490EVB-3P6	Evaluation Board for 3.3GHz to 3.8GHz Band			

Marking Diagram

- Line 1: “XXX” represents the last three digits of the lot number.
- Line 2: “YWW” has one digit for the year and two digits for week that the part was assembled. “$$” denotes the assembly site.
- Line 3: “F1490” is the part number.

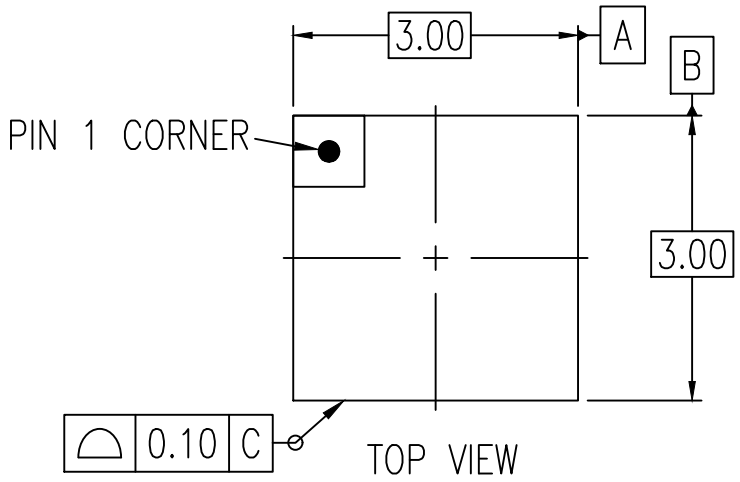
Revision History

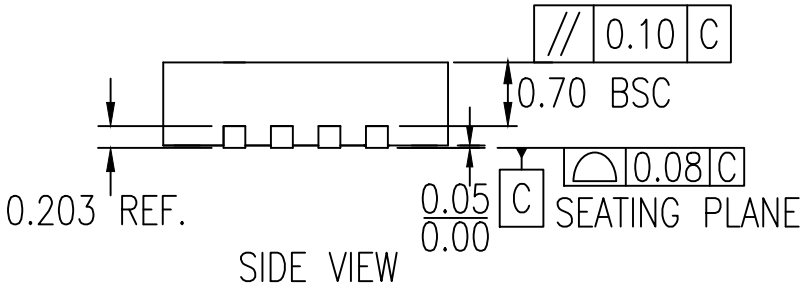
Revision Date	Description of Change
August 17, 2020	Updated pins 1 and 3 descriptions in Table 1.
May 1, 2020	Added Application Information for Power Supplies.
April 9, 2020	Updated MSL rating.
February 18, 2020	Initial release.

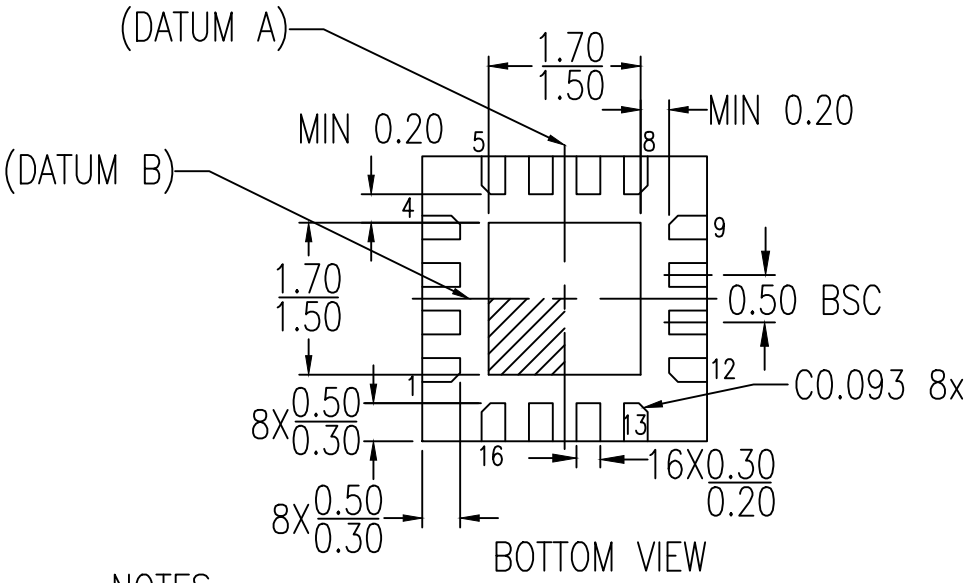
16-VFQFPN Package Outline Drawing

3.0 x 3.0 x 0.90 mm, 0.50mm Pitch, 1.60 x 1.60 mm Epad

NLG16P3, PSC-4169-03, Rev 04, Page 1

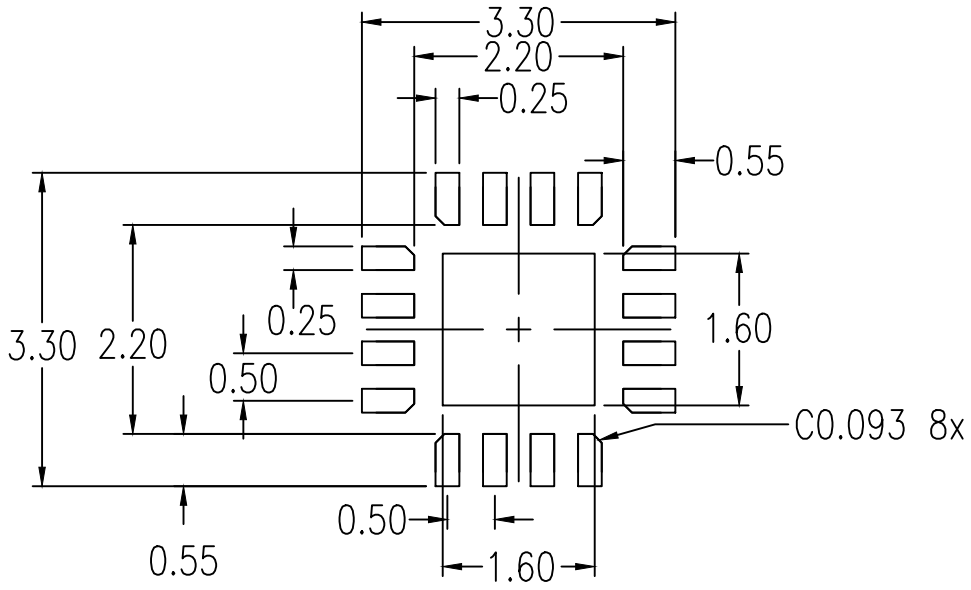






NOTES:

1. ALL DIMENSIONS ARE IN MM.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5–2009
3. PIN 1 LOCATION IDENTIFIER IS EITHER BY CHAMFER OR NOTCH



RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Sept 13, 2018	Rev 03	Change QFN to VFQFPN
Aug 18, 2020	Rev 04	Add Chamfer Dimension

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