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iNAND® *7250*

e.MMC 5.1 with HS400 Interface

REVISION HISTORY

Doc. No	Revision	Date	Description
DOC-56-34-01508	1.0	March 2017	Released version
DOC-56-34-01508	1.1	June 2017	Updated performance target and ext_CSD SKU_ID
DOC-56-34-01508	1.2	July 2017	Updated MAX_ENH_SIZE_MULT
DOC-56-34-01508	1.3	July 2017	Updated features description of unified boot and Hardware Pin Secure Boot
DOC-56-34-01508	1.4	August 2017	Updated marking drawing

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1. INTRODUCTION

1.1. General Description

Overview SanDisk iNAND 7250 is an Embedded Flash Drive (EFD) designed for write intensive applications in a wide range of home entertainment and security applications, such as Set-Top-Box (STB), Over The Top (OTT), Home Gateways, Smart TV, Smart Security Cameras and more. The iNAND 7250 utilizes an LDPC ECC machine and MLC memory to provide a robust, high performance, high quality and high endurance product. The LDPC engine significantly improves error correction enabling longer device lifetime and an increased ability to handle operation at high temperature.

The iNAND 7250 provides 8GB to 64GB of capacity and supports e.MMC 5.1. The iNAND 7250 is the ideal choice to deliver high reliability and high performance for storage applications like imaging, video, music, GPS, gaming, email, office and other new applications such as NOR replacement for embedded systems or other devices.

The design of the iNAND 7250 is based on a JEDEC compatible form factor measuring 11.5x13mm (153 balls) for all capacities to lower integration costs and accelerate time-to-market.

Architecture iNAND 7250 combines an embedded thin flash controller with advanced Multi-level Cell (MLC) NAND flash technology enhanced by SanDisk's embedded flash management software running as firmware on the flash controller. iNAND 7250 employs an industry-standard eMMC 5.1[1] interface featuring Command-Queue, HS400 interface, FFU, as well as legacy eMMC 4.51 features such as EUDA, Power Off Notifications, Packed commands, Cache, Boot / RPMB partitions, HPI, and HW Reset, making it an optimal device for both reliable code and data storage.

Like our other iNAND products, iNAND 7250 offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as an advanced power management scheme.

iNAND 7250 architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximizing flash life expectancy.

iNAND 7250 also includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

Combining high performance with features for easy integration and exceptional reliability, iNAND 7250 is an EFD designed to exceed the demands of both manufacturers and their customers.

[1] Compatible to JESD84-B51

1.2. Plug-and-Play Integration

iNAND's optimized architecture eliminates the need for complicated software integration and testing processes thereby enabling plug-and-play integration into the host system. The replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This allows manufacturers to adopt advanced NAND Flash technologies and update product lines with minimal integration or qualification efforts.

iNAND 7250 features a MMC interface allows for easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the SanDisk iNAND 7250 with MMC Interface.

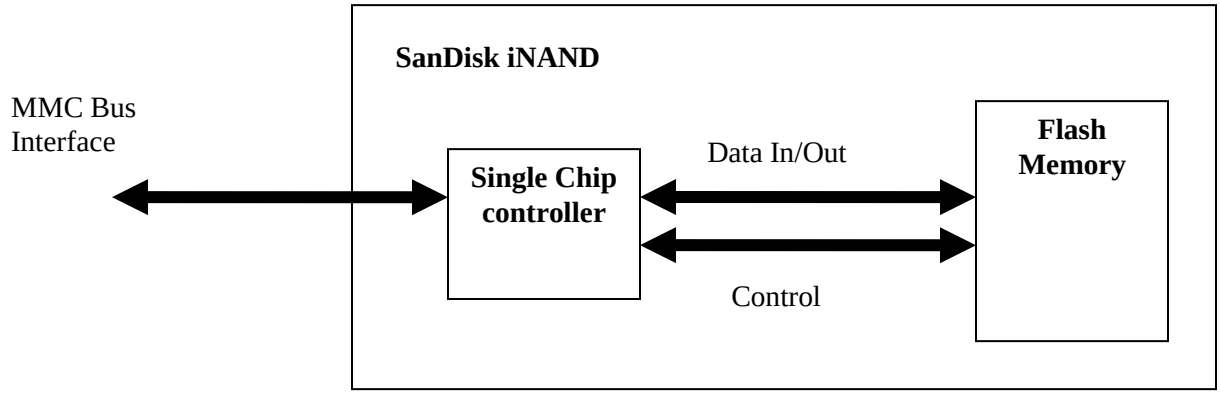

Figure 1 - iNAND 7250 with MMC Interface Block Diagram

1.3. Feature Overview

SanDisk iNAND 7250, with MMC interface, includes the following features:

- Memory controller and NAND flash
- Mechanical design that complies with JEDEC Specifications with specific optimizations for automotive applications
- Offered in three TFBGA packages of e.MMC 5.1
  - 11.5mm x 13mm x 0.8mm (8GB-16GB)
  - 11.5mm x 13mm x 1.0mm (32GB)
  - 11.5mm x 13mm x 1.2mm (64GB)
- Operating temperature range: –25C° to +85C°
- Dual power system
  - Core voltage (VCC) 2.7-3.6 V
  - I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
- 8GB - 64GB of data storage
- Supports three data bus widths: 1bit (default), 4bit, 8bit
- Complies with e.MMC Specification Ver. 5.1 HS400
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Up to 300 MB/sec bus transfer rate, using 8 parallel data lines at 200 MHz, HS400 Mode
- High data integrity with MLC memory, advanced LDPC ECC engine, automatic refresh, advanced power protection
- Flexible EUDA, Fast boot
- Up to 3K P/E cycles on MLC and 30K on SLC with 1 year data retention @ 55°C and at least 10 year data retention @ 55°C for fresh devices

1.4. MMC bus and Power Lines

SanDisk iNAND 7250 supports the MMC interface protocol. For more details regarding these buses refer to JEDEC standard No. JESD84-B51.

The iNAND bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input.
- VCCQ: Power supply line for host interface.
- VCC: Power supply line for internal flash memory.
- VDDi: iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: Ground lines.
- RCLK: Data strobe.
- VSF: Vendor specific functions used for debugging purposes.

1.4.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

2. E.MMC SELECTED FEATURES OVERVIEW

iNAND 7250 supported features list:

Table 3 – Proprietary Features list

e.MMC	Device Features	Benefit	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Max theoretical Speed	Up to 400MB/s
4.41	EUDA	Enhanced User Data Area for higher endurance	Yes
4.41	SECURE ERASE/TRIM	“True Wipe”	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	Yes
4.41	PARTITIONING & PROTECTION	Flexibility	Yes
4.41	BACKGROUND OPERATIONS	Better User Experience (low latency)	Yes
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	Yes
4.41	HARDWARE RESET	Robust System Design	Yes
4.41	HPI	Control Long Reads/Writes	Yes
4.41	RPMB	Secure Folders	Yes
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	Yes
4.5	LARGE SECTOR SIZE	Potential performance	No
4.5	SANITIZE (4.51)	“True Wipe”	Yes
4.5	PACKED COMMANDS	Reduce Host Overhead	Yes
4.5	DISCARD	Improved Performance on Full Media	Yes
4.5	DATA TAG	Performance and/or Reliability	Yes (API only)
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	Yes (API only)
4.5	CACHE	Better Sequential & Random Writes	Yes
5.0	SECURED FIELD FIRMWARE UPGRADE (sFFU)	Enables feature enhancements in the field	Yes
5.0	PRODUCTION STATE AWARENESS	Different operation during production	Yes
5.0	DEVICE HEALTH	Vital NAND info	Yes
5.1	ENHANCE STROBE	Sync between Device and Host in HS400	Yes
5.1	COMMAND QUEUE	Responsiveness	Yes
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	Yes
5.1	CACHE FLUSH AND BARRIER	Ordered Cache flushing	Yes
5.1	BKOPS CONTROLLER	Host control on BKOPs	Yes
5.1	SECURE WP	Secure Write Protect	Yes
5.1	PRE EOL	Pre End Of Life notification	Yes
Proprietary	VSF	Enable on-board debugging	Yes
Proprietary	PNM	Special product name	Yes
Proprietary	DEVICE REPORT	Device Firmware status	Yes
Proprietary	UNIFIED BOOT	Reports both boot partitions	Yes (only on CS2.2)
Proprietary	HARDWARE PIN SECURE BOOT	Enable Hardware pin secure write protect	Yes (only on CS2.2)

2.1. HS400 Interface

SanDisk 7250 supports HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 4 or 8 bit bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data. For additional information please refer to JESD84-B51 standard.

2.2. Enhanced User Data Area (EUDA)

For write intensive applications, there is a need for an area of higher endurance or performance. To address this, SanDisk 7250 allows for the definition of an enhanced user data area as specified in the JESD84-B51 standard. This area is a true SLC partition. The EUDA is a designated area of the general User Data Area. The configuration is one-time programmable.

2.3. Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the e.MMC device and instructs the e.MMC device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user/OS data. During the FFU process, the host can replace firmware files or single/all file systems.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the SanDisk lab
2. The sFFU files are handed to SanDisk's customer
3. SanDisk's customer can push the firmware updates to their end-users in a transparent way

Note 1: The sFFU process and sFFU files are protected against leakage to unauthorized entities.

Note 2: During the sFFU process the Host may retrieve the exact status of the process using the smart report feature.

For additional information please refer to JESD84-B51 standard and the SanDisk application note on this subject.

2.4. Cache

The eMMC cache is dedicated volatile memory at the size of 512KB. Caching enables to improve iNAND performance for both sequential and random access. For additional information please refer to JESD84-B51 standard.

2.5. Discard

iNAND supports discard command as defined in e.MMC 5.1 spec. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

2.6. Power off Notifications

iNAND supports power off notifications as defined in e.MMC 5.1 spec. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

2.7. Packed Commands

To enable optimal system performance, iNAND supports packed commands as defined in e.MMC 5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

2.8. Boot Partition

iNAND supports e.MMC 5.1 boot operation mode: factory configuration supplies two boot partitions each 4MB in size for 8GB-64GB.

2.9. RPMB Partition

iNAND supports e.MMC 5.1 RPMB operation mode: factory configuration supplies one RPMB partition 4MB in size for 8GB-64GB.

2.10. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.11. Sleep (CMD5)

An iNAND 7250 device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer to JESD84-B51.

2.12. Enhanced Reliable Write

iNAND 7250 supports enhanced reliable write as defined in e.MMC 5.1 spec.

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.13. Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

2.14. Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND 7250 supports the optional Secure Erase command.

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

2.15. Secure Trim

For backward compatibility reasons, iNAND 7250 support Secure Trim command. The Secure Trim5 command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

The secure trim command is performed in two steps:

1) Mark the LBA range as candidate for erase.
2) Erase the marked address range and ensure no old copies are left.

2.16. Partition Management

iNAND 7250 offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows

Factory configuration supplies two boot partitions (refer to section 2.9) implemented as enhanced storage media and one RPMB partitioning of 4MB in size (refer to section 2.10).

Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

2.17. Device Health

Device Health is similar to SMART features of modern hard disks, it provides only vital NAND flash program/erase cycles information in percentage of useful flash life span.

The host can query Device Health information utilizing standard MMC command, to get the extended CSD structure:

- DEVICE_LIFE_TIME_EST_TYP_A[268], the host may use it to query SLC device health information
- DEVICE_LIFE_TIME_EST_TYP_B[269], the host may use it to query MLC device health information

The device health feature will provide a % of the wear of the device in 10% fragments.

2.18. EOL Status

EOL status is implemented according to the eMMC 5.1 spec. One additional state (state 4) was added to INAND 7250 which indicates that the device is in EOL mode.

2.19. Enhanced Write Protection

To allow the host to protect data against erase or write iNAND 7250 supports two levels of write protect command.

The entire iNAND 7250 (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD Specific segments of iNAND 7250 may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

For additional information please refer to the JESD84-B51 standard.

2.20. High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in JESD84-B51 enables low read latency operation by suspending a lower priority operation before it is actually completed.

For additional information on the HPI function, refer to JESD84-B51.

2.21. H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B51 standard.

2.22. Host-Device Synchronization Flow (Enhanced STROBE)

The Enhanced STROBE feature as implemented in iNAND 7250 allows utilizing STROBE to synchronize also the CMD response:

- CMD clocking stays SDR (similar to legacy DDR52)
- Host commands are clocked out with the rising edge of the host clock (as done in legacy eMMC devices)
- iNAND 7250 will provide STROBE signaling synced with the CMD response in addition to DATA Out
- Host may use the STROBE signaling for DAT and CMD-Response capturing eliminating the need for a tuning mechanism

This feature requires support by the host to enable faster and more reliable operation.

2.23. Command-Queue

e.MMC Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash

3. PRODUCT SPECIFICATIONS

3.1. Typical Power Measurements

Table 4 – iNAND 7250 **Power Consumption Sleep** (Ta=25°C@1.8V/3.3V)

	8GB	16GB	32GB	64GB	Units
HS400 Sleep (CMD5 – VCCQ, VCC off)	150	150	150	150	uA
HS200 Sleep (CMD5 – VCCQ, VCC off)	150	150	150	150	uA
DDR52 Sleep (CMD5 – VCCQ, VCC off)	150	150	150	150	uA

Table 5 – iNAND 7250, **Power Consumption Peak** VCC / VCCQ (Ta=25°C@1.8V/3.3V)

		8GB	16GB	32GB	64GB	Units
Active HS400	Peak [2µs window] VCC	150	230	400	400	mA
	Peak [2µs window] VCCQ[2]	295	295	325	365	mA
Active HS200	Peak [2µs window] VCC	150	230	400	400	mA
	Peak [2µs window] VCCQ	210	210	240	260	mA
Active DDR52	Peak [2µs window] VCC	150	230	400	400	mA
	Peak [2µs window] VCCQ	200/165[3]	200/175[3]	230/195[3]	250/200[3]	mA

Table 6 - iNAND 7250, **Power Consumption RMS** VCC / VCCQ (Ta=25°C@1.8V/3.3V)

			8GB	16GB	32GB	64GB	Units
Active HS400	Read	RMS [100ms window] VCC	60	60	60	60	mA
		RMS [100ms window] VCCQ	245	245	275	300	mA
	Write	RMS [100ms window] VCC	45	85	150	160	mA
		RMS [100ms window] VCCQ	135	155	195	220	mA
Active HS200	Read	RMS [100ms window] VCC	50	50	50	50	mA
		RMS [100ms window] VCCQ	145	145	165	180	mA
	Write	RMS [100ms window] VCC	50	75	130	140	mA
		RMS [100ms window] VCCQ	105	110	130	140	mA
Active DDR52	Read	RMS [100ms window] VCC	40	40	40	40	mA
		RMS [100ms window] VCCQ	110/140[3]	110/140[3]	115/150[3]	130/160[3]	mA
	Write	RMS [100ms window] VCC	45	45	60	70	mA
		RMS [100ms window] VCCQ	95/100[3]	95/110[3]	115/125[3]	120/140[3]	mA

[2] The regulator must be able to supply the current as the peak value can last for up to 1ms

[3] 1.8V/3.3V

3.2. Operating Conditions

3.2.1. Operating and Storage Temperature Specifications

Table 5 - Operating and Storage Temperatures

Condition	Ambient Temperature (Ta)[4]
Operating	-25° C to 85° C
Storage	-40° C to 85° C

3.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND 7250 is MSL = 3.

[4] This operating temperature should be maintained on the package case in order to achieve optimized power/performance

3.3. Reliability

SanDisk iNAND 7250 product meets or exceeds NAND type of products Endurance and Data Retention requirements as per evaluated representative usage models for designed market and relevant sections of JESD47I standard.

Table 6 - Critical Reliability Characteristics

Reliability Characteristics	Description	Value
Uncorrectable Bit Error Rate (UBER)	Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events data can be lost.	**1 sector in 10^{15} bits read**

Write Endurance Specification (TBW)	Write endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload.
	TBW is characterized based on a representative mobile workload as described below:
	• 70% Sequential write, 30% Random Write.
	• Distribution of IO Transaction Sizes:
	  ○ <16KB: 77%-86%
	  ○ 16KB-128KB: 13-19%
	  ○ >128KB: 1.5-4%
	• Cache On, Packed Off
	Host data is 4K aligned
		Total Terabytes Written [TBW] Per representative Android workload:
		8GB: 20 TBW
		16GB: 40 TBW
		32GB: 80 TBW
		64GB: 160 TBW

Data Retention Specification (Years)	Fresh or Early Life Device (A device whose total write cycles to the flash is less than 10% of the maximum endurance specification)	**10 years of Data Retention @ 55°C**
	Cycled Device (Any device whose total write cycles are between 10% of the maximum write endurance specification and equal to or exceed the maximum write endurance specification)	**1 year of Data Retention @ 55°C**

3.4 Typical System Performance[5]

Table 7 – Sequential Performance[6 7]

	HS400		HS200		DDR52	
	Write (MB/s)	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)	Read (MB/s)
8GB	40	300	40	170	40	90
16GB	80	300	80	170	75	90
32GB	160	300	125	170	75	90
64GB	160	300	125	170	75	90

Table 8 – Sequential Performance – EUDA[12 13]

	HS400		HS200		DDR52	
	Write (MB/s)	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)	Read (MB/s)
8GB	60	300	60	170	60	90
16GB	120	300	120	170	75	90
32GB	240	300	140	170	75	90
64GB	240	300	140	170	75	90

Table 9 – Random Performance[8 9]

	HS400			HS200			DDR52		
	Write (IOPs)	Read (IOPs)		Write (IOPs)	Read (IOPs)		Write (IOPs)	Read (IOPs)	
	Cache ON	QD=8	QD=1	Cache ON	QD=8	QD=1	Cache ON	QD=8	QD=1
8GB	8k	17k	7.8k	6k	10k	4.5k	5.5k	10k	3.5k
16GB	14k	22k	7.8k	6k	10k	4.5k	5.5k	10k	3.5k
32GB	14k	22k	7.8k	6k	10k	4.5k	5.5k	10k	3.5k
64GB	14k	22k	7.8k	6k	10k	4.5k	5.5k	10k	3.5k

[5] All performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT).

[6] Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bit at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB.

[7] Sequential Write performance is measured for 100MB host payloads

[8] Random performance is measured with a chunk size of 4KB and address range of 1GB

[9] Random Write IOPs shown are with cache on

4. PHYSICAL SPECIFICATIONS

The SanDisk iNAND 7250 is a 153-pin, thin fine-pitched ball grid array (BGA). See Figure 2 and Table 12 for physical specifications and dimensions.

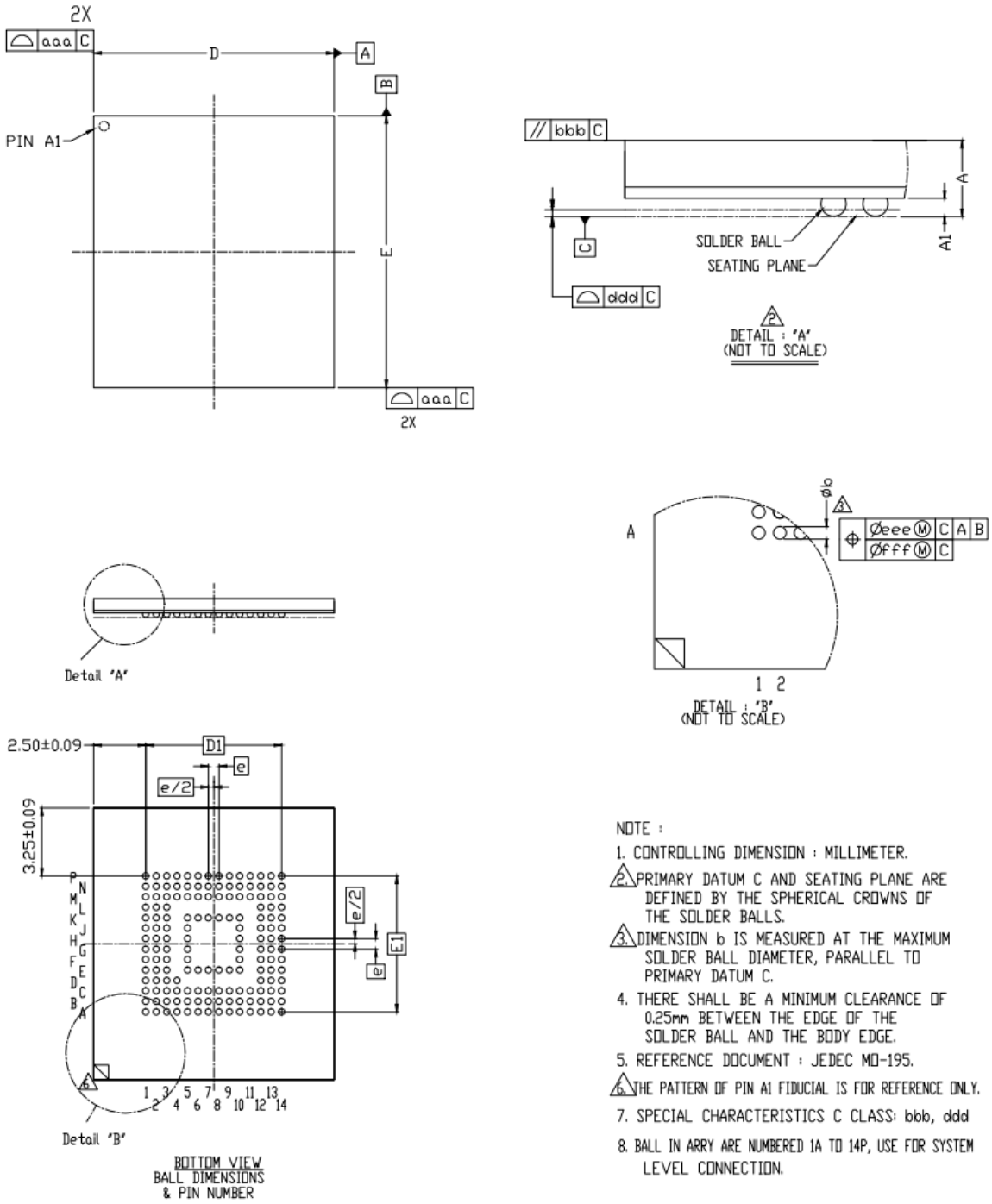

Figure 2 - INAND 7250 Package Outline Drawing

Table 10 – Package Specification

	8GB-16GB			32GB			64GB		
Symbol	**Min [mm]**	**Nom [mm]**	**Max [mm]**	**Min [mm]**	**Nom [mm]**	**Max [mm]**	**Min [mm]**	**Nom [mm]**	**Max [mm]**
A	0.6	0.7	0.8	0.8	0.9	1	1	1.1	1.2
A1	0.17	0.22	0.27	0.17	0.22	0.27	0.17	0.22	0.27
D	11.4	11.5	11.6	11.4	11.5	11.6	11.4	11.5	11.6
E	12.9	13	13.1	12.9	13	13.1	12.9	13	13.1
D1	-	6.5	-	-	6.5	-	-	6.5	-
E1	-	6.5	-	-	6.5	-	-	6.5	-
e	-	0.5	-	-	0.5	-	-	0.5	-
b	0.25	0.3	0.35	0.25	0.3	0.35	0.25	0.3	0.35
aaa	0.1			0.1			0.1		
bbb	0.1			0.1			0.1		
ddd	0.08			0.08			0.08		
eee	0.15			0.15			0.15		
fff	0.05			0.05			0.05		
MD/ME	14/14			14/14			14/14		

5. INTERFACE DESCRIPTION

5.1. MMC I/F Ball Array

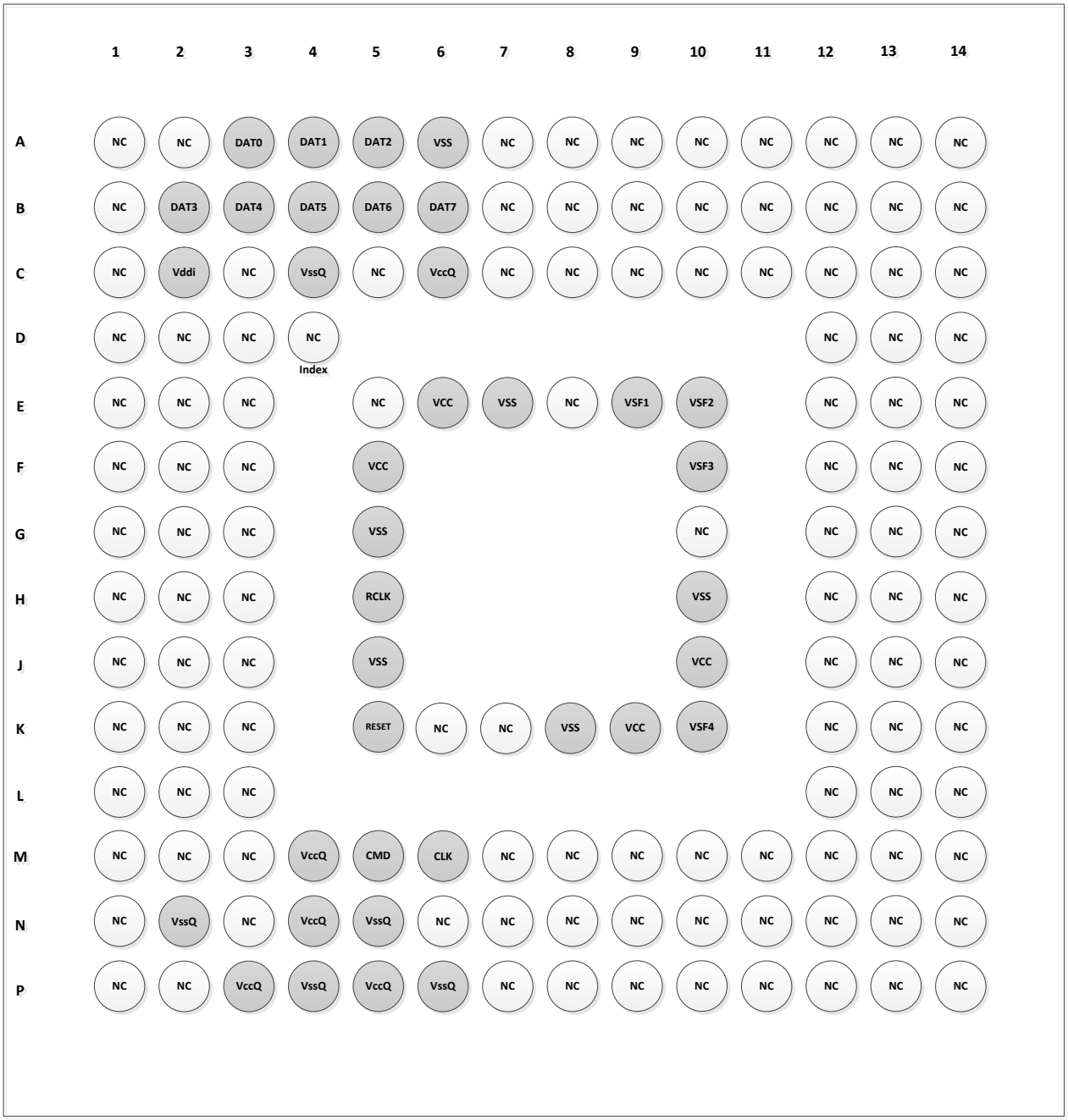

Figure 3 - 153 balls - Ball Array (Top View)

5.2. Pins and Signal Description

Table 13 contains the SanDisk iNAND 7250, with MMC interface (153 balls), functional pin assignment.

Table 11 – Functional Pin Assignment, 153 balls

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n		Hardware Reset
H5	RCLK	Output	Data Strobe
E6	VCC	Supply	Flash I/O and memory power supply
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection
G5	VSS		
H10	VSS		
K8	VSS		
A6	VSS		
J5	VSS		
C4	VSSQ	Supply	Memory controller core and MMC I/F ground connection
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground
E9	VSF1	VSF	Vendor Specific Function balls for test/debug. VSF balls should be floating and be brought out to test pads.
E10	VSF2		
F10	VSF3		
K10	VSF4		

Note: All other pins are not connected [NC] and can be connected to GND or left floating

5.3. Registers value

5.3.1. OCR Register

Parameter	DSR slice	Description	Value	Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7 - 3.6 range	1FFh	9
	[14:8]	VDD: 2.0 - 2.6 range	00h	7
	[7]	VDD: 1.7 - 1.95 range	1h	1

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready.

5.3.2. CID Register

Parameter	DSR slice	Description	Value	Width
MMC MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Card BGA	01h	2
OID	[111:104]	OEM/Application ID	00h	8
PNM	[103:56]	Product name	8GB – DG4008 16GB – DG4016 32GB – DG4032 64GB – DG4064	48
PRV	[55:48]	Product revision	01h	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

Note: Please refer to the definition of the MDT field as defined in e.MMC Spec version 5.0.

5.3.3. DSR Register

Parameter	DSR slice	Description	Value	Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Note: DSR is not implemented; in case of read, a value of 0x0404 will be returned.

5.3.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	3h	3
SPEC_VERS	[125:122]	System specification version	4h	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	8F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0h	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0h	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0h	1
DSR_IMP	[76:76]	DSR implemented	0h	1
*C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	7h	3
C_SIZE_MULT	[49:47]	Device size multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase group size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write protect group size	0Fh	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer default	0h	2
R2W_FACTOR	[28:26]	Write speed factor	2h	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0h	1
CONTENT_PROT_APP	[16:16]	Content protection application	0h	1
FILE_FORMAT_GRP	[15:15]	File format group	0h	1
COPY	[14:14]	Copy flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0h	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0h	1
FILE_FORMAT	[11:10]	File format	0h	2
ECC	[9:8]	ECC code	0h	2
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

5.3.5. EXT_CSD Register

Parameter	ECSD slice	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0h
EXT_SUPPORT	[494]	Extended partitions attribute support	3h
SUPPORTED_MODES	[493]	FFU supported modes	3h
FFU_FEATURES	[492]	FFU features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation codes timeout	10h
FFU_ARG	[490:487]	FFU Argument	0h
BARRIER_SUPPORT	[486]	Cache barrier support	1h
CMDQ_SUPPORT	[308]	Command queue support	1h
CMDQ_DEPTH	[307]	Command queue depth	1Fh
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW sectors correctly programmed	0h
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor proprietary health report	0h
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation type B (MLC)	1h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation type A (SLC)	1h
PRE_EOL_INFO	[267]	Pre EOL information	1h
OPTIMAL_READ_SIZE	[266]	Optimal read size	8h
OPTIMAL_WRITE_SIZE	[265]	Optimal write size	8h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal trim unit size	8h
DEVICE_VERSION	[263:262]	Device version	5025h
FIRMWARE_VERSION	[261:254]	Firmware version	FW Version
PWR_CL_DDR_200_360	[253]	Power class for 200MHz, DDR at VCC= 3.6V	DDh

Parameter	ECSD slice	Description	Value
CACHE_SIZE	[252:249]	Cache size	1000h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power off notification(long) timeout	19h
BKOPS_STATUS	[246]	Background operations status	Default = 0h
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	5Ah
CACHE_FLUSH_POLICY	[240]	Cache Flush Policy	1h
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at VCC = 3.6V	0h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at VCC = 1.95V	DDh
PWR_CL_200_195	[237]	Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	DDh
PWR_CL_200_130	[236]	Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM _MULT	[232]	TRIM Multiplier	3h
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	A6h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	A6h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	20h
ACCESS_SIZE	[225]	Access size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	1h (see WP group size table below)
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	3h
REL_WR_SEC_C	[222]	Reliable write sector count	1h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	10h (see WP group size table below)
S_C_VCC	[220]	Sleep current [VCC]	8GB – 5h 16GB – 6h 32GB – 7h

Parameter	ECSD slice	Description	Value
			64GB – 8h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	Production state awareness timeout	17h
S_A_TIMEOUT	[217]	Sleep/Awake time out	12h
SLEEP_NOTIFICATION_TIME	[216]	Sleep notification timeout	17h
SEC_COUNT	[215:212]	Sector count	See exported capacity table below
SECURE_WP_INFO	[211]	Secure Write Protect Info	1h
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	DDh
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	DDh
PARTITION_SWITCH_TIME	[199]	Partition switching timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	19h
DRIVER_STRENGTH	[197]	I/O Driver Strength	1Fh
CARD_TYPE	[196:195]	Card Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	8h
CMD_SET	[191]	Command Set	Default = 0h

Parameter	ECSD slice	Description	Value
			Updated in runtime
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	Dh
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in runtime by the host
DATA_STRB_MODE_SUPPORT	[184]	Data strobe mode support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h Updated in runtime by the host
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in runtime by the host
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in runtime by the host
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h Updated in runtime by the host
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in runtime by the host
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in runtime
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	20h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	15h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h Updated in runtime by the host
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in runtime by the host

Parameter	ECSD slice	Description	Value
BKOPS_EN	[163]	Enable background operations handshake	2h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by the host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by the host
PARTITIONING SUPPORT	[160]	Partitioning support	7h
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	8GB – 1B5h 16GB – 383h 32GB – 6FFh 64GB – E47h
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host
PARTITION_SETTING_ COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host
GP_SIZE_MULT	[154:143]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
PRODUCTION_STATE_AWARENESS	[133]	Production state awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR mode support	1h
VENDOR_SPECIFIC_FIELD	[127:87]	Vendor Specific Fields	Reserved
PWR_CL_DDR_266	[86]	Maximum power class for HS533	0h
CARD_TYPE_2ND_INDEX	[84]	Device HS533 support	0h
SKU_FEATURES_ID	[80]	7250 SKU identification	0h
VENDOR_SPECIFIC_FIELD	[82:64]	Vendor Specific Fields	Reserved

Parameter	ECSD slice	Description	Value
NATIVE_SECTOR_SIZE	[63]	Native sector size	0h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	Ah
CLASS_6_CTRL	[59]	Class 6 commands control	0h
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in runtime
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h Updated in runtime
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Updated in runtime by the host
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h
BARRIER_CTRL	[31]	Cache barrier	0h
MODE_CONFIG	[30]	Mode config	0h
MODE_OPERATION_CODES	[29]	Mode operation codes	0h
FFU_STATUS	[26]	FFU status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Pre loading data size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max pre loading data size	See Max Preloading size table below
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product state awareness enablement	3h AUTO_PRE_SOLDERING
SECURE_REMOVAL_TYPE	[16]	Secure Removal Type	8h
CMDQ_MODE_EN	[15]	Command queue	0h

5.3.6. User Density

The following table shows the capacity available for user data for the different device sizes:

Table 12 – Exported capacity for user data

Capacity	LBA [Hex]
8GB	0xE90E80
16GB	0x1D5A000
32GB	0x3A3E000
64GB	0x7670000

Table 13 - Write protect group size

Capacity	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
8GB	0x1	0x10	0.5MB	8MB
16GB	0x1	0x10	0.5MB	8MB
32GB	0x1	0x10	0.5MB	8MB
64GB	0x1	0x10	0.5MB	8MB

The max preloading image in iNAND 7250 is up to the exported capacity per table below

Table 14 - Max Preloading Data Size

Capacity	Max preloading Image size (in LBA HEX)
8GB	0xE90E80
16GB	0x1D5A000
32GB	0x3A3E000
64GB	0x7670000

6. HW APPLICATION GUIDELINES

6.1. Design Guidelines

- The e.MMC specification enforces single device per host channel; multi-device configuration per a single host channel is not supported.
- CLK, RCLK(DS), CMD and DATx lines should be connected to respected host signals. The e.MMC specification requires that all signals will be connected point-to-point, i.e. a single e.MMC device per host channel.
- The e.MMC hardware reset signal (RST_n) is not mandatory and could be connected to the host reset signal or left unconnected (floating) if not used.
- All power supply and ground pads must be connected.
- Make sure pull-up resistors are placed on schematic in case these are external. For further details please refer to “Table 16 - Pull-ups Definition”
- Bypass capacitors shall be placed as close to the e.MMC device as possible; normally it is recommended to have 0.1uF and 4.7uF capacitors per power supply rail, though specific designs may include a different configuration in which there are more than two capacitors:
    - VCC and VCCQ slew rates shall be minimally affected by any bypass capacitors configuration
    - It is recommended to verify the bypass capacitors requirement in the product data sheet
- VDDi bypass capacitor shall be placed on the PCB. The VDDi is an internal power node for the controller and requires capacitor in range 0.1uF – 2.2uF connected between VDDi pad and ground
- Vendor Specific Function (VSF) pins should be connected to accessible test points on the PCB (TP on schematic below). It’s recommended to have accessible ground (GND) pads near each TP on PCB
- It is recommended to layout e.MMC signals with controlled impedance of 45-55 Ohm referencing to adjusted ground plane

6.2. Capacitor Selection & Layout Guidelines

SanDisk iNAND 7250 has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 17 below.

Table 15 - 7250 Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges: Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range: High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

It is recommended that the power domains connectivity will follow figure 4:

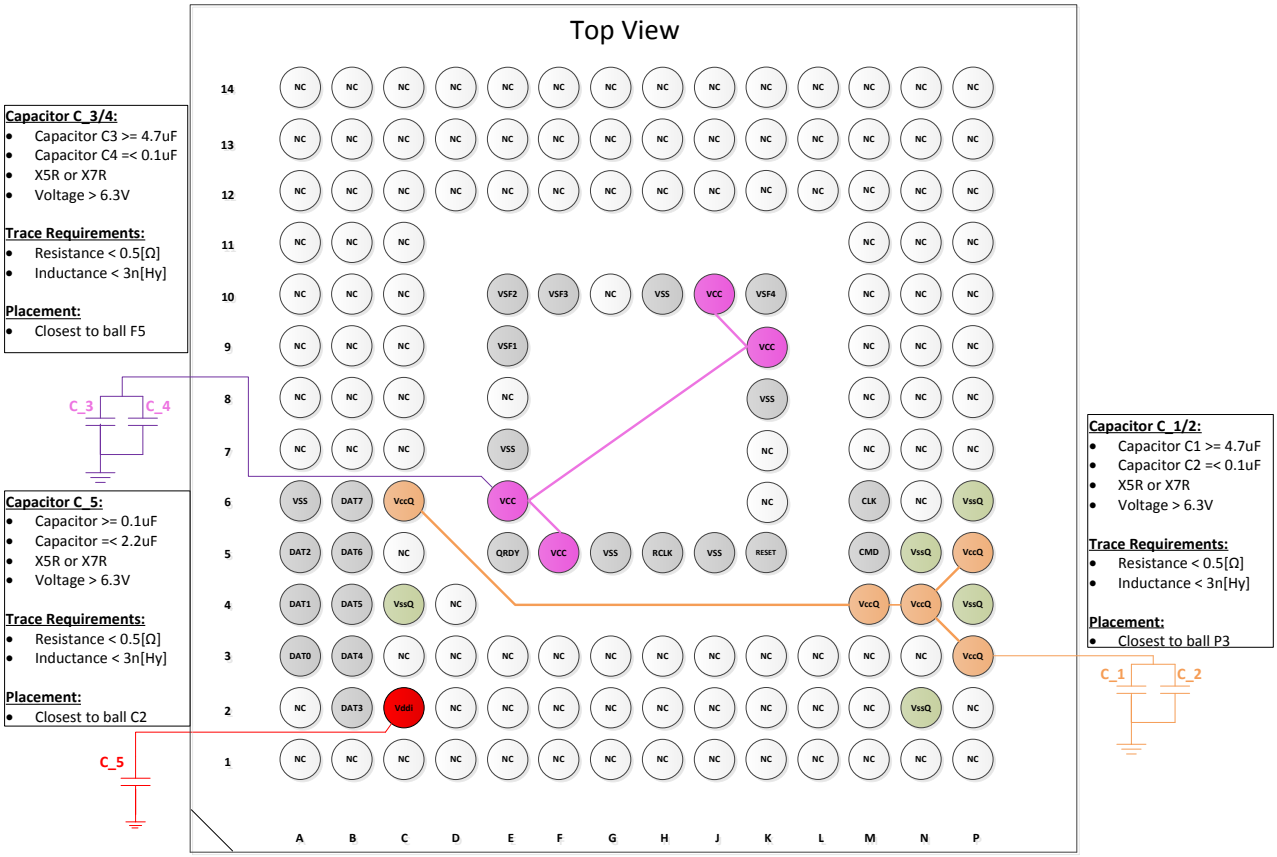

Figure 4 - Recommended Power Domain Connectivity

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends final PCB layout.

For clarity, the diagram does not include VSS connection. All balls marked VSS shall be connected to a ground (GND) plane.

It is recommended to use a X5R/X7R SMT-Ceramic capacitors rated for 6.3V/10V with footprint of 0402 or above.

When using ceramic capacitor, it should be located as close to the supply ball as possible. This will eliminate mounting inductance effects and give the internal IC rail a cleaner voltage supply

Make all of the power (high current) traces as short, direct, and thick as possible. The capacitors should be as close to each other as possible, as it reduces EMI radiated by the power traces due to the high switching currents through them. In addition, it shall also reduce mounting inductance and resistance as well, which in turn reduces noise spikes, ringing, and IR drop which produce voltage errors.

The grounds of the IC capacitors should be connected close together directly to a ground plane. It is also recommended to have a ground plane on both sides of the PCB, as it reduces noise by reducing ground loop.

The loop inductance per capacitor shall not exceed 3nH (both on VCC/VCCQ & VSS/VSSQ loops).

Cin2 shall be placed closer (from both distance & inductance POV) to the iNAND power & ground balls.

Multiple via connections are recommended per each capacitor pad. It is recommended to place the power and ground vias of the capacitor as close to each other as possible.

On test platforms, where the iNAND socket is in use, the loop inductance per capacitor shall not exceed 5nH (both on VCC/VCCQ & VSS/VSSQ loop).

No passives should be placed below the iNAND device (between iNAND & PCB).

VSF balls (VSF1/4) should have exposed and floated test pads on the PCB, with near exposed GND for better measurement.

Signal Traces:

- Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
- Traces should be45-55 ohm controlled impedance.

6.3. Reference Schematics

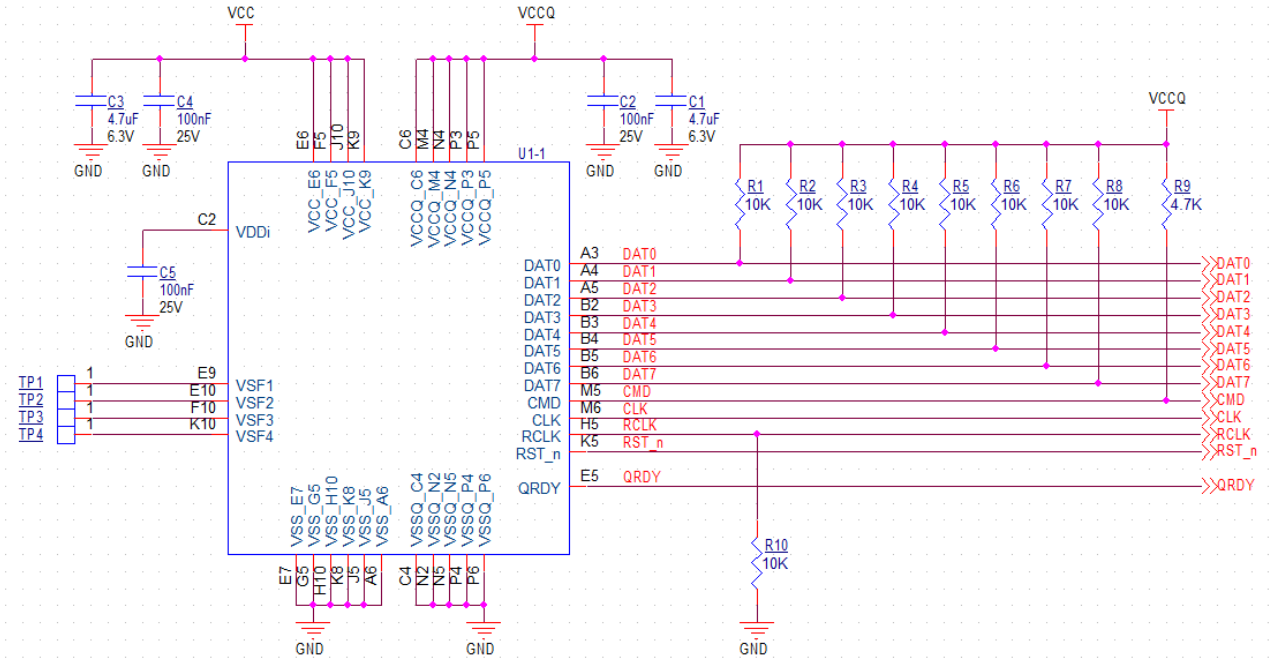

Figure 5 – e.MMC Reference Schematics

Table 16 – Pull-ups Definition

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for DAT0–7	R_{DAT}	10		100[10]	Kohm	to prevent bus floating
Pull-up resistance for CMD	R_{CMD}	4.7		100	Kohm	to prevent bus floating
Pull-down resistance for Data Strobe (RCLK)	R_{PD}	10		47	Kohm	At HS400 mode

Recommended capacitors:

CAPACITOR VALUE	MANUFACTURER	MANUFACTURER P/N
4.7uF	MURATA	GRM185R60J475ME15D
	TAIYO YUDEN	JMK107BJ475MK-T
0.1uF	MURATA	GRM155R71A104KA01D
	KYOCERA	CM05X5R104K06AH
2.2uF	PANASONIC	ECJ0EB0J225M
	SAMSUNG	CL05A225MQ5NSNC

[10] Recommended maximum pull-up is 50Kohm for 1.8V interface supply voltages. A 3V part may use the whole range up to 100Kohms

7. PROPRIETY iNAND 7250 FEATURE OVERVIEW

7.1. Device Report

The iNAND 7250 Device Report feature reflects the firmware and device status.

- Enabling Device Report Mode: Send CMD62 with argument of 0x96C9D71C - R1b Response will be returned
- Reading Device Report Data: Once the host enters Device Report mode, CMD63 with argument 0x00000000 will retrieve the report - 512 Bytes will be returned to the host (Note: CMD63 behaves similarly to CMD17)
- Resume Normal Operation Mode: Once the Device Report read command (CMD63) was completed, the device automatically goes out of Device Report mode, and resumes normal operation mode.

7.1.1. Device Report fields

Byte Offset	Size (Bytes)	Field	Comments
[3:0]	4	Avg Erase Count System	Average erase value across all **system** blocks
[7:4]	4	Reserved	
[11:8]	4	Avg Erase Count MLC	Average erase value across all **MLC** blocks
[15:12]	4	Read Reclaim Count System	Number of reads of **system** data which passed read-scrub thresholds and require reclaim
[19:16]	4	Reserved	
[23:20]	4	Read Reclaim Count MLC	Number of **MLC** reads which passed read-scrub thresholds and require reclaim
[27:24]	4	Bad Block Manufacturer	Total bad blocks detected during manufacturing process
[31:28]	4	Bad Block Runtime System	Total bad blocks in **system** partitions detected during run-time
[35:32]	4	Reserved	
[39:36]	4	Bad Block Runtime MLC	Total bad blocks in **MLC** partition detected during run-time
[43:40]	4	Patch Trial Count	Number of secure field firmware updates (sFFU) done from the beginning of the device life
[55:44]	12	Patch Release Date	Current sFFU release date
[63:56]	8	Patch Release Time	Current sFFU release hour
[67:64]	4	Cumulative Write Data Size In 100MB	Total bytes written from the host in multiples of 100 MB
[71:68]	4	VCC Voltage Drop Occurrences	Number of ungraceful power downs to the device. Counter may be inaccurate due to uncommitted counter updates during repeated voltage drops .
[75:72]	4	VCC Voltage Droop Occurrences	Number of power-droops (slight power-droop below a threshold and for a very short period of time)
[79:76]	4	Failures to Recover New Host Data After Power Loss	Counts times new host data is discarded due to power loss

[83:80]	4	Recovery Operations After Voltage Droop	Number of recovery operations done by the device while power-droop detected
[511:84]	428	Reserved	

7.2. Power-Loss indications

iNAND 7250 is also serving the host by notifying him on cases of Power-Loss events and internal handling of those events. A dedicated field in the EXT_CSD register was allocated to indicate the occurrence of Power Loss/Write Abort during the last power down. This field reports if a Power Loss was detected and recovered during the last power-up.
In order to retrieve this field, the host should issue CMD8 command – SEND_EXT_CSD. This command returns full EXT_CSD structure – 512 bytes as block of data. Following is the EXT_CSD field details:

Name	Field	Size (bytes)	Cell Type	Hex Offset	Dec. Offset
Power Loss indication	POWER_LOSS_REPORT	1	R	0x79	121

POWER_LOSS_REPORT[121] details:

- Bit[2]: RECOVERY_SUCCESS
  0x1: Recovery passed successfully
  0x0: Recovery failed
- Bit[1]: RECOVER_OLD_DATA
  0x1: Recovery to old copy of data
  0x0: No data recovery required
- Bit[0]: POWER_LOSS_DETECTED
  0x1: Unexpected Power Loss was detected - Detection is done during initialization, immediately after Power-Up

Note: In case Power Loss did not occur on last shut down, this register will show 0x00

7.2.1. Unstable Power-Supply indications

In case of Flash voltage drop, the iNAND may not be able to recover the data that was already transferred to the iNAND device, but wasn't committed in the Flash. In this case the iNAND will "abort" the current host write and return back to the host with an error indication.

iNAND 7250 will use BIT19 and BIT20 (cc_error) in the command response to indicate VDET error status to the host. the VDET error indication can be seen only if CMD13 was issued, or in the next command response.

Examples:

- Open Mode (CMD25+CMD12+CMD13):
  In both cases, where the voltage droop occurs before or after CMD12:
  CMD12 response will not have BIT19 and BIT20 set.
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response

Note: The host may send many CMD13 and the BIT19 will be set only in first CMD13 after releasing the busy.

- Close Mode (CMD23+CMD25+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
- Single Block Mode (CMD24+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response

Host shall retry latest command as long as the VDET error indication on CMD13 response (or next command response (BIT19 and BIT20 are set) is still set

7.3. Unified Boot

iNAND 7250 Unified Boot is a proprietary feature that allows the host to boot from a secondary boot partition without the need to explicitly switch to the secondary partition. When this feature is enabled, the device will transfer the data from both boot partitions to the host, first from the enabled boot partition followed by the other partition.

A typical use case is to guarantee a version of the boot will always be valid in case of Over The Air (OTA) boot update. The host can set one boot partition as permanent write protect (never to be changed) and the other as temporary write protect. The second boot will be used for update. In case OTA is corrupted or fail, host will always be able to boot based on the old version saved in boot one.

This feature is only supported on FW version CS2.2.

7.3.1. Unified Boot Support Indication

EXT_CSD Field Name	Bit(s)	Value	Description
UNI_BOOT_PROC_SUPPORT[93]	[0] Read Only	0x0 0x1	Device doesn't support Unified Boot Device supports Unified Boot

7.3.2. Enable Unified Boot

EXT_CSD Field Name	Bit(s)	Default	Description
UNI_BOOT_PROC_ENABLE[92]	[0-7] R/W	0x0 0xF2	Unified Boot is disabled Unified Boot is enabled

7.3.3. Important Considerations

The configuration of unified boot can only be performed once at the beginning of life of a device, before any data is transferred to it. After all of the parameters have been specified and committed to the device, it cannot be changed.

This functionality is disabled if either of the boot partitions have ever been write protected. The amount of data transferred for each partition is equal to the partition size, regardless of the size of the programmed image.

7.4. Hardware Pin Secure Boot

Per JEDEC e.MMC 5.1 definition, e.MMC boot partitions have 3 write protection methods:

1. Permanent Write Protection – once set, boot data cannot be written
2. Power-on Write Protection – once set, boot data cannot be written until a device reset
3. Secure Write Protection – host may set/clear write protection using a secure key

iNAND 7250 introduces a fourth method that works ***in conjunction with*** a permanently write protected boot partition.

4. Hardware Pin Secure Boot - a physical authentication procedure is required using VSF pin #4 which is verified by the device controller in order to authorize writing to a boot partition.

The physical authentication requires the host to keep VSF pin #4 at ground voltage level and restore it to floating state after the device power-up sequence is complete. This procedure would authorize the user to write to the permanently protected boot partition. Upon reset of the device the authorization to update the boot partition would be aborted and permanent write protection is restored.
Host can implement this feature by enabling a push button switch on the platform that would generate the signal below.

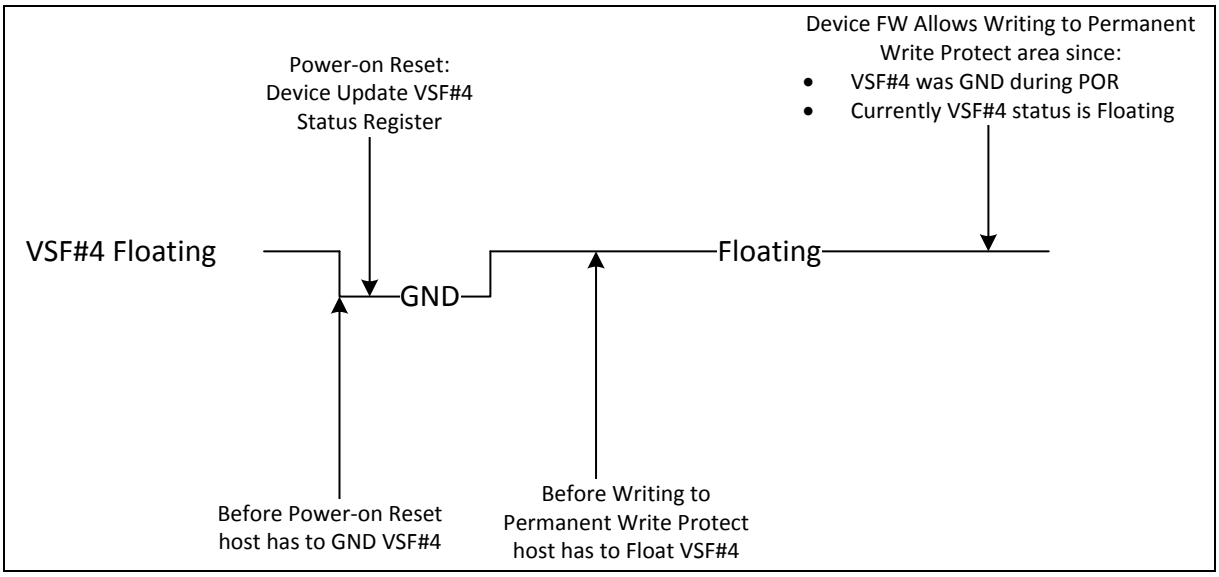

Figure 6 Power-on Sequence

This feature is only supported on FW version CS2.2.

7.4.1. Requirements

This feature is designed only for the boot partitions. It works only in addition to boot partition permanent write protection. It will not work with power-on write protection of the boot partitions. Also, it will not work with whole device permanent or temporary write protection.

7.4.2. Physical Proof Protocol Support Indication

EXT_CSD Field Name	*Bit(s)*	*Value*	*Description*
PPP_FEATURES_SUPPORT[123]	*[0] Read Only*	*0x0* *0x1*	*Device does not support HW pin* *Device supports HW pin*

7.4.3. Enable Physical Proof Protocol

EXT_CSD Field Name	*Bit(s)*	*Default*	*Description*
PPP_FEATURES_ENABLE[122]	*[0] R/W*	*0x0* *0x1*	*PPP features are disabled* *PPP features are enabled*

7.4.4. Configuration Process

NOTE: This feature must be enabled BEFORE setting permanent write protection on the boot partitions.

Step 1: Check PPP_FEATURES_SUPPORT bit 0 to determine that this feature is supported.

Step 2: Set PPP_FEATURES_ENABLE bit 0 to 1 to indicate PPP features will be used.

Step 3: Set permanent write protection of the boot partitions (BOOT_WP[173] = 0x04).

7.4.5. Authentication Process

Step 1: Host must set VSF #4 to GND before, during and for at least 2 seconds after POR.

Step 2: Host must return VSF #4 to floating state.

Step 3: If the device has determined that all the proper authentication criteria have been met, the host may now write to the protected boot partitions.

NOTE: Once authenticated, the boot partitions are write enabled until the next POR.

8. MARKING

First row: Simplified SanDisk Logo
Second row: Sales item P/N
Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'
* No ES marking for product in mass production.
Fourth row: Y- Last digit of year
WW- Work week
D- A day within the week.
MTLLLXXX – Internal use
2D barcode: Store the 12 Digital ID information as reflected in the fourth row.

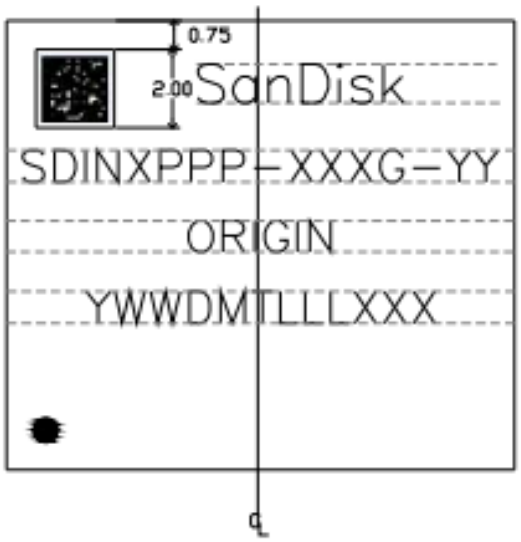

Figure 7 - Product marking 8GB-64GB

9. ORDERING INFORMATION

Table 17 – Ordering Information (-25℃ to +85℃ ambient)

Capacity	Technology	Part Number	Samples Part Number	Package	e.MMC
8GB	15nm X2 eMLC	SDINBDG4-8G	SDINBDG4-8G-Q	11.5x13x0.8mm	5.1
16GB	15nm X2 eMLC	SDINBDG4-16G	SDINBDG4-16G-Q	11.5x13x0.8mm	5.1
32GB	15nm X2 eMLC	SDINBDG4-32G	SDINBDG4-32G-Q	11.5x13x1.0mm	5.1
64GB	15nm X2 eMLC	SDINBDG4-64G	SDINBDG4-64G-Q	11.5x13x1.2mm	5.1

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