Preliminary Data Sheet - Confidential

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SanDisk® iNAND® 8521 Embedded Flash Drive

Universal Flash Storage (UFS) Version 2.1 with Gear3 / 2 Lane Interface

REVISION HISTORY

DOC. NO	REVISION	DATE	DESCRIPTION
DOC-12571	1.00	20-Feb-2018	Initial version
DOC-12571	1.01	21-Feb-2018	Minor fixes
DOC-12571	1.02	27-Feb-2018	Updates on reliability section
DOC-12571	1.03	19-Mar-2018	Updates sections 2.1, 5.2, 7.2.3
DOC-12571	1.04	21-Mar-2018	Updates sections 2.1

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1. INTRODUCTION

The SanDisk® iNAND® 8521 embedded flash drive features a Universal Flash Storage Version 2.1 (UFS v2.1) Gear3 / 2 Lane Interface. It provides superior performance suited for demanding mobile applications.

1.1. General Description

The SanDisk® iNAND® products are embedded flash drives (EFDs) designed to boost the overall performance of existing flash-based product lines, such as smartphones, tablets and automotive infotainment systems, and to enable manufacturers to bring the benefits of flash memory (rapid boot-up, high reliability, robustness, consistent performance) to new markets such as entry-level notebooks.

iNAND technology combines an embedded thin flash controller with advanced triple-level cell (TLC) NAND flash technology enhanced with embedded flash management software running as firmware on the flash controller. iNAND 8521 EFDs optimize performance and power by meeting JEDEC's UFS v2.1industry standard, which is based on the MIPI M-PHY specification for the physical layer.

The iNAND 8521 product is based on SanDisk 256Gb X3 3D NAND memory, using 64-layer technology. The memory architecture brings new levels of density, scalability and performance to the embedded flash drives. Western-Digital 3D NAND memory also provides enhanced write/erase endurance, write speeds, and energy efficiency relative to conventional 2D NAND.

1.2. Plug-and-Play Integration

The iNAND architecture is optimized to eliminate the need for complicated software integration and testing processes, thereby enabling plug-and-play integration into the host system. The replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This allows manufacturers to adopt advanced NAND flash technologies and update product lines with minimal integration or qualification efforts.

With JEDEC form factors measuring 11.5x13 mm (153 balls) for all capacities, the iNAND 8521 EFD is ideally suited for high-end mobile handsets, tablets, and automotive infotainment.

iNAND 8521 features a UFS interface, which allows for easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 below shows a block diagram of the SanDisk iNAND 8521 with UFS Interface.

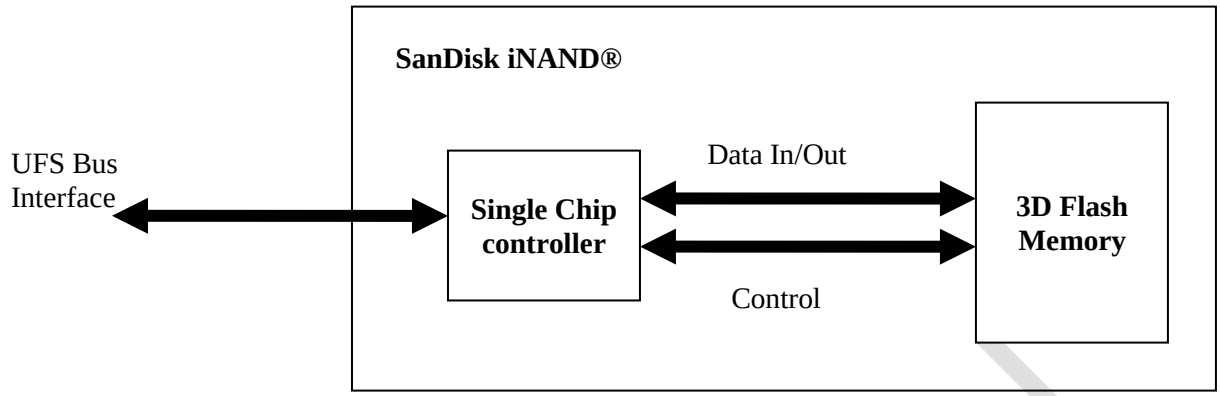


Figure 1 - iNAND® Interface Block Diagram

1.3. Feature Overview

The SanDisk® iNAND® 8521 embedded flash drive, with UFS v 2.1 interface, includes the following features:

- Memory controller and NAND flash
- Mechanical design compliant with the JEDEC Specification
- Offered in VFBGA153 package of UFS v2.1[1] 11.5mm x 13mm x 1.0mm (32GB-256GB)
- Operating temperature range of –25C° to +85C°
- Dual power system
- Core voltage (VCC) of 2.7-3.6 V
- I/O voltage (VCCQ2) of either: 1.7-1.95 V or 2.7-3.6 V
- Up to 256 GB of data storage
- UFS JEDEC specification version. 2.1 compliance
- Differential interface based on MIPI M-PHY together with the MIPI UniPro specifications
- Up to 800 MB/s bus transfer rate, using high-speed Gear3 and 2-Lane physical signals
- 8 bit-by-10 bit line coding, as defined by MIPI M-PHY
- Correction of memory field errors
- Design optimized for portable and stationary applications that require high performance and reliable data storage.

1.4. Defect and Error Management

The SanDisk® iNAND® 8521 embedded flash drive contains a sophisticated defect and error management system for exceptional data reliability. iNAND 8521 EFDs will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume additional user data space. In the extremely rare case that a Read error does occur, iNAND has innovative algorithms to recover the data.

[1] Refer to JEDEC Standards No. JESD84-B51

1.5. Power Supply

Table 1 – Power supply voltage

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage (memory)	VCC	2.7	3.6	V	
Supply Voltage (Reserved for Future Use, not required for current product)	VCCQ	1.1	1.3	V	JESD8-12A Can be left N/C
Supply Voltage (controller and IO)	VCCQ2	1.70	1.95	V	
Supply Power-Up for 3.3V	tPRUH		35	ms	5 µsec as minimal supply ramp up slew rate recommended
Supply Power-Up for 1.8V	tPRUL		25	ms	

2. PRODUCT SPECIFICATIONS

2.1. Typical Power Requirements

Table 2 – iNAND 8521 **Power Consumption Standby** (Ta=25°C@3.3/1.8V)

INTERFACE	SUPPLY VOLTAGE	32GB	64GB	128GB	256GB	UNITS
G3 2Lane	SSU VCC (off)	0	0	0	0	µA
	SSU VCCQ2	500	500	500	500	µA
	Standby Total Power	0.9	0.9	0.9	0.9	mW
G3 2Lane	Auto standby VCC	25	50	100	200	µA
	Auto standby VCCQ2	500	500	500	500	µA
	Auto Standby Total Power	1.0	1.1	1.2	1.6	mW

Table 3 - iNAND 8521, **Power Consumption Peak** (Max) VCC / VCCQ (Ta=25°C@3.3V/1.8V)

INTERFACE	SUPPLY VOLTAGE	32GB	64GB	128GB	256GB	UNITS
G3 2Lane	Peak [2µs window] VCC	250	400	580	600	mA
	Max [1ms window] VCCQ2	300	400	400	400	mA

Table 4 - iNAND 8521, **Power Consumption RMS** (Max) VCC / VCCQ (Ta=25°C@3.3V/1.8V)

INTERFACE	SUPPLY VOLTAGE	32GB	64GB	128GB	256GB	UNITS
G3 2Lane	RMS [100ms window] VCC Read	100	200	220	240	mA
	RMS [100ms window] VCCQ2 Read	250	300	310	310	mA
	Total power Read	0.8	1.2	1.3	1.4	W
	RMS [100ms window] VCC Write	60	120	180	180	mA
	RMS [100ms window] VCCQ2 Write	230	260	280	280	mA
	Total power	0.6	0.9	1.1	1.1	W

2.2. Operating Conditions

2.2.1. Operating and Storage Temperature Specifications

Table 4 - Operating and Storage Temperatures

Temperature	Minimum and Maximum Operating*	-25° C to 85° C
	Minimum and Maximum Non-Operating: After soldered onto PCBA	-40° C to 85° C

2.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND 8521 is MSL = 3.

2.3. Reliability

The SanDisk® iNAND® 8521 embedded flash drive meets or exceeds the endurance and data retention requirements for NAND type products in accordance with evaluated representative usage models for the target market and relevant sections of the JESD47I standard.

Table 5 - Critical Reliability Characteristics

RELIABILITY CHARACTERISTICS	DESCRIPTION		VALUE
Uncorrectable Bit Error Rate (UBER)	Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events data can be lost.	Read workload Ratio of reads to writes is greater than or equal to 99:1	**1 sector in 10^{12} bits read**
		Mixed workload Ratio of reads to writes is less than 99:1	**1 sector in 10^{15} bits read**

Write Endurance Specification (TBW)	Write endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload and temperature mission profile:
	Representative workload description:
	• 62% Sequential write, 38% Random Write Distribution of IO Transaction Sizes:
	  ○ <16KB: 82%
	  ○ 16KB-128KB: 17%
	  ○ >128KB: 1%
	• Cache On, Packed Off
	• Host data is 4K aligned
	
	Max temperature mission profile:
	• 30% of product lifetime: @85° C T-case
	• 70% of product lifetime: @55° C T-case
			Total Terabytes Written [TBW] Per representative Android workload:
			32GB: 35[TB]
			64GB: 70[TB]
			128GB: 140[TB]
			256GB: 280[TB]

Data Retention Specification (Years)	Fresh or Early Life Device (A device whose total write cycles to the flash is less than 10% of the maximum endurance specification)		**10 years of Data Retention @ 55°C**
	Cycled Device (Any device whose total write cycles are between 10% of the maximum write endurance specification and equal to or exceed the maximum write endurance specification)		**1 year of Data Retention @ 55°C** Note: In the case where the number of writes exceed the endurance spec read and Write performance can be intermediately reduced.

2.4. Typical System Performance

Table 6 – Typical Sequential Performance

	G3 2LANE	
	Write (MBs)	**Read (MBs)**
32GB	200	350
64GB	400	700
128GB	550	800
256GB	550	800

Table 7 – Typical Random Performance

	G3 2LANE	
	Write (IOPs)	**Read (IOPs)**
	CACHE ON	**QD=32**
32GB	30,000	15,000
64GB	40,000	30,000
128GB	45,000	50,000
256GB	45,000	40,000

Note 1: Sequential Read/Write performance is measured under Gear3/2-Lane mode with a bus, chunk size of 512KB, and data transfer of 1GB.

Note 2: Random Read/Write performance is measured under Gear3/2-Lane mode with a bus, with a chunk size of 4KB and address range of 1GB.

Note 3: All performance is measured using WDC proprietary test environment, without file system overhead and host turn-around time (HTAT).

Note 4: Sequential Write performance is measured for 100MB host payloads.

3. PHYSICAL SPECIFICATIONS

The SanDisk® iNAND® 8521 embedded flash drive is packaged in a 153-pin, thin, fine-pitched ball grid array (VFBGA153-1113-0.50). See Figures 2/3/4, and Table 8 for physical specifications and dimensions.

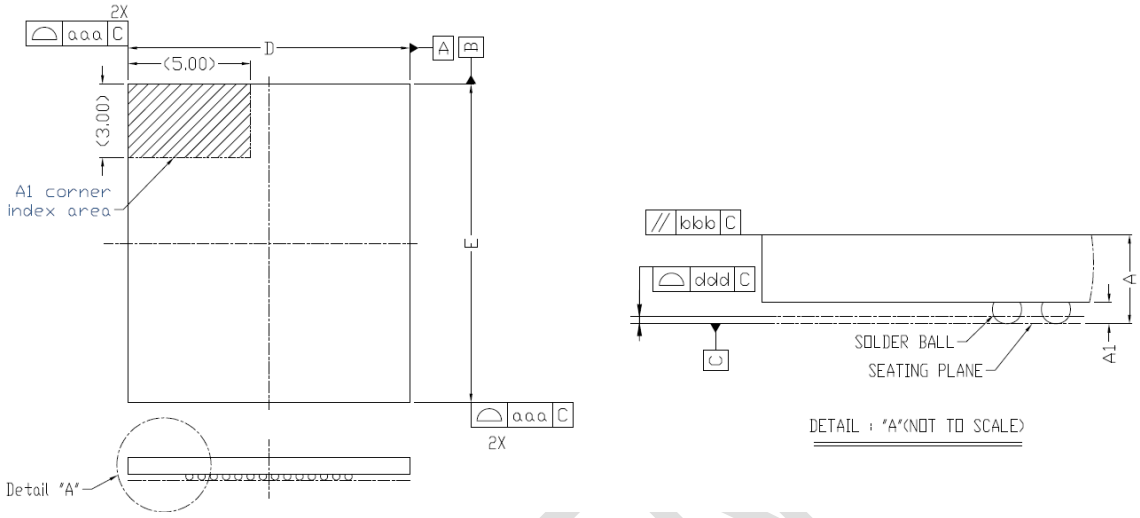


Figure 2 – iNAND 8521 – Package Outline Drawing – Top and Side View

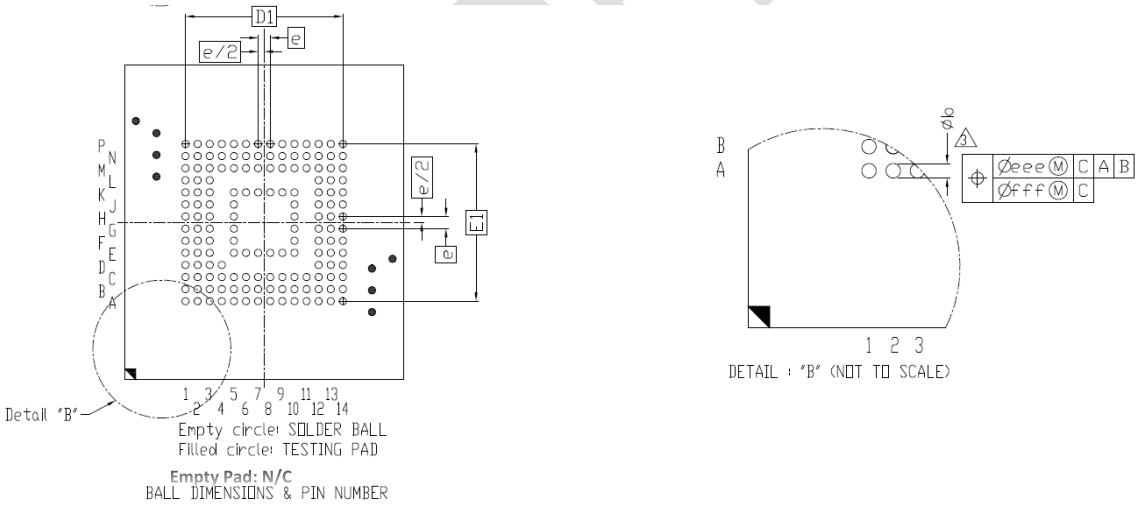


Figure 3 – iNAND 8521 – Package Outline Drawing – Bottom View

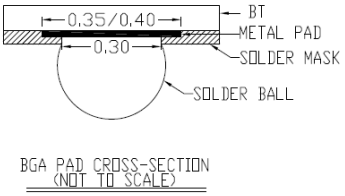


Figure 4 – iNAND 8521 – Package Outline Drawing – BGA Pad View

Table 8 – Package Specification (All Capacities):

32GB/64GB/128GB/256GB			
	DIMENSION IN MILLIMETERS		
Symbol	Minimum	Nominal	Maximum
A	0.8	-	1.0
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13	13.1
D1	-	6.5	-
E1	-	6.5	-
e	-	0.5	-
b	0.25	0.3	0.35
aaa	0.1		
bbb	0.1		
ddd	0.08		
eee	0.15		
fff	0.05		

4. INTERFACE DESCRIPTION

4.1. UFS I/F Ball Array

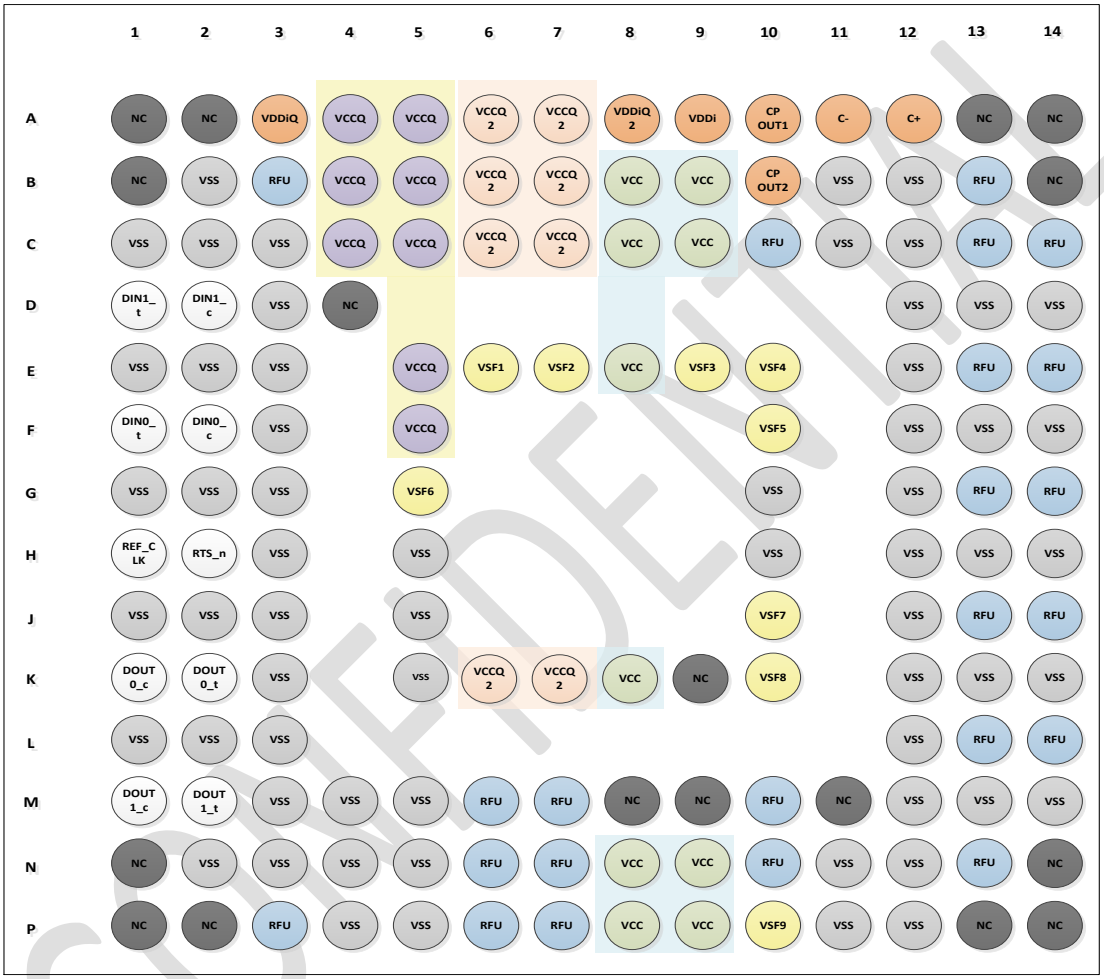


Figure 5 - 153 balls - Ball Array (Top View)

4.2. Reference schematics

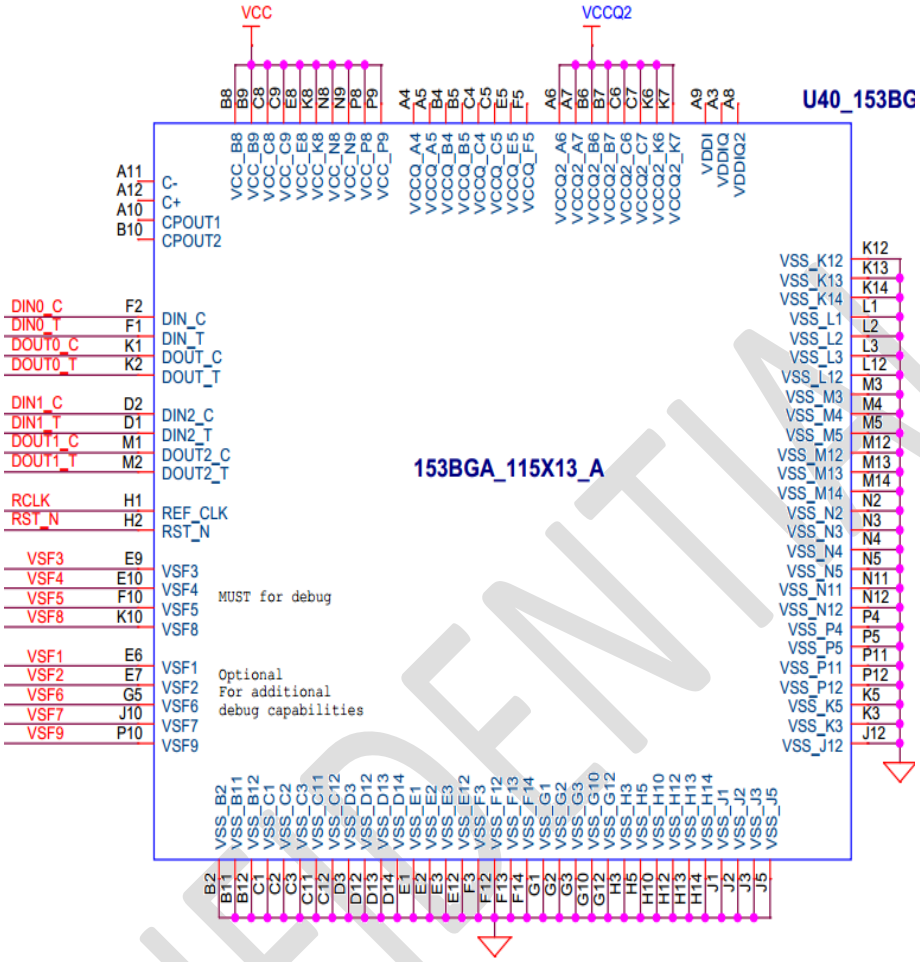


Figure 6 – Package Schematics

4.3. Pins and Signal Description

Table 9 contains the SanDisk® iNAND® 8521 embedded flash drive, with MMC interface (153 balls), functional pin assignment.

Table 9 – Functional Pin Assignment, 153 Balls

BALL NAME	TYPE	DESCRIPTION
VCC	Supply	Supply voltage for the memory devices.
VCCQ	Supply	Supply voltage used typically for the memory controller and optionally for the PHY interface and any other internal very low voltage block.
VCCQ2	Supply	Supply voltage used typically for the PHY interface and the memory controller or memory interface and any other internal low voltage block.
VDDiQ	Input	Input terminal to provided bypass capacitor for VCCQ internal regulator typically related to the memory controller or the PHY interface.
VDDiQ2	Input	Input terminal to provide bypass capacitor for VCCQ2 internal regulator, typically related to memory interface
VDDi	Input	Input terminal to provide bypass capacitor for VCC internal regulator.
VSS	Supply	Supply voltage ground.
RST_n	Input	Input hardware reset signal. This is an active low signal.
REF_CLK	Input	Input reference clock. When not active, this signal should be pull down or driven low by the host SoC.
DIN0_t / DIN1_t	Input	Downstream data lane0 and data lane1. These are differential input signals into UFS device from the host.
DIN0_c / DIN1_c	Input	
DOUT0_t / DOUT1_t	Output	Upstream data lane0 and data lane1. These are differential output signals from the UFS device to the host.
DOUT0_c / DOUT1_c	Output	
C+	Input	Optional charge pump capacitor, positive terminal.
C-	Input	Optional charge pump capacitor, negative terminal.
NC	-	No Connect. NC pins can be connected to ground or left floating.
RFU	-	Reserved for Future Use. RFU pins should be left floating.
VSFn	-	Vendor Specific Function. VSFn (n=1-9) pins should be left floating. Each vendor is able to use these pins during manufacturing.

Note: All other pins are not connected [NC] and can be connected to GND or left floating

5. UFS DESCRIPTORS, ATTRIBUTES, FLAGS AND USER DENSITY

5.1. Device Descriptor

Table 10 – Device Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x40	Descriptor Size
bDescriptorIDN	0x01	0x00	Device Descriptor Type Identifier
bDevice	0x01	0x00	Device Type
bDeviceClass	0x01	0x00	UFS Device Class (00h: Mass Storage)
bDeviceSubClass	0x01	0x00	UFS Mass Storage Subclass (00h: Embedded Bootable)
bProtocol	0x01	0x00	Protocol Supported (00h: SCSI)
bNumberLU	0x01	0x01	Number of Logical Units
bNumberWLU	0x01	0x04	Number of Well-Known Logical Units
bBootEnable	0x01	0x00	Bootable
bDescrAccessEn	0x01	0x00	Descriptor Access Enable
bInitPowerMode	0x01	0x01	Initial Power Mode
bHighPriorityLUN	0x01	0x7f	High Priority LUN
bSecureRemovalType	0x01	0x00	Secure Removal Type
bSecurityLU	0x01	0x01	Support Security LU
bBackgroundOpsTermLat	0x01	0x0F	Background Operations Termination Latency
bInitActiveICCLevel	0x01	0x0F	Initial Active ICC Level
wSpecVersion	0x02	0x0210	Specification Version
wManufactureDate	0x02	0x0116	Manufacturing Date
iManufacturerName	0x01	0x00	Index to the string which contains the Manufacturer Name Manufacture Name String Length: 0x12 Manufacture Name String Type: 0x5 Manufacture Name String (UNICODE): “WDC”
iProductName	0x01	0x01	Index to string containing Product Name Product Name String Length: 0x22 Product Name String Type: 0x5 Product Name String (UNICODE): • 32GB - "SDINDDH4-32G" • 64GB - "SDINDDH4-64G" • 128GB - "SDINDDH4-128G" • 256GB - "SDINDDH4-256G"
iSerialNumber	0x01	0x03	Index to string containing Serial Number Serial Number String Length: 0x1A Serial Number String Type: 0x5 Serial Number String (UNICODE): • BYTE 0: CRC • BYTE 1-3: MANFICTURING DATE/MONTH/YEAR

			• BYTE 4-7: RANDOM NUMBER • BYTE 8-11: RFU
iOemID	0x01	0x04	Index to string containing OEM ID OEM ID String Length: 0x32 OEM ID String Type: 0x5 OEM ID String (UNICODE): " "
wManufacturerID	0x02	0x0145	Manufacturer ID (as defined in JEDEC)
bUD0BaseOffset	0x01	0x10	Unit Descriptor 0 Base Offset
bUDConfigPLength	0x01	0x10	Unit Descriptor Configuration Length
bDeviceRTTCap	0x01	0x02	Maximum Number of Outstanding RTTs Supported
wPeriodicRTCUpdate	0x02	0x0000	Frequency and Method of Real-Time Clock Update
bUFSFeaturesSupport	0x01	0x01	UFS Features Support. This field indicates which features are supported by the device
bFFUTimeout	0x01	0x07	Field Firmware Update Timeout
bQueueDepth	0x01	0x20	Queue-Depth
wDeviceVersion	0x02	0x0000	Firmware Release ID
bNumSecureWPArea	0x01	0x20	Number of Secure Write Protect Areas
dPSAMaxDataSize	0x04	0x00000000	PSA Maximum Data Size
bPSAStateTimeout	0x01	0x11	PSA State Timeout
iProductRevisionLevel	0x01	0x02	Index to string containing Product Revision Level Product Revision String Length: 0xA Product Revision String Type: 0x5 Product Revision String (UNICODE): Firmware version Release • CH[0-1]: Major FW version (RC#) • CH[2-3]: Minor FW version (Build#)

5.2. Unit 0…31 Descriptor

Table 11 – Unit 0…31 Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x23	Size of this descriptor
bType	0x01	0x02	Unit Descriptor Type Identifier
bUnitIndex	0x01	0x0 - 0x1f	Unit Index
bLUEnable	0x01	0x01	Logical unit enable
bBootLunID	0x01	0x00	Boot LUN ID
bLUWriteProtect	0x01	0x00	Logical Unit Write Protect
bLUQueueDepth	0x01	0x00	Queue Depth
bPSASensitive	0x01	0x00	Sensitivity to soldering
bMemoryType	0x01	0x00	Memory type
bDataReliability	0x01	0x00	Data Reliability
bLogicalBlockSize	0x01	0x0C	Logical Block Size
qLogicalBlockCount	0x08	0x200000	Logical Block count

dEraseBlockSize	0x04	0x01	Erase Block size
bProvisioningType	0x01	0x03	Provisioning type
qPhyMemResourceCount	0x08	0x200000	Resource count
wContextCapabilities	0x02	0x00	Context capabilities
bLargeUnit	0x01	0x00	Large Unit

5.3. RPMB Descriptor

Table 12 – RPMB Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x23	Size of this descriptor
bDescriptorIDN	0x01	0x02	Unit Descriptor Type Identifier
bUnitIndex	0x01	0xc4	Unit Index
bLUEnable	0x01	0x01	LU enable
bBootLunID	0x01	0x00	Boot LUN ID
bLUWriteProtect	0x01	0x00	Write protect
bLUQueueDepth	0x01	0x00	Queue Depth
bPSASensitive	0x01	0x00	Sensitivity to soldering
bMemoryType	0x01	0x0f	Memory Type
bRPMBRegionEnable	0x01	0x00	RPMB region enable
bLogicalBlockSize	0x01	0x08	The size of addressable logical blocks
qLogicalBlockCount	0x08	0x0000000000010000	Total number of addressable logical blocks in the logical unit
bRPMBRegion0Size	0x01	0x80	RPMB region 0 size is defined in 128KB unit
bRPMBRegion1Size	0x01	0x00	RPMB region 1 size is defined in 128KB unit
bRPMBRegion2Size	0x01	0x00	RPMB region 2 size is defined in 128KB unit
bRPMBRegion3Size	0x01	0x00	RPMB region 3 size is defined in 128KB unit
bProvisioningType	0x01	0x00	Provisioning Type
qPhyMemResourceCount	0x08	0x0000000000010000	Total physical memory resources available in the logical unit.

5.4. Geometry Descriptor

Table 13 – Geometry Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x48	Descriptor Size
bDescriptorIDN	0x01	0x07	Geometry Descriptor Type Identifier
bMediaTechnology	0x01	0x00	Reserved
Reserved1	0x01	0x00	Reserved
qTotalRawDeviceCapacity	0x08	0x00	Total Raw Device Capacity

bMaxNumberLU	0x01	0x01	Maximum Number of Logical Units Supported
dSegmentSize	0x04	0x00002000	Segment Size Value (Defined in 512 Byte Units)
bAllocationUnitSize	0x01	0x01	Allocation Unit Size Value
bMinAddrBlockSize	0x01	0x08	Minimum Addressable Block Size (Defined in 512 Byte Units)
bOptimalReadBlockSize	0x01	0x08	Optimal Read Block Size (Defined in 512 Byte Units)
bOptimalWriteBlockSize	0x01	0x08	Optimal Write Block Size (Defined in 512 Byte Units)
bMaxInBufferSize	0x01	0x08	Maximum Data-In Buffer Size (Defined in 512 Byte Units)
bMaxOutBufferSize	0x01	0x08	Maximum Data-Out Buffer Size (Defined in 512 Byte Units)
bRPMB_ReadWriteSize	0x01	0x40	Maximum Number of RPMB Frames (256 Bytes per Frame)
bDynamicCapacityResource Policy	0x01	0x01	Dynamic Capacity Resource Policy
bDataOrdering	0x01	0x00	Out-of-Order Data Transfer Support
bMaxContexIDNumber	0x01	0x05	Maximum Number of Contexts Available
bSysDataTagUnitSize	0x01	0x00	System Data Tag Unit Size
bSysDataTagResSize	0x01	0x00	Maximum Storage Area Size allocated for system data by tagging mechanism (in Bytes)
bSupportedSecRTypes	0x01	0x09	Supported Secure Removal Types
wSupportedMemoryTypes	0x02	0x8009	Bitmap Representing Supported Memory Types
dSystemCodeMaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for System Code Memory Type
wSystemCodeCapAdjFac	0x02	0x00	Capacity Adjustment Factor for System Code Memory Type
dNonPersistMaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Non-Persistent Memory
wNonPersistCapAdjFac	0x02	0x00	Capacity Adjustment Factor for Non-Persistent Memory Type
dEnhanced1MaxNAllocU	0x04	0x00000030	Maximum Number of Allocation Units for Enhanced Memory Type 1
wEnhanced1CapAdjFac	0x02	0x0300	Capacity Adjustment Factor for Enhanced Memory Type 1
dEnhanced2MaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Enhanced Memory Type 2
wEnhanced2CapAdjFac	0x02	0x00	Capacity Adjustment Factor for Enhanced Memory Type 2
dEnhanced3MaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Enhanced Memory Type 3
wEnhanced3CapAdjFac	0x02	0x00	Capacity Adjustment Factor for Enhanced Memory Type 3
dEnhanced4MaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Enhanced Memory Type 4
wEnhanced4CapAdjFac	0x02	0x00	Capacity Adjustment Factor for Enhanced Memory Type 4
dOptimalLogicalBlockSize	0x04	0x00000008	Optimal Logical Block Size

5.5. Interconnect Descriptor

Table 14 – Interconnect Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x06	Descriptor Size
bDescriptorIDN	0x01	0x04	Interconnect Descriptor Type Identifier
bcdUniproVersion	0x02	0x0160	MIPI UniProSM Version Number (in BCD format)
bcdMphyVersion	0x02	0x0300	MIPI M-PHY® Version Number (in BCD format)

5.6. Power Descriptor

Table 15 – Power Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x62	Descriptor Size
bDescriptorIDN	0x01	0x08	Power Parameters Descriptor Type Identifier
wActiveICCLevelsVCC[0]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 0
wActiveICCLevelsVCC[1]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 1
wActiveICCLevelsVCC[2]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 2
wActiveICCLevelsVCC[3]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 3
wActiveICCLevelsVCC[4]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 4
wActiveICCLevelsVCC[5]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 5
wActiveICCLevelsVCC[6]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 6
wActiveICCLevelsVCC[7]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 7
wActiveICCLevelsVCC[8]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 8
wActiveICCLevelsVCC[9]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 9
wActiveICCLevelsVCC[10]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 10
wActiveICCLevelsVCC[11]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 11
wActiveICCLevelsVCC[12]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 12
wActiveICCLevelsVCC[13]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 13
wActiveICCLevelsVCC[14]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 14
wActiveICCLevelsVCC[15]	0x02	0x00	Maximum VCC Current Value for bActiveICCLevel = 15
wActiveICCLevelsVCCQ[0]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 0
wActiveICCLevelsVCCQ[1]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 1
wActiveICCLevelsVCCQ[2]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 2
wActiveICCLevelsVCCQ[3]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 3
wActiveICCLevelsVCCQ[4]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 4
wActiveICCLevelsVCCQ[5]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 5
wActiveICCLevelsVCCQ[6]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 6
wActiveICCLevelsVCCQ[7]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 7
wActiveICCLevelsVCCQ[8]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 8
wActiveICCLevelsVCCQ[9]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 9
wActiveICCLevelsVCCQ[10]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 10
wActiveICCLevelsVCCQ[11]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 11
wActiveICCLevelsVCCQ[12]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 12
wActiveICCLevelsVCCQ[13]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 13
wActiveICCLevelsVCCQ[14]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 14
wActiveICCLevelsVCCQ[15]	0x02	0x00	Maximum VCCQ Current Value for bActiveICCLevel = 15

wActiveICCLevelsVCCQ2[0]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 0
wActiveICCLevelsVCCQ2[1]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 1
wActiveICCLevelsVCCQ2[2]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 2
wActiveICCLevelsVCCQ2[3]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 3
wActiveICCLevelsVCCQ2[4]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 4
wActiveICCLevelsVCCQ2[5]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 5
wActiveICCLevelsVCCQ2[6]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 6
wActiveICCLevelsVCCQ2[7]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 7
wActiveICCLevelsVCCQ2[8]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 8
wActiveICCLevelsVCCQ2[9]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 9
wActiveICCLevelsVCCQ2[10]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 10
wActiveICCLevelsVCCQ2[11]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 11
wActiveICCLevelsVCCQ2[12]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 12
wActiveICCLevelsVCCQ2[13]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 13
wActiveICCLevelsVCCQ2[14]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 14
wActiveICCLevelsVCCQ2[15]	0x02	0x00	Maximum VCCQ2 Current Value for bActiveICCLevel = 15

5.7. Health Descriptor

Table 16 – Health Descriptor for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bLength	0x01	0x25	Descriptor Size
bDescriptorIDN	0x01	0x09	Device Health Descriptor Type Identifier
bPreEOLInfo	0x01	0x01	Pre End of Life Information
bDeviceLifeTimeEstA	0x01	0x00	Device Lifetime (Based on Number program/erase cycles performed, Method A)
bDeviceLifeTimeEstB	0x01	0x00	Device Lifetime (Based on Number program/erase cycles performed, Method B)
VendorPropInfo	0x20	0x00	Reserved for Vendor Proprietary Health Report (32 Bytes)

5.8. Flags

Table 17 – Flags for iNAND 8521

NAME	LENGTH (BIT)	VALUE	DESCRIPTION
fDeviceInitfDeviceInit	0x01	False	Device Initialization
fPermanentWPEn	0x01	False	Permanent Write Protection Enable
fPowerOnWPEn	0x01	False	Power On Write Protection Enable
fBackgroundOpsEn	0x01	True	Background Operations Enable
fDeviceLifeSpanModeEn	0x01	False	Device Life Span Mode

fPurgeEnable	0x01	False	Purge Enable
fPhyResourceRemoval	0x01	False	Physical Resource Removal
fBusyRTC	0x01	False	Busy Real Time Clock
PermanentlyDisableFwUpdate	0x01	False	Permanently Disable Firmware Update

5.9. Attributes

Table 18 – Attributes for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
bBootLunEn	0x01	0x1	Boot LUN Enable
bCurrentPowerMode	0x01	0x11	Current Power Mode
bActiveICCLevel	0x01	0xf	Active ICC Level
bOutOfOrderDataEn	0x01	0x0	Out of Order Data Transfer Enable
bBackgroundOpStatus	0x01	0x0	Background Operations Status
bPurgeStatus	0x01	0x0	Purge Operation Status
bMaxDataInSize	0x01	0x8	Maximum Data In Size
bMaxDataOutSize	0x01	0x8	Maximum Data-Out Size
dDynCapNeeded	0x04	0x0	Dynamic Capacity Needed
bRefClkFreq	0x01	0x1	Reference Clock Frequency Value
bConfigDescrLock	0x01	0x0	Configuration Descriptor Lock
bMaxNumOfRTT	0x01	0x2	Maximum Number of Outstanding RTTs in Device
wExceptionEventControl	0x02	0x0	Exception Event Control
wExceptionEventStatus	0x02	0x0	[Each bit represents an exception event]
dSecondsPassed	0x01	0x0	Seconds Passed from TIME BASELINE
wContextConf	0x02	0x0	Context Configuration
bDeviceFFUStatus	0x01	0x0	Device FFU Status
bPSAState	0x01	0x0	Device PSA State
dPSADataSize	0x04	0x0	Amount of data host plans to load to all logical units

5.10.Control Mode SCSI

Table 19 – Control Mode SCSI Attributes for iNAND 8521

NAME	LENGTH	VALUE	DESCRIPTION
PAGE_CODE	0x01	0x8a	Boot LUN Enable
PAGE_LENGTH	0x01	0x0a	Current Power Mode
BYTE_2	0x01	0x00	Active ICC Level
BYTE_3	0x01	0x10	Out of Order Data Transfer Enable
BYTE_4	0x01	0x00	Background Operations Status
BYTE_5	0x01	0x00	Purge Operation Status

Obsolete	0x02	0x00	Maximum Data In Size
BUSY_TIMEOUT_PERIOD	0x02	0x00	Maximum Data-Out Size
EXTENDED_SELF_TEST_COMPLETION_TIME	0x02	0x00	Dynamic Capacity Needed

5.11.VPD page 0x83 – Device Identification

Table 20 – Device Identification for iNAND 8521 (VPD page 0x83)

NAME	LENGTH	VALUE	DESCRIPTION
PAGE_PERIPHERAL	0x01	0x0	Peripheral
PAGE_CODE	0x01	0x83	Page Code
PAGE_LENGTH	0x2	0xc	Length
CODE_SET	0x01	0x2	Code Set
PROTOCOL_ID	0x01	0x0	Protocol ID
DESIGNATOR_TYPE	0x01	0x0	Designator Type
ASSOCIATION	0x01	0x0	Association
PIV	0x01	0x0	PIV
DESIGNATOR_LENGTH	0x01	0x3	String Length
DESIGNATOR_STR0	0x01	0x57	‘W’
DESIGNATOR_STR1	0x01	0x44	‘D’
DESIGNATOR_STR2	0x01	0x43	‘C’

5.12.VPD page 0xB0 – Block Limit

Table 21 – Block Limit Attributes for iNAND 8521 (VPD page 0xB0)

NAME	LENGTH	VALUE	DESCRIPTION
PAGE_PERIPHERAL	0x01	0x0	Peripheral
PAGE_CODE	0x01	0xb0	Page code 0xB0
PAGE_LENGTH	0x02	0x3c	length of the page
RESERVED	0x01	0x0	
MAX_CMP_AND_WR_LEN	0x01	0x0	Maximum value that the device server accepts in the NUMBER OF LOGICAL BLOCKS field in the COMPARE AND WRITE
OPT_TRANSFER_LEN_GRANULARITY	0x02	0x2	optimal transfer length granularity in blocks
MAX_TRANSFER_LEN	0x04	0x0	maximum transfer length in blocks
OPT_TRANSFER_LEN	0x04	0x2	optimal transfer length in blocks
MAX_PREFETCH_RD_WR_TRANSFER_LEN	0x04	0x0	maximum transfer length in blocks
MAX_UNMAP_LBA_CNT	0x04	0xffff	maximum number of LBAs that may be unmapped by an UNMAP command
MAX_UNMAP_BLOCK_DESC_CNT	0x04	0xff	maximum number of UNMAP block descriptors

OPT_UNMAP_GRANULARITY	0x04	0x1	optimal granularity in logical blocks for unmap requests
UNMAP_GRANULARITY_ALIGNMENT	0x04	0x0	LBA of the first logical block

5.13.User Density

The following table shows the capacity available for user data for the different device sizes:

Table 22: Capacity for User Data

CAPACITY	IN BYTES	IN SECTORS
32GB	32,006,733,824	62,513,152
64GB	64,013,467,648	125,026,304
128GB	128,026,935,296	250,052,608
256GB	256,053,870,592	500,105,216

6. HW APPLICATION GUIDELINES

6.1. PCB Stack-up

Table 23 –Minimal PCB Stack-Up Example

LAYER	TYPE	DESCRIPTION
1	Signal	Top
2	Plane	Ground
3	Plane	Power
4	Signal	Routing
5	Plane	Ground
6	Signal	Bottom

- Additional layers may be needed on a per-platform basis.
- Signal layers should achieve Tx/Rx differential pairs with 100Ω differential impedance through the range of operation frequencies
- The impedance of single-ended traces (such as the Ref_CLK) should be matched to 50Ω.

6.2. Return Current and References Planes

- The signal must be provided with a good path for return currents.
- Avoid gaps in signal return path.
- To reduce inductance, make the return paths as short as possible for return currents (loops). Longer loops will increase inductance.
- Full GND plane reference is recommended.
- Provide GND vias for the return current paths at the point of the layer change.
- Layer transition requires stitching vias.
- Keep clearance from plane voids.
- No plane splits.

6.3. Crosstalk Minimization

Routing traces on adjacent signal layers should not cross each other unless they are almost perpendicular.

Parallel traces on adjacent signal layers will induce crosstalk on each other.

To minimize crosstalk, please follow these routing guidelines for Tx/Rx differential pairs:

- Minimum recommended spacing from low speed signal is 3x
- Minimum recommended spacing from high speed signal is 7x

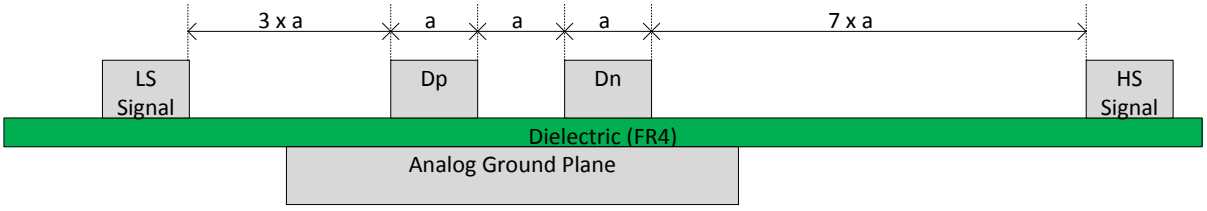


Figure 7 – Spacing of Tx/Rx Differential Pairs for Crosstalk Minimization

6.4. Channel Length Mismatch

To avoid skew, Tx/Rx differential pairs must have equal lengths. In case there is skew between bus trace lengths, mismatch should be minimal (no more than +/-1 mm). Please follow the following guidelines. The figure below provides examples of correct channel length matching.

- Differential signals require vias. However, the vias must be in the same configuration for each signal of the differential pair to ensure that both signals experience the same discontinuity. Thus, any variation in signal due to the via-induced discontinuity will be in a common mode.
- Avoid trace routing over anti-pad or other impedance discontinuities on the transmission line.
- Avoid vias ,via stubs and layer changes.
- Avoid any unnecessary pads on vias (which would add capacitance).
- Use ground return vias.
- Avoid using right-angle (90°) bends when matching channel lengths. Use mitered 45° bends instead

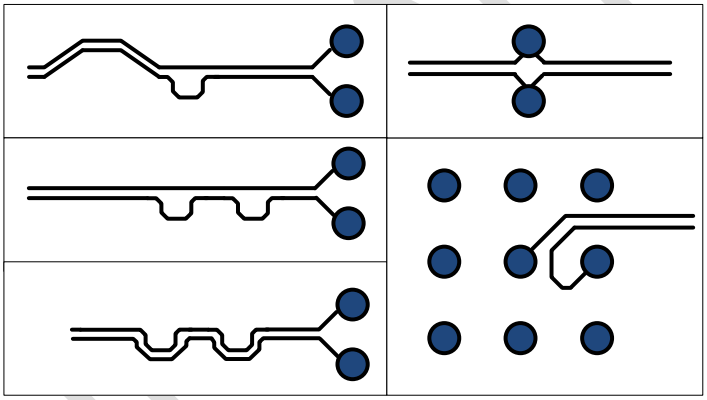


Figure 8 - Correct Channel Length Matching Example

6.5. High-Speed Differential Routing

Tx/Rx differential pairs should be routed in a tightly coupled fashion to save routing space. However, this can create an impedance control challenge. To minimize impedance mismatches, please follow these routing guidelines for Tx/Rx differential pairs:

- Use a continuous ground plane below Dp/Dn:

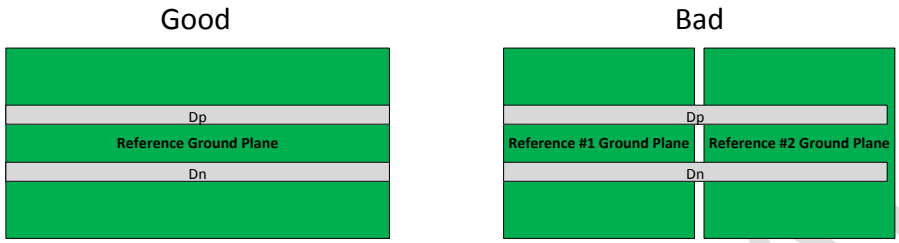


Figure 9 – Continuous Ground Plane Below Dp/D

- Add ground return vias:
  - Symmetrical ground vias (return vias) should be used to reduce discontinuity for common mode signal component.
  - Minimize Cvia (capacitance):
    - Reduce the via capture pad size.
    - Eliminate all non-functional pads.
    - Increase the via anti-pad size where possible.
  - Minimize Lvia (inductance) by minimizing the via barrel length by back-drilling.
- Verify layouts using a 2-D field solver simulation.
- When designing traces, minimize the number of components on the transmission line. If components are necessary, choose ones that induce the least amount of discontinuity.
- Traces should be referenced to GND planes rather than power planes. No matter how much decoupling is built into the design, power planes are noisier than GND planes. Referencing to a power plane can induce noise onto a high speed signal.
- Given the same trace width and copper thickness considerations, stripline routing results in lower signal attenuation compared with microstrip.

6.6. Reference Clock

Following JEDEC standard:

Table 24 – Reference Clock from UFS Specification

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Clock Rise Time	t_{IRISE}	0.4	2	nsec
Input Clock fall Time	t_{IFALL}	0.4	2	nsec

6.7. Recommended Capacitors

Table 25 – Recommended Capacitor

CAPACITOR VALUE	MANUFACTURER	MANUFACTURER P/N
4.7uF	MURATA	GRM185R60J475ME15D
	TAIYO YUDEN	JMK107BJ475MK-T
0.1uF	MURATA	GRM155R71A104KA01D
	KYOCERA	CM05X5R104K06AH
2.2uF	PANASONIC	ECJ0EB0J225M
	SAMSUNG	CL05A225MQ5NSNC

6.8. Capacitor Selection and Layout Guidelines

It is recommended that the power domain connectivity follow the figure below:

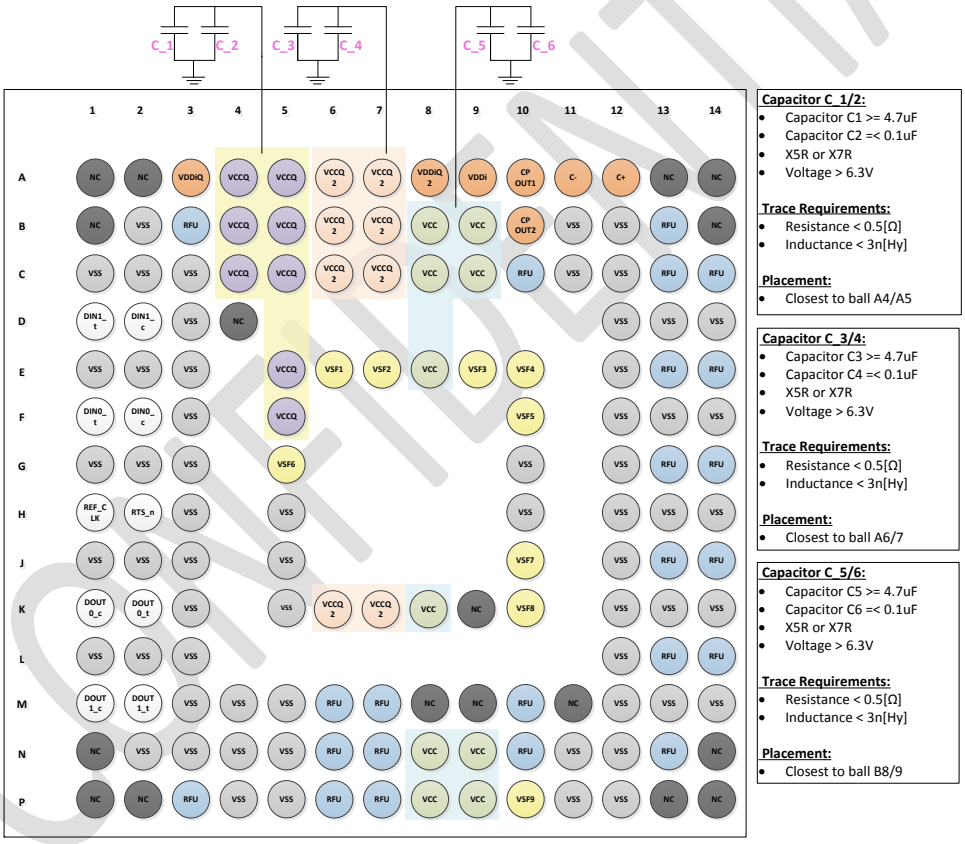


Figure 8 - Recommended Power Domain Connectivity

Figure 10 - Recommended Power Domain Connectivity

Note: Signal routing in the diagram is <u>for illustration purposes only</u> and the final routing will depend on the final PCB layout.

For clarity, this diagram does not include VSS connection. All balls marked VSS must be connected to a ground (GND) plane.

7. PROPRIETY iNAND 8521 FEATURE OVERVIEW

7.1. SmartSLC®

The iNAND SmartSLC® feature gives the customer the write performance they require, so that they will have a UX experience that makes an X3 memory look better than X2. The iNAND SmartSLC® provides the following value to the system:

- Auto-adjust iNAND performance per application need
- Improves system efficiency and UX
  - Reduce system WRITE-BUSY time by improving IO throughput
- Vertical iNAND technology:
  - Host access to iNAND NAND flash performance capabilities
  - Controller and Firmware auto-detections of hosts needs and auto-adjustment device behavior based on these host needs
  - Host (e.MMC driver) customizations and modifications in IDLE time management to allow optimized utilization of SmartSLC® capabilities

iNAND 8521 uses allocated SLC blocks within the SanDisk NAND design to implement the feature. The allocation of these blocks does not impact the as sold capacity of the device (Exported Capacity). The device uses a detection mechanism and once a pattern requiring sequential write performance is detected, the device postpones any background management operations, if feasible,) and dedicates resources to SLC programing. Any IDLE state bigger than tIDLE [ms], shall trigger migration operations to free up enough space for the next burst and eliminate potential performance drop.

iNAND SmartSLC® buffer size and Performance

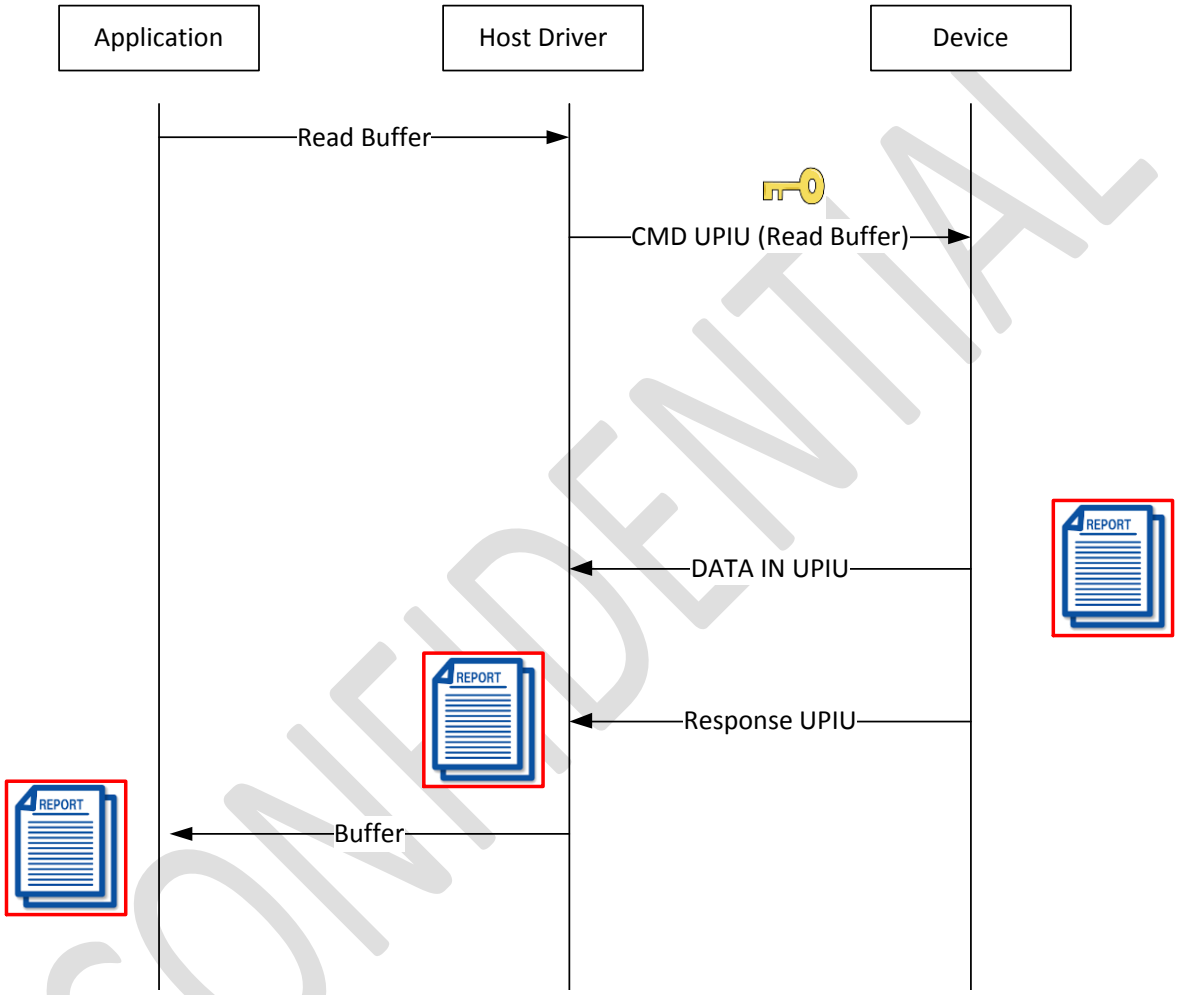
CAPACITY	BUFFER SIZE [GB]	WRITE SPEED* [MBs]
32GB	8	200
64GB	16	400
128GB	32	550
256GB	64	550

* Sequential write Performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT), 512KB chunk, enough recovery time before measurement @ Gear3/2L mode.

7.2. Device Report

7.2.1. Access Command Sequence

In order to read the Device Report in UFS, a UPIU Read Buffer command sequence shall be used. The following is the host command sequence required to retrieve the Device Report information.



7.2.2. Read Buffer CDB Parameters:

- OPCODE (Byte:0 Bit: 0-7): 3C
- MODE (Byte:1 Bit: 0-4): 01h (Vendor Specific)
- BUFFER ID (Byte:2 Bit: 0-7): 01h
- BUFFER OFFSET (Byte:3-5 Bit: 0-7): **0x7D9C69** (Key)
- ALLOCATION LEN (Byte:6-8 Bit: 0-7): 0x200 (512 bytes buffer size)

Table 11-48 — READ BUFFER command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPERATION CODE (3Ch)							
1	Reserved			MODE				
2	BUFFER ID							
3	(MSB)							
4	BUFFER OFFSET							
5								(LSB)
6	(MSB)							
7	ALLOCATION LENGTH							
8								(LSB)
9	CONTROL = 00h							

Remarks

- Device Report extraction method supports intermediate command interruptions during the Device Report extraction command flow.
- When Read Buffer command is sent with wrong argument or it is sent in a wrong sequence, the iNAND will return “all-zeros” buffer.
- Events which break the Device Report flow - Power cycle, HW reset, CMD0
- Once one of above events occurs, the iNAND state machine is reset. Therefore, after such event, the host must re-send the full command sequence to retrieve the Device Report information

7.2.3. Device Report Data Structure Output

FIELD NAME	DESCRIPTION	MOTIVATION (HOST PERSPECTIVE)	OFFSET (DEC)	SIZE [BYTES]
Average Erase Cycles Type C (Enhanced)	The Average Erase cycles value out of all Enhanced area Blocks	To check real life product endurance and lifetime	0	4
Average Erase Cycles Type A (SLC)	The Average Erase cycles value out of all SLC Blocks	To check real life product endurance and lifetime	4	4
Average Erase Cycles Type B (TLC)	The Average Erase cycles value out of all TLC Blocks	To check real life product endurance and lifetime	8	4
Read reclaim count Type C (Enhanced)	The amount of Enhanced Reads operations which passed Read-	To check iNAND data-retention preventions	12	4

	Scrub thresholds and requires reclaim	mechanism on management area		
Read reclaim count Type A (SLC)	The amount of SLC Reads operations which passed Read-Scrub thresholds and requires reclaim	To check iNAND data-retention preventions mechanism on SLC area	16	4
Read reclaim count Type B (TLC)	The amount of TLC Reads operations which passed Read-Scrub thresholds and requires reclaim	To check iNAND data-retention preventions mechanism on TLC area	20	4
Bad Block Manufactory	Number of Bad Blocks detected during manufacturing process	To check device number of Bad-Blocks	24	4
Bad Block Runtime Type C (Enhanced)	All Bad Blocks related to the Enhanced area that were detected during run-time	To check device runtime number of Bad-Blocks on Management area	28	4
Bad Block Runtime Type A (SLC)	All Bad Blocks related to the SLC area that were detected during run-time	To check device runtime number of Bad-Blocks on SLC area	32	4
Bad Block Runtime Type B (TLC)	All Bad Blocks related to the TLC area that were detected during run-time	To check device runtime number of Bad-Blocks on TLC area	36	4
Field FW Updates Count	Number of secure Field Firmware Upgrades (sFFU) done from the beginning of the device life time	To know that number of times sFFU operations were done on the device	40	4
FW Release Date	Firmware Release date	To identify device Firmware	44	12
FW Release Time	Firmware Release hour	To identify device Firmware	56	8
Cumulative Host Write data size	Accumulate the amount of Host Written payload in resolution of 100MB	To analyze host total write payload and typical daily workload	64	4
Number Vcc Voltage Drops Occurrences	Cumulative counter for voltage drops (Power-Off) during all device states (Idle/Read/Write/Erase).	To identify unstable power supply platform behavior	68	4
Number Vcc Voltage Droops Occurrences	Counts the times VDET indication was triggered due to Power-Droop (Slight power-droop below certain threshold and for a very short period of time).	To identify unstable power supply platform behavior	72	4
Number of failures recover new host data (After Write Abort)	Count the number of times iNAND dismiss new Host data due to Write Abort (either due to corrupted data or broken) command	To analyze write abort behaver by device	76	4
Total Recovery Operation After VDET	The total amount of recovery operations required to be done by the device while detecting internal slight power-droop	To analyze device recovery after VDET event occurs	80	4
Cumulative SmartSLC® write payload	Accumulate the amount of Host written payload that was written to SmartSLC® buffer in resolution of 100MB	To Track and analyze iNAND SmartSLC® behavior	84	4
Cumulative SmartSLC® BigFile mode write payload	Accumulate the amount of Host written payload that was written to SmartSLC® BigFile buffer in resolution of 100MB	To Track and analyze iNAND SmartSLC® BigFile mode behavior	88	4

Number of times SmartSLC® BigFile mode was operated during device lifetime	Count the number of times Host wrote payload to SmartSLC® BigFile mode	To Track and analyze iNAND SmartSLC® BigFile mode behavior	92	4
Average Erase Cycles of SmartSLC® BigFile mode	The Average Erase count of SmartSLC® BigFile buffer	To track and analyze iNAND SmartSLC® BigFile mode behavior	96	4
Cumulative Initialization Count	Number of device power ups event from beginning of life	To analyze number of initialization events happened during device lifetime	100	4
Max Erase Cycles Type C (Enhanced)	The Maximum Erase value out of all enhanced Blocks	To Check product endurance variance	104	~~4~~
Max Erase Cycles Type A (SLC)	The Maximum Erase value out of all SLC Blocks	To Check product endurance variance	108	4
Max Erase Cycles Type B (TLC)	The Maximum Erase value out of all TLC Blocks	To Check product endurance variance	112	4
Min Erase Cycles Type C (Enhanced)	The Minimum Erase value out of all enhanced Blocks	To Check product endurance variance	116	~~4~~
Min Erase Cycles Type A (SLC)	The Minimum Erase value out of all SLC Blocks	To Check product endurance variance	120	4
Min Erase Cycles Type B (TLC)	The Minimum Erase value out of all TLC Blocks	To Check product endurance variance	124	4
Reserved			128-151	24
Pre EOL warning level Type C (Enhanced)	Pre end-of-life (EOL) levels for device enhanced area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode.	To predict early lifetime of device	152	4
Pre EOL warning level Type B (TLC)	Pre end-of-life (EOL) levels for device TLC area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode.	To predict early lifetime of device	156	4
Uncorrectable Error Correction Code	The amount of UECC by the device	To analyze UECC probability during real lifetime	160	4
Current temperature	Indicates the current temperature of the device, in degrees Celsius	To track device environmental status	164	4
Min Temperature	Indicates the min temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status	168	4
Max Temperature	Indicates the max temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status	172	4
Reserved			176	4
Enriched Device Health Type C (Enhanced)	Device health (age) Level in resolution of 1% (1-100) for Enhanced area	To check real life product endurance and lifetime	180	4
Enriched Device Health Type B (TLC)	Device health (age) Level in resolution of 1% (1-100) for TLC area	To check real life product endurance and lifetime	184	4

8. MARKING

As illustrated in the figure below, product marking follows this format:

First row: Simplified SanDisk Logo
Second row: Sales item P/N
Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'
* No ES marking for product in mass production.
Fourth row: Y- Last digit of year
WW- Work week
D- A day within the week.
MTLLLXXX – Internal use
2D barcode: Store the 12 Digital unique ID information as reflected in the fourth row.

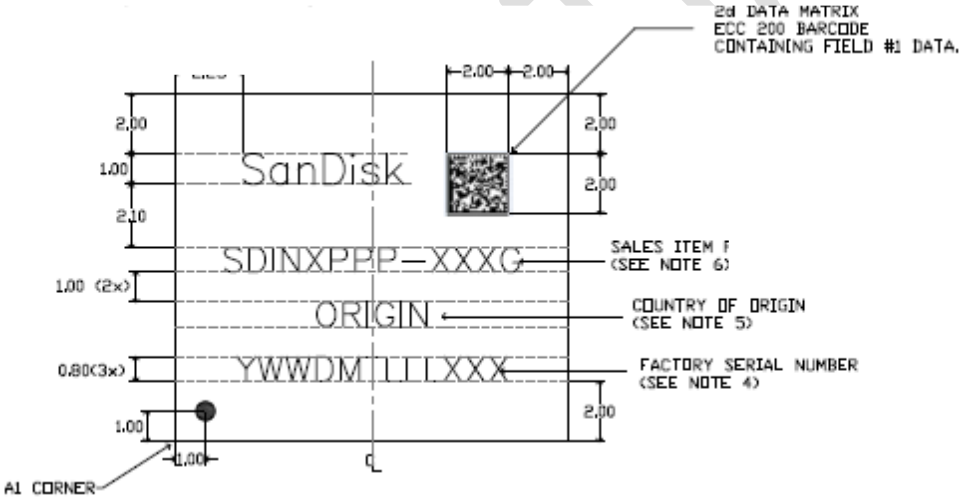


Figure 11 - Product Marking for 64G-256GB Devices

9. ORDERING INFORMATION

Table 26 – Ordering Information

CAPACITY	NO OF DIES	TECHNOLOGY	PART NUMBER	PACKAGE	UFS SPEC
32GB	1	3D-64L-X3	SDINDDH4-32G	11.5x13x1.0mm	2.1
64GB	2	3D-64L-X3	SDINDDH4-64G	11.5x13x1.0mm	2.1
128GB	4	3D-64L-X3	SDINDDH4-128G	11.5x13x1.0mm	2.1
256GB	8	3D-64L-X3	SDINDDH4-256G	11.5x13x1.0mm	2.1

Note1: Customer Code can optionally be added at the end of the part number. The Customer Code can be 3 or 4 digits. The next table provides some examples.

Table 27 – Customer Examples for Ordering Information

CUSTOMER	CUSTOMER CODE	CUSTOMER PART NUMBER	CUSTOMER SAMPLES PART NUMBER
Customer A	326	SDINBDD4-256G-326	SDINBDD4-256G-326Q
Customer B	473	SDINBDD4-64G-473	SDINBDD4-64G-473Q
Customer C	1243	SDINBDD4-128G-1243	SDINBDD4-128G-1243Q

Note2: Unique Identifier (optional) is a single character identifier specifying certain FW/HW version. For example, the unique identifier (in this case, K) in SDINBDD4-128G-K specifies a specific firmware version, while a different unique identifier (in this case, N) in SDINBDD4-128G-N specifies a different firmware version.

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