SanDisk®

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Released Data Sheet - Confidential

iNAND 7550 64GB+32Gb, 64GB+48Gb MCP

e.MMC 5.1 with Command-Queue, HS400 Interface and LPDDR4x

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REVISION HISTORY

Doc. No	Revision	Date	Description	Reference
02-05-WW-02-00020	0.1	04-Jan-2018	Initial version	

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1. INTRODUCTION

1.1. General Description

Overview iNAND 7550 MCP is an Embedded Flash Drive (EFD) with low power DRAM in one package that is designed for mobile handsets and consumer electronic devices. iNAND 7550 MCP is a hybrid device combining an embedded thin flash controller and 3D NAND flash memory, with an industry standard e.MMC 5.1interface featuring Command-Queue, HS400, FFU, as well as legacy eMMC 4.51 features such as Power Off Notifications, Packed commands, Cache, Boot / RPMB partitions, HPI, and HW Reset, make it an optimal device for both reliable code and data storage.

iNAND 7550 MCP is based on SanDisk 256Gb X3 3D NAND memory, using 64-layer technology. The memory architecture brings new levels of density, scalability and performance to the Embedded Flash Drive. SanDisk 3D NAND memory also provides enhanced write/erase endurance, write speeds and energy efficiency relative to conventional 2D NAND.

In addition to the high reliability, robustness and consistence system performance offered by the current iNAND family of products, iNAND 7550 MCP offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as an advanced power management scheme.

The iNAND 7550 MCP architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximizing flash life expectancy.

SanDisk iNAND 7550 MCP provides 64GB of memory for use in mass storage applications and is paired with up to 48 Gb of LPDDR4x DRAM. In addition to the mass-storage-specific flash memory chip and the low-power DRAM, iNAND 7550 MCP includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

Combining high performance with features for easy integration and exceptional reliability, iNAND 7550 MCP is an EFD designed to exceed the demands of both manufacturers and their customers.

1.2. Plug-and-Play Integration

iNAND's optimized architecture eliminates the need for complicated software integration and testing processes thereby enabling plug-and-play integration into the host system. The replacement of one iNAND device with another, of a newer generation, requires virtually no changes to the host. This allows manufacturers to adopt advanced NAND Flash technologies and update product lines with minimal integration or qualification efforts.

With JEDEC form factors measuring 11.5x13mm for all capacities, iNAND 7550 MCP is ideally suited for a wide variety of portable devices such as multimedia mobile handsets, tablets, and other consumer products.

iNAND 7550 MCP features a MMC interface allows easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

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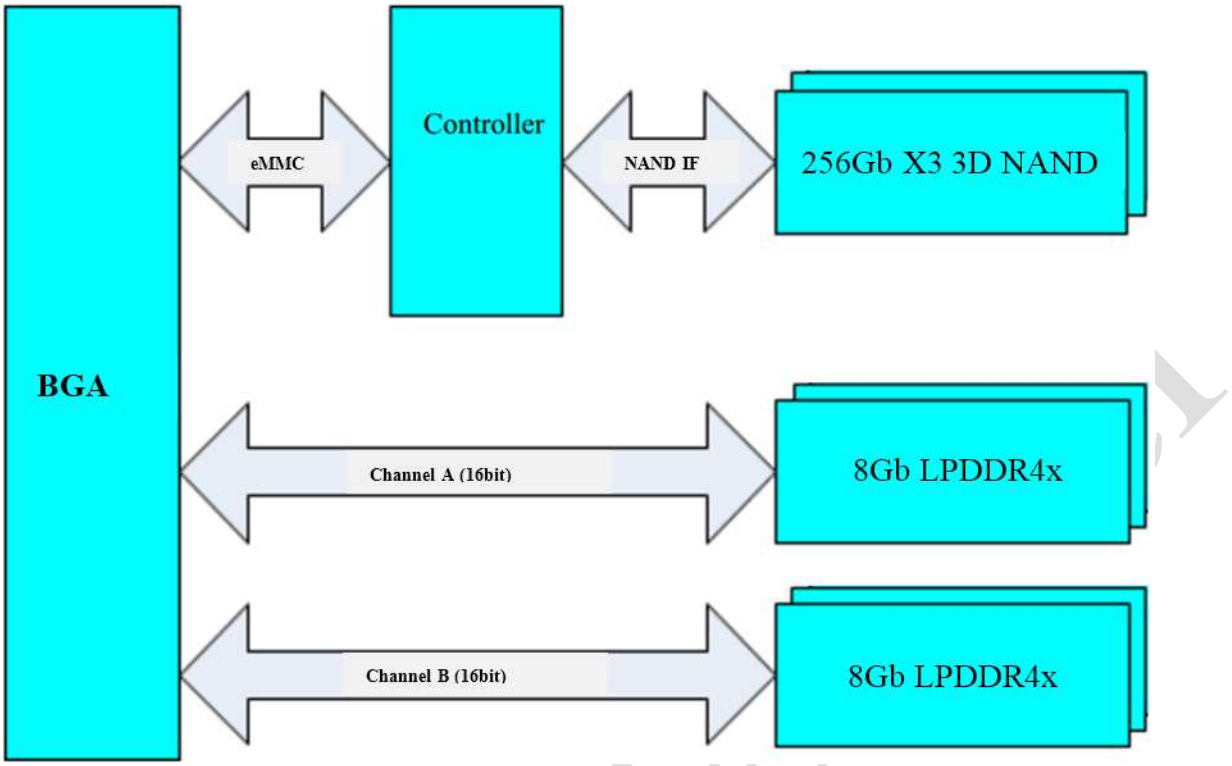

Figure 1 - SanDisk iNAND 7550 64GB+32Gb MCP with MMC Interface Block Diagram

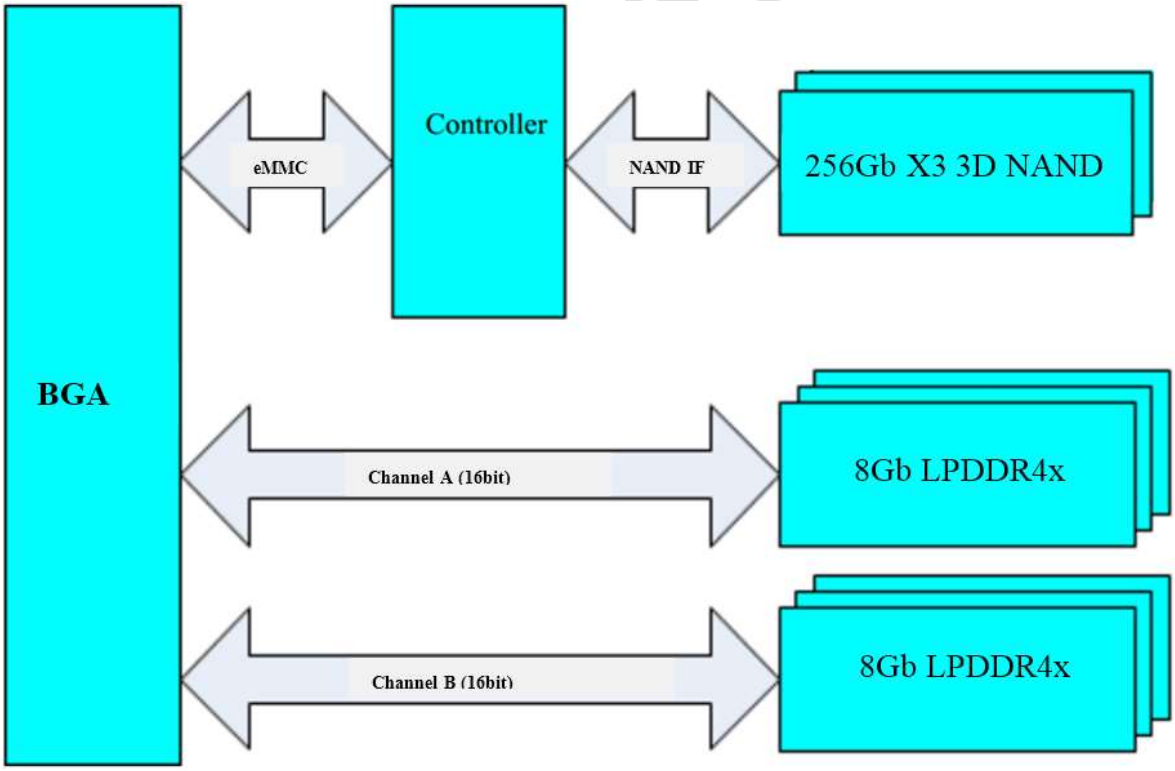

Figure 2 - SanDisk iNAND 7550 64GB+48Gb MCP with MMC Interface Block Diagram

WDC is supporting 2CS configuration only (3CS is not supported)

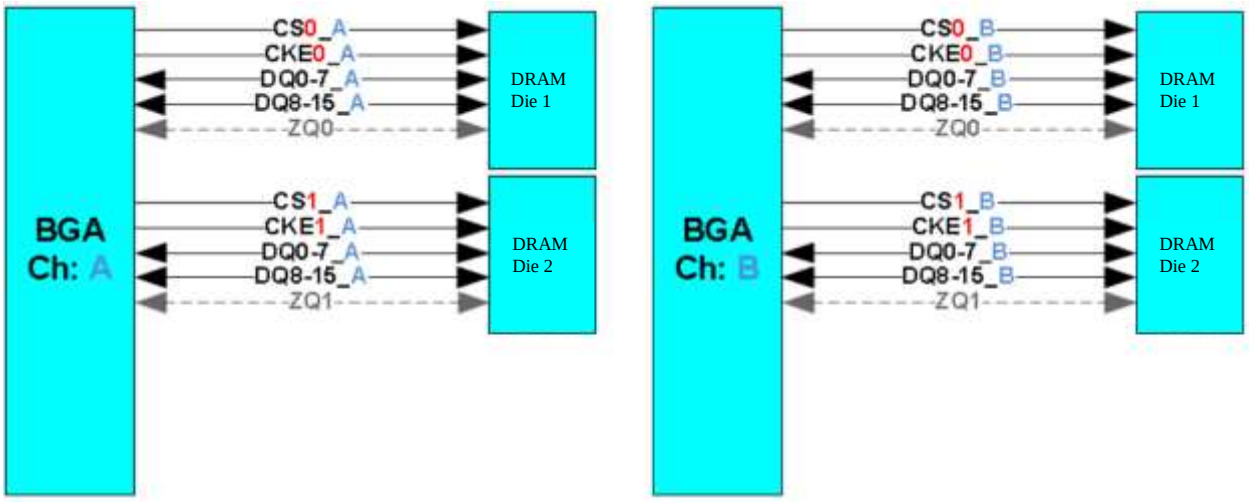

Figure 3- 32Gb 2CS

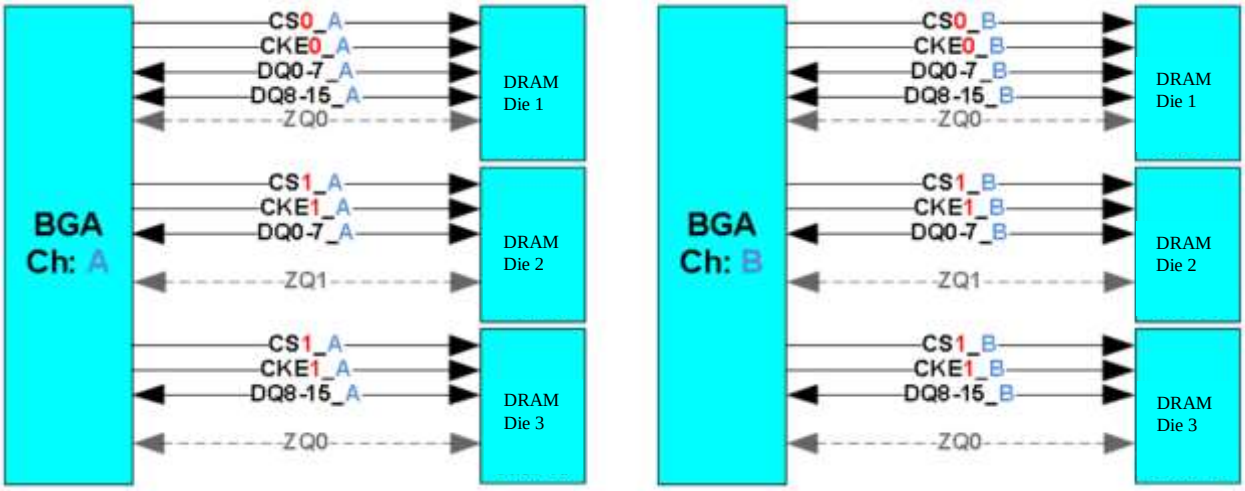

Figure 4- 48Gb 2CS

1.3. Feature Overview

SanDisk iNAND 7550 MCP, with MMC interface, includes the following features:

- Memory controller and NAND flash
- Mechanical design complies with JEDEC Specification
- Offered in two package dimensions
  - 11.5mm x 13mm x 1.0mm (64GB+32Gb LPDDR4x)
  - 11.5mm x 13mm x 1.1mm (64GB+48Gb LPDDR4x)
- Operating temperature range: –25C° to +85C°

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- Dual power system
- Core voltage (VCC) 2.7-3.6 V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
- 64 GB of data storage
- Supports three data bus widths: 1bit (default), 4bit, 8bit
- Complies with eMMC Specification Ver. 5.1 HS400
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200
- MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Up to 400 MB/sec bus transfer rate, using 8 parallel data lines at 400 MHz, HS400 Mode
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage
- RPMB Key Reset
- Low-power mobile DDR4x
    - Core power 1, Core power 2 and I/O voltage 1.7V – 1.95V, 1.06V – 1.17V, and 0.57V – 0.65V respectively
    - Up to 1866 MHz clock with 32bit data interface

1.4. Defect and Error Management

The SanDisk iNAND 7550 MCP contains a sophisticated defect and error management system for exceptional data reliability. iNAND 7550 MCP will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume additional user data space. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data

1.5. MMC bus and Power Lines

SanDisk iNAND 7550 MCP with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-B51.

The iNAND bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input.
- VCCQ: VCCQ is the power supply line for host interface.

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- VCC: VCC is the power supply line for internal flash memory.
- VDDi: VDDi is iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: Ground lines.
- RCLK: Data strobe.
- VSF: Vendor specific functions used for debugging purposes.

1.5.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

Note1: HS400 mode only supports the 1.7 – 1.95 V VCCQ option

Note2: Device operation under 3.3V VCCQ is limited to Max 1 hour

1.5.2. Low Power Mobile DDR4x Bus Operating Conditions

See Appendix A for DRAM operating condition specifications.

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1.5.3 e.MMC 5.1 Selected Features Overview

iNAND 7550 MCP supported feature list:

e.MMC	Device Features	Benefit	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Max theoretical Speed	Up to 400MB/s
4.41	SECURE ERASE/TRIM	“True Wipe”	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	Yes
4.41	PARTITIONING & PROTECTION	Flexibility	Yes
4.41	BACKGROUND OPERATIONS	Better User Experience (low latency)	Yes
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	Yes
4.41	HARDWARE RESET	Robust System Design	Yes
4.41	HPI	Control Long Reads/Writes	Yes
4.41	RPMB	Secure Folders	Yes
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	Yes
4.5	LARGE SECTOR SIZE	Potential performance	No
4.5	SANITIZE (4.51)	“True Wipe”	Yes
4.5	PACKED COMMANDS	Reduce Host Overhead	Yes
4.5	DISCARD	Improved Performance on Full Media	Yes
4.5	DATA TAG	Performance and/or Reliability	Yes (API only)
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	Yes (API only)
4.5	CACHE	Better Sequential & Random Writes	Yes
5.0	FIELD FIRMWARE UPGRADE (FFU)	Enables feature enhancements in the field	Yes
5.0	PRODUCTION STATE AWARENESS	Different operation during production	Yes
5.0	DEVICE HEALTH	Vital NAND info	Yes
5.1	ENHANCE STROBE	Sync between Device and Host in HS400	Yes
5.1	COMMAND QUEUE	Responsiveness	Yes
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	Yes
5.1	CACHE FLUSH AND BARRIER	Ordered Cache flushing	Yes
5.1	BKOPS CONTROLLER	Host control on BKOPs	Yes
5.1	SECURE WP	Secure Write Protect	Yes
5.2	HS400 TUNING	DLL Tuning command in HS400	Yes
Propriety	SMART-SLC	Fast write speed per application need	Yes
Propriety	VSF	Enable on-board debugging	Yes
Propriety	PNM	Special product name	Yes
Propriety	DEVICE REPORT	Device Firmware status	Yes
Propriety	CONTENT-PRELOADING	Preloading content at production line	Yes
Propriety	RPMB-KEY-RESET	Resetting RPMB partition key	Yes

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1.6. HS400 Interface

Support HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 4 or 8 bit bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data.

1.7. Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism,

the host downloads a new version of the firmware to the e.MMC device and instructs the e.MMC device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user / OS data. During the FFU process, the host can replace firmware files or single / all file systems.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the SanDisk lab
2. The sFFU files are handed to SanDisk's customer
3. SanDisk's customer can push the firmware updates to their end-users in a transparent way

Note 1: The sFFU process and sFFU files are protected against leakage to unauthorized entities.

Note 2: During the sFFU process the Host may retrieve the exact status of the process using the smart report feature.

For additional information please refer to JESD84-B51 standard and the SanDisk application note on this subject

1.8. Cache

The e.MMC cache is dedicated volatile memory at the size of 512KB. Caching enables to improve iNAND performance for both sequential and random access. For additional information please refer to JESD84-B51 standard.

1.9. Discard

iNAND supports discard command as defined in e.MMC 5.1 spec. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

1.10. Power off Notifications

iNAND supports power off notifications as defined in e.MMC 5.1 spec. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled. Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

1.11. Packed Commands

To enable optimal system performance, iNAND supports packed commands as defined in e.MMC5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of

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operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

1.12. Boot Partition

iNAND supports e.MMC 5.1 boot operation mode: Factory configuration supplies two boot partitions each 4MB in size.

1.13. RPMB Partition

iNAND supports e.MMC 5.1 RPMB operation mode: Factory configuration supplies one RPMB partition 16MB in size.

1.14. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

1.15. Sleep (CMD5)

An iNAND 7550 MCP device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer to JESD84-B51.

1.16. Enhanced Reliable Write

iNAND 7550 MCP supports enhanced reliable write as defined in e.MMC 5.1 spec.

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

1.17. Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation

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- Power failure
- Hardware reset

Following a sanitize operation completion, no data should remain in the unmapped host address space.

1.18. Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND 7550 MCP supports the optional Secure Erase command.

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

1.19. Secure Trim

For backward compatibility reasons, iNAND 7550 MCP supports Secure Trim command. The Secure

Trim command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

The secure trim command is performed in two steps:

1. Marks the LBA range as candidate for erase.
2. Erases the marked address range and ensures no old copies are left.

1.20. Partition Management

iNAND 7550 MCP offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore, memory block area scan be classified as follows:

- Factory configuration supplies two boot partitions (refer to section 1.12) implemented as enhanced storage media and one RPMB partitioning of 16MB in size (refer to section 1.13).
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

1.21. Device Health

Device Health is similar to SMART features of modern hard disks; it provides only vital NAND flash program/erase cycles information in percentage of the flash life span.

The host can query Device Health information utilizing standard MMC command, to get the extended CSD structure:

DEVICE_LIFE_TIME_EST_TYP_A[268], The host may use it to query SLC device health information

DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query TLC device health information

The device health feature will provide a % of the wear of the device in 10% fragments.

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1.22. EOL Status

EOL status is implemented according to the e.MMC 5.1 spec. One additional state (state 4) was added to iNAND 7550 MCP which indicates that the device is in EOL mode.

1.23. Enhanced Write Protection

To allow the host to protect data against erase or write iNAND 7550 MCP supports two levels of write protect command:

- The entire iNAND 7550 MCP (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD
- Specific segments of iNAND 7550 MCP may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register

For additional information please refer to the JESD84-B51 standard.

1.24. High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in JESD84-B51 enables low read latency operation by suspending a lower priority operation before it is actually completed.

For additional information on the HPI function, refer to JESD84-B51.

1.25. H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B51 standard.

1.26. Host-Device Synchronization Flow (Enhanced STROBE)

The Enhanced STROBE feature as implemented in iNAND 7550 MCP allows utilizing STROBE to synchronize also the CMD response:

- CMD clocking stays SDR (similar to legacy DDR52)
- Host commands are clocked out with the rising edge of the host clock (as done in legacy e.MMC devices)
- iNAND 7550 MCP will provide STROBE signaling synced with the CMD response in addition to DATA Out
- Host may use the STROBE signaling for DAT and CMD-Response capturing eliminating the need for a tuning mechanism

This feature requires support by the host to enable faster and more reliable operation.

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1.27. Command-Queue

e.MMC Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash

1.28. Frequent Used Commands in CmdQ

The Frequent Used Commands feature permits the following commands to be sent by the host when queue is non-empty FLUSH, BARRIER and DISCARD. In addition, the Frequent Used Commands feature provides alternative encodings for these commands to facilitate faster processing in device.

This feature can increase the effective performance when using Command Queue mode.

1.29. HS400 Tuning

This feature enables tuning command (CMD21) in HS400 mode, which may be used for calibration of DLL to compensate of PCB design/manufacturing differences. The Host may use adjustable sampling to determine the correct sampling point. A predefined tuning block stored in Device may be used by the Host as an aid for finding the optimal data sampling point. The Host can use CMD21 tuning command to read the tuning block.

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2. PRODUCT SPECIFICATIONS

2.1. Typical Power Requirements

Table 3 – iNAND 7550 MCP **Power Consumption Sleep** (Ta=25°C@3.3/1.8V)

	64GB	Units
HS400 Sleep (CMD5 – VCCQ, VCC off)	150	uA
HS200 Sleep (CMD5 – VCCQ, VCC off)	150	uA

Table 4 - iNAND 7550 MCP, **Power Consumption Peak** (Max) VCC / VCCQ (Ta=25°C@3.3V/1.8V)

		64GB	Units
Active HS400	Peak [2µs window] VCC	270	mA
	Max [1ms window] VCCQ	340	mA
Active HS200	Peak [2µs window] VCC	270	mA
	Max [1ms window] VCCQ	340	mA

Table 5 - iNAND 7550 MCP, **Power Consumption RMS** VCC / VCCQ (Ta=25°C@3.3V/1.8V)

			64GB	Units
HS400	RMS [100ms window] VCC	Read	80	mA
		Write	90	mA
	RMS [100ms window] VCCQ	Read	245	mA
		Write	160	mA
HS200	RMS [100ms window] VCC	Read	80	mA
		Write	90	mA
	RMS [100ms window] VCCQ	Read	245	mA
		Write	160	mA

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2.2. Operating Conditions

2.2.1. Operating and Storage Temperature Specifications

Table 6 - Operating and Storage Temperature

Temperature Case	Minimum and Maximum Operating*	-25° C to 85° C
	Minimum and Maximum Non-Operating: After soldered onto PCBA	-40° C to 85° C

* Per eMMC5.1 specification (JESD84-B50): To achieve optimized power/performance, maximum Tcase temperature should not exceed 85°C.

2.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND 7550 MCP is MSL = 3.

2.3. Reliability

SanDisk iNAND 7550 MCP product meets or exceeds NAND type of products Endurance and Data Retention requirements as per evaluated representative usage models for designed market and relevant sections of JESD47I standard.

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Table 7 - Critical Reliability Characteristics

Reliability Characteristics	Description	Value
Uncorrectable Bit Error Rate (UBER)	Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events data can be lost.	**1 sector in 10^{15} bits read**

Write Endurance Specification (TBW)	Write endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload written at certain operated temperature range.
	Representative workload description:
	• 80% Sequential write, 20% Random Write.
	• Distribution of IO Transaction Sizes:
	  ○ <16KB: 82%
	  ○ 16KB-128KB: 17%
	  ○ >128KB: 1%
	• Cache On, Packed Off
	• Host data is 4K aligned
	• 30% of product lifetime operate @85° C T-case
	• 70% of product lifetime operate @55° C T-case
		Total Terabytes Written [TBW] Per representative Android workload:
		64GB: 80[TB]

Data Retention Specification (Years)	Fresh or Early Life Device (A device whose total write cycles to the flash is less than 10% of the maximum endurance specification)	**10 years of Data Retention @ 25°C & 55°C**
	Cycled Device (Any device whose total write cycles are between 10% of the maximum write endurance specification and equal to or exceed the maximum write endurance specification)	**1 year of Data Retention @ 25°C & 55°C** Note: In the case where the number of writes exceed the endurance spec read and Write performance can be intermediately reduced.

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2.4. System Performance

Table 8 –Sequential Performance

	HS400	
	Write (MBs)	**Read (MBs)**
64GB	230	300

Table 9 – Random Performance

	HS400		
	Write (IOPs)	**Read (IOPs)**	
	Cache ON	**CmdQ ON**	**CmdQ OFF**
64GB	15K	20K	8K

Note 1: Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bit at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB.

Note 2: Random performance is measured with a chunk size of 4KB and address range of 1GB.

Note 3: All performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT).

Note 4: Sequential Write performance is measured for 400MB host payloads.

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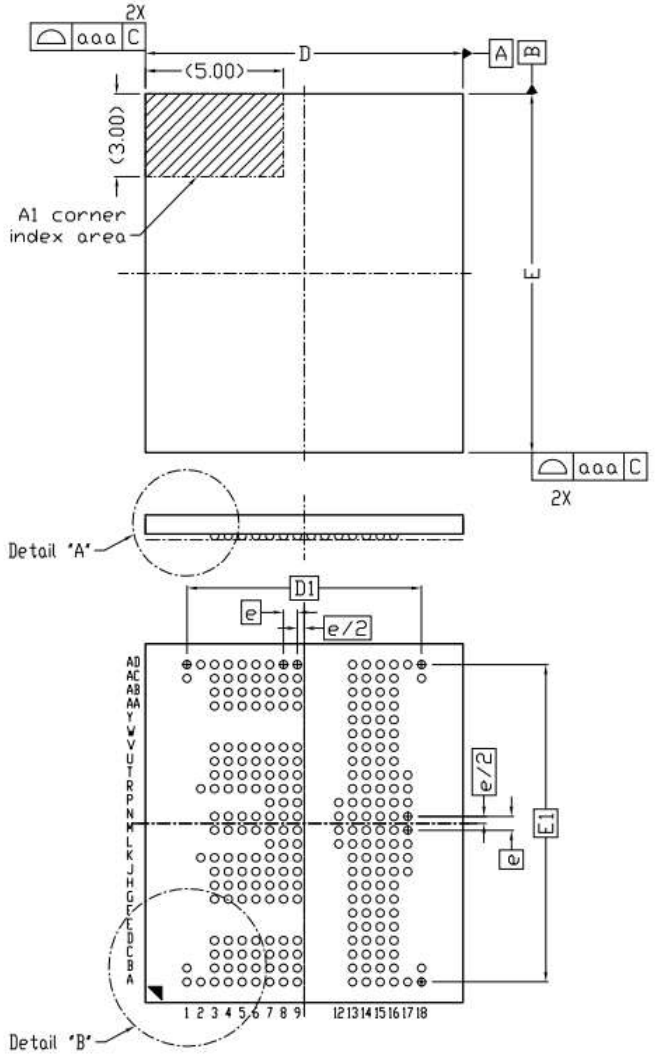
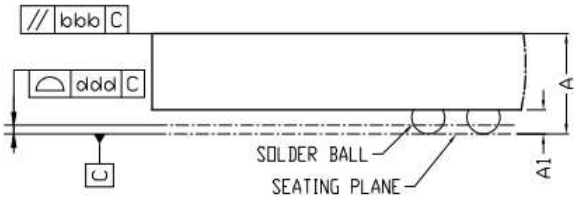
3. PHYSICAL SPECIFICATIONS



BOTTOM VIEW
BALL DIMENSIONS & PIN NUMBER



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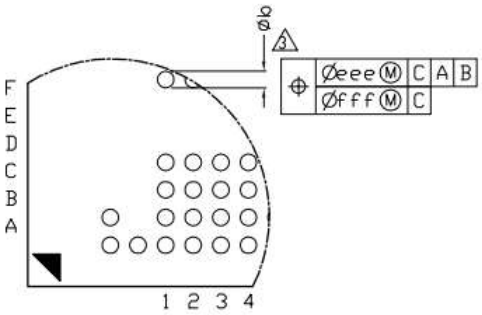

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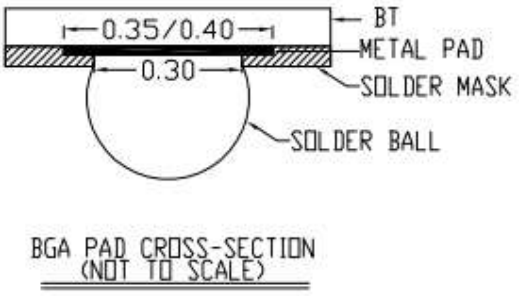

Figure 5- INAND 7550 MCP Package Outline Drawing

Table 10.1 –Package Specification 254-BGA 1.0mm (64+32 configuration)

Symbol	Dimension in millimeters		
	Minimum	Nominal	Maximum
A	0.8		1
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13	13.1
D1	-	8.5	-
E1	-	11.5	-
e	-	0.5	-
b	0.25	0.3	0.35
aaa	0.1		
bbb	0.1		
ddd	0.08		
eee	0.15		
fff	0.05		

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Table 10.2 –Package Specification 254-BGA 1.1mm (64+48 configuration)

Symbol	Dimension in millimeters		
	Minimum	Nominal	Maximum
A	0.9		1.1
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13	13.1
D1	-	8.5	-
E1	-	11.5	-
e	-	0.5	-
b	0.25	0.3	0.35
aaa	0.1		
bbb	0.1		
ddd	0.08		
eee	0.15		
fff	0.05		

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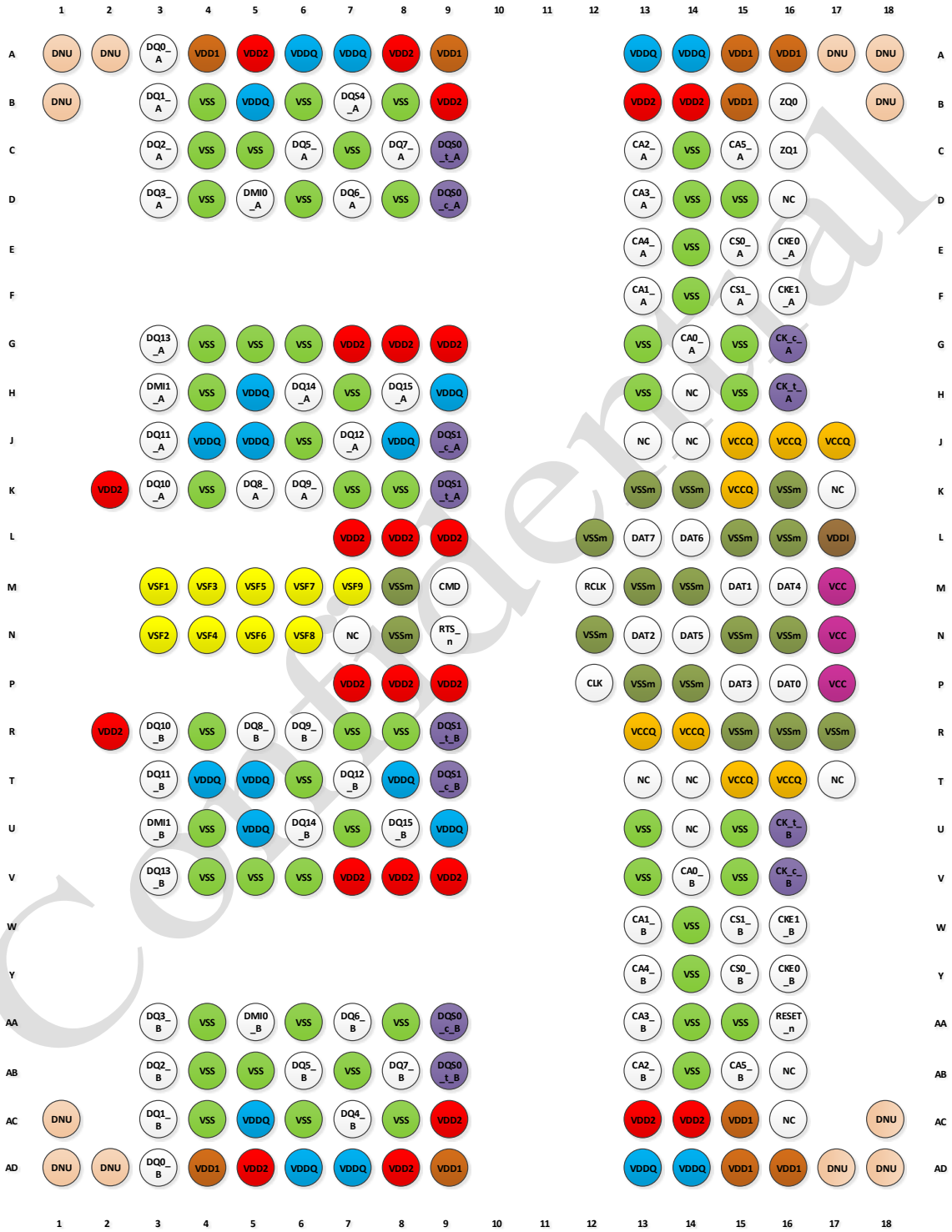
4. INTERFACE DESCRIPTION

4.1. MMC I/F Ball Array

Figure 6 - LPDDR4, 11.5x13mm, 0.5mm pitch, 254ball, 2 channel x32 MCP (top view)



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Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5:0]_B	Input	**Command/Address Inputs:** Provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. ODT-CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 and VSS.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output** : Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Read Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center aligned with Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240-Ω ± 1% resistor.
VDD1, VDD2, VDDQ	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS	GND	**Ground Reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET pin resets both channels of the die.

Table 11 – eMMC iNAND pin assignment

Ball Signal	Type	Description
DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
DAT1		
DAT2		
DAT3		
DAT4		
DAT5		
DAT6		
DAT7		
CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
QRDY	O	An optional pin, disabled by default, toggled by the device when the value of QSR changes.
CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
RST_n		Hardware Reset
RCLK	Output	Data Strobe
VCC	Supply	Flash I/O and memory power supply
VCC		
VCC		
VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
VCCQ		
VCCQ		
VCCQ		
VCCQ		
VSS	Supply	Flash I/O and memory ground connection
VSS		
VSS		
VSS		
VSS		
VSS		
VSSm	Supply	Flash I/O and memory ground connection (dedicated to eMMC)
VSSQ	Supply	Memory controller core and MMC I/F ground connection
VSSQ		
VSSQ		
VSSQ		
VSSQ		
VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground
VSF1	VSF	Vendor Specific Function balls for test/debug. VSF balls should be floating and be brought out to test pads.
VSF2		
VSF3		
VSF4		

Note: All other pins are not connected [NC] and can be connected to GND or left floating

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4.2. Registers value

4.2.1. OCR Register

Parameter	DSR slice	Description	Value	Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7 - 3.6 range	1FFh	9
	[14:8]	VDD: 2.0 - 2.6 range	00h	7
	[7]	VDD: 1.7 - 1.95 range	1h	1

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready.

4.2.2. CID Register

Parameter	DSR slice	Description	Value	Width
MMC MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Card BGA	01h	2
OID	[111:104]	OEM/Application ID	00h	8
PNM	[103:56]	Product name	32GB – DL2032	48
PRV	[55:48]	Product revision	01h	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	CRC7 checksum	CRC7 Generator	7

Note: Please refer to the definition of the MDT field as defined in eMMC Spec version 5.0.

4.2.3. DSR Register

Parameter	DSR slice	Description	Value	Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Note: DSR is not implemented; in case of read, a value of 0x0404 will be returned.

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4.2.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	3h	3
SPEC_VERS	[125:122]	System specification version	4h	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	8F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	1
DSR_IMP	[76:76]	DSR implemented	0b	1
*C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	7h	3
C_SIZE_MULT	[49:47]	Device size multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase group size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write protect group size	0Fh	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer default	0h	2
R2W_FACTOR	[28:26]	Write speed factor	2h	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0h	1
CONTENT_PROT_APP	[16:16]	Content protection application	0h	1
FILE_FORMAT_GRP	[15:15]	File format group	0h	1
COPY	[14:14]	Copy flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0h	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0h	1
FILE_FORMAT	[11:10]	File format	0h	2
ECC	[9:8]	ECC code	0h	2
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

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4.2.5. EXT_CSD Register

Parameter	ECSD slice	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0h
EXT_SUPPORT	[494]	Extended partitions attribute support	3h
SUPPORTED_MODES	[493]	FFU supported modes	3h
FFU_FEATURES	[492]	FFU features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation codes timeout	10h
FFU_ARG	[490:487]	FFU Argument	0h
BARRIER_SUPPORT	[486]	Cache barrier support	1h
CMDQ_SUPPORT	[308]	Command queue support	1h
CMDQ_DEPTH	[307]	Command queue depth	1Fh
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW sectors correctly programmed	0h
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor proprietary health report	0h
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation type B (MLC)	0h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation type A (SLC)	0h
PRE_EOL_INFO	[267]	Pre EOL information	0h
OPTIMAL_READ_SIZE	[266]	Optimal read size	8h
OPTIMAL_WRITE_SIZE	[265]	Optimal write size	8h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal trim unit size	8h
DEVICE_VERSION	[263:262]	Device version	5051h
FIRMWARE_VERSION	[261:254]	Firmware version	FW Version
PWR_CL_DDR_200_360	[253]	Power class for 200MHz, DDR at VCC= 3.6V	0h
CACHE_SIZE	[252:249]	Cache size	0h

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Parameter	ECSD slice	Description	Value
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power off notification(long) timeout	19h
BKOPS_STATUS	[246]	Background operations status	Default = 0h
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	FFh
CACHE_FLUSH_POLICY	[240]	Cache Flush Policy	1h
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at VCC = 3.6V	0h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at VCC = 1.95V	0h
PWR_CL_200_195	[237]	Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	0h
PWR_CL_200_130	[236]	Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM _MULT	[232]	TRIM Multiplier	3h
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	A6h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	A6h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	20h
ACCESS_SIZE	[225]	Access size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	1h (see WP group size table below)
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	3h
REL_WR_SEC_C	[222]	Reliable write sector count	1h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	10h (see WP group size table below)
S_C_VCC	[220]	Sleep current [VCC]	64GB: 8h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	Production state awareness timeout	17h
S_A_TIMEOUT	[217]	Sleep/Awake time out	13h
SLEEP_NOTIFICATION_TIME	[216]	Sleep notification timeout	17h

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Parameter	ECSD slice	Description	Value
SEC_COUNT	[215:212]	Sector count	See exported capacity table below
SECURE_WP_INFO	[211]	Secure Write Protect Info	1h
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	0h
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition switching timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	Ah
DRIVER_STRENGTH	[197]	I/O Driver Strength	1Fh (Reporting four strengths, but supporting only one)
CARD_TYPE	[196:195]	Card Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	8h
CMD_SET	[191]	Command Set	Default = 0h Updated in runtime
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	Dh
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in runtime by the host
DATA_STRB_MODE_SUPPORT	[184]	Data strobe mode support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h Updated in runtime by the host
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in runtime by the host
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in runtime by the host
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h

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Parameter	ECSD slice	Description	Value
			Updated in runtime by the host
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in runtime by the host
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in runtime
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	80h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	15h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h Updated in runtime by the host
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in runtime by the host
BKOPS_EN	[163]	Enable background operations handshake	2h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by the host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by the host
PARTITIONING SUPPORT	[160]	Partitioning support	7h Note: EUDA is not supported
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	0h
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host
PARTITION_SETTING_ COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host
GP_SIZE_MULT	[154:143]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
PRODUCTION_STATE_AW ARENESS	[133]	Production state awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h

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Parameter	ECSD slice	Description	Value
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR mode support	0h
VENDOR_SPECIFIC_FIELD	[127:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native sector size	0h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	Ah
CLASS_6_CTRL	[59]	Class 6 commands control	0h
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in runtime
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h Updated in runtime
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Updated in runtime by the host
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h
BARRIER_CTRL	[31]	Cache barrier	0h
MODE_CONFIG	[30]	Mode config	0h
MODE_OPERATION_CODES	[29]	Mode operation codes	0h
FFU_STATUS	[26]	FFU status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Pre loading data size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max pre loading data size	See Max Preloading size table below
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product state awareness enablement	3h AUTO_PRE_SOLDERING
SECURE_REMOVAL_TYPE	[16]	Secure Removal Type	8h
CMDQ_MODE_EN	[15]	Command queue	0h

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4.2.6. User Density

The following table shows the capacity available for user data for the different device sizes:

Table 12: Capacity for user data

Capacity	LBA [Hex]
64GB	0x747C000

Table 13: Write protect group size

Capacity	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
64GB	0x1	0x10	0.5MB	8MB

Table 14: Max Preloading Data Size

Capacity	MAX_PRE_LOADING_DATA_SIZE (in LBA Hex)	Max preloading Image in MB
64GB	2,670,998	19,681

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5. POWER DELIVERY AND CAPACITOR SPECIFICATIONS

5.1. SanDisk iNAND 7550 MCP Power Domains

SanDisk iNAND 7550 MCP has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 17 below.

Table 15 - Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges:
		Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range:
		High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

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5.2. Capacitor Connection Guidelines

		Min	Nom	Max		Capacitance
e.MMC	VCCQ (Low)	1.7	1.8	1.95	V	4.7uF + 0.1uF
	VCCQ (High)	2.7	3.3	3.6	V	4.7uF + 0.1uF
	VCC	2.7	3.3	3.6	V	4.7uF + 0.1uF
	VDDi				V	0.1uF-2.2uF
LPDDR4x	VDD1	1.7	1.8	1.95	V	-
	VDD2	1.06	1.1	1.17	V	-
	VDDQ	0.57	0.6	0.65	V	-

It is recommended to place the following capacitors on VCC & VCCQ domains:

- Cin1 = 4.7uF
    - E.g. :

Manufacturer	Manufacturer P/N
MURATA	GRM185R60J475ME15D
TAIYO YUDEN	JMK107BJ475MK-T

- Cin2 = 0.1uF
    - E.g. :

Manufacturer	Manufacturer P/N
MURATA	GRM155R71A104KA01D
KYOCERA	CM05X5R104K06AH

For VDDi (1.1V), it is recommended to place:

- 0.1uF <= Cin(VDDi) <= 2.2uF
    - E.g. :

Manufacturer	Manufacturer P/N
TAIYO YUDEN	JDK105BJ225MV
PANASONIC	ECJ0EB0J225M
SAMSUNG	CL05A225MQ5NSNC

- For HS200/400 can use 0.1 uF <= Cin(VDDi) <= 2.2uF

Capacitors Type:

- SMT-Ceramic
- X5R/X7R
- 6.3V/10V

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- Min height – 0.55mm
- Foot Print: 0402 or above

When using a low value ceramic input filter capacitor, it should be located as close to the supply ball as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply.

Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

Make all of the power (high current) traces as short, direct, and thick as possible. The capacitors should be as close to each other as possible, as it reduces EMI radiated by the power traces due to the high switching currents through them. In addition it shall also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringings, and resistive losses which produce voltage errors.

The grounds of the IC capacitors should be connected close together directly to a ground plane. It is also recommended to have a ground plane on both sides of the PCB, as it reduces noise by reducing ground loop errors as well.

The loop inductance per capacitor shall not exceed 3nH (both on VCC/VCCQ & VSS/VSSQ loops).

Cin2 shall be placed closer (from both distance & inductance POV) to the iNAND power & ground balls.

Multiple via connections are recommended per each capacitor pad.

On test platforms, where the iNAND socket is in use, the loop inductance per capacitor shall not exceed 5nH (both on VCC/VCCQ & VSS/VSSQ loop).

No passives should be placed below the iNAND device (between iNAND & PCB).

VSF balls (VSF1/4) should have exposed and floated test pads on the PCB, with near exposed GND for better measurement.

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6. PROPRIETY iNAND 7550 MCP FEATURE OVERVIEW

6.1. Content Preloading Operation Mode

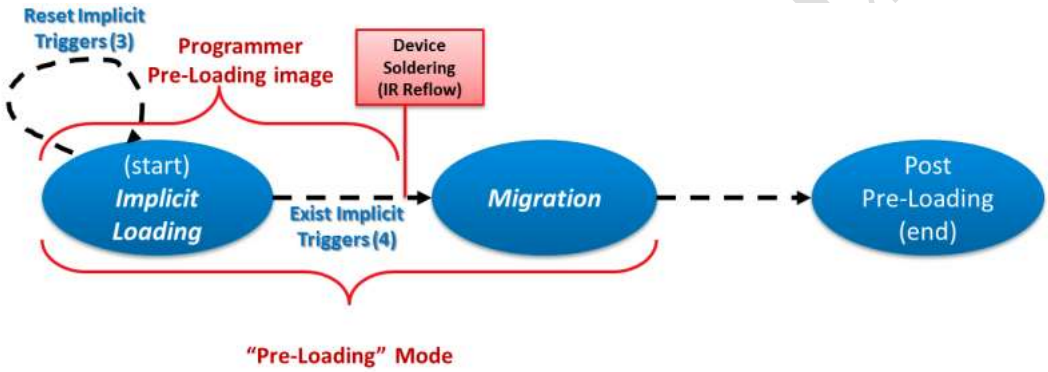
High temperature during IR-Reflow process on 3D - X3 flash devices cause significant increase of read errors on TLC blocks (Uncorrectable read errors of data that was programmed before the IR Reflow process).

This high level of read errors is higher compared to previous flash technologies

Currently this level of errors cannot be fixed by special error correction algorithms (as it was done in previous flash technologies)

To overcome these challenges iNAND 7550 MCP introduced the Pre-Loading feature, which solves the IR-Reflow process's reliability, by writing the preloaded data to the SLC area of the device.

Every iNAND 7550 MCP fresh device is defined to start in Implicit Loading state. There are several of exit triggers that will switch it to Migration state. Once Migration is completed the device will start to work in normal state.



During Implicit mode all written data (the preloaded data before IR-Reflow) will be written to the SLC area of the device.

Max preloading data allowed is 33% of the device exported capacity.

Exit triggers from Implicit to Migration stage:

- Host accumulated written data payload that is >33% of the exported capacity.
- Host switches interface to High-Speed bus (HS200/400).
- (Recommended) Host issues Vendor Specific command signals to device signaling "IR-Reflow completed"

Triggers to reset Implicit mode counters (Only possible during Implicit mode and if device switched already to Migration stage there is no option to reverse/reset it to Implicit stage anymore):

- Host erases the whole written user area.
- Host issues Vendor Specific command of "Production Restore to Default"
- Firmware Download

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During Migration state the device will do automatic relocation of the preloaded data written to SLC blocks during implicit more to TLC blocks, after IR reflow.

It is recommended to allow system BKOPs during IDLE time that will expedite the folding of the preloaded data from SLC to TLC.

6.2. SmartSLC

The iNAND SmartSLC feature gives the customer the write performance they require, so that they will have a UX experience that makes an X3 memory look better than X2. The iNAND SmartSLC provides the following value to the system:

- Auto-adjust iNAND performance per application need
- Improves system efficiency and UX
    - Reduce system WRITE-BUSY time by improving IO throughput
- Vertical iNAND technology:
    - Host access to iNAND NAND flash performance capabilities
    - Controller and Firmware auto-detections of hosts needs and auto-adjustment device behavior based on these host needs
    - Host (e.MMC driver) customizations and modifications in IDLE time management to allow optimized utilization of SmartSLC capabilities

iNAND 7550 MCP uses allocated SLC blocks within the SanDisk NAND design to implement the feature. The allocation of these blocks does not impact the as sold capacity of the device (Exported Capacity). The device uses a detection mechanism and once a pattern requiring sequential write performance is detected, the device postpones any background management operations, if feasible,) and dedicates resources to SLC programing. Any IDLE state bigger than tIDLE [ms], shall trigger migration operations to free up enough space for the next burst and eliminate potential performance drop.

iNAND SmartSLC buffer size and Performance for SDADA4CR-64G products (BigFile Mode)

Capacity (GB)	Buffer size (GB)	Write speed * (MB/s)
64GB	16	230

* Sequential write Performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT), 512KB chunk, enough recovery time before measurement @ HS400.

Emptying the iNAND SmartSLC buffer

There are a number of host enabled mechanisms that can be used to empty the SmartSLC buffer (migration). All of these modes can be enabled at the same time or only a single or a few modes can be selected. The more modes that are supported by the host, the more the buffer will be available and empty for use in observing host high speed payloads. During migration time there won't be degradation of device performance and no impact on latency and system responsiveness. Host

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optional configuration for iNAND SmartSLC:

1. IDLE only mode (PoN=1) – Recommended option.
2. BKOPs APIs with HPI
3. Sleep Notification before standby (CMD5)

	1. Host allow House-Keeping during IDLE (Auto BKOPs)		**2. Host periodically send BKOPs API (Manual BKOPs)**
SmartSLC Buffer migration	**Migration during in system IDLE with HPI**	**Migration during in system IDLE with HPI**	**Migration during BKOPs Busy**
EXT_CSD REV[192]	7h (e.MMC 5.0)	8h (e.MMC 5.1)	7h or 8h (e.MMC 5.0/5.1)
AUTO_EN BKOPS_EN[163][1]	Don't care	1h	0h
POWER_OFF_NOTIFICATION [34] (PON activated)	1h (POWERED_ON)	1h (POWERED_ON)	Don't care
BKOPS_EN BKOPS_EN[163][0]	Don't care	Don't care	1h
POWER_OFF_NOTIFICATION [34] (Sleep Notification)	No	No	No
Standby mode CMD5	If system uses CMD5 it is requires 5-10sec delay before CMD5 transmission	If system uses CMD5 it is requires 5-10sec delay before CMD5 transmission	Don't care

6.3. Device Report

iNAND 7550 MCP introduce new proprietary Device Report feature that reflects the Firmware and Device status.

- Enabling Device Report Mode: Send CMD62 with argument of 0x96C9D71C - R1b Response will be returned
- Reading Device Report Data: Once the host enters Device Report mode, CMD63 with argument 0x00000000 will retrieve the report - 512 Bytes will be returned to the host (Note: CMD63 behaves similarly to CMD17)
- Resume Normal Operation Mode: Once the Device Report read command (CMD63) was completed, the device automatically goes out of Device Report mode, and resumes normal operation mode.

Byte Offset	**Size (Bytes)**	**Field**	**Comments**
[3:0]	4	Average Erase Cycles Enhanced	The Average Program/Erase count for all Enhanced Blocks
[7:4]	4	Average Erase Cycles SLC	The Average Program/Erase count for all SLC Blocks
[B:8]	4	Average Erase Cycles MLC	The Average Program/Erase count for all MLC Blocks

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[F:C]	4	Read reclaim count Enhanced	The amount of Reads on enhanced area which passed Read-refresh thresholds and requires reclaim
[13:10]	4	Read reclaim count SLC	The amount of Reads on SLC area which passed Read-refresh thresholds and requires reclaim
[17:13]	4	Read reclaim count MLC	The amount of Reads on MLC area which passed Read-refresh thresholds and requires reclaim
[1B:18]	4	Bad Block Manufactory	All BB detected during manufacturing process
[1F:1C]	4	Bad Block Runtime Enhanced	All BB related to Enhanced partition detected during run-time
[23:20]	4	Bad Block Runtime SLC	All BB related to SLC partition detected during run-time
[27:24]	4	Bad Block Runtime MLC	All BB related to MLC partition detected during run-time
[2B:28]	4	Patch Trial Count	The number of Field Firmware Updates done from the beginning of the device life time
[37:2C]	12	Patch Release Date	Current FFU Release date
[3F:38]	8	Patch Release Time	Current FFU Release hour
[43:40]	4	Cumulative Write data size	Counts the amount of Host Writes transaction (100MB multiplication)
[47:44]	4	Number of occurrences of VCC voltage drops	Counts the number of ungraceful Power Down to the device
[4B:48]	4	Number of occurrences of VCC voltage droops	Counts the number of times Power-Droop (Slight power-droop below certain threshold) were detected
[4F:4C]	4	Number of failures recover new host data after Power Loss	Every time NEW Host data is dismissed due to Power Loss, this counter will be incremented.
[53:50]	4	Total Recovery Operations After Voltage Droop	The total amount of recovery operation required to be done by the device while power-droop was detected
[511:54]	428	Spare Fields	

Power-Loss indications:

iNAND 7550 MCP is also serving the host by notifying him on cases of Power -Loss events and internal handling of those events. A dedicated field in the EXT_CSD register was allocated to indicate the occurrence of Power Loss/Write Abort during the last power down. This field reports if a Power Loss was detected and recovered during the last power-up.

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In order to retrieve this field, the host should issue CMD8 command – SEND_EXT_CSD. This command returns full EXT_CSD structure – 512 bytes as block of data. Following is the EXT_CSD field details:

Name	Field	Size (bytes)	Cell Type	Hex Offset	Dec. Offset
Power Loss indication	POWER_LOSS_REPORT	1	R	0x79	121

POWER_LOSS_REPORT [121] details:

- Bit[2]: RECOVERY_SUCCESS
  0x1: Recovery passed successfully
  0x0: Recovery failed
- Bit[1]: RECOVER_OLD_DATA
  0x1: Recovery to old copy of data
  0x0: No data recovery required
- Bit[0]: POWER_LOSS_DETECTED
  0x1: Unexpected Power Loss was detected - Detection is done during initialization, immediately after Power-Up

Note: In case Power Loss did not occur on last shut down, this register will show 0x00.

Unstable Power-Supply indications:

In case of Flash voltage drop, the iNAND may not be able to recover the data that was already transferred to the iNAND device, but wasn't committed in the Flash. In this case the iNAND will "abort" the current host write and return back to the host with an error indication.

iNAND 7550 MCP will use BIT19 and BIT20 (cc_error) in the command response to indicate VDET error status to the host. The VDET error indication can be seen only if CMD13 was issued, or in the next command response.

Examples:

- Open Mode (CMD25+CMD12+CMD13):
  In both cases, where the voltage droop occurs before or after CMD12:
  CMD12 response will not have BIT19 and BIT20 set.
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
  Note: The host may send many CMD13 and the BIT19 will be set only in first CMD13 after releasing the busy.
- Close Mode (CMD23+CMD25+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
- Single Block Mode (CMD24+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response

Host shall retry latest command as long as the VDET error indication on CMD13 response (or next command response (BIT19 and BIT20 are set) is still set.

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7. MARKING

First row: Simplified SanDisk Logo

Second row: Sales item P/N

Third row: Country of origin i.e. ‘TAIWAN’ or ‘CHINA’

Fourth row: Y- Last digit of year

WW- Work week

D- A day within the week

MTLLLXXX – Internal use

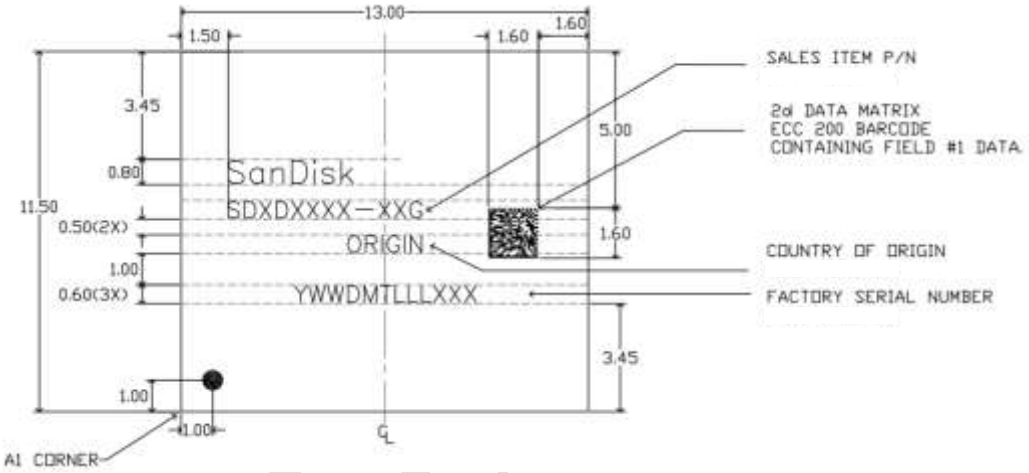

Figure 7 - Product marking

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8. ORDERING INFORMATION

Capacity – NAND	Capacity – LPDDR4x	Part Number	Package	eMMC
64GB	32Gb	SDADA4CR-64G	11.5mm x 13mm x 1.0mm	5.1
64GB	48Gb	SDADA4DR-64G	11.5mm x 13mm x 1.1mm	5.1

Note 1: Generic part number has a "G" after the capacity and custom part number does not. Customer Code (optional) will be added at the end of the part number. The Customer Code can be up to 4 digits. Example:

Customer	Customer Code	Customer Part Number
Customer A	326	SDADA4CR-64-326
Customer B	4733	SDADA4CR-64-4733

Note 2: Unique Identifier (optional) is a single character identifier specifying certain custom attributes. E.g., Suffix "T" added to the P/N indicates tape/reel. SDADA4CR-64G would become SDADA4CR-64G-T. The default P/Ns are shipped in trays.

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Appendix A – 8 Gb LPDDR4X SDRAM FEATURES

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2 = 1.1V (1.06V to 1.17V)
- VDDQ = 0.6V (0.57V to 0.65V)
- Programmable CA ODT and DQ ODT with VSSQ termination
- VOH compensated output driver
- Single data rate command and address entry
- Double data rate architecture for data Bus;
  - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
- DMI pin support for write data masking and DBIdc functionality
- Programmable RL (Read Latency) and WL (Write Latency)
- Burst length: 16 (default), 32 and On-the-fly
  - On the fly mode is enabled by MRS
- Auto refresh and self refresh supported
- All bank auto refresh and directed per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- Background ZQ Calibration

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IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

All values are based on 2 channel.

IDD specifications (1/3)

Table - LPDDR4 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	3200	3733	Units	Notes
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD0_1$	VDD1	24.2		mA	
	$IDD0_2$	VDD2	68.6		mA	
	$IDD0_Q$	VDDQ	1.32		mA	3
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD2P_1$	VDD1	1.95		mA	
	$IDD2P_2$	VDD2	6.75		mA	
	$IDD2P_Q$	VDDQ	0.8		mA	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2PS_1$	VDD1	1.95		mA	
	$IDD2PS_2$	VDD2	6.75		mA	
	$IDD2PS_Q$	VDDQ	0.8		mA	3
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2N_1$	VDD1	1.95		mA	
	$IDD2N_2$	VDD2	37.3		mA	
	$IDD2N_Q$	VDDQ	1.32		mA	3
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2NS_1$	VDD1	1.95		mA	
	$IDD2NS_2$	VDD2	31.3		mA	
	$IDD2NS_Q$	VDDQ	1.32		mA	3
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3P_1$	VDD1	9		mA	
	$IDD3P_2$	VDD2	9		mA	
	$IDD3P_Q$	VDDQ	0.8		mA	3

IDD specifications (2/3)

Parameter/Condition	Symbol	Power Supply	3200	3733	Units	Notes
Active power-down standby current with clock stop:	$IDD3PS_1$	VDD1	9		mA	
CK_t=LOW, CK_c=HIGH;	$IDD3PS_2$	VDD2	9		mA	
CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3PS_Q$	VDDQ	0.8		mA	4
Active non-power-down standby current:	$IDD3N_1$	VDD1	13.2		mA	
tCK = tCKmin;	$IDD3N_2$	VDD2	38.3		mA	
CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3N_Q$	VDDQ	1.32		mA	4
Active non-power-down standby current with clock stopped:	$IDD3NS_1$	VDD1	13.2		mA	
CK_t=LOW, CK_c=HIGH;	$IDD3NS_2$	VDD2	31.1		mA	
CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3NS_Q$	VDDQ	1.32		mA	4
Operating burst READ current:	$IDD4R_1$	VDD1	25	28	mA	
tCK = tCKmin;	$IDD4R_2$	VDD2	386	440	mA	
CS is LOW between valid commands; One bank is active; BL = 8; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_Q$	VDDQ	181	183	mA	5
Operating burst WRITE current:	$IDD4W_1$	VDD1	28	30	mA	
tCK = tCKmin;	$IDD4W_2$	VDD2	334	382	mA	
CS is LOW between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4W_Q$	VDDQ	1.32	1.32	mA	4
All-bank REFRESH Burst current:	$IDD5_1$	VDD1	93.1		mA	
tCK = tCKmin;	$IDD5_2$	VDD2	253		mA	
CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5_Q$	VDDQ	1.32		mA	4
All-bank REFRESH Average current:	$IDD5AB_1$	VDD1	8		mA	
tCK = tCKmin;	$IDD5AB_2$	VDD2	48		mA	
CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5AB_Q$	VDDQ	1.32		mA	4

IDD specifications (3/3)

Parameter/Condition	Symbol	Power Supply	3200	3733	Units	Notes

Per-bank REFRESH Average current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI/8;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	$IDD5PB_1$	VDD1	8.1		mA	

	$IDD5PB_2$	VDD2	48		mA	
	$IDD5PB_Q$	VDDQ	1.32		mA	4
Self refresh current (85°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled	$IDD6_1$	VDD1	8.1		mA	6,7,9
	$IDD6_2$	VDD2	19.8		mA	6,7,9
	$IDD6_Q$	VDDQ	0.8		mA	4,6,7,9
Self refresh current (45°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6_1$	VDD1	1.65		mA	6,7,9
	$IDD6_2$	VDD2	3.69		mA	6,7,9
	$IDD6_Q$	VDDQ	0.3		mA	4,6,7,9
Self refresh current (25°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6_1$	VDD1	0.87		mA	6,7,9
	$IDD6_2$	VDD2	1.4		mA	6,7,9
	$IDD6_Q$	VDDQ	0.3		mA	4,6,7,9
Self refresh current (105°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6ET_1$	VDD1	28.5		mA	6,7,10
	$IDD6ET_2$	VDD2	42		mA	6,7,10
	$IDD6ET_Q$	VDDQ	0.33		mA	4,6,7,10

Notes:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. This is the general definition that applies to full array Self Refresh.
7. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
8. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
9. IDD6 85°C is guaranteed, IDD6 for 25°C and 45°C is typical of the distribution of the arithmetic mean.
10. IDD6ET is a typical value, is sampled only, and is not tested.

AC TIMING PARAMETERS (1/9)

Table - Core Parameters

Parameter	Symbol	min / max	Data Rate 533	1066	1600	2133	2667	3200	3733	4267	Unit	Note
ACTIVE to ACTIVE command period	tRC	min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)								ns	
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)								ns	
Self Refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)								ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 5nCK)								ns	
CAS to CAS delay	tCCD	min	8								tCK(avg)	2
CAS to CAS delay Masked Write w/ECC	tCCDMW	min	4 * tCCD								tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 8nCK)								ns	
RAS to CAS Delay	tRCD	min	max(18ns, 4nCK)								ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns,4nCK)								ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 4nCK)								ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)								ns	
		max	min(9 * tREFI * Refresh Rate, 70.2)								us	3
Write Recovery Time	tWR	min	max{18ns, 4nCK}								ns	
Write to Read Command Delay	tWTR	min	max(10ns, 8nCK)								ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 4ncK)								ns	
Precharge to Precharge Delay	tPPD	min	4								tCK	
Four Bank Activate Window	tFAW	min	40								ns	

Notes:
1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.
3. Refresh Rate is specified by MR4 OP[2:0].

Table - Clock timings

Parameter	Symbol	min / max	LPDDR4 1600	LPDDR4 2400	LPDDR4 3200	LPDDR4 4200	Unit	Note
Clock Timing								
Average Clock Period	tCK(avg)	min	1.25	0.833	0.625	0.467	ns	
		max	100	100	100	100		
Average high pulse width	tCH(avg)	min	0.46	0.46	0.46	tbd	tCK(avg)	
		max	0.54	0.54	0.54	tbd		
Average low pulse width	tCL(avg)	min	0.46	0.46	0.46	tbd	tCK(avg)	
		max	0.54	0.54	0.54	tbd		
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min				ns	
		max	-					
Absolute clock HIGH pulse width	tCH(abs)	min	0.43	0.43	0.43	tbd	tCK(avg)	
		max	0.57	0.57	0.57	tbd		
Absolute clock LOW pulse width	tCL(abs)	min	0.43	0.43	0.43	tbd	tCK(avg)	
		max	0.57	0.57	0.57	tbd		
Clock Period Jitter	tJIT(per)	min	-70	-50	-40	tbd	ps	
		max	70	50	40	tbd		
Maximum Clock Jitter between two consecutive clock cycles	tJIT(cc)	min	-				ps	
		max	140	100	80	tbd		

AC TIMING PARAMETERS (2/9)

Table - ZQ Calibration timings

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
ZQ Calibration Time	tZQCAL	max	1								us	
ZQ Calibration Latch Quiet Time	tZQLAT	max	max(30ns, 8nCK)								ns	
Calibration Reset Time	tZQRESET	max	max(50ns, 3nCK)								ns	

Table - DQ Tx Voltage and Timings (Read Timing parameters)

Parameter	Symbol	min max	1600/ 1867	2133/ 2400	3200	4266	Unit	Note
Data Timing								
DQS_t,DQS_c to DQ Skew	tDQSQ	max	0.18				UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min	min(tQSH, tQSL)				UI	1
DQ output window time total, per pin (DBI-Disabled)	tQW_total	min	0.75	0.73	0.7	0.7	UI	1,4
DQ output window time deterministic, per pin (DBI-Disabled)	tQW_dj	min	tbd	tbd	tbd	tbd	UI	1,4,3
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	max	tbd	tbd	tbd	tbd	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-enabled)	tQH_DBI	min	min(tQSH_DBI, tQSL_DBI)				UI	1
DQ output window time total, per pin (DBI-enabled)	tQW_total_DBI	min	tbd	tbd	tbd	tbd	UI	1,4
Read preamble	tRPRE	min	1.8				tCK(avg)	
Read postamble	tRPST	min	0.4				tCK(avg)	
Extended Read postamble	tRPSTE	min	1.4				tCK(avg)	
DQS Low-impedance time from CK_t, CK_c	tLZ(DQS)	min	(RL x tCK) + tDQSCK(Min) - (tPRE(Max) x tCK) - 200ps				ps	
DQS High-impedance time from CK_t, CK_c	tHZ(DQS)	max	(RL x tCK) + tDQSCK(Max) + (RPST(Max) x tCK) - 100ps				ps	
DQ Low-impedance time from CK_t, CK_c	tLZ(DQ)	min	(RL x tCK) + tDQSCK(Min) - 200ps				ps	
DQ High-impedance time from CK_t, CK_c	tHZ(DQ)	max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps				ps	
Data Strobe Timing								
DQS output access time from CK/CK#	tDQSCK	min	1.5				ns	8
		max	3.5					
DQSCK Temperature Drift	tDQSCK_temp	max	4				ps/C	9
DQSCK Volgate Drift	tDQSCK_volt	max	7				ps/mV	10
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	max	1.0				ns	11,12
DQS Output Low Pulse Width (DBI Disabled)	tQSL	min	tCL(abs)-0.05				tCK(avg)	4,5
DQS Output High Pulse Width (DBI Disabled)	tQSH	min	tCH(abs)-0.05				tCK(avg)	4,6
DQS Output Low Pulse Width (DBI Enabled)	tQSL_DBI	min	tCL(abs)-0.045				tCK(avg)	5,7
DQS Output High Pulse Width (DBI Enabled)	tQSH_DBI	min	tCH(abs)-0.045				tCK(avg)	6,7

Notes:

1. DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
2. The deterministic component of the total timing. Measurement method tbd.
3. This parameter will be characterized and guaranteed by design.
4. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) - 0.04.
5. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
6. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
7. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs).
8. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max

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voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The volage supply noise must comply to the component Min-Max DC Operating conditions.

9. tDQSCK_temp max delay variation as a function of Temperature.
10. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/ abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.
11. The same voltage and temperature are applied to tDQS2CK_rank2rank.
12. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
13. UI=tCK(avg)min/2

Table - DQ Rx Voltage and Timing Parameters (Write Timing Parameters)

Symbol	Parameter	min max	1600/1867[A)]	2133/2400	3200	4266	Unit	Note
VdIVW_total	Rx Mask voltage p-p total	max	140	140	140	120	mV	1,2,3,5
VdIVW_dV	Rx Mask voltage - deterministic	max	tbd	tbd	tbd	tbd	mV	1,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	max	0.22	0.22	0.25	0.25	UI	1,2,4,5
TdIVW_dj	Rx deterministic timing	max	tbd	tbd	tbd	tbd	UI	1,5
TdIVW_1bit	Rx timing window 1bit toggle (At VdIVW voltage levels)	max	tbd	tbd	tbd	tbd	UI	1,2,4,5 ,14
VIHL_AC	DQ AC input pulse amplitude p-p	min	180	180	180	170	mV	7,15
TdIPW	DQ input pulse width (At Vcent_DQ)	min	0.45	0.45	0.45	0.45	UI	8
TDQS2DQ	DQ to DQS offset	min	200	200	200	200	ps	9
		max	800	800	800	800		
TDQDQ	DQ to DQ offset	max	30	30	30	30	ps	10
TDQS2DQ_temp	DQ to DQS offset temperature variation	max	0.6	0.6	0.6	0.6	ps/°C	11
TDQS2DQ_volt	DQ to DQS offset voltage variation	max	33	33	33	33	ps/50mV	12
TDQS2DQ_rank2rank	DQ to DQS offset rank to rank	max	200	200	200	200	ps	17,18
tDQSS	Write command to 1st DQS latching transition	min	0.75				tCK(avg)	
		max	1.25					
tDQSH	DQS input high-level width	min	0.4				tCK(avg)	
tDQSL	DQS input low-level width	min	0.4				tCK(avg)	
tDSS	DQS falling edge to CK setup time	min	0.2				tCK(avg)	
tDSH	DQS falling edge hold time from CK	min	0.2				tCK(avg)	
tWPRE	Write preamble	min	1.8				tCK(avg)	
tWPST	0.5 tCK Write postamble	min	0.4				tCK(avg)	
tWPSTE	1.5 tCK Write postamble	min	1.4				tCK(avg)	
SRIN_dIVW	Input slew rate over VdIVW_total	min	1	1	1	1	V/ns	13
		max	7	7	7	7		

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >250KHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels.
5. Defined over the DQ internal Vref range. The Rx mask at the pin must be within the internal Vref DQ range irrespective of the input signal common mode.
6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd
7. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
8. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
9. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature vari-

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ation.

10. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
11. TDQS2DQ max delay variation as a function of temperature.
12. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2.
13. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
14. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
15. VIHL_AC does not have to be met when no transitions are occurring.
16. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
17. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

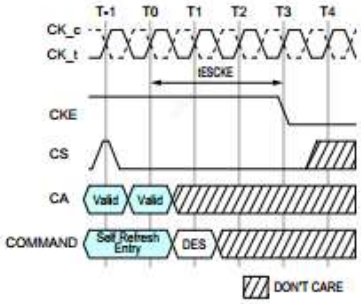
A. The following Rx voltage and timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min/2= 625ps for DQ=1600. For example the TdIVW_total(ps) =0.22*625ps= 137.5ps.

Table - Self-Refresh Timing Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Delay from Self Refresh Entry to CKE Input Low	tESCKE	min	max(1.75ns,3tCK)								nCK	1
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)								ns	1
Self refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)								ns	1,2

Note

1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.



2. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are only allowed during this period.

Table - Command Address Input Parameters

Symbol	Parameter	min max	DQ-1333[A)]	DQ-1600/ 1867	DQ-3200	DQ-4266	Unit	Note
VcIVW	Rx Mask voltage p-p	max	175	175	155	145	mV	1,2,4
tcIVW	Rx timing window	max	0.3	0.3	0.3	0.3	UI	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	min	210	210	190	180	mV	5,8
TcIPW	CA input pulse width	min	0.55	0.55	0.6	0.6	UI	6
SRIN_cIVW	Input slew rate over VcIVW	min	1	1	1	1	V/ns	7
		max	7	7	7	7		

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal Vref range. The Rx mask at the pin must be within the internal Vref CA range irrespective of the input signal common mode.

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5. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
6. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
8. VIHL_AC does not have to be met when no transitions are occurring.
9. UI=tCK(avg)min/2

A. The following Rx voltage and timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min= 1.5ns for DQ=1333. For example the TcIVW(ps) = 0.3*1.5ns=450ps.

Table - Boot Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Clock Cycle Time	tCKb	min	Note 1, 2								ns	
		max	Note 1, 2									
Address & Control Input Setup Time	tISb	min	1150								ps	
Address & Control Input Hold Time	tIHb	min	1150								ps	
DQS Output Data Access Time from CK/CK#	tDQSCKb	min	2								ns	
		max	10									
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb	max	1.2								ns	

Notes
1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

Table - Mode Register Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Additional time after tXP has expired until the MRR command may be issued	tMRRI	min	tRCD + 3nCK								ns	
MODE REGISTER Write command period	tMRW	min	max(10ns, 10nCK)								ns	
MODE REGISTER Read command period	tMRR	min	8								nCK	
Mode Register Write Set Command Delay	tMRD	min	max(14ns, 10nCK)								ns	

Table - VRCG Enable/Disable Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
VREF high current mode enable time	tVRCG_Enable	max	200								ns	
VREF high current mode disable time	tVRCG_Disable	max	100								ns	

Table - Command Bus Training Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Clock and Command Valid after CKE Low	tCKELCK	min	max(7.5ns, 5nCK)								tCK	
Data Setup for Vref Training Mode	tDStrain	min	2								ns	
Data Hold for Vref Training Mode	tDHtrain	min	2								ns	
Asynchronous Data Read	tADR	max	20								ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	min	RU(tADR/tCK)								tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	min	10								ns	1
First CA Bus Training Command Following CKE Low	tCAENT	min	250								ns	
Vref Step Time – multiple steps	tVref_long	max	250								ns	

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Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Vref Step Time – one step	tVref_short	max	80								ns	
Valid Clock Requirement before CS High	tCKPRECS	min	2*tCK + tXP								-	
Valid Clock Requirement after CS High	tCKPSTCS	min	max (7.5ns, 5nCK)								-	
Minimum delay from CS to DQS toggle in command bus training	tCS_Vref	min	2								tCK	
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	min	10								ns	
Clock and Command valid before CKE HIGH	tCKCKEH	min	2								tCK	
CA Bus Training CKE High to DQ Tri-state	tMRZ	min	1.5								ns	
ODT turn-on latency from CKE	tCKELODTon	min	20								ns	
ODT turn-off latency from CKE	tCKELODToff	min	20								ns	

Notes:

1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

Table - Write Leveling Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	min	20								tCK	
Write preamble for Write Leveling	tWLWPRE	min	20								tCK	
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	min	40								tCK	
Write leveling output delay	tWLO	min	0								ns	
		max	20									
Valid Clock Requirement before DQS Toggle	tCKPRDQS	min	max(7.5ns, 4nCK)									
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	min	max(7.5ns, 4nCK)									
Write leveling hold time	tWLH	min			150	100		75		50	ps	1,2
Write leveling setup time	tWLS	min			150	100		75		50	ps	1,2
Write leveling invalid window	tWLIVW_Total	min			240	160		120		90	ps	1,2

Notes:

1. In addition to the traditional setup and hold time specifications above, there is value in a invalid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW_Total is defined in a similar manner to tdIVW_Total, except that here it is a DQS invalid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling invalid window.

   The DQS input mask for timing with respect to CK is shown in the following figure. The "total" mask (TdiVW_total) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

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Figure - DQS_t/DQS_c and CK_t/CK_c at DRAM Latch

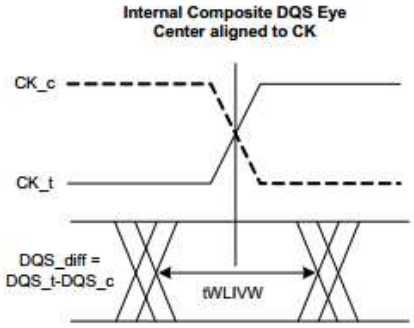

Table - Read Preamble Training Timings

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Delay from MRW command to DQS Driven out	tSDO	max	min(tMRD, 15ns)								tCK	1

Table - MPC [Write FIFO] AC Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Additional time after tXP has expired until MPC [Write FIFO] command may be issued	tMPCWR	min	tRCD + 3nCK									

Table - DQS Interval Oscillator AC Timing

Parameter	Symbol	min max	Value	Unit	Note
Delay time from OSC stop to Mode Register Readout	tOSCO	min	max(40ns,8nCK)	ns	

Table - Frequency Set Point Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Frequency Set Point Switching Time	tFC_Short	min	200								ns	1
	tFC_Middle	min	200								ns	1
	tFC_Long	min	250								ns	1
Valid Clock Requirement after entering FSP change	tCKFSPE	min	max(7.5ns, 4nCK)									
Valid Clock Requirement before 1st valid command after FSP change	tCKFSPX	min	max(7.5ns, 4nCK)									

Notes:
1. Frequency Set Point Switching Time depends on value of Vref(ca) setting: MR12 OP[5:0] and Vref(ca) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table "tFC value maping".
   Additionally change of Frequency Set Point may affect Vref(dq) setting. Setting time of Vref(dq) level is same as Vref(ca) level.

AC TIMING PARAMETERS (8/9)

Table - CA ODT setting timing

Parameter	Symbol	Min/Max	LPDDR4-1600/1866/2133/2400/3200/4266	Units	Note
ODT CA Value Update Time	tODTUP	Min	RU(tbd ns/tCK(avg))		

Table - Power Down Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	min	Max(7.5ns,4nCK)								-	
Delay from valid command to CKE input LOW	tCMDCKE	min	Max(1.75ns,3nCK)								ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	min	Max(5ns,5nCK)								ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	min	1.75								ns	
Valid CS Requirement after CKE Input low	tCKELCS	min	Max(5ns, 5nCK)								ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	min	Max(1.75ns, 3nCK)								ns	1
Exit power- down to next valid command delay	tXP	min	Max(7.5ns, 5nCK)								ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	min	1.75								ns	
Valid CS Requirement after CKE Input High	tCKEHCS	min	Max(7.5ns, 5nCK)								ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	min	Max(14ns, 10nCK)								ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	min	Max(1.75ns, 3nCK)								ns	1

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).
   For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 3.75ns has transpired.
   The case which 3nCK is applied to is shown below.

Figure - tCMDCKE Timing

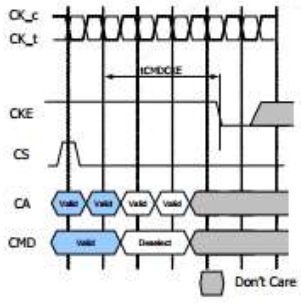

Table - PPR Timing Parameters

Parameter	Symbol	LPDDR4		Unit	Notes
		Min	Max		
PPR Programming Time	tPGM	1000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting Time	tPGMPST	50	-	us	

AC TIMING PARAMETERS (9/9)

Table - Temperature Derating for AC timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
DQS Output access time from CK_t/CK_c (derated)	tDQSCKd	max	3600								ps	1
RAS-to-CAS delay (derated)	tRCDd	min	tRCD + 1.875								ns	1
Activate-to-Activate command period (derated)	tRCd	min	tRC + 3.75								ns	1
Row active time (derated)	tRASd	min	tRAS + 1.875								ns	1
Row precharge time (derated)	tRPd	min	tRP + 1.875								ns	1
Active bank A to Active bank B (derated)	tRRDd	min	tRRD + 1.875								ns	1

Notes:
1. Timing derating applies for operation at 85°C to 105°C

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