Western Digital.

DATA SHEET

iNAND® MC MU321 64GB+48Gb, 128GB+32Gb, 128GB+48Gb MCP

Universal Flash Storage (UFS) Version 2.1 Standard with Gear3/2 Lane Interface and LPDDR4x

Revision History

Revision	Date	Description	Reference
0.2	November 2, 2018	Preliminary version.	

Western Digital Technologies, Inc. or its affiliates' (collectively "Western Digital") general policy does not recommend the use of its products in life support applications where in a failure or malfunction of the product may directly threaten life or injury. Per Western Digital Terms and Conditions of Sale, the user of Western Digital products in life support applications assumes all risk of such use and indemnifies Western Digital against all damages.

This document is for information use only and is subject to change without prior notice. Western Digital assumes no responsibility for any errors that may appear in this document, nor for incidental or consequential damages resulting from the furnishing, performance or use of this material.

Absent a written agreement signed by Western Digital or its authorized representative to the contrary, Western Digital explicitly disclaims any express and implied warranties and indemnities of any kind that may, or could, be associated with this document and related material, and any user of this document or related material agrees to such disclaimer as a precondition to receipt and usage hereof.

Each user of this document or any product referred to herein expressly waives all guaranties and warranties of any kind associated with this document any related materials or such product, whether expressed or implied, including without limitation, any implied warranty of merchantability or fitness for a particular purpose or non-infringement. Each user of this document or any product referred to herein also expressly agrees Western Digital shall not be liable for any incidental, punitive, indirect, special, or consequential damages, including without limitation physical injury or death, property damage, lost data, loss of profits or costs of procurement of substitute goods, technology, or services, arising out of or related to this document, any related materials or any product referred to herein, regardless of whether such damages are based on tort, warranty, contract, or any other legal theory, even if advised of the possibility of such damages.

This document and its contents, including diagrams, schematics, methodology, work product, and intellectual property rights described in, associated with, or implied by this document, are the sole and exclusive property of Western Digital. No intellectual property license, express or implied, is granted by Western Digital associated with the document recipient's receipt, access and/or use of this document or the products referred to herein; Western Digital retains all rights hereto.

This document and Western Digital communications to the user associated therewith, shall be treated as Western Digital Corporation's proprietary and confidential information, protected by the recipient as such, and used by the recipient only for the purpose authorized in writing by Western Digital Corporation. This document shall be covered as Western Digital Corporation's confidential information under all applicable nondisclosure agreements between the recipient and Western Digital Corporation.

Table of Contents

LIST OF FIGURES

LIST OF TABLES

1.0 INTRODUCTION

The Western Digital® iNAND® MC MU321 is an Embedded Flash Drive (EFD) integrated with low power DRAM. It is a hybrid device that combines an embedded thin flash controller and 3D NAND flash memory, with an industry standard Universal Flash Storage, Version 2.1 (UFS v2.1) Gear3 / 2 Lane Interface that provides superior performance suited for demanding mobile applications.

1.1 General Description

The device combines an embedded thin flash controller with advanced Triple- Level Cell (TLC) NAND flash technology that is enhanced by embedded flash management software running as firmware on the flash controller. The device adheres to the JEDEC industry-standard UFSv2.1 MIPI M-PHY specification as the physical layer for optimized performance and power.

The device is configured with 256Gb X3 3D NAND memory using 96-layer technology and is available in capacities of 64GB and 128GB. The memory architecture brings new levels of density, scalability and performance to the Embedded Flash Drive. The 3D NAND memory also provides enhanced write/ erase endurance, write speeds and energy efficiency relative to conventional 2D NAND. The 3D NAND memory is paired with up to 48Gb of LPDDR4x DRAM.

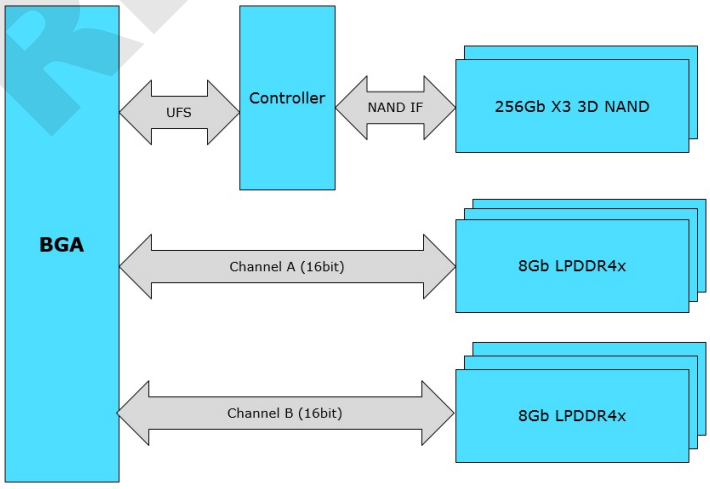
1.2 Plug-and-Play Integration

The optimized architecture eliminates the need for complicated software integration and testing processes, thereby enabling plug-and-play integration with the host system.

The physical specification of the device consists of a JEDEC form factor measuring 11.5 x 13mm (254 balls).

The device features a UFS interface that allows for easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device. Figure 1-1 shows a functional block diagram of the device with UFS Interface.

Figure 1-1. 64GB+48Gb MCP with UFS Bus Interface



Note: The 128GB+32Gb MCP will have 4 flash die stack instead of 2 and 4 DRAM die stack instead of 6; 128+48Gb MCP will have 4 flash die stack instead of 2.

Figure 1-2. 32Gb 2CS

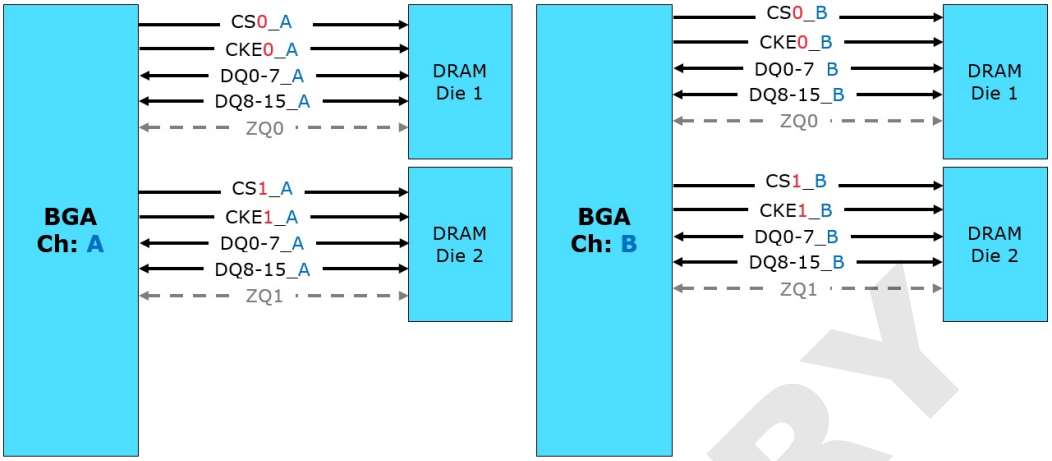
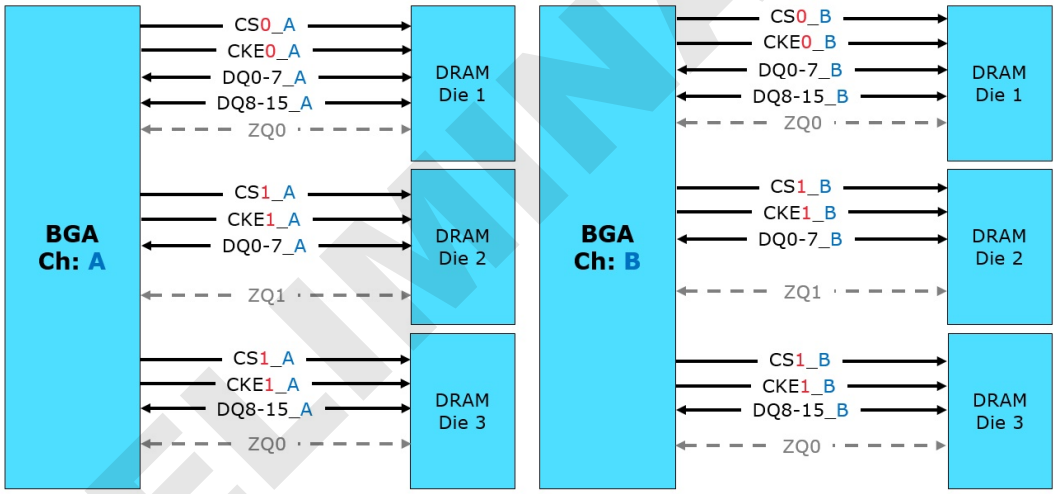


Figure 1-3. 48Gb 2CS



Note: WDC only supports the 2CS configuration; the 3CS configuration is not supported.

1.3 Feature Overview

The device with UFS interface includes the following features:

- Memory controller and NAND flash
- Mechanical design adheres to JEDEC Specification
- Offered in three packages
  - 11.5mm x 13mm x 1.0mm (64GB+48Gb LPDDR4x)
  - 11.5mm x 13mm x 1.0mm (128GB+32Gb LPDDR4x)
  - 11.5mm x 13mm x 1.1mm (128GB+48Gb LPDDR4x)
- Operating temperature range: -25°C to +85°C
- Dual power system
- Core voltage (VCC): 2.7-3.6 V
- I/O voltage (VCCQ2): 1.7-1.95V
- 64/128GB of data storage.
- Adheres to JEDEC UFS Specification, Version 2.1
- Content Preloading before IR-Reflow
- Differential interface based on MIPI M-PHY together with the MIPI UniPro specifications.
- Bus transfer rate of up to 800 MB/second, using high-speed Gear3 / 2-Lane physical signals.
- 8bit-by-10bit line coding, as defined by MIPI M-PHY
- Correction of memory field errors.
- Designed for portable and stationary applications that require high performance and reliable data storage.
- Low-Power Mobile DDR4x:
  - Core Power 1, Core Power 2 and I/O voltage 1.7V - 1.95V, 1.06V - 1.17V, and 0.57V - 0.65V respectively
  - Up to 1866MHz clock with 32-bit data interface

1.4 Defect and Error Management

The device features a sophisticated defect and error management system for exceptional data reliability. The device will automatically rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume additional user data space. In the extremely rare case that a read error does occur, the device has innovative data recovery algorithms.

1.5 Power Supply Requirements

Table 1-1. Power Supply Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Supply Voltage (memory)	VCC	2.7	3.6	V	Limited to 1 hour.
Supply Voltage (Reserved for Future Use; not required for current product)	VCCQ_	1.14	1.26	V	JESD8-12A (can be not-connected)
Supply Voltage (Controller and IO)	VCCQ2	1.70	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	Recommended 5µsec as minimal supply ramp-up slew rate.
Supply power-up for 1.8V	tPRUL		25	ms	

1.6 Low Power Mobile DDR4x Bus Operating Conditions

See *Section 10.0 Appendix A: 8Gb LPDDR4x SDRAM Features on page 41* for DRAM operating condition specifications.

2.0 Product Specifications

2.1 Typical Power Requirements

Table 2-1. Power and Current Consumption – Standby

Parameter	Conditions	64GB	128GB	Units
Standby Current ICC (VCC=off)	Ta=25°C, 3.3V, @Gear3/2-Lane	0	0	µA
Standby Current ICCQ2	Ta=25°C, 1.8V, @Gear3/2-Lane	400	400	µA
Standby Power	Ta=25°C, 1.8V/3.3V, @Gear3/2-Lane	0.75	0.75	mW

Table 2-2. Power Consumption – Peak and Max

Parameter	Conditions	64GB	128GB	Units
Peak Current ICC	Window 2µs, 3.3V, @Gear3/2-Lane	400	580	mA
Max Current ICCQ2	Window 1ms, 1.8V, @Gear3/2-Lane	450	450	mA

Table 2-3. Power Consumption – Maximum RMS

Parameter	Conditions	64GB	128GB	Units
RMS Current ICC	Window 100ms, Ta=25°C, 3.3V, @Gear3/2-Lane	230	280	mA
RMS Current ICCQ2	Window 100ms, Ta=25°C, 1.8V, @Gear3/2-Lane	320	320	mA
Total Power	Ta=25°C, 1.8V/3.3V, @Gear3/2-Lane interface	1.3	1.5	W

Note: Measured at full performance without host overhead.

2.2 Operating Conditions

2.2.1 Operating and Storage Temperature Specifications

Table 2-4. Operating and Storage Temperature

Operating Temperature[1]		Non-Operating Temperature	
Minimum	**Maximum**	**Minimum**	**Maximum**
-25°C	85°C	-40°C	85°C

[1] This operating temperature should be maintained on the package case (T-case) to achieve optimized power and performance.

2.2.2 Moisture Sensitivity

The moisture sensitivity level for the device is MSL = 3.

2.3 Reliability

The device meets or exceeds Endurance and Data Retention requirements as per evaluated representative usage models for designed market and relevant sections of the JESD47I standard.

Table 2-5. Critical Reliability Characteristics

Reliability Characteristics	Description	Value
UBER	The Uncorrectable Bit Error Rate (UBER) will not exceed one (1) sector in the specified number of bits read (in such rare events, data can be lost). ■ **Mostly Read Workload**: Ratio of reads to writes in greater than or equal to 99:1. ■ **Mixed Workload**: Ratio to writes is less than 99:1.	■ **Mostly Read Workload**: 1 sector in 10^{12} bits read. ■ **Mixed Workload**: 1 sector in 10^{15} bits read.
Write Endurance Specification (TBW)	Write Endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and is dependent upon the workload and temperature mission profile: **Representative Workload Description**: ■ 62% Sequential write, 38% Random Write Distribution of I/O Transaction Sizes: – <16KB: 82% – 16KB-128KB: 17% – >128KB: 1% ■ Cache On, Packed Off ■ Host Data is 4K aligned **Maximum Temperature Mission Profile**: ■ 30% of product lifetime: @85° C T-case ■ 70% of product lifetime: @55° C T-case	Total Terabytes Written [TBW] per representative Android workload: ■ 64GB: 80[TB] ■ 128GB: 160[TB]
Data Retention	Fresh or Early Life Device: A device having a total number of write cycles to the flash that is less than 10% of the maximum endurance specification.	10 years of Data Retention @ 55°C.
	Cycled Device: A device having a total number of write cycles between 10% of the maximum write endurance and equal to or greater than the maximum write endurance specification.	1 year of Data Retention @ 55°C. *Note*: In the case where the number of writes exceed the endurance specification, Read and Write performance can be intermediately reduced.

2.4 Typical System Performance

Table 2-6. Typical Sequential Performance

	Gear3 2-Lane	
Capacity	**Write (MBs)**	**Read (MBs)**
64GB	400	700
128GB	550	800

Table 2-7. Typical Random Performance

	Gear3 2-Lane	
Capacity	**Write IOPS**	**Read IOPS**
64GB	50,000	30,000
128GB	55,000	50,000

NOTE:

- Sequential Read/Write performance is measured under Gear3/2-Lane mode with a bus, chunk size of 512KB, and data transfer of 1GB.
- Random Read/Write performance is measured under Gear3/2-Lane mode with a bus, with a chunk size of 4KB and address range of 1GB.
- All performance is measured using a proprietary test environment, without file system overhead and host turn-around time (HTAT).
- Sequential Write performance is measured for 100MB host payloads.
- Read performance is measured in Queue-Depth of 32.

3.0 PHYSICAL SPECIFICATIONS

Figure 3-1. 254-Ball Package – Top, Side and Bottom View

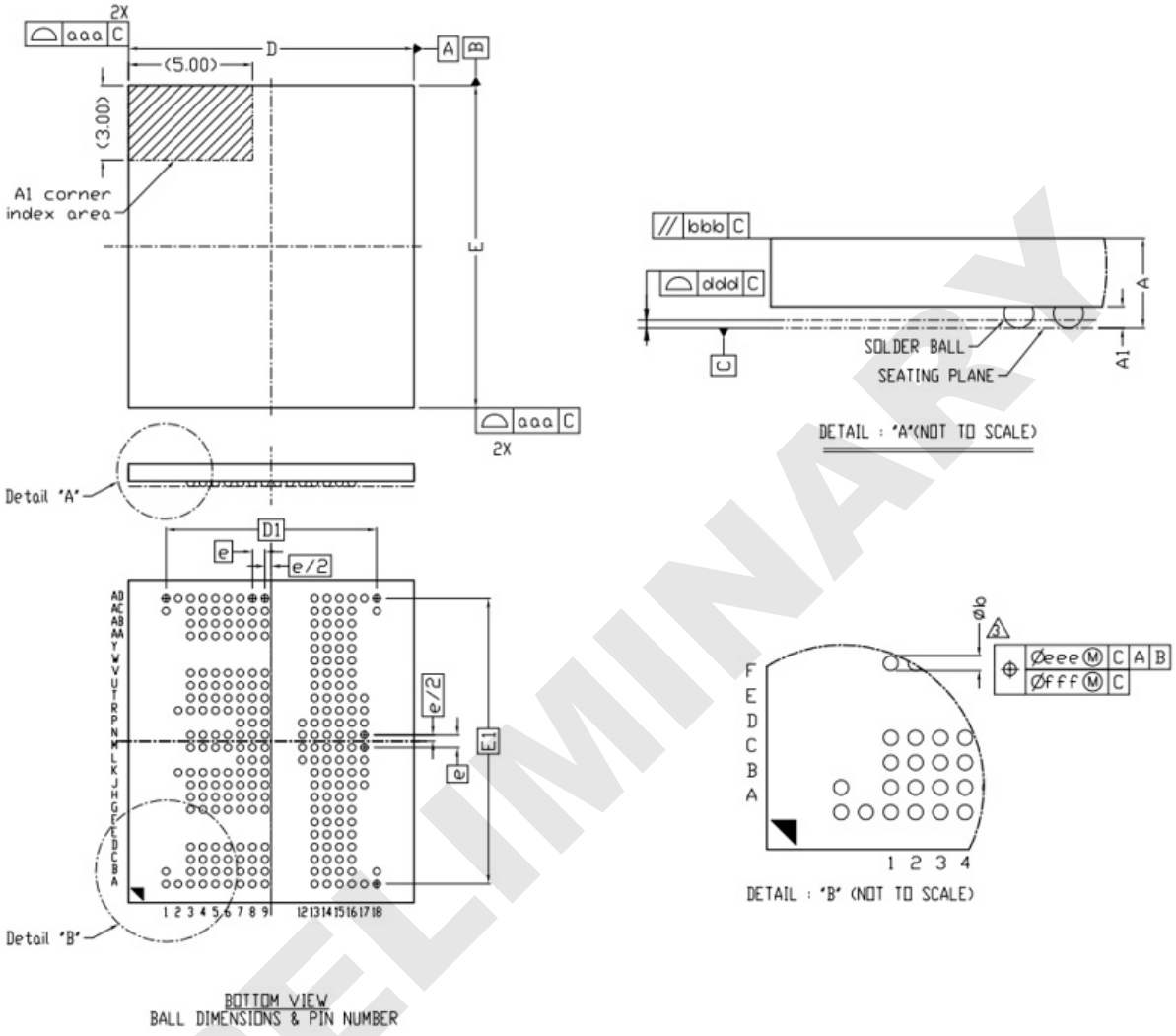


Figure 3-2. BGA Pad View

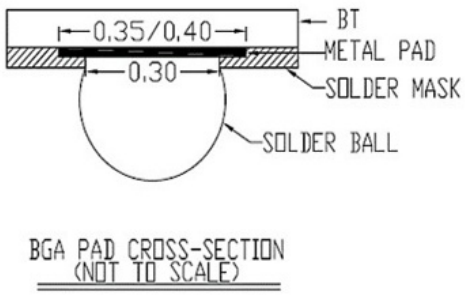


Table 3-1. Package Specifications 254-BGA 1.0mm (64+48, 128+32 Configuration)

Dimensions (Millimeters)			
Symbol	**Minimum**	**Nominal**	**Maximum**
A	0.8	—	1.0
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13.0	13.1
D1	—	8.5	—
E1	—	11.5	—
e	—	0.5	—
b	0.25	0.3	0.35
aaa		0.1	
bbb		0.1	
ddd		0.08	
eee		0.15	
fff		0.05	

Table 3-2. Package Specifications 254-BGA 1.1mm (128+48 Configuration)

Dimensions (Millimeters)			
Symbol	**Minimum**	**Nominal**	**Maximum**
A	0.9	—	1.1
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13.0	13.1
D1	—	8.5	—
E1	—	11.5	—
e	—	0.5	—
b	0.25	0.3	0.35
aaa		0.1	
bbb		0.1	
ddd		0.08	
eee		0.15	
fff		0.05	

4.0 Interface Description

4.1 uMCP Ball Array

Figure 4-1. LPDDR4x, 11.5x13mm, 0.5mm pitch, 254-Ball, 2Channel x32 MCP (Top View)

4.2 Pins and Signal Description

Table 4-1 lists the functional ball assignments, signals and descriptions.

Table 4-1. iNAND Functional Pin Assignments

Ball Name	Type	Description
VCC	Supply	Supply voltage for the memory devices.
VCCQ_	Supply	Supply voltage used typically for the memory controller and optionally for the PHY interface and any other internal very low voltage block.
VCCQ2	Supply	Supply voltage used typically for the PHY interface and the memory controller or memory interface and any other internal low voltage block.
VDDiQ_	Input	Input terminal to provided bypass capacitor for VCCQ internal regulator typically related to the memory controller or the PHY interface.
VDDiQ2	Input	Input terminal to provide bypass capacitor for VCCQ2 internal regulator, typically related to memory interface.
VDDi	Input	Input terminal to provide bypass capacitor for VCC internal regulator.
VSS	Supply	Supply voltage ground.
RST_n	Input	Input hardware reset signal. This is an active low signal.
REF_CLK	Input	Input reference clock. When not active, this signal should be pull down or driven low by the host SoC.
DIN0_t / DIN1_t	Input	Downstream data lane0 and data lane1. These are differential input signals into UFS device from the host.
DIN0_c / DIN1_c	CLK	
DOUT0_t / DOUT1_t		Upstream data lane0 and data lane1. These are differential output signals from the UFS device to the host.
DOUT0_c / DOUT1_c	RCLK	
C+	Input	Optional charge pump capacitor, positive terminal.
C-	Input	Optional charge pump capacitor, negative terminal.
NC	—	No Connect. NC pins can be connected to ground or left floating.
RFU	—	Reserved for Future Use. RFU pins should be left floating.
VSFn	—	Vendor Specific Function. VSFn (n=1-9) pins should be left floating. Each vendor can use these pins during manufacturing.

Note: All other pins are Not Connected (NC) and can be connected to GND or be floating.

Table 4-2. LPDDR4x Signal Descriptions

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B. CL_c_B	Input	**Clock**: CK_t and CK_c are differential clock inputs. All address, command, and control input signal are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC Timings for CA parameters are referenced to CK. Each channel, A and B, has its own clock pair.
CKE_A CKE_B	Input	**Clock Enable**: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers and output drivers. Power-saving modes are entered and exited via CKE transitions.
CS_A CS_B	Input	**Chip Select**: CS is part of the command code. Each channel, A and B, has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	**Command/Address Inputs**: These signals provide the Command and Address inputs according to the Command Truth Table. Each channel, A and B, has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control**: The ODT_CA pin is ignored by LPDDR4x devices. The ODT-CS/CA/CA function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 and VSS.
DQ[15:0]_A DQ[15:0]_B	I/O	**Data Input/Output**: Bi directional data bus.
DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B	I/O	**Read Strobe**: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center-aligned with Data. Each byte of data has a Data Strobe signal pair. Each channel, A and B, has its own DQS strobes.
DMI[1:0]_A DMI[1:0]_B	I/O	**Data Mask Inversion**: DMI is a bi-directional signal that is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a Mode Register setting. Each byte of data has a DMI signal. Each channel, A and B, has its own DMI signals.
ZQ	Reference	**Calibration Reference**: ZQ is used to calibrate the output driver strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ using a 240Ohm ±1% resistor.
VDD1, VDD2, VDDQ	Supply	**Power Supplies**: Isolated on the die for improved noise immunity.
VSS	GND	**Ground (GND) Reference**: Power supply GND reference.
RESET_n	Input	**RESET**: When asserted LOW, the RESET pin will reset both channels of the die.

5.0 UFS Descriptor, Attributes, Flags, and User Density

5.1 Device Descriptor

Table 5-1. Device Descriptors

Name	Length	Value	Description
bLength	0x01	0x40	Descriptor Size
bDescriptorIDN	0x01	0x00	Device Descriptor Type Identifier
bDevice	0x01	0x00	Device Type
bDeviceClass	0x01	0x00	UFS Device Class (00h: Mass Storage)
bDeviceSubClass	0x01	0x00	UFS Mass Storage Subclass (00h: Embedded Bootable)
bProtocol	0x01	0x00	Protocol Supported by UFS Device (00h: SCSI)
bNumberLU	0x01	0x01	Number of Logical Units
bNumberWLU	0x01	0x04	Number of Well-Known Logical Units
bBootEnable	0x01	0x00	Bootable
bDescrAccessEn	0x01	0x00	Descriptor Access Enable
bInitPowerMode	0x01	0x01	Initial Power Mode
bHighPriorityLUN	0x01	0x7f	High Priority LUN
bSecureRemovalType	0x01	0x03	Secure Removal Type
bSecurityLU	0x01	0x01	Support Security LU
bBackgroundOpsTermLat	0x01	0x0F	Background Operations Termination Latency
bInitActiveICCLevel	0x01	0x0F	Initial Active ICC Level
wSpecVersion	0x02	0x0210	Specification Version
wManufactureDate	0x02	0xMMYY	Manufacturing Date
iManufacturerName	0x01	0x00	Index to the String containing the Manufacturer Name Manufacture Name String Length: 0x12 Manufacture Name String Type: 0x5 Manufacture Name String (UNICODE): "WDC"
iProductName	0x01	0x01	Index to the String containing the Product Name Product Name String Length: 0x22 Product Name String Type: 0x5 Product Name String (UNICODE): ■ 64GB+48Gb – "SDDDC4DR-64G" ■ 128GB+32Gb- "SDDDC4CR-128G" ■ 128GB+48Gb- "SDDDC4DR-128G"
iSerialNumber	0x01	0x03	Index to the String containing the Serial Number Serial Number String Length: 0xC Serial Number String Type: 0x5 Serial Number String (UNICODE): ■ BYTE 0: CRC ■ BYTE 1-3: MANFICTURING DATE/MONTH/YEAR ■ BYTE 4-7: RANDOM NUMBER ■ BYTE 8-11: RFU
iOemID	0x01	0x04	Index to the String containing the OEM ID OEM ID String Length: 0x32 OEM ID String Type: 0x5 OEM ID String (UNICODE): " "
wManufacturerID	0x02	0x0145	Manufacturer ID Code (assigned by JEDEC).
bUD0BaseOffset	0x01	0x10	Unit Descriptor 0 Base Offset

Name	Length	Value	Description
bUDConfigPLength	0x01	0x10	Unit Descriptor Configuration Length
bDeviceRTTCap	0x01	0x02	Maximum Number of Outstanding RTTs Supported
wPeriodicRTCUpdate	0x02	0x0000	Frequency and Method of Real-Time Clock Update
bUFSFeaturesSupport	0x01	0x01	UFS Features Support. This field indicates which features are supported by the device. (FFU and PSA are supported)
bFFUTimeout	0x01	0x07	Field Firmware Update Timeout
bQueueDepth	0x01	0x20	Queue-Depth
wDeviceVersion	0x02	0x0000	Firmware Release ID
bNumSecureWPArea	0x01	0x20	Number of Secure Write Protect Areas
dPSAMaxDataSize	0x04	0x00000000	PSA Maximum Data Size; different for each device capacity.
bPSAStateTimeout	0x01	0x11	PSA State Timeout
iProductRevisionLevel	0x01	0x02	Index to the String containing the Product Revision Level Product Revision String Length: 0x4 Product Revision String Type: 0x5 Product Revision String (UNICODE): Firmware Version Release ■ CH[0-1]: Major FW version (RC#) ■ CH[2-3]: Minor FW version (Build#)

5.2 Unit 0...31 Descriptor

Table 5-2. Unit 0...31 Descriptor

Name	Length	Value	Description
bLength	0x01	0x23	Size of this descriptor.
bType	0x01	0x02	Unit Descriptor Type Identifier
bUnitIndex	0x01	0x0 – 0x1f	Unit Index
bLUEnable	0x01	0x01	LU Enable
bBootLunID	0x01	0x00	Boot LUN ID
bLUWriteProtect	0x01	0x00	LU Write Protect
bLUQueueDepth	0x01	0x00	Queue Depth
bPSASensitive	0x01	0x00	Sensitivity to Soldering
bMemoryType	0x01	0x00	Memory Type
bDataReliability	0x01	0x00	Data Reliability
bLogicalBlockSize	0x01	0x0C	Logical Block Size
qLogicalBlockCount	0x08	0x20000	Logical Block Count
dEraseBlockSize	0x04	0x01	Erase Block Size
dProvisioningType	0x01	0x03	Provisioning Type
qPhyMemResourceCount	0x08	0x200000	Resource Count
wContextCapabilities	0x02	0x00	Context Capabilities
bLargeUnit	0x01	0x00	Large Unit

5.3 RPMB Descriptor

Table 5-3. RPMD Descriptor

Name	Length	Value	Description
bLength	0x01	0x23	Size of this descriptor.
bDescriptorIDN	0x01	0x02	Unit Descriptor Type Identifier
bUnitIndex	0x01	0xc4	Unit Index
bLUEnable	0x01	0x01	LU enable
bBootLunID	0x01	0x00	Boot LUN ID
bLUWriteProtect	0x01	0x00	Write Protect
bLUQueueDepth	0x01	0x00	Queue Depth
bPSASensitive	0x01	0x00	Sensitivity to Soldering
bMemoryType	0x01	0x0f	Memory Type
bRPMBRegionEnable	0x01	0x00	RPMB Region Enable
bLogicalBlockSize	0x01	0x08	The Size of Addressable Logical Blocks
qLogicalBlockCount	0x08	0x0000000000010000	Total Number of Addressable Logical Blocks in the Logical Unit
bRPMBRegion0Size	0x01	0x80	RPMB Region 0 Size is defined in 128KB unit
bRPMBRegion1Size	0x01	0x00	RPMB Region 1 Size is defined in 128KB unit
bRPMBRegion2Size	0x01	0x00	RPMB Region 2 Size is defined in 128KB unit
bRPMBRegion3Size	0x01	0x00	RPMB Region 3 Size is defined in 128KB unit
bProvisioningType	0x01	0x00	Provisioning Type
qPhyMemResourceCount	0x08	0x0000000000010000	Total Physical Memory Resources available in the Logical Unit.

5.4 Geometry Descriptor

Table 5-4. Geometry Descriptor

Name	Length	Value	Description
bLength	0x01	0x48	Descriptor Size
bDescriptorIDN	0x01	0x07	Geometry Descriptor Type Identifier
bMediaTechnology	0x01	0x00	Reserved
Reserved1	0x01	0x00	Reserved
qTotalRawDeviceCapacity	0x08	0x00	Total Raw Device Capacity
bMaxNumberLU	0x01	0x01	Maximum Number of Logical Units supported.
dSegmentSize	0x04	0x00002000	Segment Size Value (Defined in 512-Byte Units)
bAllocationUnitSize	0x01	0x01	Allocation Unit Size Value
bMinAddrBlockSize	0x01	0x08	Minimum Addressable Block Size (Defined in 512-Byte Units)
bOptimalReadBlockSize	0x01	0x08	Optimal Read Block Size (Defined in 512-Byte Units)
bOptimalWriteBlockSize	0x01	0x08	Optimal Write Block Size (Defined in 512-Byte Units)

Name	Length	Value	Description
bMaxInBufferSize	0x01	0x08	Maximum Data-in Buffer Size (Defined in 512-Byte Units)
bMaxOutBufferSize	0x01	0x08	Max. Data-out Buffer Size (Defined in 512-Byte Units)
bRPMB_ReadWriteSize	0x01	0x40	Maximum Number of RPMB Frames (256 Bytes per Frame)
bDynamicCapacityResourcePolicy	0x01	0x01	Dynamic Capacity Resource Policy
bDataOrdering	0x01	0x00	Support for Out-of-Order Data Transfer
bMaxContexIDNumber	0x01	0x05	Maximum Number of Contexts Available
bSysDataTagUnitSize	0x01	0x00	System Data Tag Unit Size
bSysDataTagResSize	0x01	0x00	Maximum Storage Area Sized allocated for system data by tagging mechanism (in Bytes).
bSupportedSecRTypes	0x01	0x09	Supported Secure Removal Types
wSupportedMemoryTypes	0x02	0x8009	Bitmap Representing Supported Memory Types
dSystemCodeMaxNAllocU	0x04	0x00	Maximum Number of Allocation Unites for System Code Memory Type
wSystemCodeCapAdjFac	0x02	0x00	Capacity Adjustment Factor for the System Code Memory Type
dNonPersistMaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Non-Persistent Memory
wNonPersistCapAdjFac	0x02	0x00	Capacity Adjustment Factor for the Non-Persistent Memory Type
dEnhanced1MaxNAllocU	0x04	0x00000030	Maximum Number of Allocation Units for Enhanced Memory Type 1
wEnhanced1CapAdjFac	0x02	0x0300	Capacity Adjustment Factor for the Enhanced Memory Type 1
dEnhanced2MaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Enhanced Memory Type 2
wEnhanced2CapAdjFac	0x02	0x00	Capacity Adjustment Factor for the Enhanced Memory Type 2
dEnhanced3MaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Enhanced Memory Type 3
wEnhanced3CapAdjFac	0x02	0x00	Capacity Adjustment Factor for the Enhanced Memory Type 3
dEnhanced4MaxNAllocU	0x04	0x00	Maximum Number of Allocation Units for Enhanced Memory Type 4
wEnhanced4CapAdjFac	0x02	0x00	Capacity Adjustment Factor for the Enhanced Memory Type 3
dOptimalLogicalBlockSize	0x04	0x00000008	Optimal Logical Block Size

5.5 Interconnect Descriptor

Table 5-5. Interconnect Descriptor

Name	Length	Value	Description
bLength	0x01	0x06	Descriptor Size
bDescriptorIDN	0x01	0x04	Interconnect Descriptor Type Identifier
bcdUniproVersion	0x02	0x0160	MIPI UniProSM Version Number (in BCD Format)
bcdMphyVersion	0x02	0x0300	MIPI M-PHY® Version Number (in BCD Format)

5.6 Power Descriptor

Table 5-6. Power Descriptor

Name	Length	Value	Description
bLength	0x01	0x62	Descriptor Size
bDescriptorIDN	0x01	0x08	Power Parameters Descriptor Type Identifier
wActiveICCLevelsVCC[0]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 0
wActiveICCLevelsVCC[1]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 1
wActiveICCLevelsVCC[2]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 2
wActiveICCLevelsVCC[3]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 3
wActiveICCLevelsVCC[4]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 4
wActiveICCLevelsVCC[5]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 5
wActiveICCLevelsVCC[6]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 6
wActiveICCLevelsVCC[7]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 7
wActiveICCLevelsVCC[8]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 8
wActiveICCLevelsVCC[9]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 9
wActiveICCLevelsVCC[10]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 10
wActiveICCLevelsVCC[11]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 11
wActiveICCLevelsVCC[12]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 12
wActiveICCLevelsVCC[13]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 13
wActiveICCLevelsVCC[14]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 14
wActiveICCLevelsVCC[15]	0x02	0x00	Maximum VCC current value for bActiveICCLevel = 15
wActiveICCLevelsVCCQ[0]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 0
wActiveICCLevelsVCCQ[1]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 1
wActiveICCLevelsVCCQ[2]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 2
wActiveICCLevelsVCCQ[3]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 3
wActiveICCLevelsVCCQ[4]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 4
wActiveICCLevelsVCCQ[5]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 5
wActiveICCLevelsVCCQ[6]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 6
wActiveICCLevelsVCCQ[7]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 7

Name	Length	Value	Description
wActiveICCLevelsVCCQ[8]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 8
wActiveICCLevelsVCCQ[9]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 9
wActiveICCLevelsVCCQ[10]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 10
wActiveICCLevelsVCCQ[11]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 11
wActiveICCLevelsVCCQ[12]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 12
wActiveICCLevelsVCCQ[13]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 13
wActiveICCLevelsVCCQ[14]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 14
wActiveICCLevelsVCCQ[15]	0x02	0x00	Maximum VCCQ current value for bActiveICCLevel = 15
wActiveICCLevelsVCCQ2[0]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 0
wActiveICCLevelsVCCQ2[1]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 1
wActiveICCLevelsVCCQ2[2]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 2
wActiveICCLevelsVCCQ2[3]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 3
wActiveICCLevelsVCCQ2[4]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 4
wActiveICCLevelsVCCQ2[5]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 5
wActiveICCLevelsVCCQ2[6]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 6
wActiveICCLevelsVCCQ2[7]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 7
wActiveICCLevelsVCCQ2[8]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 8
wActiveICCLevelsVCCQ2[9]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 9
wActiveICCLevelsVCCQ2[10]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 10
wActiveICCLevelsVCCQ2[11]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 11
wActiveICCLevelsVCCQ2[12]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 12
wActiveICCLevelsVCCQ2[13]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 13
wActiveICCLevelsVCCQ2[14]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 14
wActiveICCLevelsVCCQ2[15]	0x02	0x00	Maximum VCCQ2 current value for bActiveICCLevel = 15

5.7 Health Descriptor

Table 5-7. Health Descriptor

Name	Length	Value	Description
bLength	0x01	0x25	Descriptor Size
bDescriptorIDN	0x01	0x09	Device Health Descriptor Type Identifier
bPreEOLInfo	0x01	0x01	Pre-End-of-Life Information
bDeviceLifeTimeEstA	0x01	0x00	Device Lifetime (based on Number of Program/Erase Cycles performed, Method A)
bDeviceLifeTimeEstB	0x01	0x00	Device Lifetime (based on Number of Program/Erase Cycles performed, Method B)
VendorPropInfo	0x20	0x00	Reserved for Vendor Proprietary Health Report (32 Bytes)

5.8 Flags

Table 5-8. Flags

Name	Length (Bit)	Value	Description
fDeviceInitfDeviceInit	0x01	False	Device Initialization
fPermanentWPEn	0x01	False	Permanent Write Protection Enable
fPowerOnWPEn	0x01	False	Power-On Write Protection Enable
fBackgroundOpsEn	0x01	True	Background Operations Enable
fDeviceLifeSpanModeEn	0x01	False	Device Life Span Mode
fPurgeEnable	0x01	False	Purge Enable
fPhyResourceRemoval	0x01	False	Physical Resource Removal
fBusyRTC	0x01	False	Busy Real Time Clock
PermanentlyDisableFwUpdate	0x01	False	Permanently Disable Firmware Update

5.9 Attributes

Table 5-9. Attributes

Name	Length	Default Value	Description
bBootLunEn	0x01	0x1	Boot LUN Enable
bCurrentPowerMode	0x01	0x11	Current Power Mode
bActiveICCLevel	0x01	0xf	Active ICC Level
bOutOfOrderDataEn	0x01	0x0	Out-of-Order Data Transfer Enable
bBackgroundOpStatus	0x01	0x0	Background Operations Status
bPurgeStatus	0x01	0x0	Purge Operation Status
bMaxDataInSize	0x01	0x8	Maximum Data-In Size
bMaxDataOutSize	0x01	0x8	Maximum Data-Out Size
dDynCapNeeded	0x04	0x0	Dynamic Capacity Needed
bRefClkFreq	0x01	0x1	Reference Clock Frequency. Default value is 26MHz. Host may modify the value during boot phase.
bConfigDescrLock	0x01	0x0	Configuration Descriptor Lock
bMaxNumOfRTT	0x01	0x2	Maximum Current Number of Outstanding RTTs in device.
wExceptionEventControl	0x02	0x0	Exception Event Control
wExceptionEventStatus	0x02	0x0	Each bit represents an exception event.
dSecondsPassed	0x01	0x0	Seconds passed from TIME BASELINE
wContextConf	0x02	0x0	Context Configuration
bDeviceFFUStatus	0x01	0x0	Device FFU Status
bPSAState	0x01	0x0	Device PSA State
dPSADataSize	0x04	0x0	The amount of data that the host plans to load to all logical units.

5.10 Control Mode SCSI

Table 5-10. Control Mode SCSI

Name	Length	Value	Description
PAGE_CODE	0x01	0x8a	Boot LUN Enable
PAGE_LENGTH	0x01	0x0a	Current Power Mode
BYTE_2	0x01	0x00	Active ICC Level
BYTE_3	0x01	0x10	Out-of-Order Data Transfer Enable
BYTE_4	0x01	0x00	Background Operations Status
BYTE_5	0x01	0x00	Purge Operation Status
Obsolete	0x02	0x00	Maximum Data-In Size
BUSY_TIMEOUT_PERIOD	0x02	0x00	Maximum Data-Out Size
EXTENDED_SELF_TEST_COMPLETION_TIME	0x02	0x00	Dynamic Capacity Needed

5.11 VPD Page 0x83 – Device Identification

Table 5-11. VPD Page 0x83 - Device Identification

Name	Length	Value	Description
PAGE_PERIPHERAL	0x01	0x0	Peripheral
PAGE_CODE	0x01	0x83	Page Code
PAGE_LENGTH	0x2	0xc	Length
CODE_SET	0x01	0x2	Code Set
PROTOCOL_ID	0x01	0x0	Protocol ID
DESIGNATOR_TYPE	0x01	0x0	Designator Type
ASSOCIATION	0x01	0x0	Association
PIV	0x01	0x0	PIV
DESIGNATOR_LENGTH	0x01	0x3	String Length
DESIGNATOR_STR0	0x01	0x57	'W'
DESIGNATOR_STR1	0x01	0x44	'D'
DESIGNATOR_STR2	0x01	0x43	'C'

5.12 VPD Page 0xB0 – Block Limit

Table 5-12. VPD Page 0xB0 - Block Limit

Name	Length	Value	Description
PAGE_PERIPHERAL	0x01	0x0	Peripheral
PAGE_CODE	0x01	0xb0	Page Code 0xB0
PAGE_LENGTH	0x02	0x3c	Length of the Page

Name	Length	Value	Description
RESERVED	0x01	0x0	Reserved
MAX_CMP_AND_WR_LEN	0x01	0x0	Maximum value that the device server accepts in the NUMBER OF LOGICAL BLOCKS field in the COMPARE AND WRITE.
OPT_TRANSFER_LEN_GRANULARITY	0x02	0x2	Optimal Transfer Length Granularity in Blocks
MAX_TRANSFER_LEN	0x04	0x0	Maximum Transfer Length in Blocks
OPT_TRANSFER_LEN	0x04	0x0	Optimal Transfer Length in Blocks
MAX_PREFETCH_RD_WR_TRANSFER_LEN	0x04	0x0	Maximum Transfer Length in Blocks
MAX_UNMAP_LBA_CNT	0x04	0xffff	Maximum Number of LBAs that may be unmapped by an UNMAP command.
MAX_UNMAP_BLOCK_DESC_CNT	0x04	0xff	Maximum Number of UNMAP Block Descriptors
OPT_UNMAP_GRANULARITY	0x04	0x1	Optimal Granularity in Logical Blocks for UNMAP requests.
UNMAP_GRANULARITY_ALIGNMENT	0x04	0x0	LBA of the First Logical Block

5.13 User Density

Table 5-13 shows the capacity available for user data for the different device sizes.

Table 5-13. Capacity for User Data

Capacity	Bytes
64GB	64,013,467,648
128GB	128,026,935,296

6.0 HW Application Guidelines

6.1 Design Guidelines

The following guidelines are suggested for system designers, system integrators, hardware engineers and software developers that are planning to integrate iNAND devices into an overall system.

6.2 PCB Stack-up

Table 6-1 is an example of a minimal PCB stack-up.

Table 6-1. PCB Stack-up Example

Layer	Type	Description
1	Signal	Top
2	Plane	Ground
3	Plane	Power
4	Signal	Routing
5	Plane	Ground
6	Signal	Bottom

- Additional layers may be needed on a per-platform basis.
- Signal layers should achieve Tx/Rx differential pairs with 100Ω differential impedance through the range of operation frequencies.
- The impedance of single-ended traces (such as the Ref_CLK) should be matched to 50Ω.

6.3 Return Current and References Planes

- The signal must be provided with a good path for return currents.
- Avoid gaps in the signal return path.
- To reduce inductance, make the return paths as short as possible for the return currents (loops) as longer loops will increase inductance.
- Full GND plane reference is recommended.
- Provide GND vias for the return current paths at the point of the layer change.
- Layer transition requires stitching vias.
- Keep clearance from plane voids.
- No plane splits.

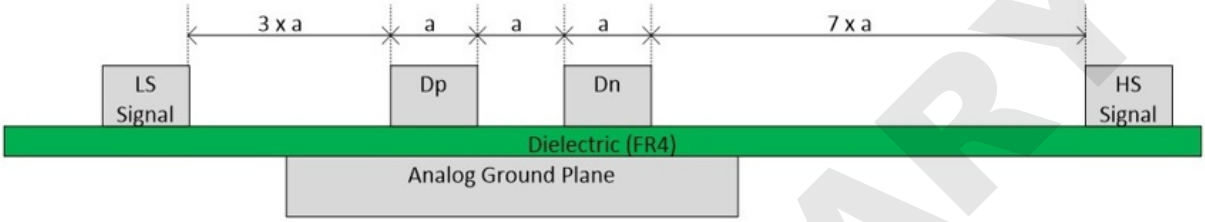
6.4 Crosstalks Minimization

Routing traces on adjacent signal layers should not cross each other unless they are almost perpendicular. Parallel traces on adjacent signal layers will induce crosstalk on each other.

To minimize crosstalk, follow these routing guidelines for Tx/Rx differential pairs:

- Minimum recommended spacing from low speed signal is 3x.
- Minimum recommended spacing from high speed signal is 7x.

Figure 6-1. Crosstalks Minimization Example



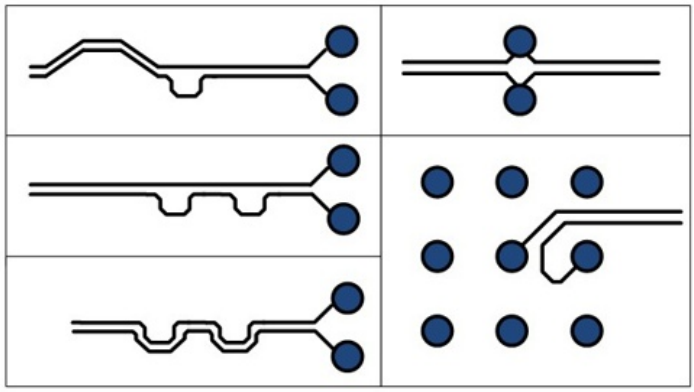
Note: Recommended structure for differential pairs is GSSG.

6.5 Channel Length Mismatch

To avoid skew, Tx/Rx differential pairs must have equal lengths. If skew occurs between bus trace lengths, mismatch should be minimal (no more than ±1mm).

- Differential signals require vias; however, the vias must be in the same configuration for each signal of the differential pair to ensure that both signals experience the same discontinuity. Therefore, any variation in signal due to the via-induced discontinuity will be in a common mode.
- Avoid trace routing over anti-pad or other impedance discontinuities on the transmission line.
- Avoid vias, via stubs and layer changes.
- Avoid any unnecessary pads on vias (which would add capacitance).
- Use ground return vias.
- Avoid using right-angle (90°) bends when matching channel lengths. Use mitered 45° bends instead.

Figure 6-2. Examples of Correct Channel Length Matching

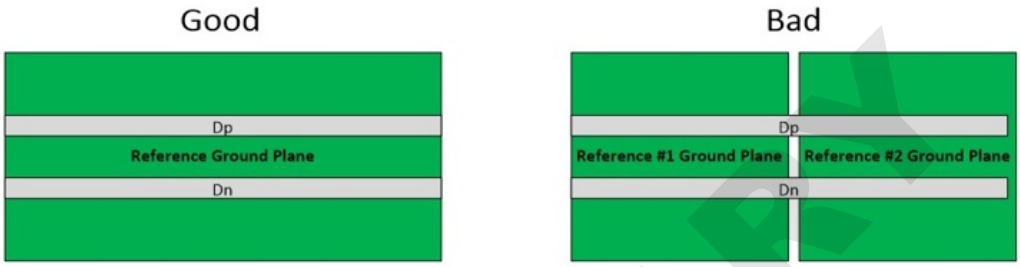


6.6 High-Speed Differential Routing

Tx/Rx differential pairs should be routed in a tightly coupled fashion to save routing space. However, this can create an impedance control challenge. To minimize impedance mismatches, follow these routing guidelines for Tx/Rx differential pairs:

- Use a continuous ground plane below Dp/Dn as shown in Figure 6-3.

Figure 6-3. High-Speed Differential Routing Examples



- Add ground return vias:
  - Symmetrical ground vias (return vias) should be used to reduce discontinuity for common mode signal component.
  - Minimize Cvia (capacitance):
    - Reduce the via capture pad size.
    - Eliminate all non-functional pads.
    - Increase the via anti-pad size where possible.
  - Minimize Lvia (inductance) by minimizing the via barrel length by back-drilling.
- Verify layouts using a 2-D field solver simulation.
- When designing traces, minimize the number of components on the transmission line. If components are necessary, choose ones that induce the least amount of discontinuity.
- Traces should be referenced to GND planes rather than power planes. No matter how much decoupling is built into the design, power planes are noisier than GND planes. Referencing to a power plane can induce noise onto a high speed signal.
- Given the same trace width and copper thickness considerations, stripline routing results in lower signal attenuation compared with microstrip.

6.7 Reference Clock

Table 6-2 lists the UFS Specification (JEDEC) reference clock parameters.

Table 6-2. UFS Reference Clock Specification

Parameter	Symbol	Minimum	Maximum	Unit
Input Clock Rise Time	t_{IRISE}	0.4	2	nsec
Input Clock Fall Time	t_{IFALL}	0.4	2	nsec

6.8 Recommended Capacitors

Table 6-3. Recommended Capacitors

Capacitor Value	Manufacturer	Manufacturer Part Number
4.7µF	MURATA	GRM185R60J475ME15D
	TAIYO YUDEN	JMK107BJ475MK-T
0.1µF	MURATA	GRM155R71A104KA01D
	KYOCERA	CM05X5R104K06AH
2.2µF	PANASONIC	ECJ0EB0J225M
	SAMSUNG	CL05A225MQ5NSNC

7.0 Proprietary Features Overview

7.1 Content Preloading Operation Mode

Elevated temperatures during the IR-Reflow process on 3D - X3 flash devices may cause a significant increase of read errors on TLC blocks (Uncorrectable read errors of data that were programmed before the IR Reflow process). This level of read errors is higher compared to previous flash technologies. Currently, this level of errors cannot be prevented by special error correction algorithms (as previously deployed in earlier flash technologies).

To overcome these challenges, the device introduced a propriety content pre-loading feature, which solves the IR-Reflow process reliability issue, by writing the preloaded data to the SLC area of the device.

Every new iNAND device is defined to start in the implicit loading state. There are several exit triggers that will switch it to the Migration state. Once the Migration is completed, the device will start to function in the Normal state.

The maximum image data size that can programmed on the device is described in Table 7-1.

Table 7-1. Content Preloading Maximum Size

Capacity	Bytes
64GB	19,204,040,294
128GB	38,408,080,588

7.2 SmartSLC®

The iNAND SmartSLC® feature enhances write performance, thereby providing the customer with a UX experience that makes an X3 memory look better than X2. The SmartSLC® adds the following value to the system:

- Auto-adjust device performance per application need
- Improves system efficiency and UX
  - Reduces system WRITE-BUSY time by improving I/O throughput.
- Vertical iNAND technology:
  - Host access to iNAND NAND flash performance capabilities.
  - Controller and Firmware auto-detections of hosts needs and auto-adjustment device behavior based on these host needs.
  - Host (driver) customizations and modifications in IDLE time management to allow optimized utilization of SmartSLC capabilities.

The device uses allocated SLC blocks within the NAND design to implement the feature. The allocation of these blocks does not impact the as sold capacity of the device (Exported Capacity). The device uses a detection mechanism and once a pattern requiring sequential write performance is detected, the device postpones any background management operations, (if feasible), and dedicates resources to SLC programing. Any IDLE state larger than tIDLE [ms], shall trigger migration operations to free up enough space for the next burst and eliminate potential performance drop.

Table 7-2. SmartSLC Buffer Size and Performance

Capacity	Buffer Size (GB)	Write Speed[1] [MBs]
64GB	16	400
128GB	32	550

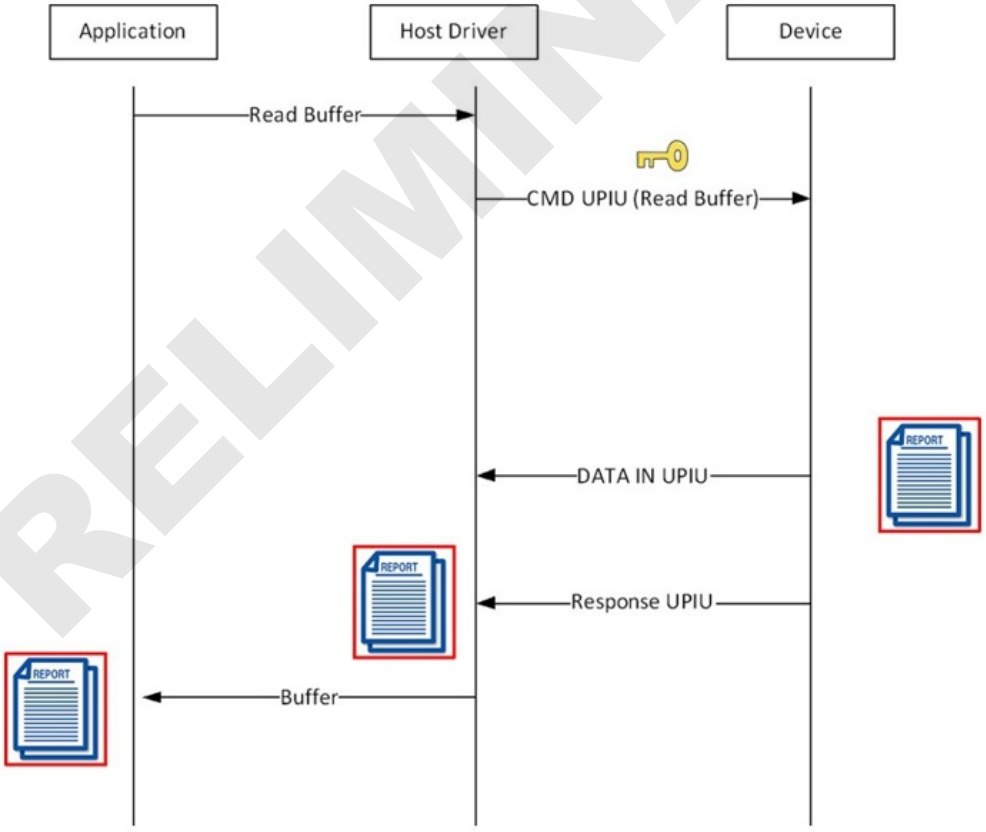
[1] *Sequential write Performance is measured using a proprietary test environment, without file system overhead and host turn-around time (HTAT), a 512KB chunk, and enough recovery time before measurement @ Gear3/2L mode.*

7.3 Device Report

7.3.1 Access Command Sequence

To read the Device Report in UFS, a UPIU Read Buffer command sequence is used. Figure 7-1 shows the host command sequence that is required to retrieve the Device Report information.

Figure 7-1. Host Command Sequence - UPIU Read Buffer Command



7.3.2 Read Buffer CDB Parameters

Table 7-3. READ BUFFER (10) CDB Parameters

Parameter	Byte/Bit	Value
OPCODE	(Byte: 0 Bit: 0-7):	3c
MODE	(Byte: 1 Bit: 0-4):	01h (Vendor Specific)
BUFFER ID	(Byte: 2 Bit: 0-7):	01h
BUFFER OFFSET	(Byte: 3-5 Bit: 0-7):	Key
ALLOCATION LENGTH	(Byte: 6-8 Bit: 0-7):	0x200 (512 bytes buffer size)

Table 7-4. READ BUFFER Command

		Bit							
		7	6	5	4	3	2	1	0
Byte	0	OPERATION CODE (3Ch)							
	1	Reserved			MODE				
	2	BUFFER ID							
	3	(MSB)							
	4	BUFFER OFFSET							
	5								(LSB)
	6	(MSB)							
	7	ALLOCATION LENGTH							
	8								(LSB)
	9	CONTROL = 00h							

REMARKS:

- The Device Report extraction method supports intermediate command interruptions during the Device Report extraction command flow.
- When the READ BUFFER command is sent with a wrong argument or sent in a wrong sequence, the iNAND will return "all-zeros" buffer.
- Events that break the Device Report flow are: Power Cycle, HW Reset, CMD0
- If one of the above events occurs, the iNAND state machine is reset. Therefore, after such event, the host must re-send the full command sequence to retrieve the Device Report information.

7.3.3 Device Report Data Structure Output

Table 7-5. Device Report Data Structure Output

Field Name	Description	Motivation (Host Perspective)	Offset (Dec)	Size [Bytes]
Average Erase Cycles Type C (Enhanced)	The Average Erase cycles value out of all Enhanced Area Blocks.	To check real life product endurance and lifetime.	0	4
Average Erase Cycles Type A (SLC)	The Average Erase cycles value out of all SLC Blocks.	To check real life product endurance and lifetime.	4	4
Average Erase Cycles Type B (TLC)	The Average Erase cycles value out of all TLC Blocks.	To check real life product endurance and lifetime.	8	4
Read reclaim count Type C (Enhanced)	The amount of Enhanced Reads operations which passed Read-Scrub thresholds and requires reclaim.	To check iNAND data-retention preventions mechanism on management area.	12	4
Read reclaim count Type A (SLC)	The amount of SLC Reads operations which passed Read-Scrub thresholds and requires reclaim.	To check iNAND data-retention preventions mechanism on SLC area.	16	4
Read reclaim count Type B (TLC)	The amount of TLC Reads operations which passed Read-Scrub thresholds and requires reclaim.	To check iNAND data-retention preventions mechanism on TLC area.	20	4
Bad Block Manufactory	Number of Bad Blocks detected during manufacturing process.	To check device number of Bad-Blocks.	24	4
Bad Block Runtime Type C (Enhanced)	All Bad Blocks related to the Enhanced area that were detected during run-time.	To check device runtime number of Bad-Blocks on Management area.	28	4
Bad Block Runtime Type A (SLC)	All Bad Blocks related to the SLC area that were detected during run-time.	To check device runtime number of Bad-Blocks on SLC area.	32	4
Bad Block Runtime Type B (TLC)	All Bad Blocks related to the TLC area that were detected during run-time.	To check device runtime number of Bad-Blocks on TLC area.	36	4
Field FW Updates Count	Number of secure Field Firmware Upgrades (sFFU) done from the beginning of the device life time.	To know that number of times sFFU operations were done on the device.	40	4
FW Release Date	Firmware Release Date	To identify device Firmware.	44	12
FW Release Time	Firmware Release Hour	To identify device Firmware.	56	8
Cumulative Host Write Data Size	Accumulate the amount of Host Written payload in resolution of 100MB.	To analyze host total write payload and typical daily workload.	64	4
Number Vcc Voltage Drops Occurrences	Cumulative counter for voltage drops (Power-Off) during all device states (Idle/Read/Write/Erase).	To identify unstable power supply platform behavior.	68	4
Number Vcc Voltage Droops Occurrences	Counts the times VDET indication was triggered due to Power-Droop (slight power-droop below certain threshold and for a very short period).	To identify unstable power supply platform behavior.	72	4
Number of Failures Recover New Host Data (After Write Abort)	Count the number of times iNAND dismissed new Host data due to Write Abort (either due to corrupted data or broken) command.	To analyze write abort behavior by device.	76	4
Total Recovery Operation After VDET	The total amount of recovery operations required to be done by the device while detecting internal slight power-droop.	To analyze device recovery after VDET event occurs.	80	4

Field Name	Description	Motivation (Host Perspective)	Offset (Dec)	Size [Bytes]
Cumulative SmartSLC Write Payload	Accumulate the amount of Host written payload that was written to the SmartSLC buffer in resolution of 100MB.	To track and analyze SmartSLC behavior.	84	4
Cumulative SmartSLC BigFile Mode Write Payload	Accumulate the amount of Host written payload that was written to SmartSLC BigFile buffer in resolution of 100MB.	To track and analyze iNAND SmartSLC BigFile mode behavior.	88	4
Number of times SmartSLC BigFile mode was operated during device lifetime.	Count the number of times Host wrote payload to SmartSLC BigFile mode.	To track and analyze iNAND SmartSLC BigFile mode behavior.	92	4
Average Erase Cycles of SmartSLC BigFile mode	The Average Erase count of SmartSLC BigFile buffer.	To track and analyze SmartSLC BigFile mode behavior.	96	4
Cumulative Initialization Count	Number of device power-ups events from beginning of life.	To analyze number of initialization events happened during device lifetime.	100	4
Max Erase Cycles Type C (Enhanced)	The Maximum Erase value out of all enhanced Blocks.	To check product endurance variance.	104	4
Max Erase Cycles Type A (SLC)	The Maximum Erase value out of all SLC Blocks.	To check product endurance variance.	108	4
Max Erase Cycles Type B (TLC)	The Maximum Erase value out of all TLC Blocks.	To check product endurance variance.	112	4
Min Erase Cycles Type C (Enhanced)	The Minimum Erase value out of all enhanced Blocks.	To check product endurance variance.	116	4
Min Erase Cycles Type A (SLC)	The Minimum Erase value out of all SLC Blocks.	To check product endurance variance.	120	4
Min Erase Cycles Type B (TLC)	The Minimum Erase value out of all TLC Blocks.	To check product endurance variance.	124	4
Reserved	Reserved	Reserved	128-151	24
Pre-EOL warning level Type C (Enhanced)	Pre-end-of-life (EOL) levels for device enhanced area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and activated Read Only mode.	To predict early lifetime of device.	152	4
Pre-EOL Warning Level Type B (TLC)	Pre-end-of-life (EOL) levels for device TLC area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and activated Read Only mode.	To predict early lifetime of device.	156	4
Uncorrectable Error Correction Code	The amount of UECC by the device.	To analyze UECC probability during real lifetime.	160	4
Current Temperature	Indicates the current temperature of the device in degrees Celsius.	To track device environmental status.	164	4
Min Temperature	Indicates the minimum temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status.	168	4
Max Temperature	Indicates the maximum temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status.	172	4

Field Name	Description	Motivation (Host Perspective)	Offset (Dec)	Size [Bytes]
Reserved	Reserved	Reserved	176	4
Enriched Device Health Type C (Enhanced)	Device health (age) Level in resolution of 1% (1-100) for Enhanced area.	To check real life product endurance and lifetime.	180	4
Enriched Device Health Type B (TLC)	Device health (age) Level in resolution of 1% (1-100) for TLC area.	To check real life product endurance and lifetime.	184	4
Reserved			188	3
Current Power Mode	Device Internal Power State (5 States: Highest 4; Lowest 0)	Indicates the internal device power/performance state.	191	1
Enriched Device Health (SLC)	Device Health (Age) Level in 1% resolution (1-100).	To check real life product endurance and lifetime.	192	4
Pre-EOL Warning Level (SLC)	Pre-End-of-Life (EOL) levels: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and has entered Read Only mode.	To predict early lifetime of device.	196	4
Number of IO Voltage Droops Occurrences	Counts Power-Droop (Slight power-droop below certain threshold and for a very short period).	To identify unstable power supply platform behavior.	200	4
Cumulative Host Read Data Size	Counts the number of host reads transactions in resolution of 100MB.	To analyze host total read payload and typical daily workload.	204	4
Bitflip Detection Counter	Counts the number of SRAM bit-flip detections.	To identify abnormal device behavior.	208	4
Bitflip Correction Counter	Counts the number of SRAM bit-flip corrections.	To identify abnormal device behavior.	212	2

8.0 Product Marking

Table 8-1 lists the position of each element that appears on the label.

Table 8-1. Product Marking Elements

Row	Description
1	Simplified Logo
2	Sales Item P/N
3	Country of Origin, e.g., "TAIWAN" or "CHINA" 2D Barcode: A 12-digit unique ID that reflects the "Sales Item P/N".
4	■ Y - Last digit of year ■ WW - Work Week ■ D - A day within the week (1 to 7) ■ MTLLLXXX - Internal use

9.0 Ordering Information

Table 9-1. Ordering Information

Capacity NAND	Capacity LPDDR4x	Part Number	Package	UFS Spec
64GB	48Gb	SDDDC4DR-64G	11.5mm x 13mm x 1.0mm	2.1
128GB	32Gb	SDDDC4CR-128G	11.5mm x 13mm x 1.0mm	2.1
128GB	48Gb	SDDDC4DR-128G	11.5mm x 13mm x 1.1mm	2.1

Note: A generic part number has a "G" following the capacity, but for a custom part number, an optional Customer Code is added at the end of the part number. The Customer Code can be up to four (4) digits. See Table 9-2 as an example.

Table 9-2. Ordering Information Customer Examples

Customer	Customer Code	Customer Part Number
Customer A	1209	SDDDC4DR-64-1209
Customer B	1217	SDDDC4DR-64-1217

Note: An optional Unique Identifier is a single character that specifies certain custom attributes, e.g., the suffix "T" added to the part number indicates tape/reel. SDDDC4DR-64G would become SDDDC4DR-64GT. The default part numbers are shipped in trays.

10.0 Appendix A: 8Gb LPDDR4x SDRAM Features

The following is a list of the 8Gb LPDDR4x SDRAM features:

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2 = 1.1V (1.06V to 1.17V)
- VDDQ = 0.6V (0.57V to 0.65V)
- Programmable CA ODT and DQ ODT with VSSQ termination
- VOH compensated output driver
- Single data rate command and address entry
- Double data rate architecture for Data Bus; two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
- DMI pin support for write data masking and DBIdc functionality
- Programmable RL (Read Latency) and WL (Write Latency)
- Burst length: 16 (default), 32 and On-the-Fly; On-the-Fly mode is enabled by MRS
- Auto-Refresh and Self-Refresh supported
- All Bank Auto-Refresh and Directed Per Bank Auto-Refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- Background ZQ Calibration

10.1 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, except for IDD6ET which is for the entire extended temperature range.

Note: All values are based on two (2) channel.

Table 10-1. LPDDR4x IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	3200 3733	Units	Notes
Operating one back active-precharge current: tCK = tCKmin; tRCmin; CKE = HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD0_1$	VDD1	24.2	mA	
	$IDD0_2$	VDD2	68.6	mA	
	$IDD0_Q$	VDDQ	1.32	mA	3
Idle power-down standby current: tCK = tCKmin; CKE = LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD2P_1$	VDD1	1.95	mA	
	$IDD2P_2$	VDD2	6.75	mA	
	$IDD2P_Q$	VDDQ	0.8	mA	3
Idle power-down standby current with clock stop: CK_t = LOW; CK_c = HIGH CKE = LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD2PS_1$	VDD1	1.95	mA	
	$IDD2PS_2$	VDD2	6.75	mA	
	$IDD2PS_Q$	VDDQ	0.8	mA	3
Idle non- power-down standby current: tCK = tCKmin; CKE = HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD2N_1$	VDD1	1.95	mA	
	$IDD2N_2$	VDD2	37.3	mA	
	$IDD2N_Q$	VDDQ	1.32	mA	3
Active power-down standby current: tCK = tCKmin; CKE = LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD3P_1$	VDD1	9	mA	
	$IDD3P_2$	VDD2	9	mA	
	$IDD3P_Q$	VDDQ	0.8	mA	3
Active power-down standby current: tCK = tCKmin; CKE = LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD3P_1$	VDD1	9	mA	
	$IDD3P_2$	VDD2	9	mA	
	$IDD3P_Q$	VDDQ	0.8	mA	3
Active power-down standby with clock stop: CK_t = LOW, CK_C = HIGH CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD3PS_1$	VDD1	9	mA	
	$IDD3PS_2$	VDD2	9	mA	
	$IDD3PS_Q$	VDDQ	0.8	mA	4

Parameter/Condition	Symbol	Power Supply	3200	3733	Units	Notes
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD3N_1$	VDD1	13.2		mA	
	$IDD3N_2$	VDD2	38.3		mA	
	$IDD3N_Q$	VDDQ	1.32		mA	4
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD3NS_1$	VDD1	13.2		mA	
	$IDD3NS_2$	VDD2	31.1		mA	
	$IDD3NS_Q$	VDDQ	1.32		mA	4
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 8; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	25	28	mA	
	$IDD4R_2$	VDD2	386	440	mA	
	$IDD4R_Q$	VDDQ	181	183	mA	5
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4W_1$	VDD1	28	30	mA	
	$IDD4W_2$	VDD2	334	382	mA	
	$IDD4W_Q$	VDDQ	1.32	1.32	mA	4
All-bank REFRESH Burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5_1$	VDD1	93.1		mA	
	$IDD5_2$	VDD2	253		mA	
	$IDD5_Q$	VDDQ	1.32		mA	4
All-bank REFRESH Average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5AB_1$	VDD1	8		mA	
	$IDD5AB_2$	VDD2	48		mA	
	$IDD5AB_Q$	VDDQ	1.32		mA	4
Per-bank REFRESH Average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5PB_1$	VDD1	8.1		mA	
	$IDD5PB_2$	VDD2	48		mA	
	$IDD5PB_Q$	VDDQ	1.32		mA	4
Self-Refresh current (85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled	$IDD6_1$	VDD1	8.1		mA	6,7,9
	$IDD6_2$	VDD2	19.8		mA	6,7,9
	$IDD6_Q$	VDDQ	0.8		mA	4,6,7,9

Parameter/Condition	Symbol	Power Supply	3200 3733	Units	Notes
Self-Refresh current (45°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6_1$	VDD1	8.1	mA	6,7,9
	$IDD6_2$	VDD2	19.8	mA	6,7,9
	$IDD6_Q$	VDDQ	0.8	mA	4,6,7,9
Self-Refresh current (25°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6_1$	VDD1	0.87	mA	6,7,9
	$IDD6_2$	VDD2	1.4	mA	6,7,9
	$IDD6_Q$	VDDQ	0.3	mA	4,6,7,9
Self-Refresh current (105°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6ET_1$	VDD1	28.5	mA	6,7,10
	$IDD6ET_2$	VDD2	1.4	mA	6,7,10
	$IDD6ET_Q$	VDDQ	0.3	mA	4,6,7,10

NOTE:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled; MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40ohm.
6. This is the general definition that applies to full-array Self-Refresh.
7. Supplier data sheets may contain additional Self-Refresh IDD values for temperature subranges within the Standard or Elevated Temperature Ranges.
8. VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2 for all IDD measurements.
9. IDD6 85°C is guaranteed; IDD6 for 25°C and 45°C is typical of the distribution of the arithmetic mean.
10. IDD6ET is a typical value, and is only sampled but not tested.

10.2 AC Timing Parameters

Table 10-2. AC Timing Parameters – Core Parameters

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
ACTIVE to ACTIVE Command Period	tRC	Min	tRAS + tRPab (with all bank precharge) tRAS + tRPpb (with per-bank precharge)								ns	
Minimum Self-Refresh Time (Entry to Exit)	tSR	Min	max (15ns, 3nCK)								ns	
Self-Refresh to Next Valid Command Delay	tXSR	Min	max (tRFCab + 7.5ns, 2nCK)								ns	
Exit Power Down to Next Valid Command	tXP	Min	max (7.5ns, 5nCK)								ns	
CAS to CAS Delay	tCCD	Min	8								tCK(avg)	2
CAS to CAS Delay Masked Write w/ECC	tCCDMW	Min	4 * tCCD								tCK(avg)	
Internal Read to Precharge Command Delay	tRTP	Min	max (7.5ns, 8nCK)								ns	
RAS to CAS Delay	tRCD	Min	max (18ns, 4nCK)								ns	
Row Precharge Time (Single Bank)	tRPpb	Min	max (18ns, 4nCK)								ns	
Row Precharge Time (All Banks) – 8 Banks	tRPab	Min	max (21ns, 4nCK)								ns	
Row Active Time	tRAS	Min	max (42ns, 3nCK)								ns	
		Max	min (9 * tREFI * Refresh Rate, 70.2)								µs	3
Write Recovery Time	tWR	Min	max (18ns, 4nCK)								ns	
Write to Read Command Delay	tWTR	Min	max (10ns, 8nCK)								ns	
Active Bank A to Active Bank B	tRRD	Min	max (10ns, 4nCK)								ns	
Precharge to Precharge Delay	tPPD	Min	4								tCK	
Four Bank Active Window	tFAW	Min	40								ns	

NOTE:

1. Precharge to Precharge Timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16; for BL32 an additional 8 tCK(avg) delay is needed.
3. Refresh Rate is specified by MR4 OP[2:0].

Table 10-3. AC Timing Parameters – Clock Timings

Parameter	Symbol	Min/ Max	LPDDR4 1600	LPDDR4 2400	LPDDR4 3200	LPDDR4 4200	Unit	Note
Average Clock Period	tCK(avg)	Min	1.25	0.833	0.625	0.467	ns	
		Max	100	100	100	100		
Average High Pulse Width	tCH(avg)	Min	0.46	0.46	0.46	TBD	tCK(avg)	
		Max	0.54	0.54	0.54	TBD		
Average Low Pulse Width	tCL(abs)	Min	0.46	0.46	0.46	TBD	tCK(avg)	
		Max	0.54	0.54	0.54	TBD		
Absolute Clock Period	tCL(abs)	Min	tCK(avg)min + tJIT(per)min				ns	
		Max	—					
Absolute Clock HIGH Pulse Width	tCH(abs)	Min	0.43	0.43	0.43	TBD	tCK(avg)	
		Max	0.57	0.57	0.57	TBD		
Absolute Clock LOW Pulse Width	tCL(abs)	Min	0.43	0.43	0.43	TBD	tCK(avg)	
		Max	0.57	0.57	0.57	TBD		
Clock Period Jitter	tJIT(abs)	Min	-70	-50	-40	TBD	ns	
		Max	70	50	40	TBD		
Maximum Clock Jitter between Two Consecutive Clock Cycles	tJIT(cc)	Min					ns	
		Max	140	100	80	TBD		

Table 10-4. AC Timing Parameters – Calibration Timings

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
ZQ Calibration Time	tZQCAL	Max	1								µ	
ZQ Calibration Latch Quiet Time	tzQLAT	Max	max (30ns, 8nCLK)								ns	
Calibration Reset Time	tQZRESET	Max	max (50ns, 3nCLK)								ns	

Table 10-5. DQ Tx Voltage and Timings (Read Timing Parameters)

Parameter	Symbol	Min/ Max	1600 1867	2133 2400	3200	4266	Unit	Note
Data Timing								
DQS_t, DQS_c to DQ Skew	tDQSQ	Max	0.18				UI	1
DQ Output Hold Time Total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	min (tQSH, tQSL)				UI	1

Parameter	Symbol	Min/ Max	1600 1867	2133 2400	3200	4266	Unit	Note
DQ Output Hold Time Total from DQS_t, DQS_c (DBI Disabled)	tQW_total	Min	0.75	0.73	0.7	0.7	UI	1,4
DQ Output Window Time Total Deterministic, per Pin (DBI-Disabled)	tQW_dj	Min	TBD	TBD	TBD	TBD	UI	1,4,3
DQS_t, DQS_c to DQ Skew Total, per Group, per Access (DBI Enabled)	tDQSQ_DBI	Max	TBD	TBD	TBD	TBD	UI	1
DQ Output Hold Time Total from DQS_t, DQS_c (DBI Enabled)	tQH_DBI	Min	min (tQSH_DBI, tQSL_DBI)				UI	1
DQ Output Window Time Total per Pin (DBI Enabled)	tQW_total_DBI	Min	TBD	TBD	TBD	TBD	UI	1,4
READ Preamble	tRPRE	Min	1.8				tCK(avg)	
Extended READ Postamble	tRPSTE	Min	1.4				tCK(avg)	
DQS Low-Impedance Time from CK_t, CK_c	tLZ(DQS)	Min	(RL x tCK) + tDQSCK(min) - (tPRE(max) x tCK) - 200ps				ps	
DQS High-Impedance Time from CK_t, CK_c	tHZ(DQS)	Max	(RL x tCK) + tDQSCK(max) - (RPST(max) x tCK) - 100ps				ps	
DQ Low-Impedance Time from CK_t, CK_c	tLZ(DQ_)	Min	(RL x tCK) + tDQSCK(min) - 200ps				ps	
DQ High-Impedance Time from CK_t, CK_c	tHZ(DQ_)	Max	(RL x tCK) + tDQSCK(max) + tDQSQ(max)+(BL/2 x tCK)-100ps				Ps	
Data Strobe Timing								
DQS Output Access Time from CK/CK#	tDQSCK	Min	1.5				ns	8
		Max	3.5					
DQSCK Temperature Drift	tDQSCK_temp	Max	4				ps/C	9
DQSCK Voltage Drift	tDQSCK_volt	Max	7				ps/mV	10
CK to DQS Rank to Rank Variation	tDQSCK_rank2 rank	Max	1.0				ns	11,12
DQS Output Low Pulse Width (DBI Disabled)	tQSL	Min	MintCL(abs)-0.05				tCK(avg)	4,5
DQS Output High Pulse Width (DBI Disabled)	tQSH	Min	tCH(abs)-0.05				tCK(avg)	4,6
DQS Output Low Pulse Width (DBI Enabled)	tQSL_DBI		tCL(abs)-0.045				tCK(avg)	5,7
DQS Output High Pulse Width (DBI Enabled)	tQSH_DBI		tCH(abs)-0.045				tCK(avg)	5,7

NOTE:

1. DQ to DQS differential jitter where the total includes the sum of deterministic and random timings for a specified BER. The BER specification and measurement method are TBD.
2. The deterministic component of the total timing. The measurement method is TBD.
3. This parameter will be characterized and guaranteed by design.
4. This parameter is a function of input clock jitter. These values assume the minimum tCH(abs) and tCL(abs). When the input clock jitter minimum tCH(abs) and tCL(abs) are 0.44 or greater of tCK(avg), the minimum value of tQSL will be tCL(abs)-00.04 and the tQSH will be tCH(abs)-0.04.
5. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on the falling edge to the next consecutive rising edge.
6. tQSH describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on the falling edge to the next consecutive rising edge.
7. This parameter is a function of input clock jitter. These values assume the minimum tCH(abs) and tCL(abs).
8. This includes the DRAM process, voltage and temperature variation and the AC noise impact for frequencies >20MHz and a maximum voltage of 45mVp-p from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Mix-Max DC operating conditions.
9. The tDQSCK_temp maximum delay variation is a function of Temperature.
10. The tDQSCK_volt maximum delay variation is a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate the timing variation due to VDDQ and VDD2 noise <20MHz. The host controller does not need to account for any variation due to VDDQ and VDD2 noise >20MHz. The voltage supply noise must comply to the component Min-Max DC operating conditions. The voltage variation is defined as the max(abs(tDQSCKmin@V1-tDQSCKmax@V2)/abs(V2-V2). VDDQ = VDD2 is assumed for the testing measurement.
11. The same voltage and temperature are applied to tDQS2CK_rank2rank.
12. The tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
13. UI = tCK(avg)min/2.

Table 10-6. DQ Rx Voltage and Timings (Write Timing Parameters)

Parameter	Symbol	Min/ Max	1600 1867[1]	2133 2400	3200	4266	Unit	Note
Rx Mask Voltage p-p Total	VdIVW_total	Max	140	140	140	120	mV	1,2,3,5
Rx Mask Voltage - Deterministic	VdIVW_dV	Max	TBD	TBD	TBD	TBD	mV	1,5
Rx Timing Window Total (at VdIVW Voltage Levels)	TdIVW_total	Max	0.22	0.22	0.25	0.25	UI	1,2,4,5
Rx Deterministic Timing	TdIVW_dj	Max	TBD	TBD	TBD	TBD	UI	1,5
Rx Timing Window 1 Bit Toggle (at VdI Voltage Levels)	TdIVW_1bit	Max	TBD	TBD	TBD	TBD	UI	1,2,4,5, 14
DQ AC Input Pulse Amplitude p-p	VIHIL_AC	Min	180	180	180	170	mV	7,15
DQ Input Pulse Width (at Vcent_DQ)	TdIPW	Min	0.45	0.45	0.45	0.45	UI	8
DQ to DQS Offset	TDQS2DQ	Min	200	200	200	200	ps	9
		Max	800	800	800	800		
DQ to DQ Offset	TDQDQ	Max	30	30	30	30	ps	10
DQ to DQS Offset Temperature Variation	TDQS2DQ_temp	Max	0.6	0.6	0.6	0.6	ps/C	11
DQ to DQS Offset Voltage Variation	TDQS2DQ_volt	Max	33	33	33	33	ps/ 50mV	12
DQ to DQS Offset Rank-to-Rank	TDQS2DQ_rank2rank	Max	200	200	200	200	ps	17
Write Command to 1ST DQS Latching Transition	tDQSS	Min	0.75				tCK(avg)	
		Max	1.25					
DQS Input High-Level Width	tDQSH	Min	0.4				tCK(avg)	
DQS Input Low-Level Width	tDQSL	Min	0.4				tCK(avg)	
DQS Falling Edge to CK Setup Time	tDSS	Min	0.2				tCK(avg)	
DQS Falling Edge Hold Time from CK	tDSH	Min	0.2				tCK(avg)	
Write Preamble	tWPRE	Min	1.8				tCK(avg)	
0.5 tCK Write Postamble	tWPST	Min	0.4				tCK(avg)	
1.5 tCK Write Postamble	tWPSTE	Min	1.4				tCK(avg)	
Input Slew Rate Over VdIVW_total	SRIN_dIVW	Min	1	1	1	1	V/ns	13
		Max	7	7	7	7		

[1] *The following Rx voltage and timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. The timing parameters in UI can be converted to absolute time values where tCK(avg)min/2=625ps for DQ=1600. For example, the TdIVW_total(ps)=0.22*625ps=137.5ps.*

NOTE:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ to DQS voltage AC noise impact for frequencies >250KHz at a fixed temperature on the package. The voltage supply noise must comply with the component Min-Max DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual Dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels.
5. Defined over the DQ internal Vref range. The Rx mask at the pin must be within the internal Vref DQ range irrespective of the input signal common mode.
6. Deterministic component of the total Rx mask voltage or timing. The parameter will be characterized and guaranteed by design. The measurement method is TBD.
7. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total IU. No timing requirement above level. VIHL AC is the peak-to-peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 minimum must be met both above and below Vcent_DQ.
8. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
9. DQ to DQS offset is within byte DRAM pin to DRAM internal latch. It includes the DRAM process, voltage and temperature variation.
10. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
11. TDQS2DQ maximum delay variation as a function of temperature.
12. TDQS2DQ maximum delay variation as a function of the DC voltage variation for VDDQ and VDD2.
13. Input slew rate over VdIVW mask centered at Vcent_DQ(pin_mid).
14. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
15. VIHL_AC does not have to be met when no transitions are occurring.
16. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
17. The tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Table 10-7. Self-Refresh Timing Parameters

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Delay from Self-Refresh Entry to CKE Input Low	tESCKE	Min	max (1.75ns, 3tCK)								nCK	1
Minimum Self-Refresh Time (Entry to Exit)	tSR	Min	max (15ns, 3nCK)									1
Self-Refresh Exit to Next Valid Command Delay	tXSR	Min	max (tRFCab + 7.5ns, 2nCK)									1,2

NOTE:

1. Delay time must satisfy both analog time (ns) and clock count (tCK), meaning that tESCKE will not expire until CK has toggled through at least three (3) full cycles (3 * tCK) and 1.75ns has transpired. The case that applies to 3tCK is shown in Figure 10-1.
2. The MRR-1, CAS-2, SRX, MPC, MRW-1 and MRW-2 commands (except for PASR bank/segment setting) are only allowed during this period.

Figure 10-1. 3tCK Case Example

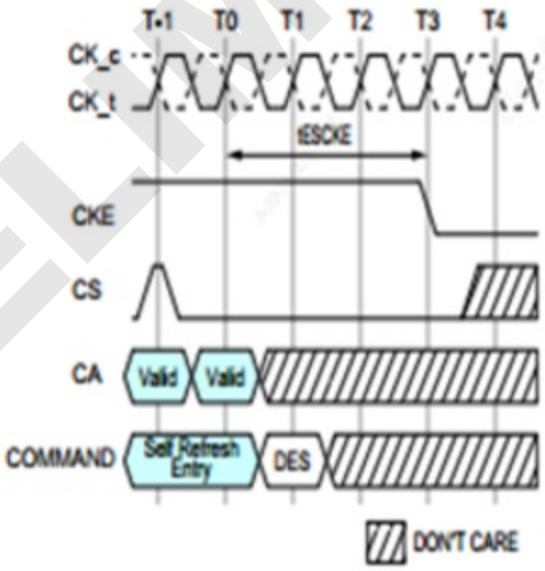


Table 10-8. Command Address Input Parameters

Parameter	Symbol	Min/ Max	DQ-1333[1]	DQ-1600 DQ-1867	DQ-3200	DQ-4266	Unit	Note
Rx Mask Voltage p-p	VcIVW	Max	175	175	155	145	mV	1,2,4
Rx Timing Window	tcIVW	Max	0.3	0.3	0.3	0.3	UI	1,2,3,4
CA AC Input Pulse Amplitude pk-pk	VIHL_AC	Min	210	210	190	180	mV	5,8
CA Input Pulse Width	TcIPW	Min	0.55	0.55	0.6	0.6	UI	6
Input Slew Rate Over VcIVW	SRIN_cIVW	Min	1	1	1	1	V/ms	7
		Max	7	7	7	7		

[1] *The following Rx voltage and timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. The timing parameters in UI can be converted to absolute time values where tCK(avg)min/2=1.5ns for DQ=1333. For example, the TdIVW_total(ps)=0.3*1.5=450ps.*

NOTE:

1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal Vref range; the Rx mask at the pin must be within the internal Vref CA range irrespective of the input signal common mode.
5. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. There is no timing requirement above this level. VIHL AC is the peak-to-peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2min must be met above and below Vcent_CA.
6. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
7. Input slew rate over VcIVW mask centered at Vcent_CA(pin mid).
8. VIHL_AC does not have to be met when no transitions are occurring.
9. UI = tCK(avg)min/2.
10. The following Rx voltage and timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. The timing parameters in UI can be converted to absolute time values where tCK(avg)min/2=1.5ns for DQ=1333. For example, the TdIVW_total(ps)=0.3*1.5=450ps.

Table 10-9. Boot Parameters

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Clock Cycle Time	tCKb	Min	Note 1, Note 2								ns	
		Max	Note 1, Note 2									
Address and Control Input Setup Time	tISb	Min	1150								ps	
Address and Control Input Hold Time	tIHb	Min	1150								ps	
DQS Output Data Access Time from CK/CK#	tDQSCKb	Min	2								ns	
		Max	10									
Data Strobe Edge to Output Data Edge	tDQSQb	Max	1.2								ns	

NOTE:

1. Minimum tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by Min tCKb; the higher boot frequency is system dependent.

Table 10-10. Mode Register Parameters

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Additional time after tXP has expired until the MRR Command may be issued.	tMRRI	Min	tRCD + 3nCK								ns	
MODE REGISTER Write Command Period	tMRW	Min	max (10ns, 10nCK)								ns	
MODE REGISTER Read Command Period	tMRR	Min	8								nCK	
MODE REGISTER Write Set Command Delay	tMRD	Min	max (14ns, 10nCK)								ns	

Table 10-11. VRCG Enable/Disable Timing

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
VREF High Current Mode Enable Time	tVRCG_Enable	Min	200								ns	
VREF High Current Mode Disable Time	tVRCG_Disable	Min	100								ns	
Clock and Command Valid after CKE Low	tCKELCK	Min	max (7.5ns, 5nCK)								tCK	
Clock Setup for Vref Training Mode	tDStrain	Min	2								ns	
Data Hold for Vref Training Mode	tDHtrain	Min	2								ns	
Asynchronous Data Read	tADR	Min	20								ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)								tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10								ns	1
First CA Bus Training Command following CKE Low	tCAENT	Min	250								ns	
Vref Step Time Multiple Steps	tVref_long	Max	250								ns	
Vref Step Time One Step	tVref_short	Max	80								ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2 * tCL + tXP								—	
Valid Clock Requirement after CS High	tCKPSTCS	Min	Minmax (7.5ns, 5nCK)								—	
Minimum Delay from CS to DQS Toggle in Command Bus Training	tCS_Vref	Min	2								tCK	
Minimum Delay from CKE High to Strobe High Impedance	tCKEHDQS	Min	10								ns	
Clock and Command Valid before CKE High	tCKCKEH	Min	2								tCK	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5								ns	
ODT Turn-on Latency from CKE	tCKELODTon	Min	20								ns	
ODT Turn-off Latency from CKE	tCKELODToff		20								ns	

NOTE:

1. DQS_t must retain a low level during the tDQSCKE period and DQS_c must retain a high level.
2. If tCACD is violated, the data for sample that violate tCACD will be unavailable except for the last sample (where tCACD after the sample is met). Valid data for the last sample will be available after tADR.

Table 10-12. Write Leveling Parameters

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
DQS_t/DQS_c Delay after Write-Leveling Mode is programmed.	tWLD-QSEN	Min	20								tCK	
Write Preamble for Write Leveling	tWLWPRE	Min	20								tCK	
First DQS_t/DQS_c Edge after Write-Leveling Mode is programmed.	tWLMRD	Min	40								tCK	
Write Leveling Output Delay	tWDO	Min	0								ns	
		Max	20									
Valid Clock Requirement before DQS Toggle	tCKPRDQS	Min	max (7.5ns, 4nCK)									
Valid Clock Requirement after DQS Toggle	tCKPST-DQS	Min	max (7.5ns, 4nCK)									
Write Leveling Hold Time	tWLH	Min			150	100		75		50		1,2
Write Leveling Setup Time	tWLS	Min			150	100		75		50		1,2
Write Leveling Invalid Window	tWLIVW_-Total	Min			240	160		120		50		1,2

NOTE:

1. In addition to the usual setup and hold time specifications outlined in the above table, there is value in an invalid window specification for write-leveling training. As the training is derived from each device, the worst-case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW_Total is like tdIVW_Total with the exception that in this case it is a DQS invalid window with respect to CK. This would need to account for all VT (Voltage and Temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling invalid window.

The DQS input mask for time with respect to CK is shown in the following figure. The "total" mask (tdiVW_Total) defines the time the input signal must not encroach for the DQS input to be successfully captured by CK with a BER of lower than TBD. The mask is a receiver property and is not the valid data-eye.

Figure 10-2. DQS_t/DQS_c and CK_t/CK_c at DRAM Latch

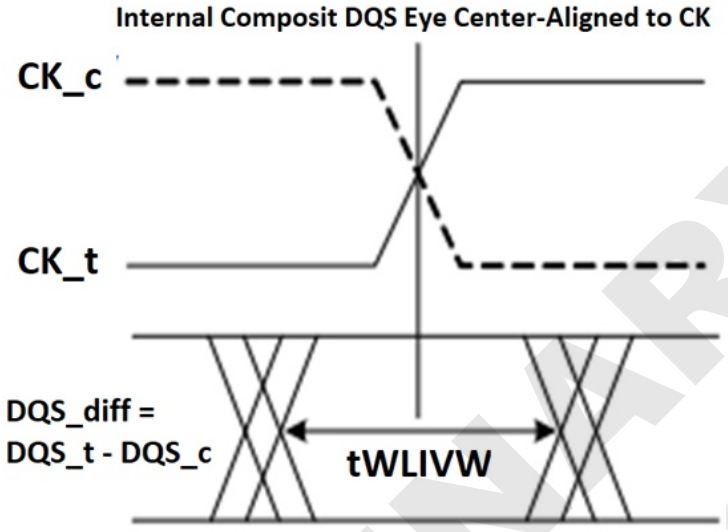


Table 10-13. Read Preamble Training Timings

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Delay from MRW Command to DQS Driven Out	tSDO	Max	min (tMRD, 15ns)								tCK	1

Table 10-14. MPC [Write FIFO] AC Timing

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Additional time after tXP has expired until MPC [Write FIFO] command may be used.	tMPCWR	Min	tRCD + 3nCK									

Table 10-15. DQS Interval Oscillator AC Timing

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Delay Time from QSC Stop to Mode Register Readout	tQSCO	Min	max (40ns, 8nCK)								ns	

Table 10-16. Frequency Set-Point Timing

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Frequency Set Point Switching Time	tFC_Short	Min	200								ns	1
	tFC_Middle	Min	200								ns	1
	tFC_Long	Min	250								ns	1
Valid Clock Requirement after entering FSP Charge	tCKFSPE	Min	max (7.5ns, 4nCK)									
Valid Clock Requirement before First Valid Command after FSP Charge	tCKFSPX	Min	max (7.5ns, 4nCK)									

NOTE:

1. The Frequency Set Point Switching Time is dependent on the value of the Vref(ca) parameter: MR12 OP[5:0] and Vref(ca) Range: MR12 OP[6:0] of FSP-OP 0 and 1. In addition, any change to the Frequency Set Point may affect the Vref(dq) setting. The set time of the Vref(dq) level is the same as that of the Vref(ca) level.

Table 10-17. CA ODT Setting Timing

Parameter	Symbol	Min/ Max	LPDDR4-1600/1866/2133/2400/3200/4266	Unit	Note
ODT CA Value Update Time	tODTUP	Min	RU (TBD ns/tCK(avg))		

Table 10-18. Power Down Timing

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
CKE Minimum Pulse Width (HIGH and LOW Pulse Width)	tCKE	Min	max (7.5ns, 4nCK)									
Delay from Valid Command to CKE Input LOW	tCMDCKE	Min	max (1.75ns, 3nCK)								ns	1
Valid Clock Requirement after CKE Input LOW	tCKELCK	Min	max (5ns, 5nCK)ns								ns	1
Valid CS Requirement before CKE Input LOW	tCSCKE	Min	1.75								ns	
Valid CS Requirement before CKE Input LOW	tCKELCS	Min	max (5ns, 5nCK)								ns	
Valid Clock Requirement before CKE Input HIGH	tCKCKEH	Min	max (1.75ns, 3nCK)								ns	1

Parameter	Symbol	Min/ Max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	DDR4 3733	DDR4 4267	Unit	Note
Exit Power Down to Next Valid Command Delay	tXP	Min	max (7.5ns, 5nCK)								ns	1
Valid CS Requirement before CKE Input HIGH	tCSCKEH	Min	1.75								ns	
Valid CS Requirement after CKE Input HIGH	tCKEHCS	Min	max (7.5ns, 5nCK)								ns	
Valid Clock and CS Requirement after CKE Input LOW after MRW Command	tMRWCKEL	Min	max (14ns, 10nCK)								ns	1
Valid Clock and CS Requirement after CKE Input LOW after ZQ Calibration Start Command	tZQCKE	Min	max (1.75ns, 3nCK)								ns	1

NOTE:

1. The Delay Time must satisfy both analog time (ns) and clock count (nCK). For example, tCMDCKE will not expire until CK has toggled through at least three (3) full cycles (3 * tCK) and 3.75ns has transpired. Figure 10-3 below shows the instance when 3nCK occurs.

Figure 10-3. tCMDCKE Timing

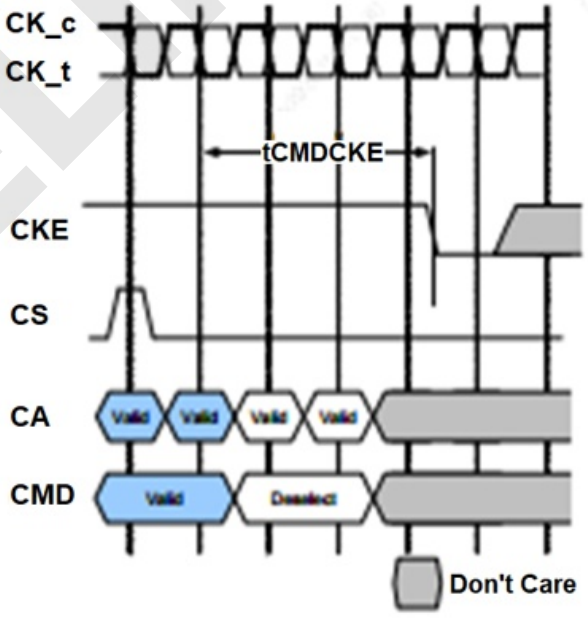


Table 10-19. PPR Timing Parameters

		LPDDR4			
Parameter	**Symbol**	**Minimum**	**Maximum**	**Unit**	**Notes**
PPR Programming Time	tPGM	1000	—	ms	
PPR Exit Time	tPGM_Exit	15	—	ns	
New Address Setting Time	tPGMPST	50	—	µs	

Table 10-20. Temperature Derating for AC Timing

Parameter	**Symbol**	**Min/ Max**	**DDR4 533**	**DDR4 1066**	**DDR4 1600**	**DDR4 2133**	**DDR4 2667**	**DDR4 3200**	**DDR4 3733**	**DDR4 4267**	**Unit**	**Note**
DQS Output Access Time from CK_t/CK_c (derated)	tDQSCKd	Max	3600								ps	1
RAS-to-CAS Delay (derated)	tRCDd	Min	tRCD + 1.875								ns	1
Activate-to-Activate Command Period (derated)	tRCd	Min	tRC + 3.75								ns	1
Row Active Time (derated)	tRASd	Min	tRAS + 1.875								ns	1
Row Precharge Time (derated)	tRPd	Min	tRP + 1.875								ns	1
Active Bank A to Active Bank B (derated)	tRRDd	Min	tRRD + 1.875								ns	1

Note: The timing derating applies for operation at 85°C to 105°C.

10.3 MR25 Register Information (MA[5:0] = 19H)

Table 10-21. MR25 Register Information (MA[5:0] = 19H)

OP[7]	**OP[6]**	**OP[5]**	**OP[4]**	**OP[3]**	**OP[2]**	**OP[1]**	**OP[0]**
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

LPDDR4 supports Fail Row address repair as an optional feature and it is readable through MR25 OP[7:0]. PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, LPDDR4 can correct 1Row per Bank.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair.

Fail Row Address Repair

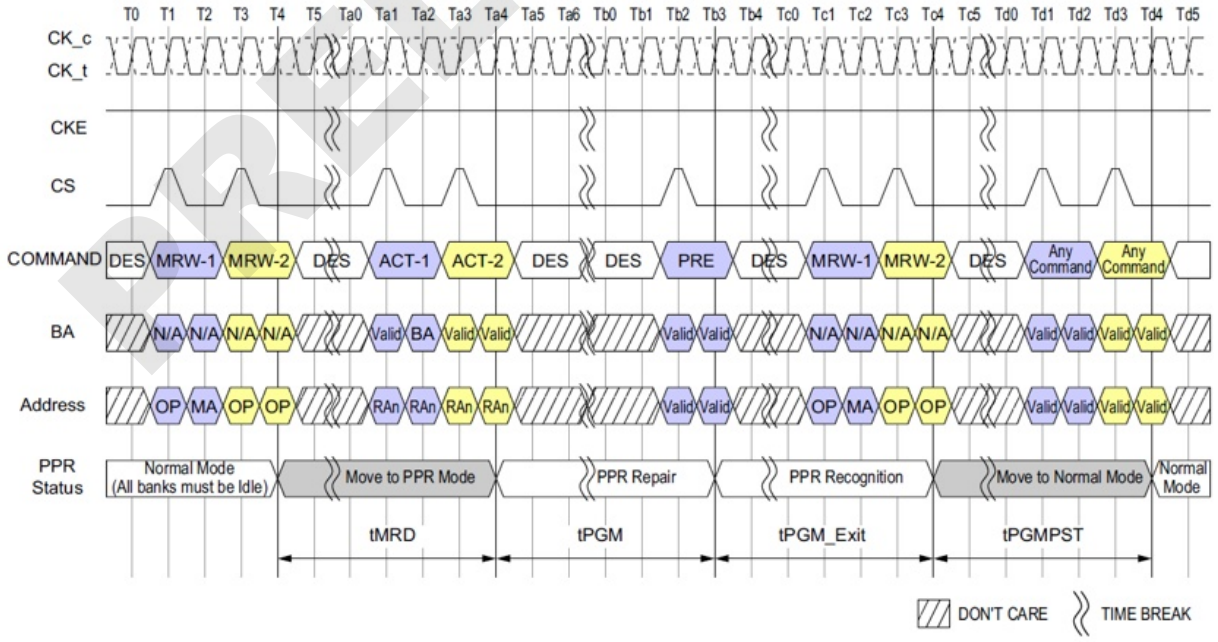
Following is the procedure of PPR:

1. Before entering 'PPR' mode, All banks must be Pre-charged.
2. Enable PPR using MR4 bit "OP4=1" and wait tMRD.
3. Issue ACT command with Fail Row address.
4. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE.
5. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address.
6. Exit PPR with setting MR4 bit "OP4=0".
7. LPDDR4 will accept any valid command after tPGMPST.
8. In More than one fail address repair case, repeat Step 2 and 7.

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [OP4=0] and by tPGMPST.

Figure 10-4 shows PPR related MR bits and its operation.

Figure 10-4. PPR Timing



10.4 MR4 Register Information (MA[5:0] = 04H)

Table 10-22. MR4 Register Information (MA[5:0] = 04H)

Function	Register Type	Operand	Data	Notes
PPR Resource	Read	OP[7:0]	0B: PPR Resource is not available 1B: PPR Resource is available	

Table 10-23. MR4 Register Information (MA[5:0] = 04H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000_B: SDRAM Low temperature operating limit exceeded 001_B: 4x refresh 010_B: 2x refresh 011_B: 1x refresh (default) 100_B: 0.5x refresh 101_B: 0.25x refresh, no de-rating 110_B: 0.25x refresh, with de-rating 111_B: SDRAM High temperature operating limit exceeded	1,2,3,4, 7,8,9
SR Abort (Self Refresh Abort)	Write	OP[3]	0_B: Disable (default) 1_B: Enable	9,11
PPRE (Post-package repair entry/ exit)	Write	OP[4]	0_B: Exit PPR mode (default) 1_B: Enter PPR mode	5,9
Thermal Offset (Vender Specific Function)	Write	OP[6:5]	00_B: No offset, 0~5°C gradient (default) 01_B: 5°C offset, 5~10°C gradient 10_B: 10°C offset, 10~15°C gradient 11_B: Reserved	10
TUF (Temperature Update Flag)	Read	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	6,7,8

NOTE:

1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. OP[2:0]=011_B corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1_B, the device temperature is greater than 85°C.
2. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the LPDDR4-SDRAM will set OP[2:0]=110_B. See derating timing requirements in Table 10-20 on page 59.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000_B or 111_B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence(Te).
8. See the section on "temperature Sensor" for information on the recommended frequency of reading MR4.
9. OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
10. Refer to the supplier data sheet for vendor specific function.
11. Self Refresh abort feature is available for higher density devices starting with 12Gb device.

11.0 Contact Information

Western Digital Technologies, Inc.
951 SanDisk Drive, Milpitas, CA 95035-7933
Phone: +1-408-801-1000
Fax: +1-408-801-8657
Email: oemproducts@wdc.com

Western Digital®

Western Digital
5601 Great Oaks Parkway
San Jose, CA 95119
U.S.A.

For service and literature:
support.wdc.com
www.wdc.com
800.ASK.4WDC North America
+800.6008.6008 Asia Pacific
00800.ASK.4WDEU Europe (toll free where available)
+31.88.0062100 Europe/Middle East/Africa

02-05-WW-04-00037-P3
November 2018