

# MC14175B

## Quad Type D Flip-Flop

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input (R) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and  $\bar{Q}$ ). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

### Features

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

| Parameter   | Symbol            | Value                  | Unit               |
|---|-------------------|------------------------|--------------------|
| DC Supply Voltage Range                           | $V_{DD}$          | -0.5 to +18.0          | V                  |
| Input or Output Voltage Range (DC or Transient)   | $V_{in}, V_{out}$ | -0.5 to $V_{DD}$ + 0.5 | V                  |
| Input or Output Current (DC or Transient) per Pin | $I_{in}, I_{out}$ | $\pm 10$               | mA                 |
| Power Dissipation per Package (Note 1)            | $P_D$             | 500                    | mW                 |
| Ambient Temperature Range                         | $T_A$             | -55 to +125            | $^{\circ}\text{C}$ |
| Storage Temperature Range                         |                   | -65 to +150            | $^{\circ}\text{C}$ |
| Lead Temperature (8-Second Soldering)             |                   | 260                    | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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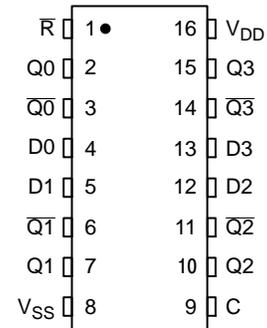


SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966

### PIN ASSIGNMENT



### MARKING DIAGRAMS



SOIC-16



SOEIAJ-16

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Package

### ORDERING INFORMATION

| Device         | Package             | Shipping†        |
|----------------|---------------------|------------------|
| MC14175BDG     | SOIC-16 (Pb-Free)   | 48 Units/Rail    |
| MC14175BDR2G   | SOIC-16 (Pb-Free)   | 2500/Tape & Reel |
| NLV14175BDR2G* | SOIC-16 (Pb-Free)   | 2500/Tape & Reel |
| MC14175BFELG   | SOEIAJ-16 (Pb-Free) | 2000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

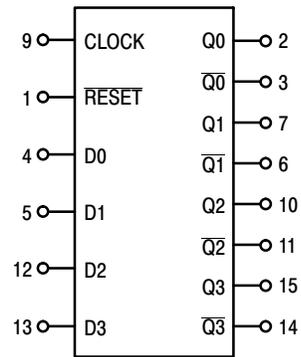
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## TRUTH TABLE

| Inputs |      |       | Outputs |           |
|--------|------|-------|---------|-----------|
| Clock  | Data | Reset | Q       | $\bar{Q}$ |
|        | 0    | 1     | 0       | 1         |
|        | 1    | 1     | 1       | 0         |
|        | X    | 1     | Q       | $\bar{Q}$ |
| X      | X    | 0     | 0       | 1         |

No Change

X = Don't Care



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8

Figure 1. Block Diagram

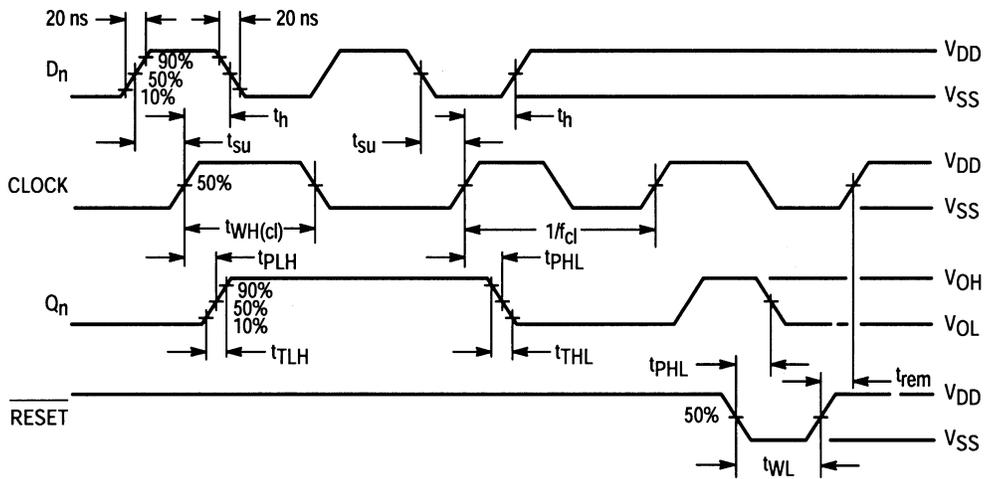


Figure 2. Timing Diagram

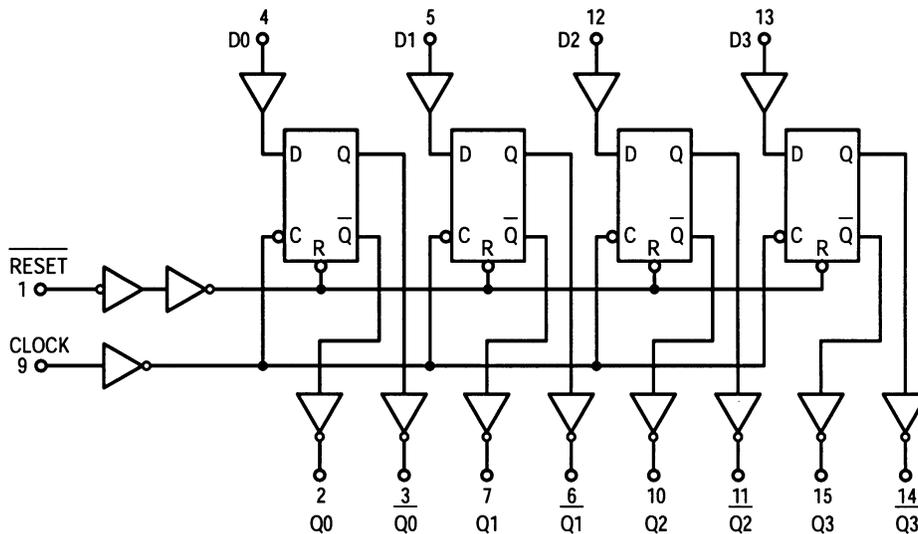


Figure 3. Functional Block Diagram

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

| Characteristic  | Symbol                | $V_{DD}$<br>Vdc | -55°C  |           | 25°C  |                 |           | 125°C |           | Unit      |
|---|-----------------------|-----------------|--|-----------|-------|-----------------|-----------|-------|-----------|-----------|
|   |                       |                 | Min  | Max       | Min   | Typ<br>(Note 2) | Max       | Min   | Max       |           |
| Output Voltage<br>$V_{in} = V_{DD}$ or 0  | "0" Level<br>$V_{OL}$ | 5.0             | -  | 0.05      | -     | 0               | 0.05      | -     | 0.05      | Vdc       |
|   |                       | 10              | -  | 0.05      | -     | 0               | 0.05      | -     | 0.05      |           |
| 15  |                       | -               | 0.05   | -         | 0     | 0.05            | -         | 0.05  |           |           |
| $V_{in} = 0$ or $V_{DD}$  | "1" Level<br>$V_{OH}$ | 5.0             | 4.95   | -         | 4.95  | 5.0             | -         | 4.95  | -         | Vdc       |
|   |                       | 10              | 9.95   | -         | 9.95  | 10              | -         | 9.95  | -         |           |
|   |                       | 15              | 14.95  | -         | 14.95 | 15              | -         | 14.95 | -         |           |
| Input Voltage<br>( $V_O = 4.5$ or $0.5$ Vdc)<br>( $V_O = 9.0$ or $1.0$ Vdc)<br>( $V_O = 13.5$ or $1.5$ Vdc)                                 | "0" Level<br>$V_{IL}$ | 5.0             | -  | 1.5       | -     | 2.25            | 1.5       | -     | 1.5       | Vdc       |
|   | 10                    | -               | 3.0  | -         | 4.50  | 3.0             | -         | 3.0   |           |           |
| ( $V_O = 0.5$ or $4.5$ Vdc)<br>( $V_O = 1.0$ or $9.0$ Vdc)<br>( $V_O = 1.5$ or $13.5$ Vdc)  | "1" Level<br>$V_{IH}$ | 5.0             | 3.5  | -         | 3.5   | 2.75            | -         | 3.5   | -         | Vdc       |
|   |                       | 10              | 7.0  | -         | 7.0   | 5.50            | -         | 7.0   | -         |           |
| 15  |                       | 11              | -  | 11        | 8.25  | -               | 11        | -     |           |           |
| Output Drive Current<br>( $V_{OH} = 2.5$ Vdc)<br>( $V_{OH} = 4.6$ Vdc)<br>( $V_{OH} = 9.5$ Vdc)<br>( $V_{OH} = 13.5$ Vdc)                   | Source<br>$I_{OH}$    | 5.0             | -3.0   | -         | -2.4  | -4.2            | -         | -1.7  | -         | mAdc      |
|   | 5.0                   | -0.64           | -  | -0.51     | -0.88 | -               | -0.36     | -     |           |           |
| ( $V_{OL} = 0.4$ Vdc)<br>( $V_{OL} = 0.5$ Vdc)<br>( $V_{OL} = 1.5$ Vdc)   | Sink<br>$I_{OL}$      | 5.0             | 0.64   | -         | 0.51  | 0.88            | -         | 0.36  | -         | mAdc      |
|   |                       | 10              | 1.6  | -         | 1.3   | 2.25            | -         | 0.9   | -         |           |
| 15  |                       | 4.2             | -  | 3.4       | 8.8   | -               | 2.4       | -     |           |           |
| Input Current   | $I_{in}$              | 15              | -  | $\pm 0.1$ | -     | $\pm 0.00001$   | $\pm 0.1$ | -     | $\pm 1.0$ | $\mu$ Adc |
| Input Capacitance<br>( $V_{in} = 0$ )   | $C_{in}$              | -               | -  | -         | -     | 5.0             | 7.5       | -     | -         | pF        |
| Quiescent Current<br>(Per Package)  | $I_{DD}$              | 5.0             | -  | 5.0       | -     | 0.005           | 5.0       | -     | 150       | $\mu$ Adc |
|   |                       | 10              | -  | 10        | -     | 0.010           | 10        | -     | 300       |           |
|   |                       | 15              | -  | 20        | -     | 0.015           | 20        | -     | 600       |           |
| Total Supply Current (Notes 3 & 4)<br>(Dynamic plus Quiescent,<br>Per Package)<br>( $C_L = 50$ pF on all outputs, all<br>buffers switching) | $I_T$                 | 5.0             | $I_T = (1.7 \mu\text{A/kHz}) f + I_{DD}$<br>$I_T = (3.4 \mu\text{A/kHz}) f + I_{DD}$<br>$I_T = (5.0 \mu\text{A/kHz}) f + I_{DD}$ |           |       |                 |           |       |           | $\mu$ Adc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$  where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.004$ .

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## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

| Characteristic  | Symbol             | $V_{DD}$<br>Vdc | All Types        |                   |                   | Unit          |
|---|--------------------|-----------------|------------------|-------------------|-------------------|---------------|
|   |                    |                 | Min              | Typ<br>(Note 6)   | Max               |               |
| Output Rise and Fall Time<br>$t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$                | $t_{TLH}, t_{THL}$ | 5.0<br>10<br>15 | –<br>–<br>–      | 100<br>50<br>40   | 200<br>100<br>80  | ns            |
| Propagation Delay Time — Clock to Q, Q<br>$t_{PLH}, t_{PHL} = (0.9 \text{ ns/pF}) C_L + 175 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 72 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$ | $t_{PLH}, t_{PHL}$ | 5.0<br>10<br>15 | –<br>–<br>–      | 220<br>90<br>70   | 400<br>160<br>120 | ns            |
| Propagation Delay Time — Reset to Q, Q<br>$t_{PHL} = (0.9 \text{ ns/pF}) C_L + 280 \text{ ns}$<br>$t_{PHL} = (0.36 \text{ ns/pF}) C_L + 112 \text{ ns}$<br>$t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$                           | $t_{PHL}, t_{PLH}$ | 5.0<br>10<br>15 | –<br>–<br>–      | 325<br>130<br>100 | 500<br>200<br>150 | ns            |
| Clock Pulse Width   | $t_{WH}$           | 5.0<br>10<br>15 | 250<br>100<br>75 | 110<br>45<br>35   | –<br>–<br>–       | ns            |
| Reset Pulse Width   | $t_{WL}$           | 5.0<br>10<br>15 | 200<br>80<br>60  | 100<br>40<br>30   | –<br>–<br>–       | ns            |
| Clock Pulse Frequency   | $f_{cl}$           | 5.0<br>10<br>15 | –<br>–<br>–      | 4.5<br>11<br>14   | 2.0<br>5.0<br>6.5 | mHz           |
| Clock Pulse Rise and Fall Time  | $t_{TLH}, t_{THL}$ | 5.0<br>10<br>15 | –<br>–<br>–      | –<br>–<br>–       | 15<br>5.0<br>4.0  | $\mu\text{s}$ |
| Data Setup Time   | $t_{su}$           | 5.0<br>10<br>15 | 120<br>50<br>40  | 60<br>25<br>20    | –<br>–<br>–       | ns            |
| Data Hold Time  | $t_h$              | 5.0<br>10<br>15 | 80<br>40<br>30   | 40<br>20<br>15    | –<br>–<br>–       | ns            |
| Reset Removal Time  | $t_{rem}$          | 5.0<br>10<br>15 | 250<br>100<br>80 | 125<br>50<br>40   | –<br>–<br>–       | ns            |

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

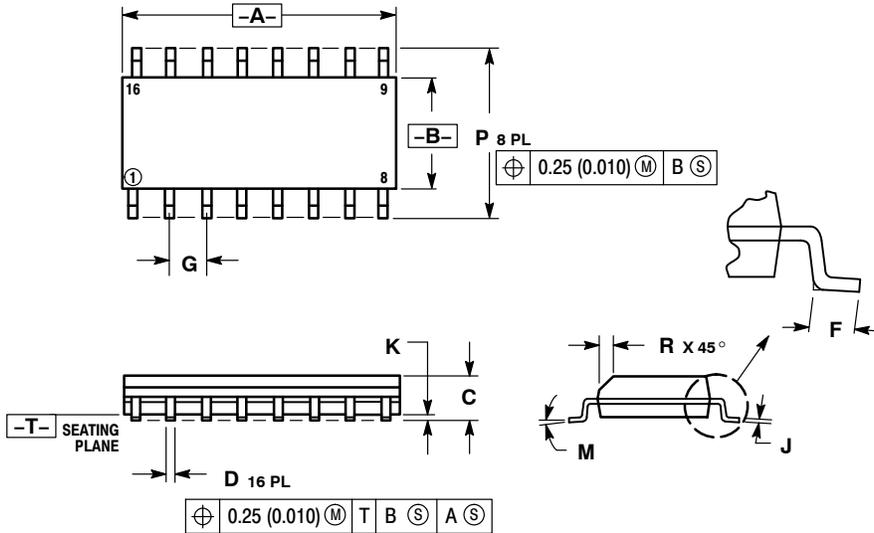
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SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



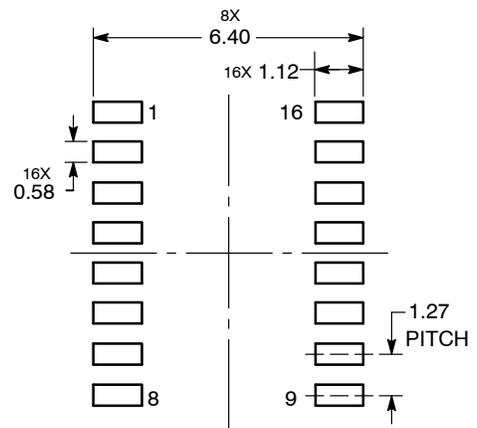
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

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