FP6606AC

USB Dual Ports Charging Controller USB-PD/HVDCP for Type-C and HVDCP for Type-A

Description

The FP6606AC is a simplified USB Power Delivery 3.0 protocol controller. It integrated functions for HiSilicon Fast Charging Protocol (FCP) and Qualcomm Quick Charge 2.0/3.0. It also supports USB Type-A and Type-C (1A1C). When 1A1C connector plug into simultaneously, output voltage will down to 5V.

The FP6606AC monitors the CC pin to detect a USB Type-C attach/detach. It is capable providing output voltage of 5V to 15V. The FP6606AC implements VBUS detection and VBUSC discharge for the implementation of compliant connection ports. The protection features include over-voltage (VBUS, D+/D-, CC1/CC2).

Additionally, the FP6606AC also monitors USB D+/D- data line, connector plug in/out and automatically adjust the output voltage depending on different device requirement. It is capable providing output voltage of 3.6V to 12V.

Features

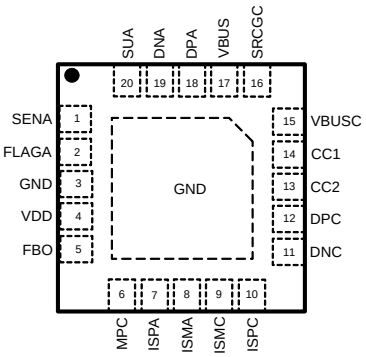
- VDD Supply Voltage: 3.2V to 6.8V
- Supports USB Type-C and USB PD 3.0 (simplified)
  -- 5V to 15V VBUS Source Only
  -- CC1/CC2 Source Terminator 3A
- Supports HiSilicon Fast Charging Protocol (FCP)
- Supports Qualcomm® Quick Charge™ 2.0/3.0 Class A
- Automatically Selects FCP and QC2.0/3.0 Protocols
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line
- USB A Port Plug in Detection
- Multi-Ports Control Application
- Over-Voltage Protection and VBUSC Discharge Function
- SSOP-20L、TQFN-20L (3mmx3mm)、CPC-16L Packages

Applications

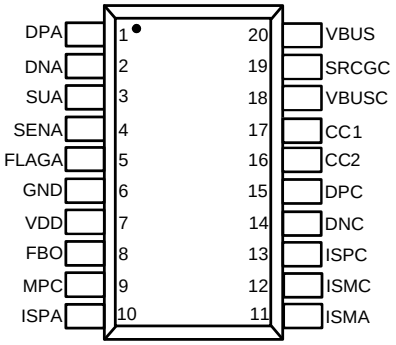
- Wall-Adapter
- Car Charger
- Power Strip
- USB Power Output Ports

Pin Assignments

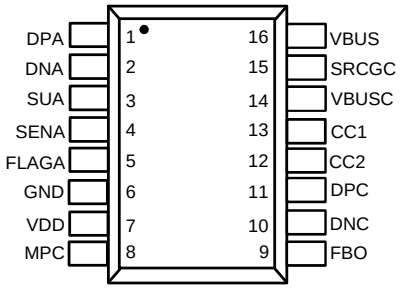
W4 Package TQFN-20L (3mmx3mm)



N3 Package SSOP-20L



P5 Package CPC-16L



Ordering Information

FP6606AC□□

- Package Type
  - N3: SSOP-20L
  - W4: TQFN-20L (3mmx3mm)
  - P5: CPC-16L
- Option Code
  - Please Reference Option Code Information

Option Code Information

Option Code	5V	9V	12V	15V	20V	Capability
A	3A	2A	1.5A	-	-	18W
B	3A	2A	1.5A	1.2A	-	18W
D	3A	3A	2.5A	2A	-	30W
E	3A	3A	3A	3A	-	45W
L	3A	3A	-	2A	1.5A	30W
M	3A	3A	-	3A	2.25A	45W

Typical Application Circuit

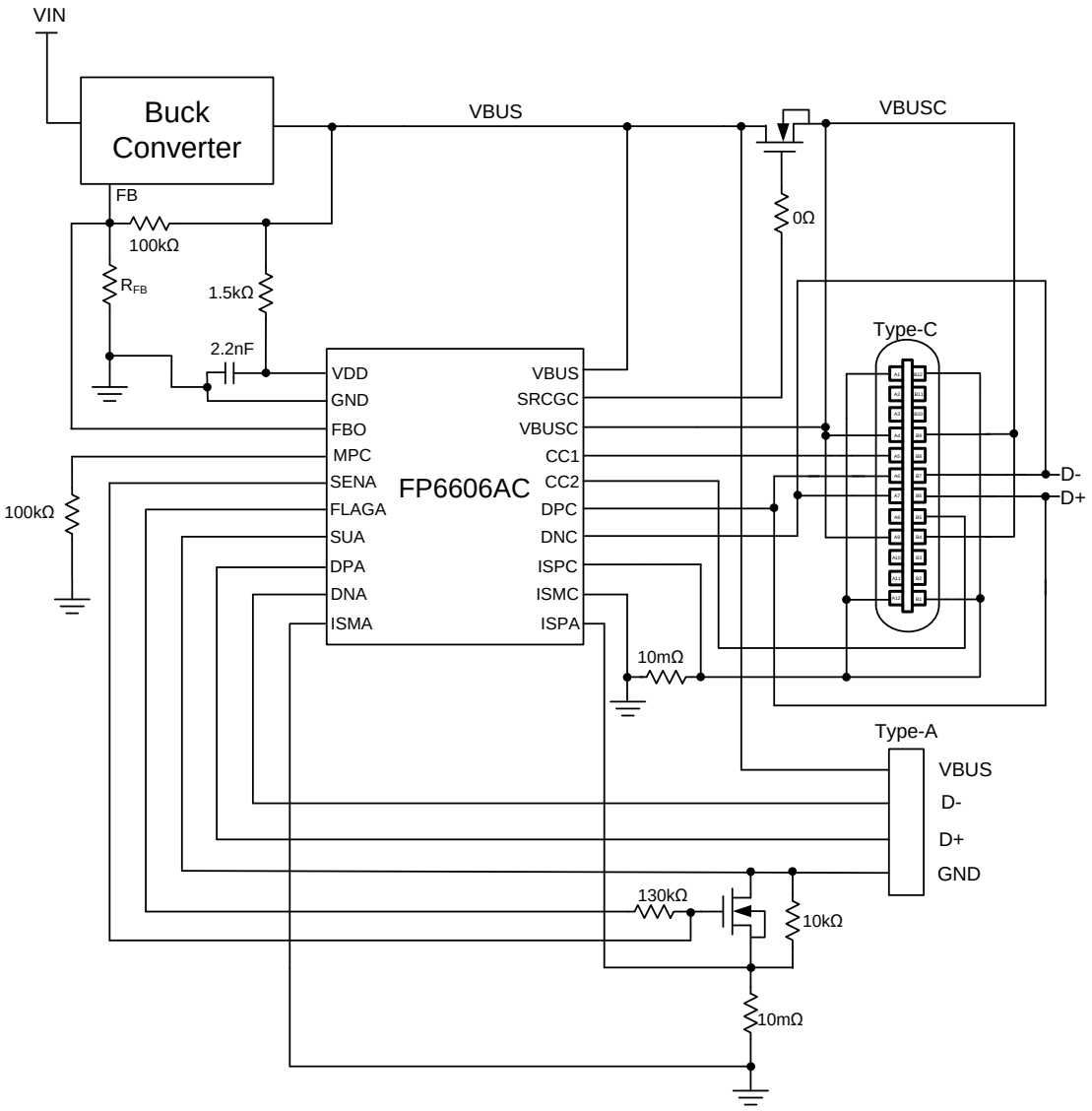


Figure1. SSOP-20L and TQFN-20 Packages Typical Application Schematic

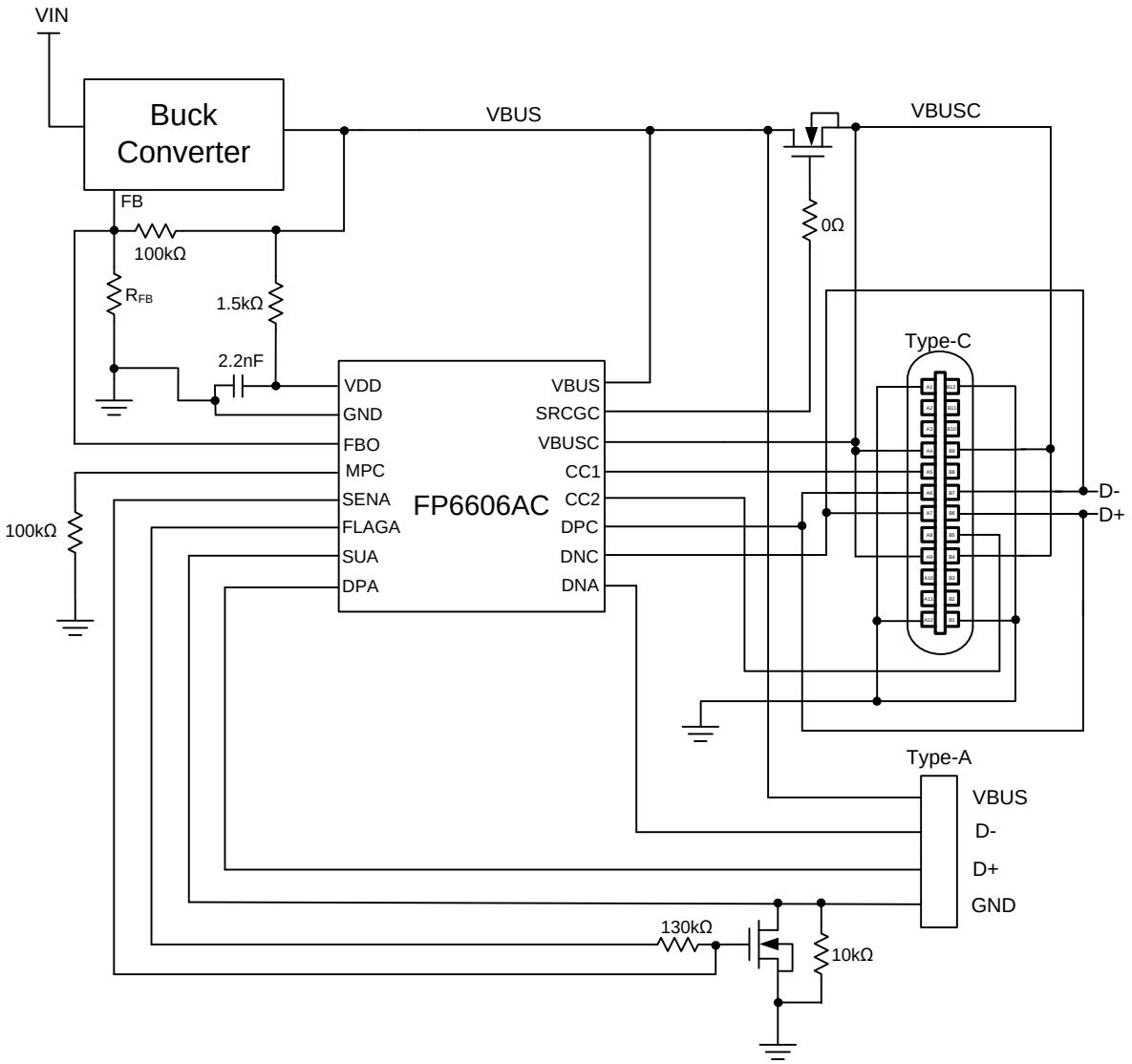


Figure2. CPC-16L Package Typical Application Schematic

Block Diagram

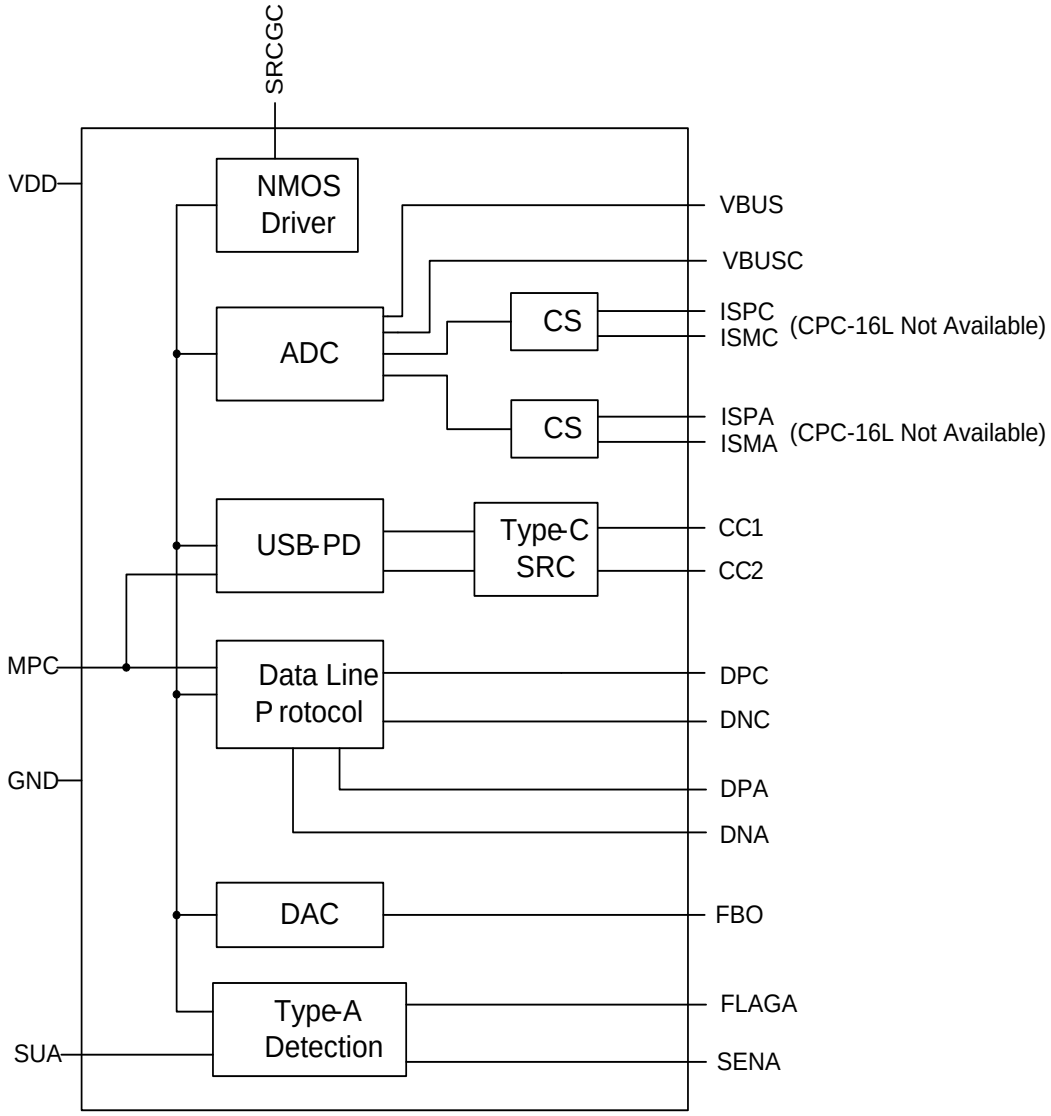


Figure3. Block Diagram of FP6606AC

Functional Pin Description

Pin Name	Pin No.			Pin Function
	SSOP-20L	TQFN-20L	CPC-16L	
DPA	1	18	1	USB D+ data line of Type-A. Recommended this pin connect without resistors(open) or with a resistor higher than 1MΩ connect to GND.
DNA	2	19	2	USB D− data line of Type-A.
SUA	3	20	3	Sense voltage function for Type-A connecter plug in.
SENA	4	1	4	Detection function Pin. Detect USB Type-A whether is device existence.
FLAGA	5	2	5	N-MOSFET gate node control. When Type-A plug in, FLAGA function will be activated high, Type-A plug out, FLAGA pin will be activated low.
GND	6	3	6	Power ground. The exposed pad must be connected to GND and well solder to a large PCB copper area for maximum power dissipation.
VDD	7	4	7	Supply input voltage pin.
FBO	8	5	9	Output voltage control pin. Current sink\source function for FB node.
MPC	9	6	8	Multi-ports control pin. Connect a 100kΩ resistor to GND.
ISPA	10	7	NA	Positive input of current sense amplifier of Type-A. Connect to the current sense resistor on the VBUS power path.
ISMA	11	8	NA	Negative input of current sense amplifier of Type-A. Connect to the current sense resistor on the VBUS power path.
ISMC	12	9	NA	Negative input of current sense amplifier of Type-C. Connect to the current sense resistor on the VBUS power path.
ISPC	13	10	NA	Positive input of current sense amplifier of Type-C. Connect to the current sense resistor on the VBUS power path.
DNC	14	11	10	USB D- data line of Type-C.
DPC	15	12	11	USB D+ data line of Type-C.
CC2	16	13	12	Type-C Configuration channel signal 2.
CC1	17	14	13	Type-C Configuration channel signal 1.
VBUSC	18	15	14	VBUS voltage detection for Type-C connector side.
SRCGC	19	16	15	N-MOSFET gate node control pin.
VBUS	20	17	16	VBUS voltage detection pin.

Absolute Maximum Ratings (Note 1)

- Input Supply Voltage VDD ---------- -0.3V to +7V
- DPA, DNA, SUA, SENA---------- -0.3V to +18V
- CC1, CC2 ,DPC,DNC ---------- -0.3V to +18V
- SRCGC ,VBUS, VBUSC ---------- -0.3V to +35V
- ISPA, ISMA, ISPC, ISMC---------- -0.3V to +6.5V
- FBO,MPC,FLAGA---------- -0.3V to +6.5V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec) ---------- +260°C
- Package Thermal Resistance, (θ_{JA}) (Note 2)
  - SSOP-20L ---------- 72.25°C/W
  - TQFN-20L(3mmx3mm) ---------- 68°C/W
  - CPC-16L ---------- TBD
- Package Thermal Resistance, (θ_{JC})
  - SSOP-20L ---------- 26.1°C/W
  - TQFN-20L(3mmx3mm) ---------- 30°C/W
  - CPC-16L ---------- TBD

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

Recommended Operating Conditions

- Input Supply Voltage (VDD) ---------- +3.2V to +6.8V
- Operating Temperature Range (T_A) ---------- -40°C to +125°C
- Junction Temperature (T_J) ---------- -40°C to +125°C

Electrical Characteristics

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VDD Input Voltage Range	V_{DD}		3.2		6.8	V
Input UVLO Threshold	V_{DD_UVLO}	V_{DD} Rising	3.1	3.3	3.5	V
	V_{DD_HYS}	V_{DD} Falling	2.45	2.6	2.75	V
VDD Supply Current	I_{DD_SUP}	V_{DD}=5V, Nothing Attach	20	33	45	μA
VDD Shunt Voltage	V_{DD_SHDN}		5.9	6.4	6.8	V
N-MOSFET Gate Driver						
SRCGC Sourcing Current		V_{DD}=4V 0V ≤ V_{SRCGC} – V_{BUSC} ≤ 6V			1	μA
Sourcing Voltage (ON) between SRCGC and VBUS		V_{DD}=3.2V to 6.8V	5		15	V
VBUS						
VBUS Over Voltage Protection			17.1	18	18.9	V
VBUS Bleed Discharge Resistance	$R_{\_Bleed}$		8	10	12.5	kΩ
VBUS Discharge Resistance	$R_{\_DIS}$			400		Ω
VBUSC Bleed Discharge Resistance	$R_{\_CBLEED}$		8	10	12.5	kΩ
VBUSC Discharge Resistance	$R_{\_CDIS}$			400		Ω
USB Type-A						
A_Plug in SUA Threshold	$V_{\_TH\text{-}USBAIN}$		0.57	0.83	1.02	V
A_Plug in De-bounce Time	$T_{\_USBAIN\text{-}DEB}$			200		μs
A_Plug out SUA Threshold	$V_{\_TH\text{-}USBAOUT}$			0.2		V
DPA/DNA OV Threshold (Note 3)	$V_{\_DPDNOV}$	In QC Mode		4		V
USB Type-C						
DPC/DNC OV Threshold (Note 3)	$V_{\_DPDNOV}$	In QC Mode		4		V
CCOV Rising (Note 3)	$V_{\_CCOV\text{-}rising}$			1.04*V_{DD}		V
CCOV Falling (Note 3)	$V_{\_CCOV\text{-}falling}$			V_{DD}		V

Electrical Characteristics (Continued)

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
DPA High Glitch Filter Time	$T_{GLITCH(BC)-DPA-H}$		1000	1250	1500	ms
DNA Low Glitch Filter Time	$T_{GLITCH(BC)-DNA-L}$			1		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)\ CHANGE}$		20	40	60	ms
DNA Pull-Down Resistance	$R_{DNA(DWN)}$			20		kΩ
Continuous Mode Glitch Filter Time	$T_{GLITCH-CONT-\ CHANGE}$		100		200	ms
DPA Leakage Resistance	$R_{DAT-LKG}$	V_{DD}=3.2 to 6.4V VDPA=0.6-3.6V Switch SW1=off	300	500	800	kΩ
Switch SW1 On-Resistance	$R_{DS\_ON\_N1}$	V_{DD}=5V,SW1=200μA			40	Ω
UP/Down Current Step	I_{UP}, I_{DOWN}	I_{UP} =0μA (5V),40μA (9V) 70μA (12V),100μA (15V) I_{DOWN}=14μA (3.6V)		2		μA
DCP Charging Mode						
$DPA_{\_0.48V}$ / $DNA_{\_0.48V}$ Line Output Voltage			0.44	0.48	0.52	V
$DPA_{\_0.48V}$ / $DNA_{\_0.48V}$ Line Output Impedance				900		kΩ
Apple Mode						
$DPA_{\_2.7V}$ / $DNA_{\_2.7V}$ Line Output Voltage			2.57	2.7	2.84	V
$DPA_{\_2.7V}$ / $DNA_{\_2.7V}$ Line Output Impedance				33.6		kΩ
DNA SECTION (FCP)						
DNA FCP Tx Valid Output High	V_{TX-VOH}		2.55		3.6	V
DNA FCP Tx Valid Output Low	V_{TX-VOL}				0.3	V
DNA FCP Rx Valid Output High	V_{RX-VIH}		1.4		3.6	V
DNA FCP Rx Valid Output Low	V_{RX-VIL}				1.0	V
DNA Output Pull-Low Resistance	R_{PD}		400	500	600	Ω
Unit Interval for FCP PHY Communication	UI	F_{CLK}=125kHz	144	160	180	μs

Electrical Characteristics (Continued)

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sense (ISPA / ISPC and ISMA / ISMC)						
Current Sense Range				64		mV
Resolution				0.5		mV
Accuracy		R=10mΩ,I_{out}=3A	29.25	30	30.75	mV

Note 3: Guarantee by design.

Function Description

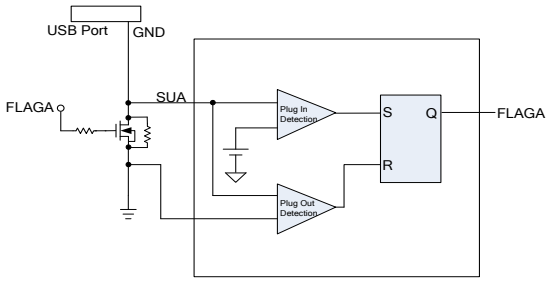
Multi-Ports Control

Use for single VBUS source and multi USB channel applications. Connect all MPC pins on different Fitipower USB ICs together and connect a 100kΩ resistor to GND. FP6606AC will auto detect the attachments between all Fitipower USB ICs and will auto decide multi-ports operation is allowed or not.

Plug In Detect

When device plugs in or out, the FP6606AC can auto detect and into standby or operation mode.

1. Plug In detection is used for USB device plug in. When device plug in, FLAGA pin alerts active high.
2. Plug Out detection is used for USB device plug out. When plug out detected, FLAGA pin active low.



VBUS Control

The FP6606AC is a controller so that it must be combined with power stage. The FBO pin of FP6606AC must be connected to the feedback node of power stage. The VBUS control of FP6606AC is implemented by sourcing/sinking current from FBO pin.

VBUSC Discharge

When Type-C device plug out connector, N-MOSFET will be turned off. At this moment in time, FP6606AC execute VBUSC discharge function to avoid Type-C connector existing remaining voltage. If Type-C connector exist remaining voltage, when device plug in, it maybe damage device.

Configuration Channel Protection

When CC1/CC2 pin is touched by the external power in abnormal situation, the CC1/CC2 pin of both sink device and source device may be damaged. In order to protect the CC1/CC2 pin of the devices from damage in abnormal situation, the FP6606AC will return the output voltage to default output voltage 5V.

Data Line Interface (D+/D-)

FP6606AC supports QC 2.0/3.0 and FCP protocol on the D+/D− data line. The related registers are assigned to the vendor define registers. When the FP6606AC is configured as QC 2.0/3.0/FCP mode, both D+ and D− pin are applied to 2.7V. If sink device has the function of QC 2.0/3.0/FCP, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will be automatically connected to D− pin by FP6606AC and this process is called the short mode for USB BC1.2 specification. If D+ is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the FP6606AC will enter QC 2.0/3.0/FCP operation mode. The QC 2.0/3.0 could be classed as the following table.

D+	D-	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

When the voltage of D+ pin and D− pin simultaneously satisfy these two inequalities VDAT(REF)< D+ < VSEL_REF and D− > VSEL_REF, the FP6606AC would enter continuous mode.

In the continuous mode, each voltage pulse on D− pin generated by sink device is between 3V and 1V. At the same time, the low level of pulse should be keep at least 200μs (default). If the specified conditions are satisfied, the FBO pin will source 2μA (default) per pulse. The maximum source current is 70μA for output voltage 12V.

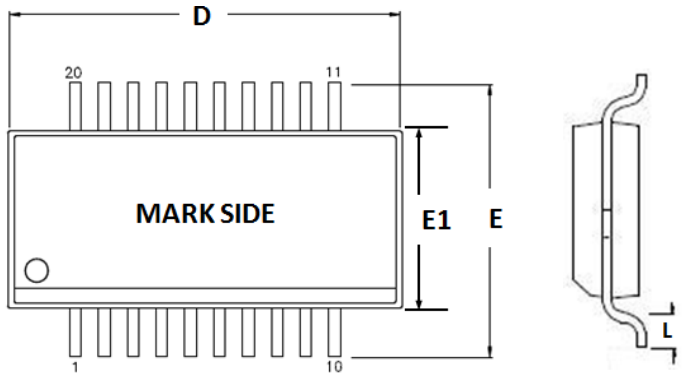
If the sink device doesn't support QC 2.0/3.0, the FP6606AC will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than VDAT(REF) and the output default voltage 5V is also applied.

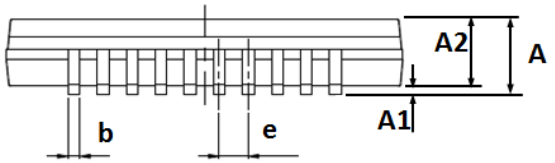
Data Line Protection

When DPx/DNx pin is touched by the external power in abnormal situation, the D+/D− pin of both sink device and source device may be damaged. In order to protect the DPx/DNx pin of the devices from damage in abnormal situation, the FP6606AC will return the output voltage to default output voltage 5V when the voltage of DPx/DNx pin is higher than 4V.

Outline Information

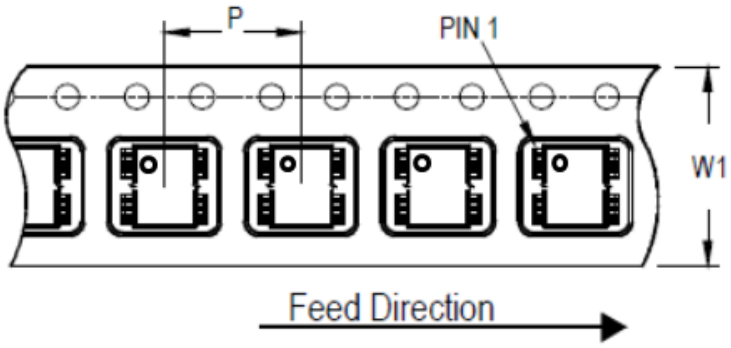
SSOP(150mil)-20L Package (Unit: mm)

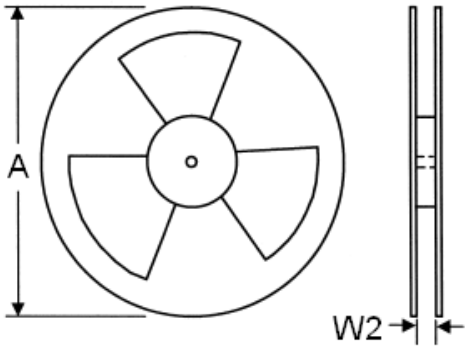




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.34	1.76
A1	0.10	0.26
A2	1.30	1.50
E	5.79	6.20
D	8.55	8.75
L	0.40	1.27
b	0.20	0.31
e	0.635 BSC	
E1	3.80	4.00

Carrier dimensions

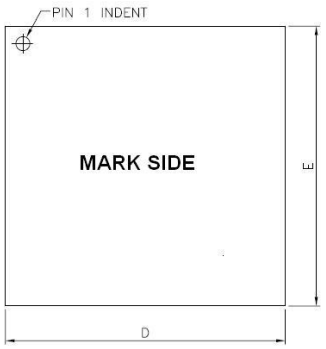


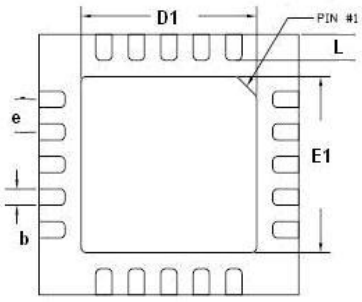


Tape Size (W1)mm	Pocket Pitch (P)mm	Reel Size (A)		Reel Width (W2)mm	Empty Cavity Length(mm)	Units per Reel
		(in)	(mm)			
16	8	13	330	16.4	400~1000	4000

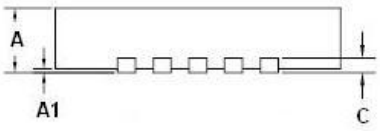
Outline Information (Continued)

TQFN-20L 3mm×3mm (pitch 0.4mm) Package (Unit: mm)

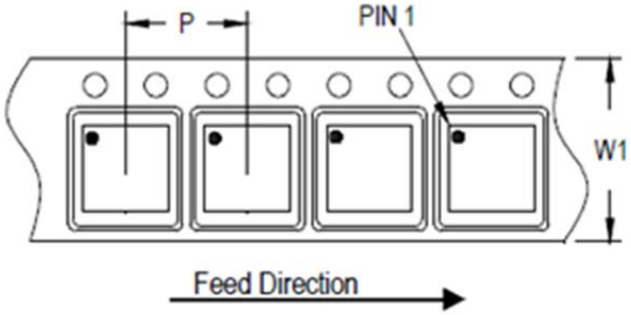


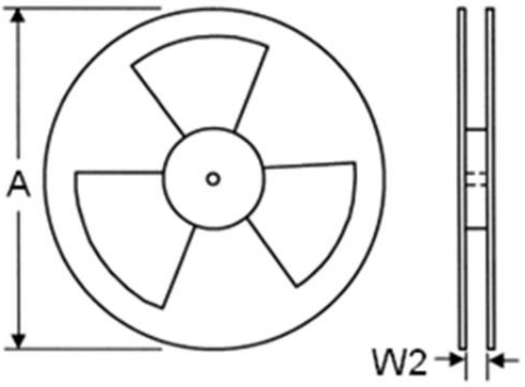


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.18	0.25
E	3.00 BSC	
E1	1.55	1.75
D	3.00 BSC	
D1	1.55	1.75
L	0.30	0.50
b	0.15	0.25
e	0.40 BSC	



Carrier dimensions

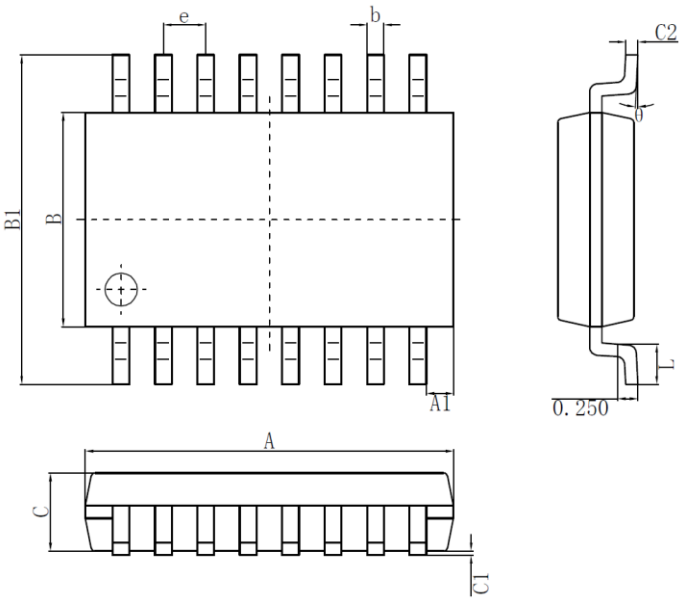




Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000

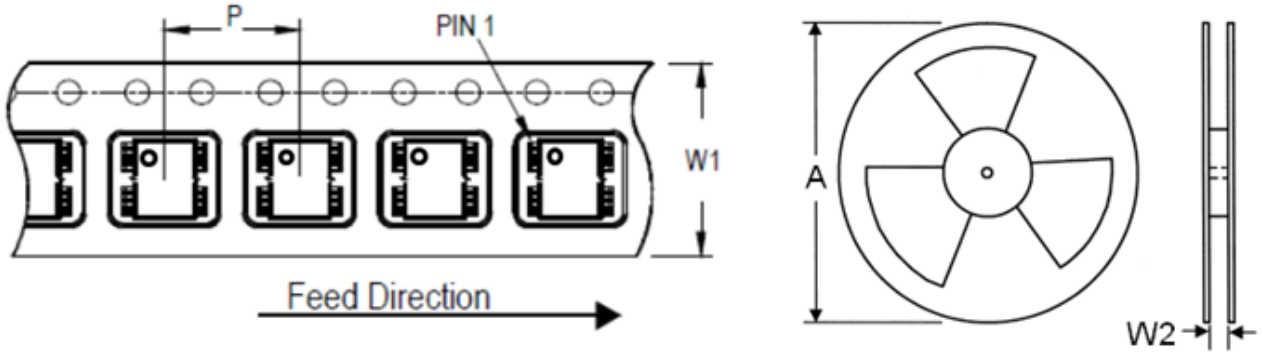
Outline Information (Continued)

CPC-16L Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	4.50	4.70
A1	0.29	0.39
B	2.50	2.70
B1	3.85	4.15
C	0.85	1.05
C1	0.00	0.15
C2	0.15	0.18
e	0.53(BSC)	
b	0.16	0.26
L	0.40	0.60

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A) in	Reel Size (A) mm	Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
12	8	15	380	12.5	300~1000	7,500