

Ultra-Low-Power, Highly Integrated MCU

K32 L2 MCU Family

The K32 L2 MCU family, an expansion of the K32 L series, is designed to deliver a unique balance of core efficiency, low-power modes, memory scalability and mixed signal integration.

OVERVIEW

The K32 L2 MCU family's low-leakage architecture, combined with its power-optimized peripherals and security features (such as cryptographic acceleration technology, cyclic redundancy check and a true random number generator), make it ideal for consumer, industrial and IoT applications requiring a low-priced, power efficient option with longer battery life.

This family includes a low power Arm[®] Cortex[®]-M0+ processor, ideal for applications that require a mix of reduce cost and power with a longer battery life. With options scaling from 64 KB to 512 KB Flash and from 32 kB to 128 kB SRAM, the K32 L2 family offers a wide range of memory resources to fit different application tasks within a small-form factor, low power, and highly integrated design.

The expansion of the K32 L series further demonstrates NXP's investment in secure and power-optimized MCUs for next generation power-conscious and low-leakage applications.

TARGET APPLICATIONS

- Industrial and Building Automation
 - Factory Automation
 - Robotics
 - Building HVAC
 - Security and Access Control
- Consumer
 - Battery-Operated Applications
 - USB Peripherals
 - Low-Power Applications
- Smart home
 - Door Locks
 - Smart Thermostats
 - Lighting Control
 - Security Systems



To reduce development effort and speed time to market, take advantage of NXP's comprehensive offering of development tools and MCUXpresso software which provides an open-source software development kit (SDK), an easy-to-use integrated development environment (IDE) and a comprehensive suite of system configuration tools.

ENABLEMENT

- ▶ Freedom Development Platforms
- Support for NXP's MCUXpresso, IAR Embedded Workbench[®] and Keil IDEs
- Full integration with NXP's MCUXpresso SDK
- Support for multiple RTOSes including FreeRTOS™

ORDERABLE PART NUMBERS

K32 L2 MCU FAMILY BLOCK DIAGRAM



| Product | | Memory | | Security | | | Package | |
|---------------|--------------------|------------|-----------|--------------|--------------|--------------|------------|-------------------|
| Part Number | Samples/Production | Flash (kB) | SRAM (kB) | Crypto | CRC | TRNG | Pin count | Package |
| K32L2B11Vxx0A | Q3 2019/Q4 2019 | 64 | 32 | | | | 32, 48, 64 | QFN, LQFP, MAPBGA |
| K32L2B21Vxx0A | Q3 2019/Q4 2019 | 128 | 32 | | | | 32, 48, 64 | QFN, LQFP, MAPBGA |
| K32L2B31Vxx0A | Q3 2019/Q4 2019 | 256 | 32 | | | | 32, 48, 64 | QFN, LQFP, MAPBGA |
| K32L2A31Vxx1A | Q4 2019/Q1 2020 | 256 | 128 | \checkmark | \checkmark | \checkmark | 64, 100 | LQFP |
| K32L2A41Vxx1A | Q4 2019/Q1 2020 | 512 | 128 | \checkmark | \checkmark | \checkmark | 64, 100 | LQFP |

K32 L2 MCU PLATFORM

| Features | Benefits | | | | | |
|---------------------------------|--|--|--|--|--|--|
| Ultra Low Power | Low-power Arm[®] Cortex[®]-M0+ core Multiple low-power modes enabling the reduction of dynamic power consumption Low-power serial peripheral interfaces supporting low-power operation modes without waking up the core | | | | | |
| Memory | 64 - 512 kB of flash memory to address different needs and provide scalability options 32 - 128 kB of SRAM memory 16 - 32 kB of ROM with integrated bootloader | | | | | |
| High Mixed-Signal Integration | Up to 16-bit ADC with configurable resolution, sample time and conversion speed/power and single or differential input mode operations support 12-bit DAC with DMA support 1.2 V high-accuracy internal voltage reference High-speed comparator with internal 6-bit DAC | | | | | |
| Connectivity and Communications | USB 2.0 Full Speed integrated with low-voltage regulator 4-8 channel DMA for peripheral and memory servicing with reduced CPU loading Up to three I2C, up to three LPUART and up to three SPI serial interfaces with DMA support FlexIO interface with capability of emulating multiple serial interfaces | | | | | |
| Security* | Cryptographic acceleration unit supporting acceleration of DES, 3DES, AES, MD5, SHA-1 and SHA-256 algorithms Hardware accelerated True Random Number Generator | | | | | |
| HMI | Capacitive touch sense interface supporting up to 16 external electrodes* GPIO with pin interrupt support | | | | | |
| Package Options | Small, high pin-count package options including: BGA, LQFP and QFN | | | | | |
| Comprehensive Enablement | Complete development hardware, software stacks, drivers and RTOS for fast time to market and easy design | | | | | |
| *K32 L2A devices only | | | | | | |

www.nxp.com/K32L2

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