HIP4020

Half Amp Full Bridge Power Driver for Small 3V, 5V, and 12V DC Motors

In the Functional Block Diagram of the HIP4020, the four switches and a load are arranged in an H-configuration so that the drive voltage from terminals OUTA and OUTB can be cross-switched to change the direction of current flow in the load. This is commonly known as 4-quadrant load control. As shown Figure 1, switches Q_1 and Q_4 are conducting or in an ON state when current flows from V_{DD} through Q_1 to the load, and then through Q_4 to terminal V_{SSB}; where load terminal OUTA is at a positive potential with respect to OUTB. Switches Q_1 and Q_4 are operated synchronously by the control logic. The control logic switches Q_3 and Q_2 to an open or OFF state when Q_1 and Q_4 are switched ON. To reverse the current flow in the load, the switch states are reversed where Q_1 and Q_4 are OFF while Q_2 and Q_3 are ON. Consequently, current then flows from V_{DD} through Q_3, through the load, and through Q_2 to terminal V_{SSA}, and load terminal OUTB is then at a positive potential with respect to OUTA.

Terminals ENA and ENB are ENABLE inputs for the Logic A and B Input Controls. The ILF output is an Overcurrent Limit Fault Flag Output and indicates a fault condition for either Output A or B or both. The V_{DD} and V_{SS} are the Power Supply reference terminals for the A and B Control Logic Inputs and ILF Output. While the V_{DD} positive power supply terminal is internally connected to each bridge driver, the V_{SSA} and V_{SSB} power supply terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. The use of level shifters in the gate drive circuitry to the NMOS (low-side) output stages allows controlled level shifting of the output drive relative to ground.

Features

- Two independent controlled complementary MOS power output half H-drivers (full-bridge) for nominal 3V to 12V power supply operation
- Split ±voltage power supply option for output drivers
- Load switching capabilities to 0.5A
- Single supply range +2.5V to +15V
- Low standby current
- CMOS/TTL compatible input logic
- Over-temperature shutdown protection
- Overcurrent limit protection
- Overcurrent fault flag output
- Direction, braking and PWM control
- Pb-free plus anneal (RoHS compliant)

Applications

- DC motor driver
- Relay and solenoid drivers
- Stepper motor controller
- Air core gauge instrument driver
- Speedometer displays
- Tachometer displays
- Remote power switch
- Battery operated switch circuits
- Logic and microcontroller operated switch

Related Literature

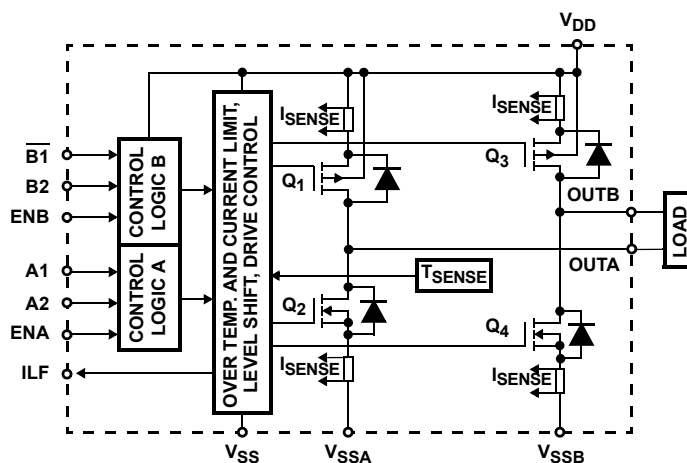For a full list of related documents, visit our website:

- HIP4020 device page
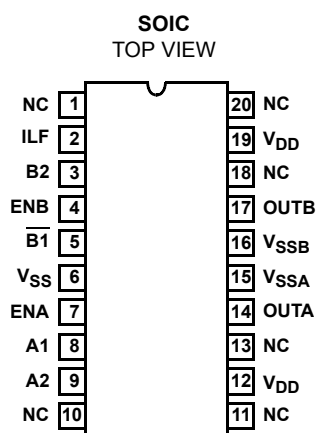

FIGURE 1. BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
HIP4020IBZ	HIP4020IBZ	-40 to 85	-	20 Ld SOIC	M20.3
HIP4020IBZT	HIP4020IBZ	-40 to 85	1k	20 Ld SOIC	M20.3

NOTES:

1. See TB347 for details about reel specifications.

2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), see the HIP4020 device page. For more information about MSL, see TB363.

Pinout

SOIC
TOP VIEW

NC	1	20 NC
ILF	2	19 V_{DD}
B2	3	18 NC
ENB	4	17 OUTB
$\overline{B1}$	5	16 V_{SSB}
V_{SS}	6	15 V_{SSA}
ENA	7	14 OUTA
A1	8	13 NC
A2	9	12 V_{DD}
NC	10	11 NC

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
12, 19	V_{DD}	Positive power supply pins; internally common and externally connect to the same positive supply (V+).
15	V_{SSA}	Negative power supply pin; negative or ground return for Switch Driver A; externally connect to the supply (V-).
16	V_{SSB}	Negative power supply pin; negative or Ground return for Switch Driver B; externally connect to the supply (V-).
6	V_{SS}	Common ground pin for the Input Logic Control circuits. It can be used as a common ground with V_{SSA} and V_{SSB}.
8, 5	A1, $\overline{B1}$	Input pins used to control the direction of output load current to/from OUTA and OUTB, respectively. When connected, A1 and $\overline{B1}$ can be controlled from the same logic signal to change the directional rotation of a motor.
9, 3	A2, B2	Input pins used to force a low state on OUTA and OUTB, respectively. When connected, A2 and B2 can be controlled from the same logic signal to activate dynamic braking of a motor.
7, 4	ENA, ENB	Input pins used to enable Switch Driver A and Switch Driver B, respectively. When low, the respective output is in a high impedance (Z) off-state. Since each switch driver is independently controlled, OUTA and OUTB can be separately PWM controlled as half H-switch drivers.
14, 17	OUTA, OUTB	Respectively, Switch Driver A and Switch Driver B output pins.
2	ILF	Current limiting fault output flag pin; when in a high logic state, signifies that Switch Driver A or B, or both are in a Current Limiting Fault mode.

Absolute Maximum Ratings

Supply Voltage; V_{DD} to V_{SS} or V_{SSA} or V_{SSB} . . . .+15V
Negative Output Supply Voltage, (V_{SSA}, V_{SSB}) . . . . (Note 4)
DC Logic Input Voltage (Each Input) . . . (V_{SS} -0.5V) to (V_{DD} +0.5V)
DC Logic Input Current (Each Input) . . . .±15mA
ILF Fault Output Current. . . . .±15mA
Output Load Current, (Self Limiting, see Elec. Spec.) . . . . ±$I_{O(LIMIT)}$

Operating Conditions T_A = 25°C

Typical Operating Supply Voltage Range, V_{DD} . . . .   +3 to +12V
Low Voltage Logic Retention, Minimum V_{DD}. . . . .+2V
Idle Supply Current; No Load, V_{DD} = +5V. 0.8mA
Typical P+N Channel $r_{DS(ON)}$, V_{DD} = +5V, 0.5A Load 2Ω

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} (°C/W)
    Plastic SOIC Package   105
Maximum Storage Temperature Range. . . . .-65°C to 150°C
Maximum Junction Temperature . . . . 150°C
Pb-Free Reflow Profile. . . . . see TB493

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

4. V_{SS} is the required common ground reference for the logic input switching. The load currents may be switched positive and negative in reference to the V_{SS} common ground by using a split supply for V_{DD} (positive) to V_{SSA} and V_{SSB} (negative). For an uneven split in the supply voltage, the maximum negative output supply voltage for V_{SSA} and V_{SSB} is limited by the maximum V_{DD} to V_{SSA} or V_{SSB} ratings. Since the V_{DD} pins are internally tied together, the voltage on each V_{DD} pins must be equal and common.

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = 25°C, V_{DD} = +5V, V_{SSA} = V_{SSB} = V_{SS} = 0V, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	I_{LEAK}	V_{DD} = +15V	-	-	25	nA
Low Level Input Voltage	V_{IL}		V_{SS}	-	0.8	V
High Level Input Voltage	V_{IH}		2	-	V_{DD}	V
ILF Output Low, Sink Current	I_{OH}	V_{OUT} = 0.4V, V_{DD} = +12V	15	-	-	mA
ILF Output High, Source Current	I_{OL}	V_{OUT} = 11.6V, V_{DD} = +12V	-	-	-15	mA
Input Capacitance	C_{IN}		-	2	-	pF
P-Channel $r_{DS(ON)}$, Low Supply Voltage	$r_{DS(ON)}$	V_{DD} = +3V, I_{SOURCE} = 250mA	-	1.6	2.5	Ω
N-Channel $r_{DS(ON)}$, Low Supply Voltage	$r_{DS(ON)}$	V_{DD} = +3V, I_{SINK} = 250mA	-	1	1.5	Ω
P-Channel $r_{DS(ON)}$, High Supply Voltage	$r_{DS(ON)}$	V_{DD} = +12V, I_{SOURCE} = 400mA	-	0.6	1.2	Ω
N-Channel $r_{DS(ON)}$, High Supply Voltage	$r_{DS(ON)}$	V_{DD} = +12V, I_{SINK} = 400mA	-	0.5	1.1	Ω
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$	V_{DD} = +6V, V_{SS} = 0V, V_{SSA} = V_{SSB} = -6V	480	625	1500	mA
OUTA, OUTB Sink Current Limiting	-$I_{O(LIMIT)}$	V_{DD} = +6V, V_{SS} = 0V, V_{SSA} = V_{SSB} = -6V	480	800	1500	mA
Idle Supply Current; No Load	I_{DD}		-	0.8	1.5	mA
OUTA, OUTB Voltage High	V_{OH}	I_{SOURCE} = 450mA	4.2	4.5	-	V
OUTA, OUTB Voltage Low	V_{OL}	I_{SINK} = 450mA	-	0.4	0.6	V
OUTA, OUTB Voltage High	V_{OH}	V_{DD} = +3V, I_{SOURCE} = 250mA	2.415	2.6	-	V
OUTA, OUTB Voltage Low	V_{OL}	V_{DD} = +3V, I_{SINK} = 250mA	-	0.25	0.375	V
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$	V_{DD} = +12V	480	625	1500	mA
OUTA, OUTB Sink Current Limiting	-$I_{O(LIMIT)}$	V_{DD} = +12V	480	800	1500	mA
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$	V_{DD} = +3V	480	625	1500	mA
OUTA, OUTB Sink Current Limiting	-$I_{O(LIMIT)}$	V_{DD} = +3V	480	800	1500	mA
Thermal Shutdown	T_{SD}		-	145	-	°C

Electrical Specifications $T_A = 25°C$, $V_{DD} = +5V$, $V_{SSA} = V_{SSB} = V_{SS} = 0V$, unless otherwise specified   **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response Time: V_{EN} to V_{OUT} Turn-On: Prop Delay	t_{PLH}	$I_O = 0.5A$ (Note 6)	-	2.5	-	µs
Rise Time	t_r		-	4	-	µs
Turn-Off: Prop Delay	t_{PHL}		-	0.1	-	µs
Fall Time	t_f		-	0.1	-	µs

NOTE:

6. See the Truth Table and the V_{EN} to V_{OUT} Switching Waveforms. Current I_O refers to I_{OUTA} or I_{OUTB} as the output load current. Note that ENA controls OUTA and ENB controls OUTB. Each Half H-switch has independent control from the respective A1, A2, ENA or $\overline{B1}$, B2, ENB inputs. See the terminal Information table for external pin connections to establish mode control switching. Figure 2 on page 4 shows a typical application circuit used to control a DC Motor.
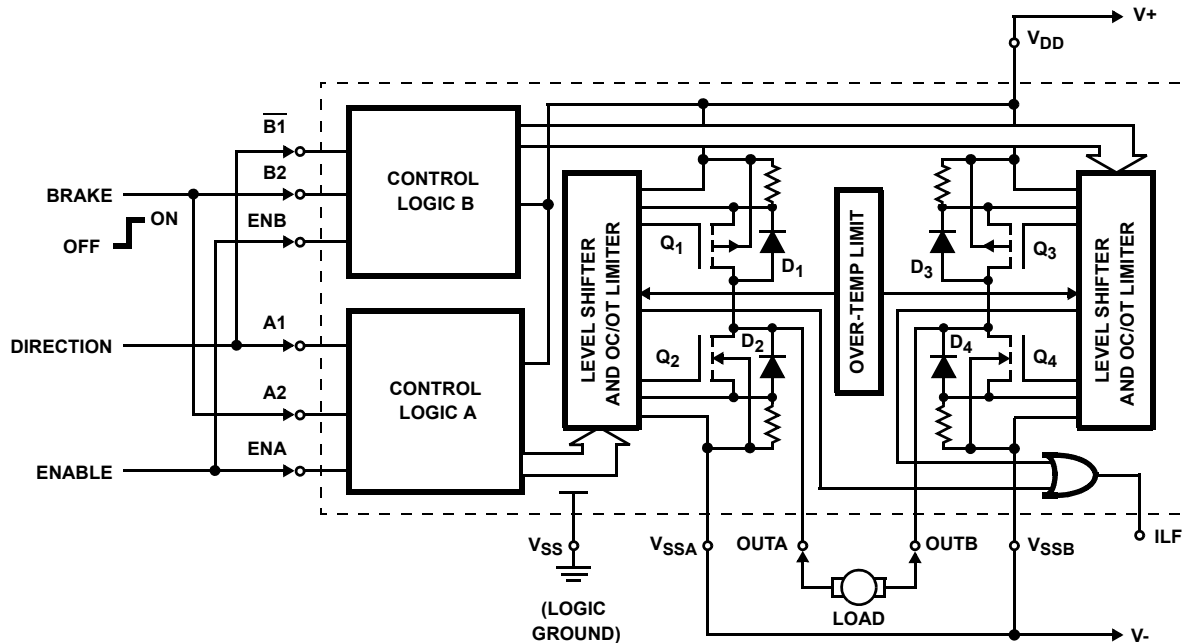
FIGURE 2. TYPICAL MOTOR CONTROL APPLICATION CIRCUIT SHOWING DIRECTIONAL AND BRAKING CONTROL

TRUTH TABLE

SWITCH DRIVER A				SWITCH DRIVER B			
INPUTS			OUTPUT	INPUTS			OUTPUT
A1	A2	ENA	OUTA	$\overline{B1}$	B2	ENB	OUTB
H	L	H	OH	L	L	H	OH
L	L	H	OL	H	L	H	OL
H	H	H	OL	L	H	H	OL
L	H	H	OL	H	H	H	OL
X	X	L	Z	X	X	L	Z

L = Low logic level; H = High logic level
Z = High Impedance (off state)
OH = Output High (sourcing current to the output terminal)
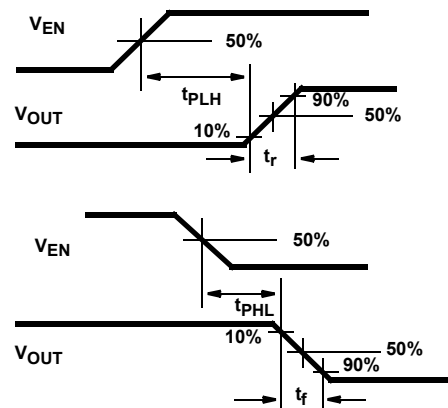OL = Output Low (sinking current from the output terminal)
X = Do not Care

FIGURE 3. SWITCHING WAVEFORMS

Application

The HIP4020 is designed to detect load current feedback from sampling resistors of low value in the source connections of the output drivers to V_{DD}, V_{SSA} and V_{SSB} (see Figure 2). When the sink or source current at OUTA or OUTB exceeds the preset OC (Overcurrent) limiting value of 550mA typical, the current is held at the limiting value. If the Over-Temperature (OT) Shutdown Protection limit is exceeded, temperature sensing BiMOS circuits limit the junction temperature to 150°C typical.

Figure 2 shows the Full H-switch in a small motor-drive application. The left (A) and right (B) H-switch's are controlled from the A and B inputs using the A and B control logic to the MOS output transistors Q_1, Q_2, Q_3, and Q_4. The circuit is intended to safely start, stop, and control rotational direction for a motor requiring no more than 0.5A of supply current. The stop function includes a dynamic braking feature.

With the enable inputs low, the MOS transistors Q_1 and Q_3 are OFF; which cuts-off supply current to OUTA and OUTB. With the brake terminal low and enable inputs high, either Q_1 and Q_4 or Q_3 and Q_2 are driven into conduction by the direction input control terminal. The MOS output transistor pair chosen for conduction is determined by the logic level applied to the direction control; resulting in either Clockwise (CW) or Counter-Clockwise (CCW) shaft rotation.

When the brake terminal is switched high (while holding the enable input high), the gates of both Q_2 and Q_4 are driven high. Current flowing through Q_2 (from the motor terminal OUTA) at the moment of dynamic braking continues to flow through Q_2 to the V_{SSA} and V_{SSB} external connection, and then continues through diode D_4 to the motor terminal OUTB. As such, the resistance of the motor winding (and the

series-connected path) dissipates the kinetic energy stored in the system. Reversing rotation, current flowing through Q_4 (from the motor terminal OUTB), at the moment of dynamic braking, would continue to flow through Q_4 to the V_{SSB} and V_{SSA} tie, and then continue through diode D_2 to the motor terminal OUTA, to dissipate the stored kinetic energy as previously described.

Where V_{DD} to V_{SS} are the power supply reference terminals for the control logic, the lowest practical supply voltage for proper logic control should be no less than 2.0V. The V_{SSA} and V_{SSB} terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. However, the maximum supply level from V_{DD} to V_{SSA} or V_{SSB} must not be greater than the absolute maximum supply voltage rating.

Terminals A1, $\overline{B1}$, A2, B2, ENA, and ENB are internally connected to protection circuits intended to guard the CMOS gate-oxides against damage due to electrostatic discharge. (See Figure 4) Inputs ENA, ENB, A1, $\overline{B1}$, A2, and B2 have protection and level converters for TTL or CMOS Input Logic. These inputs are designed to typically provide ESD protection up to 2kV. However, these devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.
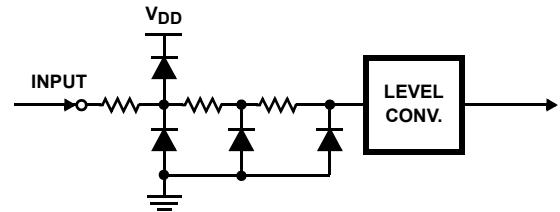

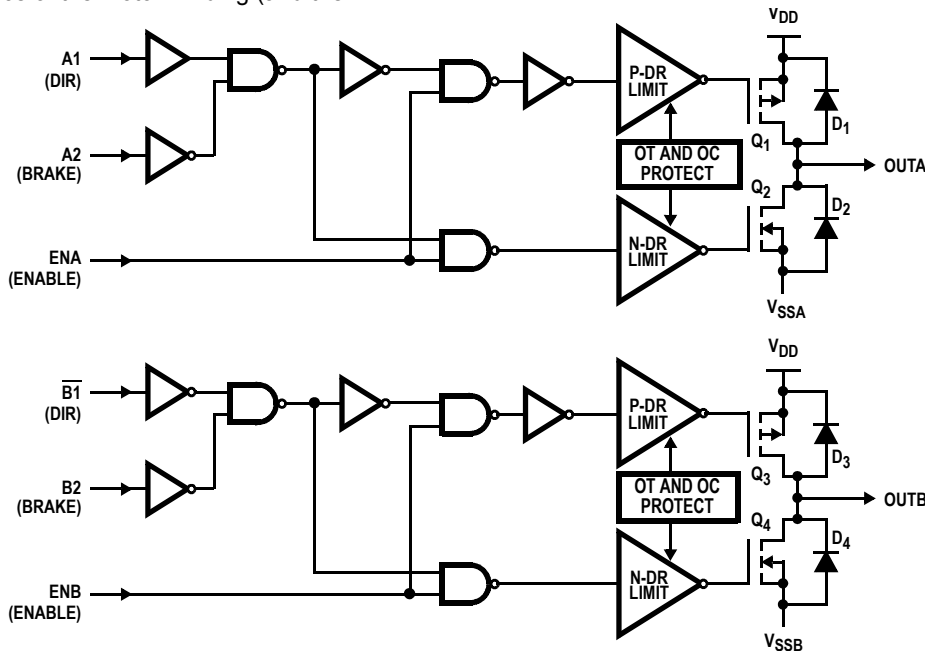**FIGURE 4. LOGIC INPUT ESD INTERFACE PROTECTION**

FIGURE 5. EQUIVALENT CONTROL LOGIC A AND B SHOWN DRIVING THE OUTA AND OUTB OUTPUT DRIVERS

Typical Performance Curves

FIGURE 6. TYPICAL CHARACTERISTIC OF THE P-MOSFET OUTPUT DRIVER DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE, $T_{AMBIENT}$ = 25°C

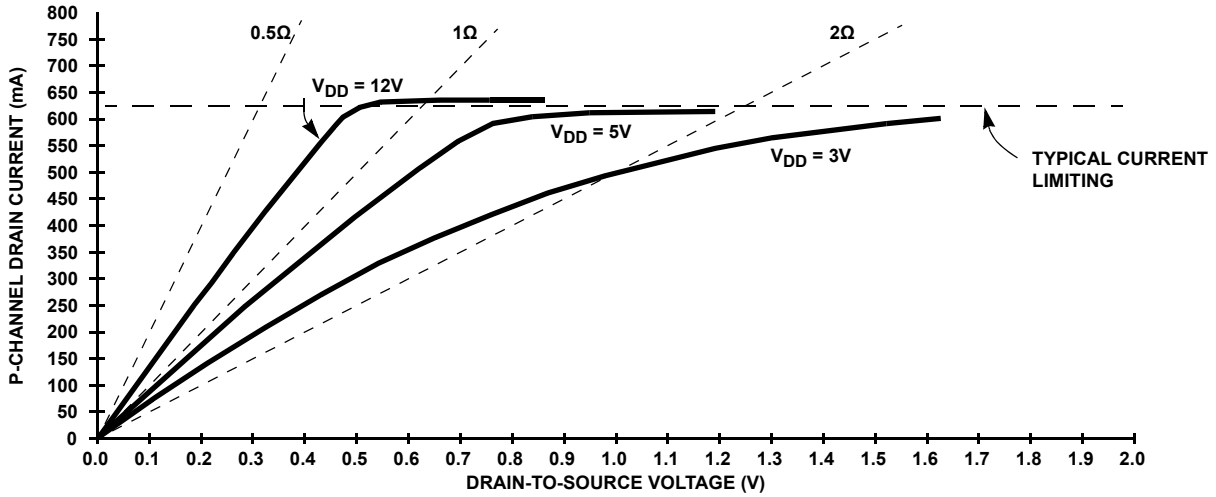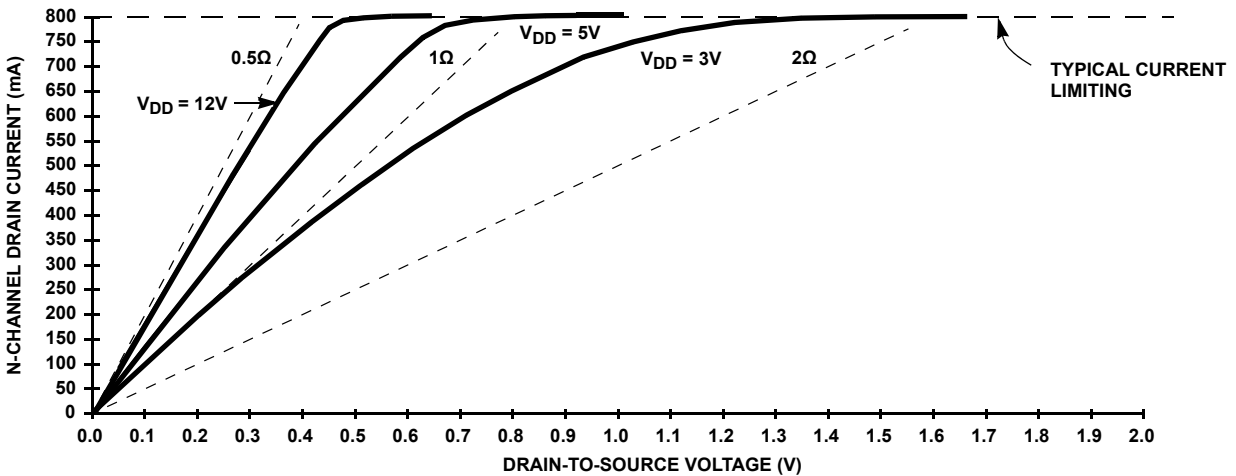FIGURE 7. TYPICAL CHARACTERISTIC OF THE N-MOSFET OUTPUT DRIVER DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE, $T_{AMBIENT}$ = 25°C
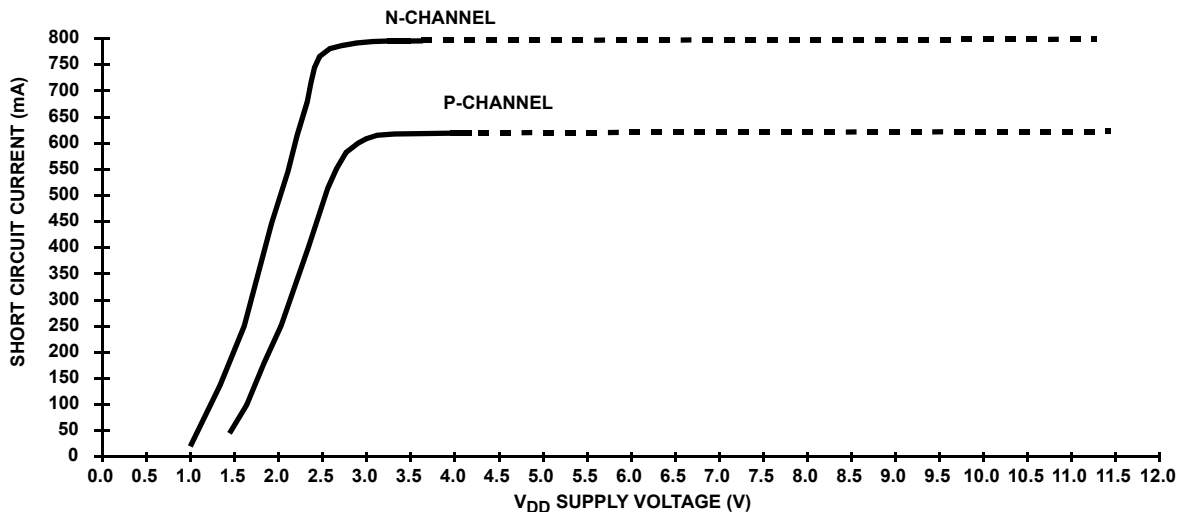

FIGURE 8. TYPICAL CHARACTERISTIC OF THE P AND N OUTPUT DRIVER SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE, $T_{AMBIENT}$ = 25°C
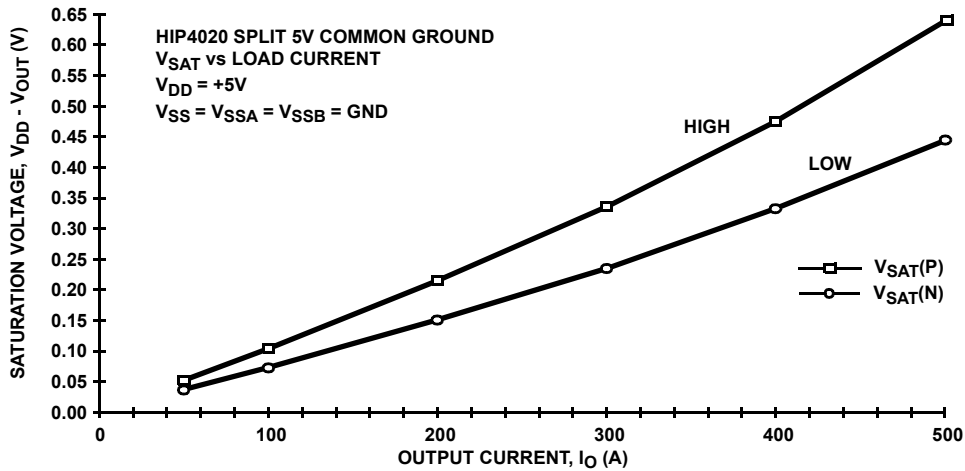
Typical Performance Curves (Continued)

FIGURE 9. TYPICAL CHARACTERISTIC OF SATURATION VOLTAGE vs OUTPUT CURRENT USING A +5V SUPPLY, $T_{AMBIENT}$ = 25°C
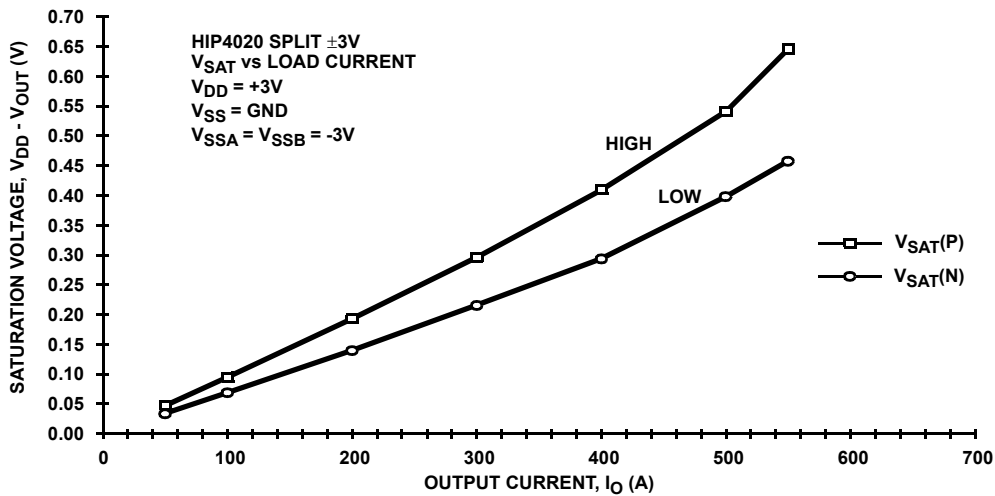
FIGURE 10. TYPICAL CHARACTERISTIC OF SATURATION VOLTAGE vs OUTPUT CURRENT USING A ±3V SPLIT SUPPLY, OUTPUT REFERENCE EQUAL LOGIC GROUND, $T_{AMBIENT}$ = 25°C
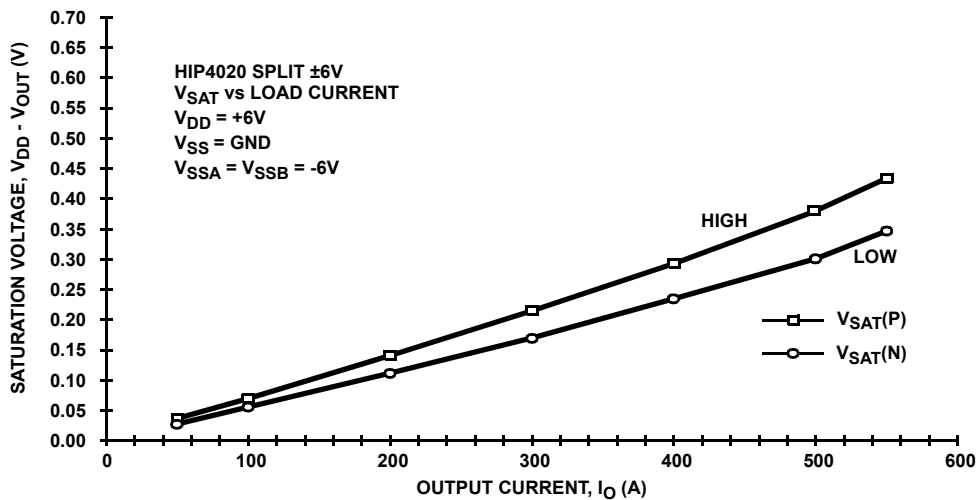

FIGURE 11. TYPICAL CHARACTERISTIC OF SATURATION VOLTAGE vs OUTPUT CURRENT USING A ±6V SPLIT SUPPLY, OUTPUT REFERENCE EQUAL LOGIC GROUND, $T_{AMBIENT}$ = 25°C

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE	REVISION	CHANGE
Feb 8, 2019	FN3976.5	Added Related Literature section. Updated Ordering information table by removing retired part, added new notes, and moved to page 2. Moved Pin Descriptions below Pinout section. Added TB493 reference under Thermal Information section. Moved Note 6 to end of EC table. Updated P-Channel r$_{DS(ON)}$, Low Supply Voltage maximum specification from 2.1 to 2.5. Removed About Intersil section. Updated disclaimer.
Sep17, 2015	FN3976.4	- Updated Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M20.3 to latest revision changes are as follow: Top View: Corrected "7.50 BSC" to "7.60/7.40" (no change from rev 2; error was introduced in conversion) Changed "10.30 BSC" to "10.65/10.00" (no change from rev 2; error was introduced in conversion) Side View: Changed "12.80 BSC" to "13.00/12.60" (no change from rev 2; error was introduced in conversion) Changed "2.65 max" to "2.65/2.35" (no change from rev 2; error was introduced in conversion) Changed Note 1 from "ANSI Y14.5M-1982." to "ASME Y14.5M-1994"

Package Outline Drawing

M20.3
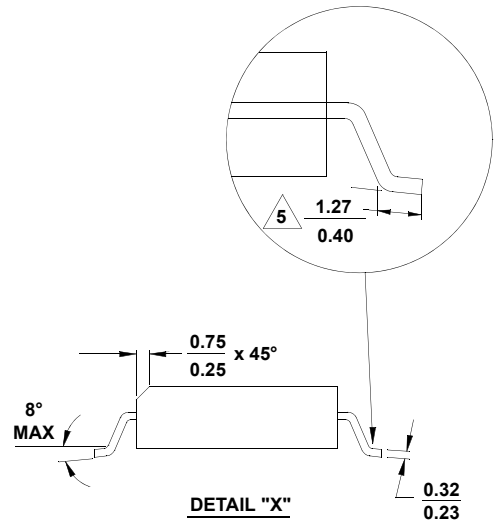20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)
Rev 3, 2/11
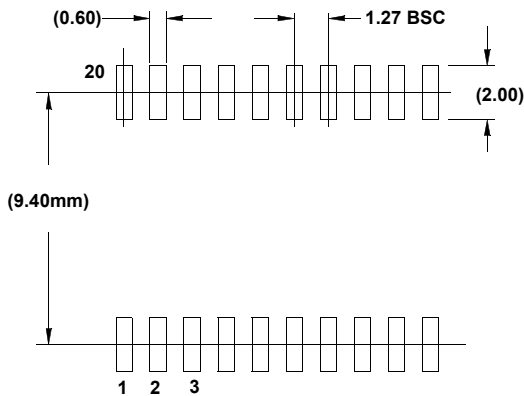
For the most recent package outline drawing, see M20.3.
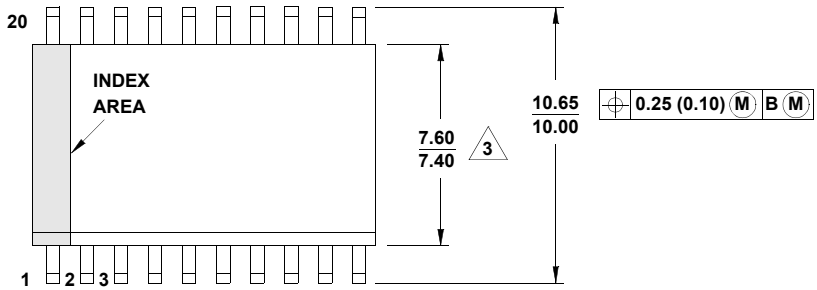
TOP VIEW
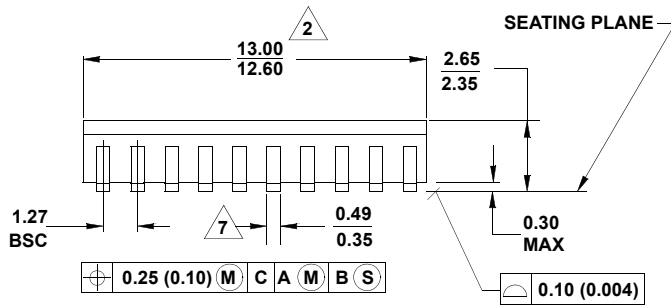
SIDE VIEW

DETAIL "X"

TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

3. Dimension does not include interlead lash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

5. Dimension is the length of terminal for soldering to a substrate.

6. Terminal numbers are shown for reference only.

7. The lead width as measured 0.36mm (0.14 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)

8. Controlling dimension: MILLIMETER.

9. Dimensions in ( ) for reference only.

10. JEDEC reference drawing number: MS-013-AC.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard":   Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/