RL78/G1A

RENESAS MCU

R01DS0151EJ0210
Rev.2.10
Nov 30, 2016

Combines Multi-channel 12-Bit A/D Converter, True Low Power Platform (as low as 66 µA/MHz, and 0.57 µA for RTC + LVD), 1.6 V to 3.6 V operation, 16 to 64 Kbyte Flash, 41 DMIPS at 32 MHz

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 1.6 V to 3.6 V operation from a single supply
- Stop (RAM retained): 0.23 µA, (LVD enabled): 0.31 µA
- Halt (RTC + LVD): 0.57 µA
- Snooze: 0.7 mA (UART), 0.6 mA (ADC)
- Operating: 66 µA/MHz

16-bit RL78 CPU Core
- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory
- Density: 16 KB to 64 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data Flash with background operation
- Data flash size: 4 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 3.6 V

RAM
- 2 KB to 4 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 32 MHz with +/– 1% accuracy over voltage (1.8 V to 3.6 V) and temperature (–20 °C to +85 °C)
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 12 setting options (Interrupt and/or reset function)

Data Memory Access (DMA) Controller
- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Up to 6 x I^2C master
- Up to 1 x I^2C multi-master
- Up to 6 x CSI/SPI (7-, 8-bit)
- Up to 3 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

Extended-Function Timers
- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog
- ADC: Up to 28 channels, 12-bit resolution, 3.375 µs conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test

General Purpose I/O
- 3.6 V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature
- Standard: –40 °C to +85 °C
- Extended: −40 °C to +105 °C

Package Type and Pin Count
From 3 mm x 3 mm to 10 mm x 10 mm
QFP: 48, 64
QFN: 32, 48
LGA: 25
BGA: 64

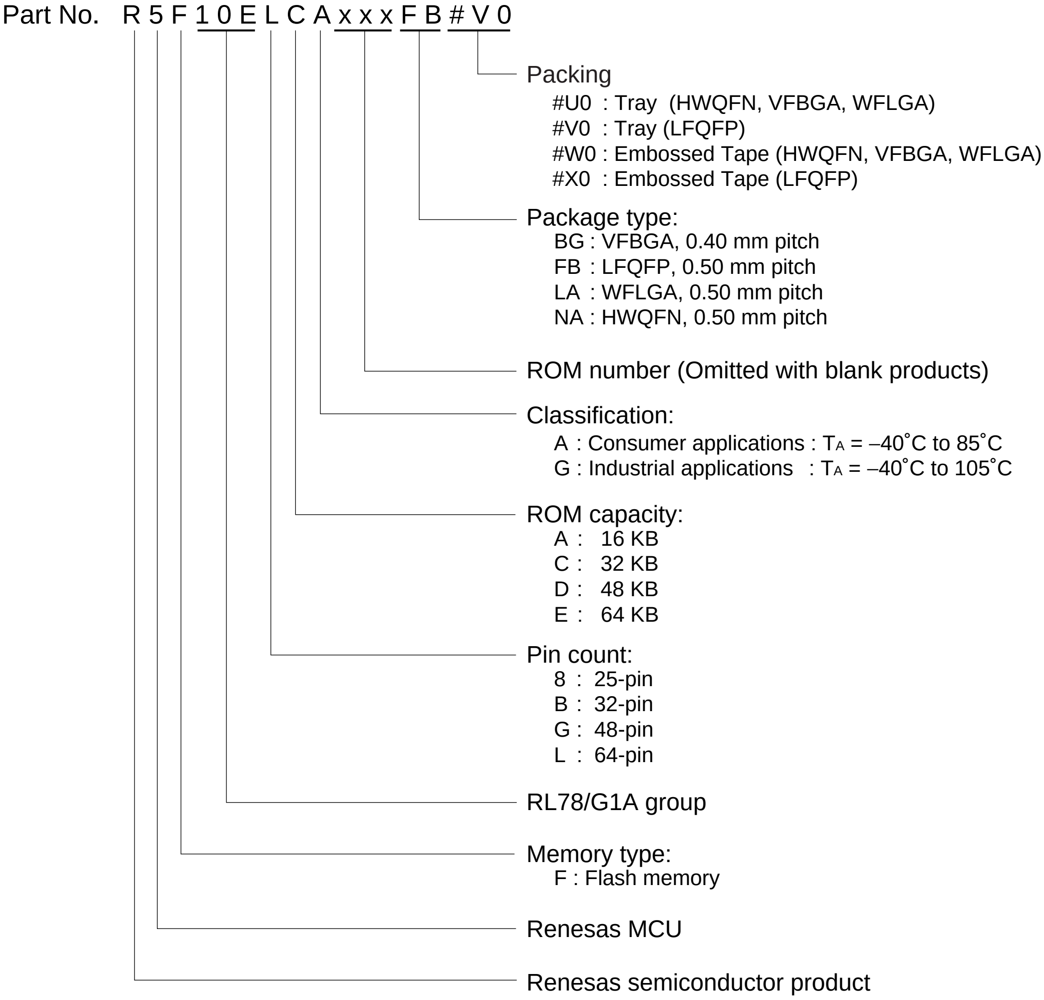
○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1A			
			25 pins	32 pins	48 pins	64 pins
64 KB	4 KB	4 KB Note	R5F10E8E	R5F10EBE	R5F10EGE	R5F10ELE
48 KB	4 KB	3 KB	R5F10E8D	R5F10EBD	R5F10EGD	R5F10ELD
32 KB	4 KB	2 KB	R5F10E8C	R5F10EBC	R5F10EGC	R5F10ELC
16 KB	4 KB	2 KB	R5F10E8A	R5F10EBA	R5F10EGA	–

Note This is about 3 KB when the self-programming function and data flash function are used. (For details, see **3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T$_A$ = –40 to +105°C)**)

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1A



Part No. R 5 F 1 0 E L C A x x x F B # V 0

Packing
#U0 : Tray (HWQFN, VFBGA, WFLGA)
#V0 : Tray (LFQFP)
#W0 : Embossed Tape (HWQFN, VFBGA, WFLGA)
#X0 : Embossed Tape (LFQFP)

Package type:
BG : VFBGA, 0.40 mm pitch
FB : LFQFP, 0.50 mm pitch
LA : WFLGA, 0.50 mm pitch
NA : HWQFN, 0.50 mm pitch

ROM number (Omitted with blank products)

Classification:
A : Consumer applications : T_A = –40°C to 85°C
G : Industrial applications : T_A = –40°C to 105°C

ROM capacity:
A : 16 KB
C : 32 KB
D : 48 KB
E : 64 KB

Pin count:
8 : 25-pin
B : 32-pin
G : 48-pin
L : 64-pin

RL78/G1A group

Memory type:
F : Flash memory

Renesas MCU

Renesas semiconductor product

Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

<R> **Table 1-1. List of Ordering Part Numbers**

Pin count	Package	Fields of Application[Note]	Ordering Part Number
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	A	R5F10E8AALA#U0, R5F10E8CALA#U0, R5F10E8DALA#U0, R5F10E8EALA#U0, R5F10E8AALA#W0, R5F10E8CALA#W0, R5F10E8DALA#W0, R5F10E8EALA#W0
		G	R5F10E8AGLA#U0, R5F10E8CGLA#U0, R5F10E8DGLA#U0, R5F10E8EGLA#U0, R5F10E8AGLA#W0, R5F10E8CGLA#W0, R5F10E8DGLA#W0, R5F10E8EGLA#W0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F10EBAANA#U0, R5F10EBCANA#U0, R5F10EBDANA#U0, R5F10EBEANA#U0, R5F10EBAANA#W0, R5F10EBCANA#W0, R5F10EBDANA#W0, R5F10EBEANA#W0
		G	R5F10EBAGNA#U0, R5F10EBCGNA#U0, R5F10EBDGNA#U0, R5F10EBEGNA#U0, R5F10EBAGNA#W0, R5F10EBCGNA#W0, R5F10EBDGNA#W0, R5F10EBEGNA#W0
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F10EGAAFB#V0, R5F10EGCAFB#V0, R5F10EGDAFB#V0, R5F10EGEAFB#V0, R5F10EGAAFB#X0, R5F10EGCAFB#X0, R5F10EGDAFB#X0, R5F10EGEAFB#X0
		G	R5F10EBAGNA#V0, R5F10EBCGNA#V0, R5F10EBDGNA#V0, R5F10EBEGNA#V0, R5F10EBAGNA#X0, R5F10EBCGNA#X0, R5F10EBDGNA#X0, R5F10EBEGNA#X0
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F10EGAANA#U0, R5F10EGCANA#U0, R5F10EGDANA#U0, R5F10EGEANA#U0, R5F10EGAANA#W0, R5F10EGCANA#W0, R5F10EGDANA#W0, R5F10EGEANA#W0
		G	R5F10EGAGNA#U0, R5F10EGCGNA#U0, R5F10EGDGNA#U0, R5F10EGEGNA#U0, R5F10EGAGNA#W0, R5F10EGCGNA#W0, R5F10EGDGNA#W0, R5F10EGEGNA#W0
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F10ELCAFB#V0, R5F10ELDAFB#V0, R5F10ELEAFB#V0, R5F10ELCAFB#X0, R5F10ELDAFB#X0, R5F10ELEAFB#X0
		G	R5F10ELCGFB#V0, R5F10ELDGFB#V0, R5F10ELEGFB#V0, R5F10ELCGFB#X0, R5F10ELDGFB#X0, R5F10ELEGFB#X0
	64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)	A	R5F10ELCABG#U0, R5F10ELDABG#U0, R5F10ELEABG#U0, R5F10ELCABG#W0, R5F10ELDABG#W0, R5F10ELEABG#W0
		G	R5F10ELCGBG#U0, R5F10ELDGBG#U0, R5F10ELEGBG#U0, R5F10ELCGBG#W0, R5F10ELDGBG#W0, R5F10ELEGBG#W0

<R> **Note** For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1A**.

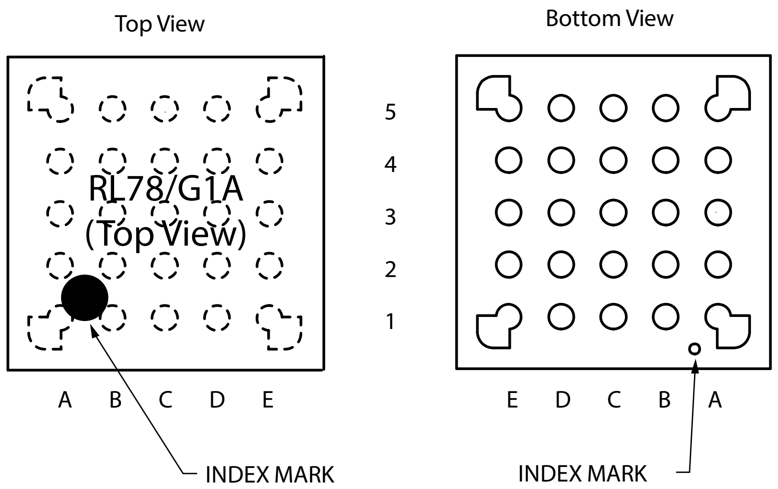
Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 25-pin products

<R>

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)



	A	B	C	D	E	
5	P40/TOOL0	$\overline{\text{RESET}}$	P03/ANI16/ RxD1/TO00/ (KR1)	P23/ANI3/ (KR3)	AV$_{SS}$	5
4	P122/X2/ EXCLK	P137/INTP0	P02/ANI17/ TxD1/TI00/ (KR0)	P22/ANI2/ (KR2)	AV$_{DD}$	4
3	P121/X1	V$_{DD}$	P21/ANI1/ AV$_{REFM}$	P11/ANI20/ SI00/SDA00/ RxD0/ TOOLRxD	P10/ANI18/ SCK00/SCL00	3
2	REGC	V$_{SS}$	P30/ANI27/ SCK11/SCL11/ INTP3	P51/ANI25/ SO11/INTP2	P50/ANI26/ SI11/SDA11 INTP1	2
1	P60/SCLA0	P61/SDAA0	P31/ANI29/TI03/ TO03/PCLBUZ0 /INTP4	P12/ANI21/ SO00/TxD0/ TOOLTxD	P20/ANI0/ AV$_{REFP}$	1
	A	B	C	D	E	

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

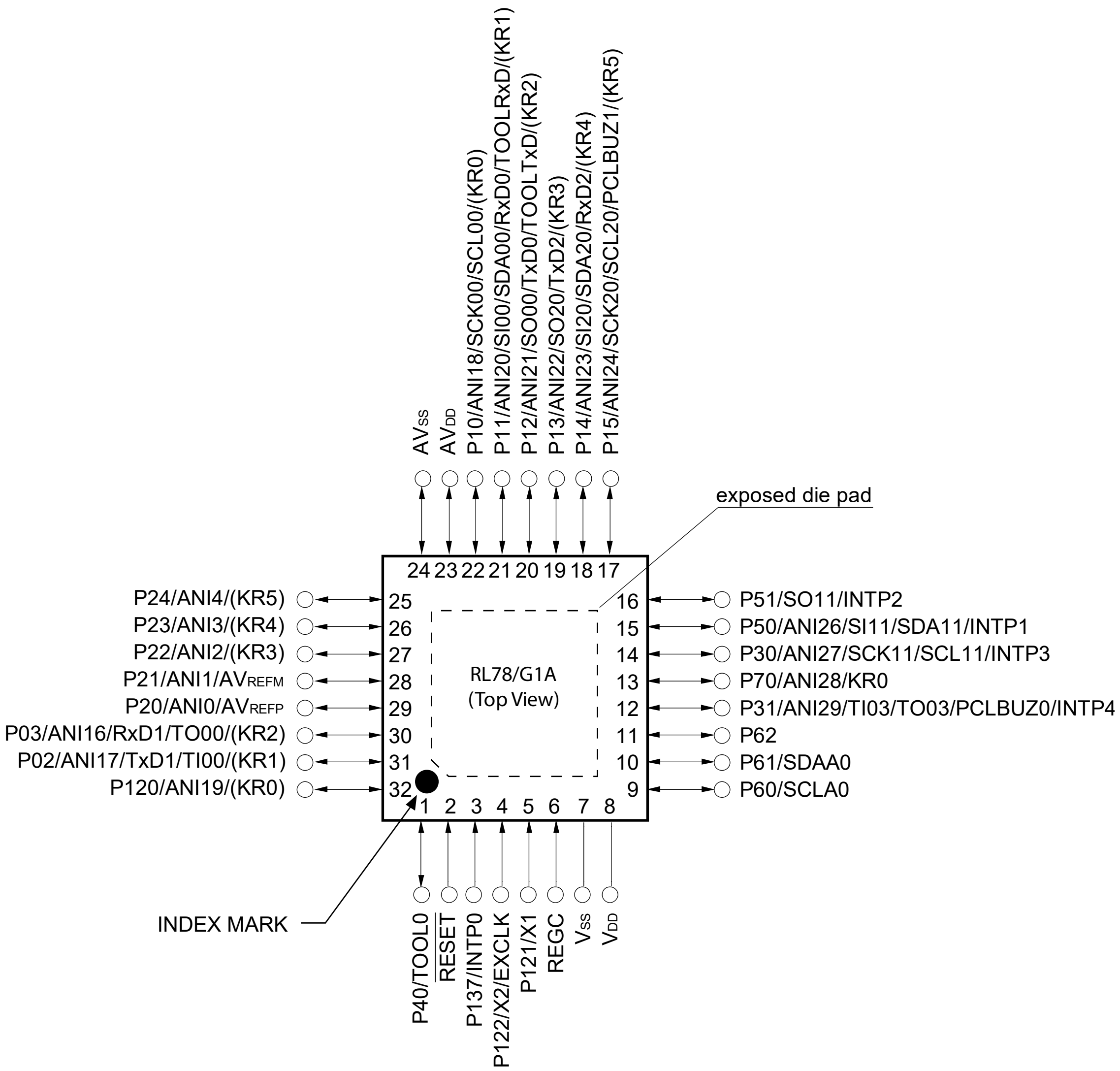
Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)

<R>



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

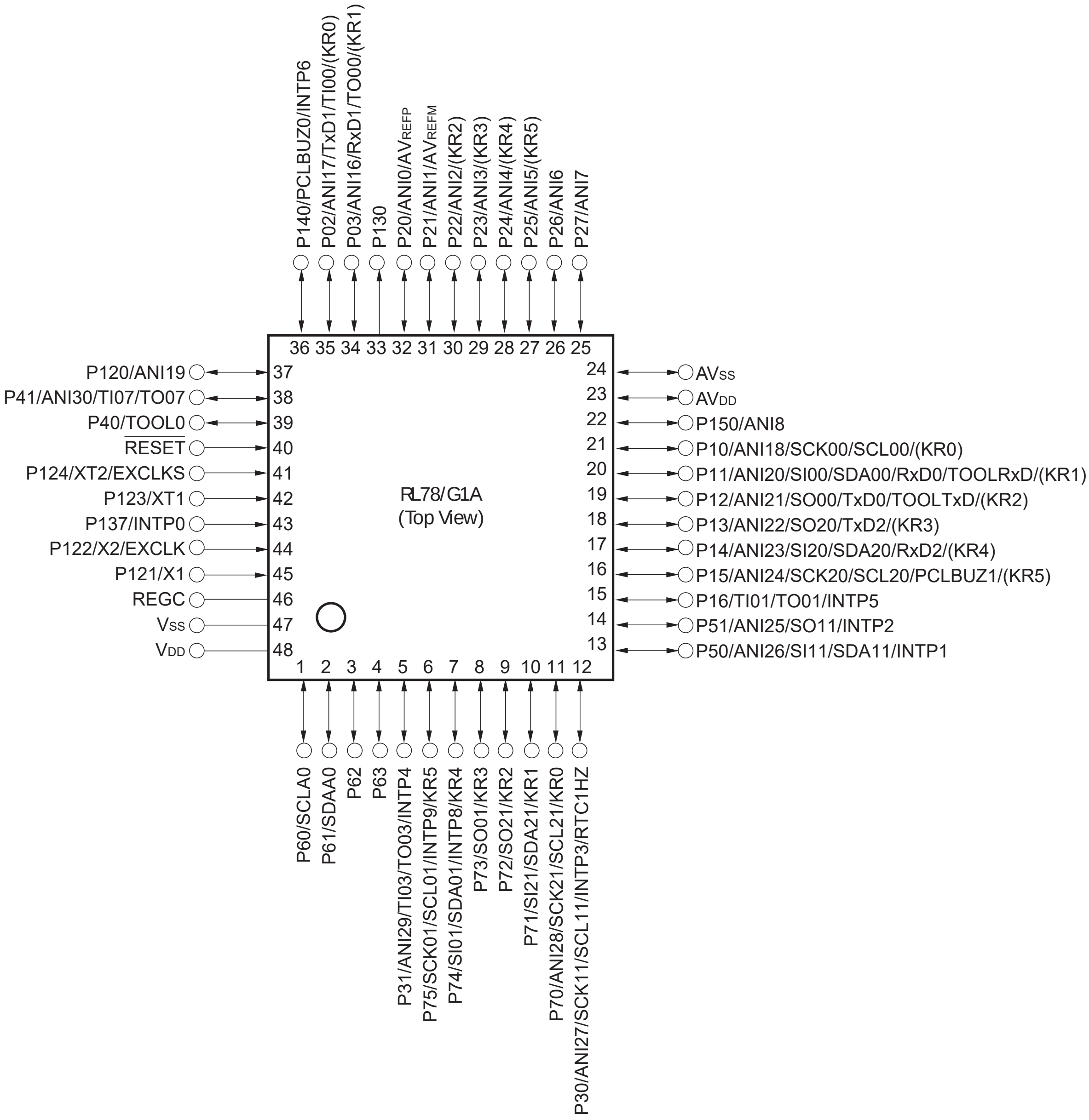
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> **3.** It is recommended to connect an exposed die pad to V_{SS}.

1.3.3 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

<R>



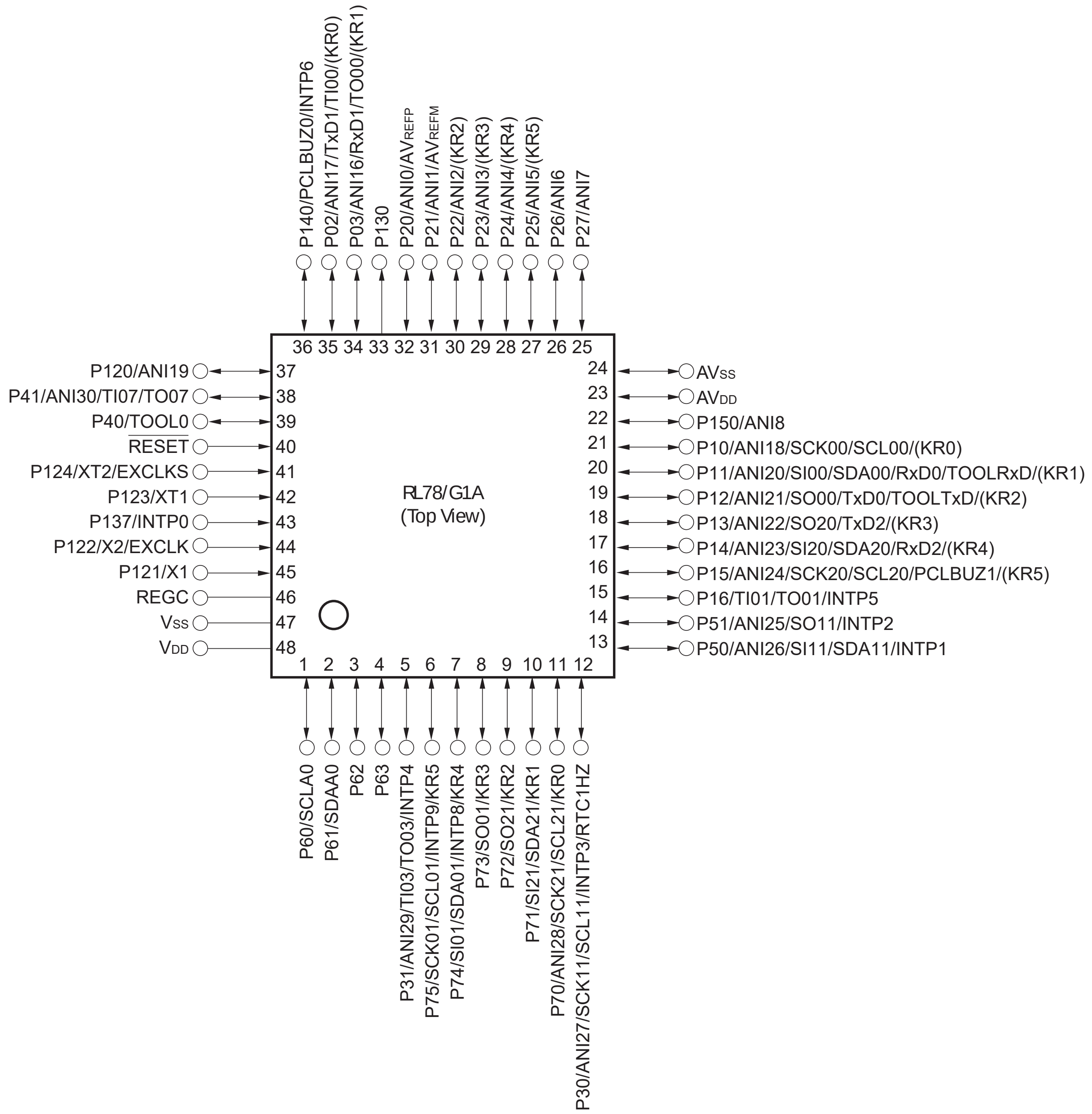
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

<R>



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.4 64-pin products

- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

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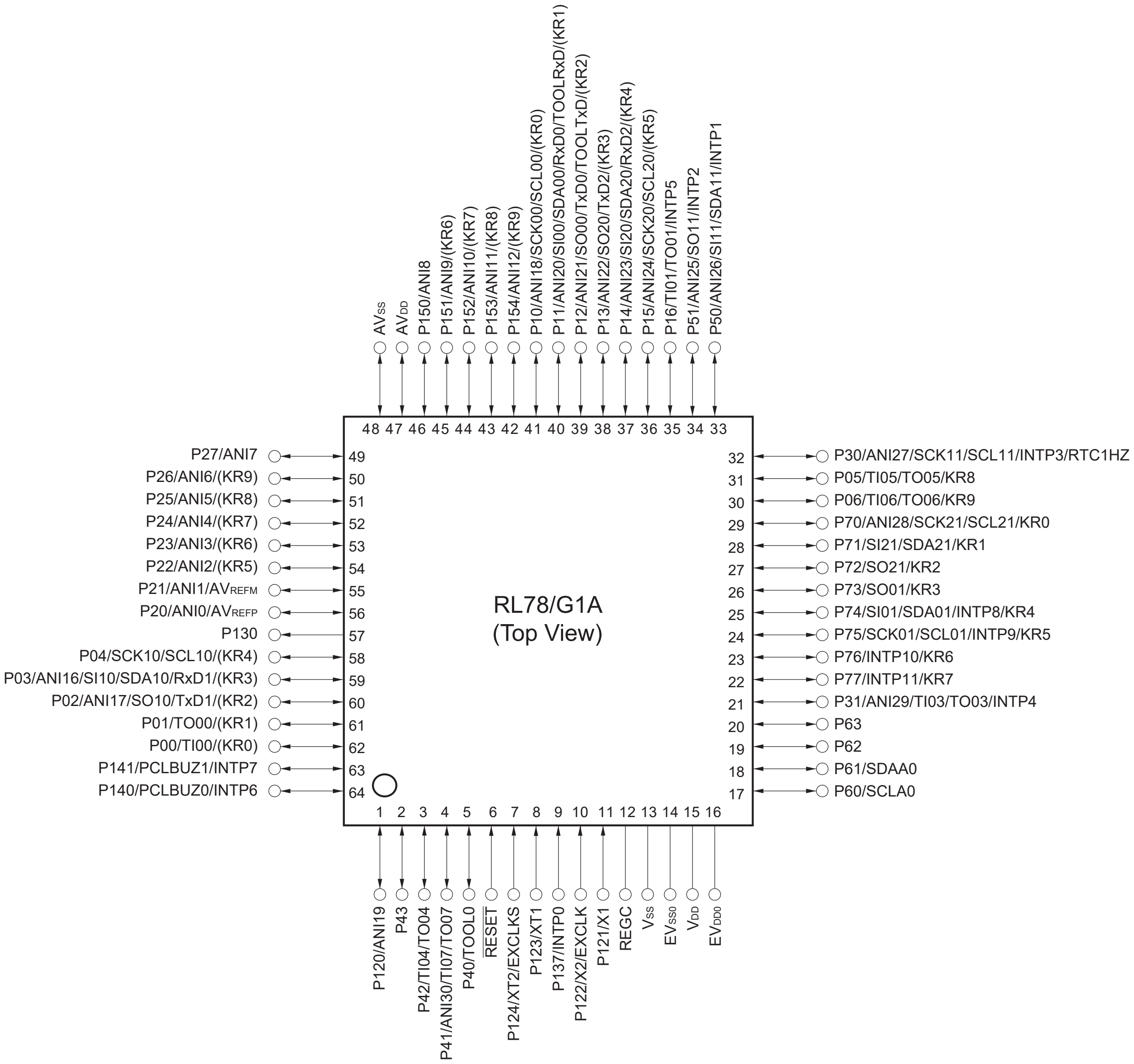


Cautions 1. Make EV$_{SS0}$ pin the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$ pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

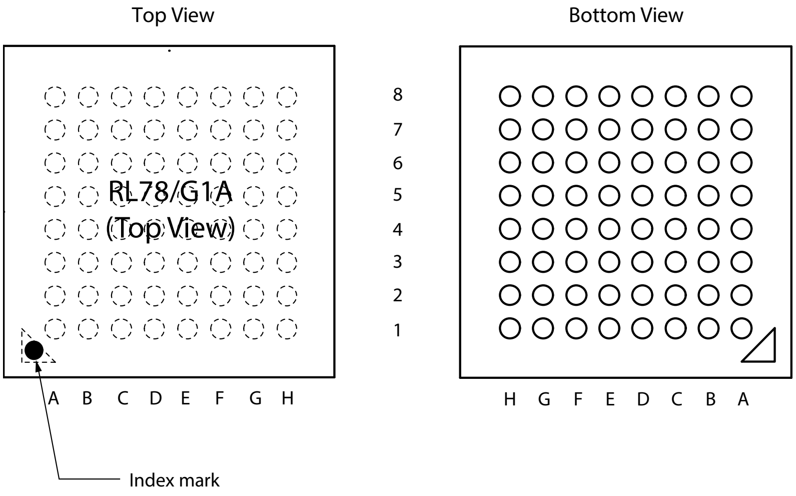
Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD0}$ pins and connect the V$_{SS}$ and EV$_{SS0}$pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)

<R>



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05/KR8	C1	P51/ANI25/SO11/INTP2	E1	P153/ANI11/(KR8)	G1	AV_{DD}
A2	P30/ANI27/SCK11/SCL11/INTP3/RTC1HZ	C2	P71/SI21/SDA21/KR1	E2	P154/ANI12/(KR9)	G2	P25/ANI5/(KR8)
A3	P70/ANI28/SCK21/SCL21/KR0	C3	P74/SI01/SDA01/INTP8/KR4	E3	P10/ANI18/SCK00/SCL00/(KR0)	G3	P24/ANI4/(KR7)
A4	P75/SCK01/SCL01/INTP9/KR5	C4	P16/TI01/TO01/INTP5	E4	P11/ANI20/SI00/SDA00/RxD0/TOOLRxD/(KR1)	G4	P22/ANI2/(KR5)
A5	P77/INTP11/KR7	C5	P15/ANI24/SCK20/SCL20/(KR5)	E5	P03/ANI16/SI10/SDA10/RxD1/(KR3)	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/ANI30/TI07/TO07	G6	P02/ANI17/SO10/TxD1/(KR2)
A7	P60/SCLA0	C7	V_{SS}	E7	$\overline{RESET}$	G7	P00/TI00/(KR0)
A8	EV_{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/ANI26 /SI11/SDA11/INTP1	D1	P13/ANI22/SO20/TxD2/(KR3)	F1	P150/ANI8	H1	AV_{SS}
B2	P72/SO21/KR2	D2	P06/TI06/TO06/KR9	F2	P151/ANI9/(KR6)	H2	P27/ANI7
B3	P73/SO01/KR3	D3	P12/ANI21/SO00/TxD0/TOOLTxD/(KR2)	F3	P152/ANI10/(KR7)	H3	P26/ANI6/(KR9)
B4	P76/INTP10/KR6	D4	P14/ANI23/SI20/SDA20/RxD2/(KR4)	F4	P21/ANI1/AV_{REFM}	H4	P23/ANI3/(KR6)
B5	P31/ANI29/TI03/TO03/INTP4	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10/(KR4)	H5	P20/ANI0/AV_{REFP}
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V_{DD}	D7	REGC	F7	P01/TO00/(KR1)	H7	P140/PCLBUZ0/INTP6
B8	EV_{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

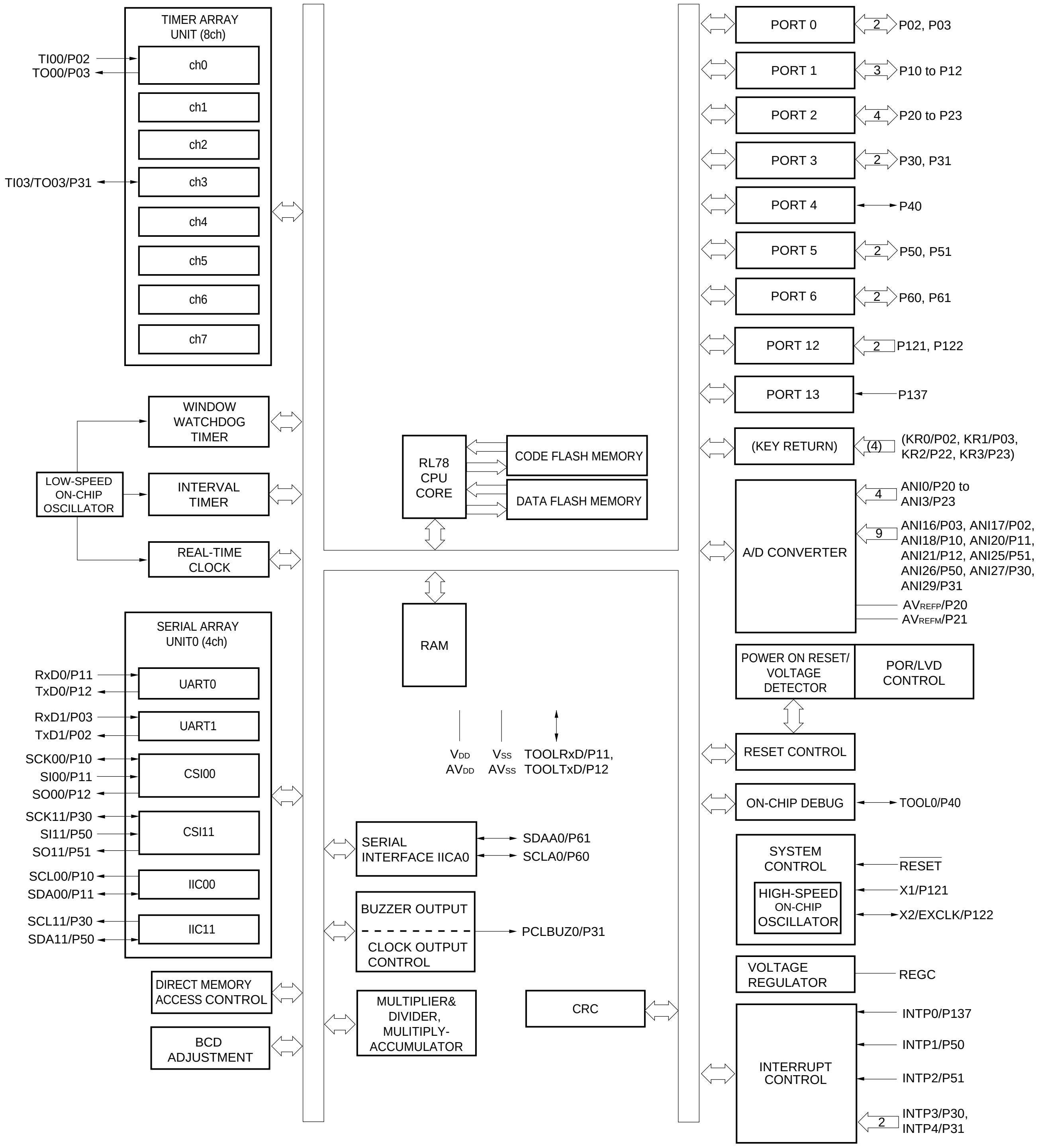
1.4 Pin Identification

ANI0 to ANI12, ANI16 to ANI30:	Analog input
AV_{DD}:	Analog power supply
AV_{SS}:	Analog ground
AV_{REFM}:	A/D converter reference potential (– side) input
AV_{REFP}:	A/D converter reference potential (+ side) input
EV_{DD0}:	Power supply for port
EV_{SS0}:	Ground for port
EXCLK:	External clock input (main system clock)
EXCLKS:	External clock input (subsystem clock)
INTP0 to INTP11:	Interrupt Request from External
KR0 to KR9:	Key return
P00 to P06:	Port 0
P10 to P16:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40 to P43:	Port 4
P50, P51:	Port 5
P60 to P63:	Port 6
P70 to P77:	Port 7
P120 to P124:	Port 12
P130, P137:	Port 13
P140, P141:	Port 14
P150 to P154:	Port 15

PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time clock correction clock (1 Hz) output
RxD0 to RxD2:	Receive data
SCK00, SCK01, SCK10, SCK11, SCK20, SCK21:	Serial clock input/output
SCLA0, SCL00, SCL01, SCL10, SCL11, SCL20, SCL21:	Serial clock output
SDAA0, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21:	Serial data input/output
SI00, SI01, SI10, SI11, SI20, SI21:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21:	Serial data output
TI00, TI01, TI03 to TI07:	Timer input
TO00, TO01, TO03 to TO07:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TxD0 to TxD2:	Transmit data
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)

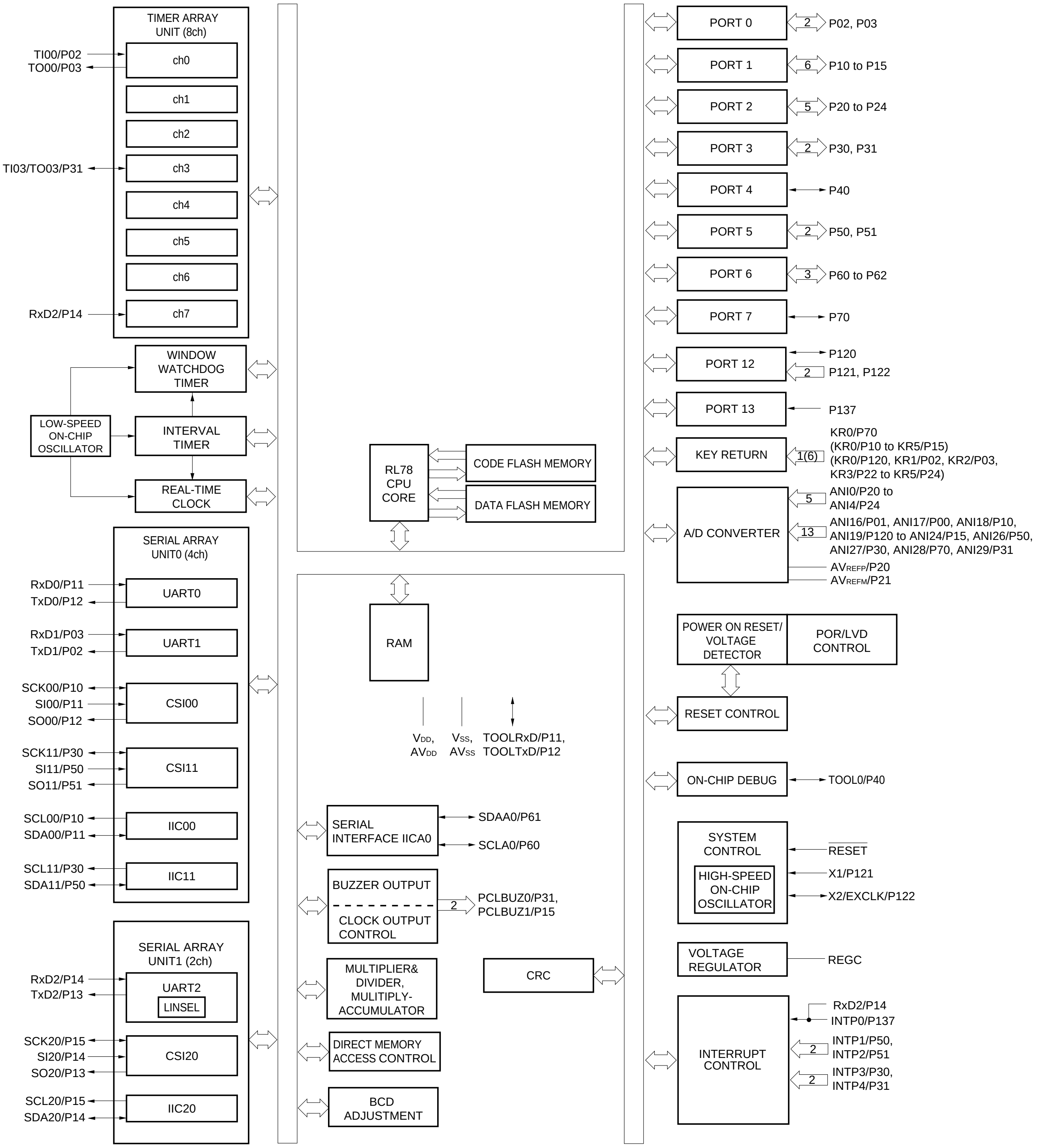
1.5 Block Diagram

1.5.1 25-pin products



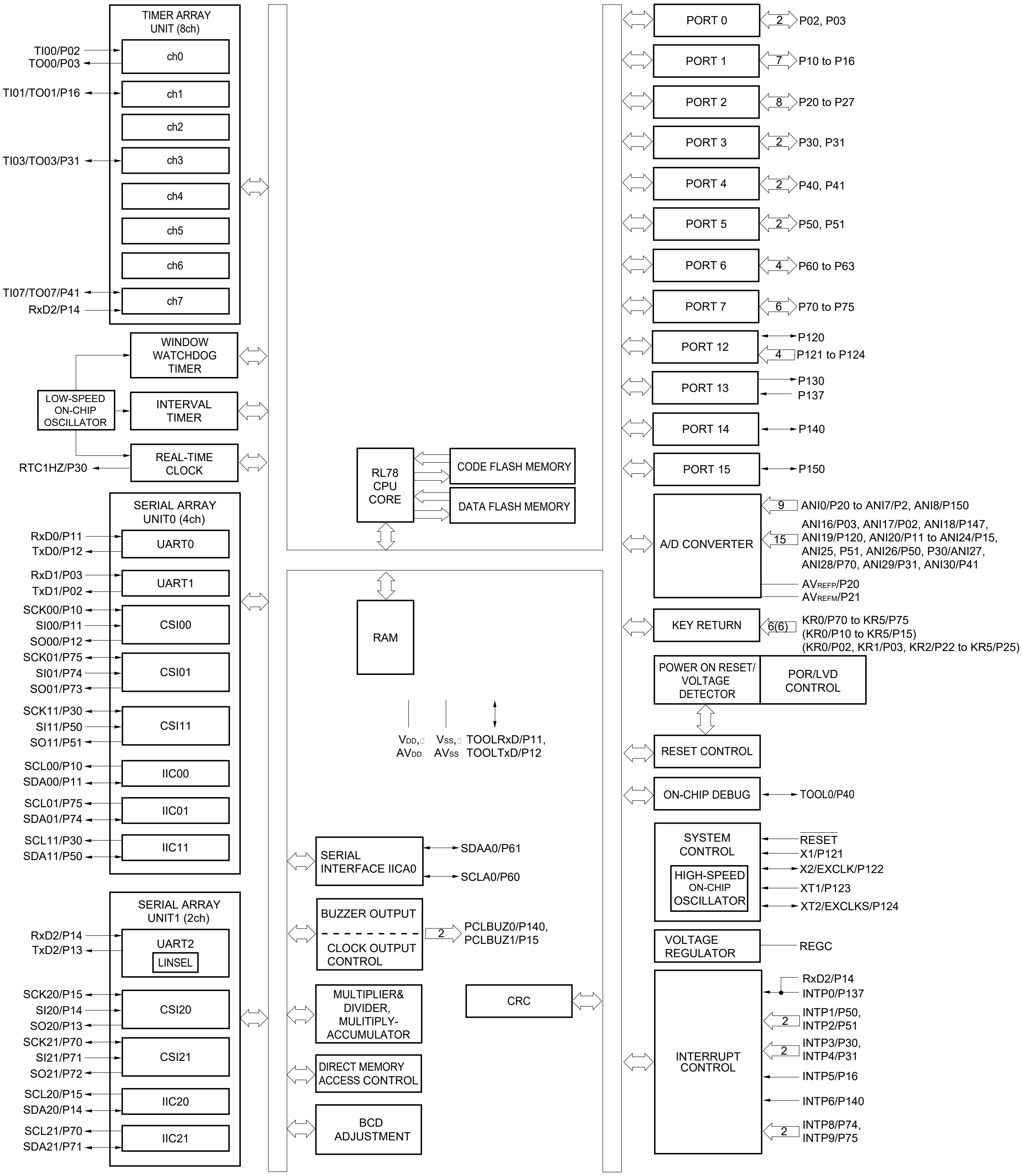
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.2 32-pin products



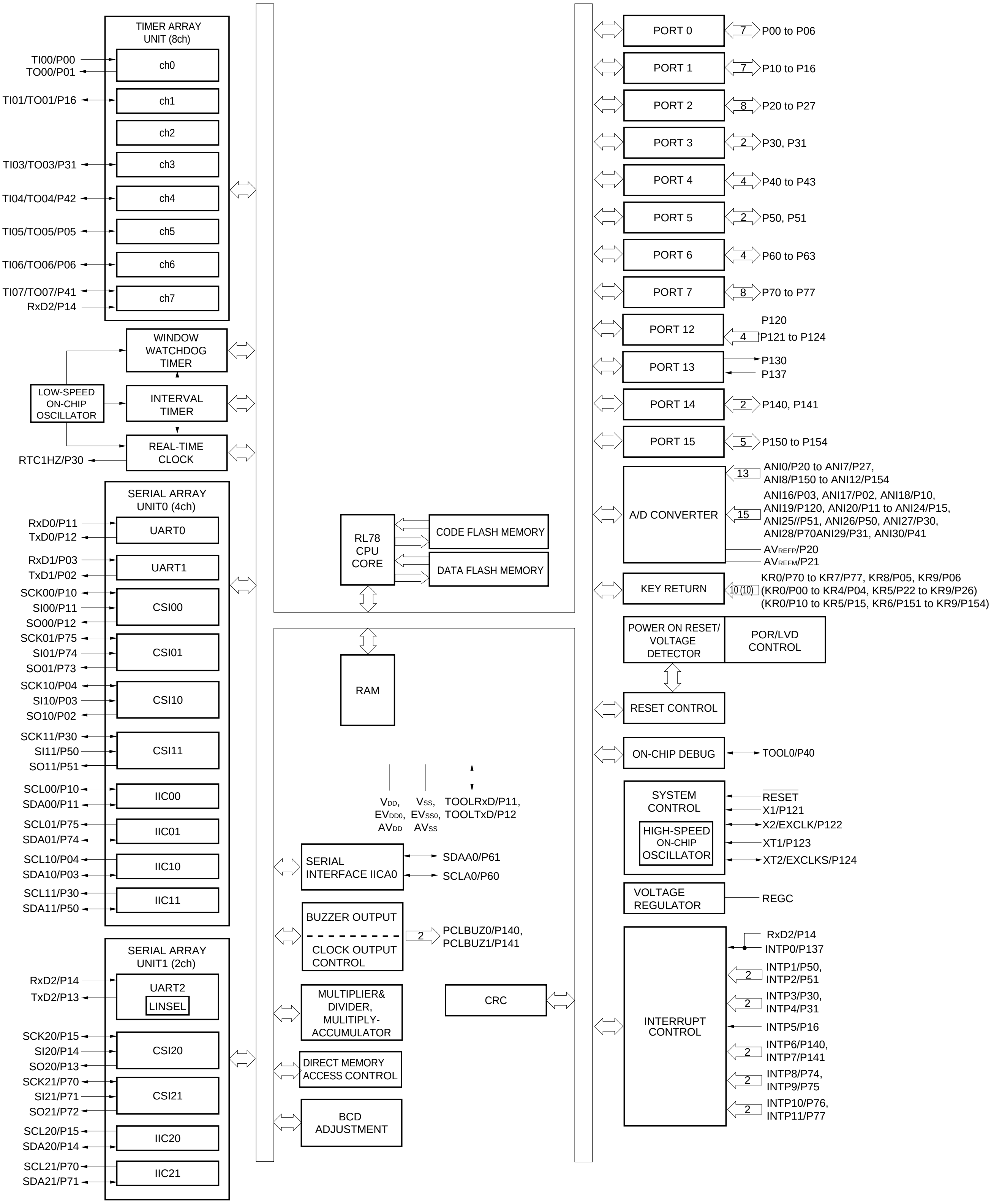
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.3 48-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

(1/2)

Item		25-pin	32-pin	48-pin	64-pin
		R5F10E8x	R5F10EBx	R5F10EGx	R5F10ELx
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2 to 4 Note 1	2 to 4 Note 1	2 to 4 Note 1	2 to 4 Note 1
Address space		1 MB			
<R> Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)			
	High-speed on-chip oscillator	HS (High-speed main) mode : 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode : 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode : 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode : 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)			
Subsystem clock		–		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.)	
Low-speed on-chip oscillator		15 kHz (TYP.)			
General-purpose register		(8-bit register × 8) × 4 bank			
Minimum instruction execution time		0.03125 µs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)			
		0.05 µs (High-speed system clock: f_{MX} = 20 MHz operation)			
		–		30.5 µs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	19	26	42	56
	<R> CMOS I/O	14 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)	20 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)	32 (N-ch O.D. I/O [V_{DD} withstand voltage]: 11)	46 (N-ch O.D. I/O [V_{DD} withstand voltage]: 12)
	CMOS input	3	3	5	5
	CMOS output	–	–	1	1
	N-ch open-drain I/O (6 V tolerance)	2	3	4	4
Timer	16-bit timer	8 channels			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel Note 2		1 channel	
	12-bit interval timer (IT)	1 channel			
	Timer output	2 channels (PWM outputs: 1 Note 3)		4 channels (PWM outputs: 3 Note 3)	7 channels (PWM outputs: 6 Note 3)
	RTC output	–		1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

Notes 1. In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C)**)

<R> **2.** Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f_{IL}) is selected.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (**6.9.3 Operation as multiple PWM output function**).

(2/2)

Item		25-pin	32-pin	48-pin	64-pin
		R5F10E8x	R5F10EBx	R5F10EGx	R5F10ELx
Clock output/buzzer output		1	2	2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/12-bit resolution A/D converter		13 channels	18 channels	24 channels	28 channels
Serial interface		[25-pin products] • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel [32-pin products] • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^{2}C: 1 channel/UART (UART supporting LIN-bus): 1 channel [48-pin products] • CSI: 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • CSI: 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^{2}C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • CSI: 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I^{2}C: 2 channels/UART (UART supporting LIN-bus): 1 channel			
	I^{2}C bus	1 channel	1 channel	1 channel	1 channel
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)			
DMA controller		2 channels			
Vectored interrupt sources	Internal	24	27	27	27
	External	6	6	10	13
Key interrupt		0 ch (4 ch)[Note 1]	1 ch (6 ch)[Note 1]	6 ch	10 ch
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution[Note 2] • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)			
Voltage detector		• Rising edge : 1.67 V to 3.14 V (12 stages) • Falling edge : 1.63 V to 3.06 V (12 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 3.6 V			
Operating ambient temperature		T_A = –40 to +85°C (A: Consumer application), T_A = –40 to +105°C (G: Industrial application)			

Notes 1. Can be used by the Peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (T_A = –40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications T_A = –40 to +85°C
R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA
R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA
R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA
R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB
R5F10ELCABG, R5F10ELDABG, R5F10ELEABG
G: Industrial applications When T_A = –40 to +105°C products is used in the range of T_A = –40 to +85°C
R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB
R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA
R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0} or EV_{SS0} pin, replace EV_{DD0} with V_{DD}, or replace EV_{SS0} with V_{SS}.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +6.5	V
	EV_{DD0}		–0.5 to +6.5	V
	AV_{DD}		–0.5 to +4.6	V
	AV_{REFP}		–0.3 to AV_{DD} +0.3[Note 3]	V
	EV_{SS0}		–0.5 to +0.3	V
	AV_{SS}		–0.5 to +0.3	V
	AV_{REFM}		–0.3 to AV_{DD} +0.3[Note 3] and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD} +0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	–0.3 to EV_{DD0} +0.3 and –0.3 to V_{DD} +0.3[Note 2]	V
	V_{I2}	P60 to P63 (N-ch open-drain)	–0.3 to +6.5	V
	V_{I3}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	–0.3 to V_{DD} +0.3[Note 2]	V
	V_{I4}	P20 to P27, P150 to P154	–0.3 to AV_{DD} +0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	–0.3 to EV_{DD0} +0.3[Note 2]	V
	V_{O2}	P20 to P27, P150 to P154	–0.3 to AV_{DD} +0.3[Note 2]	V
Analog input voltage	V_{AI1}	ANI16 to ANI30	–0.3 to EV_{DD0} +0.3 and –0.3 to $AV_{REF(+)}$ +0.3[Notes 2, 4]	V
	V_{AI2}	ANI0 to ANI12	–0.3 to AV_{DD} +0.3 and –0.3 to $AV_{REF(+)}$ +0.3[Notes 2, 4]	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Must be 4.6 V or lower.

4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS}: Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	–40	mA
		Total of all pins –170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	–70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	–100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P154	–0.1	mA
		Total of all pins		–1.3	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f_X)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	1.8 V ≤ V_{DD} ≤ 3.6 V	–1.0		+1.0	%
			1.6 V ≤ V_{DD} < 1.8 V	–5.0		+5.0	%
		–40 to –20 °C	1.8 V ≤ V_{DD} ≤ 3.6 V	–1.5		+1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	–5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(1/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	1.6 V ≤ EV_{DD0} ≤ 3.6 V			–10.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			–10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			–5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			–2.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			–19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			–10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			–5.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ EV_{DD0} ≤ 3.6 V			–29.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P154	1.6 V ≤ AV_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ AV_{DD} ≤ 3.6 V			–1.3	mA

Notes **1**. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				50.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P154				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ AV_{DD} ≤ 3.6 V			5.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	$0.8EV_{DD0}$		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} ≤ 3.6 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P154		$0.7AV_{DD}$		AV_{DD}	V
	V_{IH4}	P60 to P63		$0.7EV_{DD0}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0		$0.2EV_{DD0}$	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P154		0		$0.3AV_{DD}$	V
	V_{IL4}	P60 to P63		0		$0.3EV_{DD0}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –2.0 mA	EV_{DD0} – 0.6			V
			1.8 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –1.5 mA	EV_{DD0} – 0.5			V
			1.6 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –1.0 mA	EV_{DD0} – 0.5			V
	V_{OH2}	P20 to P27, P150 to P154	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OH2} = –100 μA	AV_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P154	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OL3} = 1.0 mA			0.4	V

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (5/5)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141	$V_I = EV_{DD0}$				1	μA
	I_{LIH2}	P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P20 to P27, P150 to P154	$V_I = AV_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141	$V_I = EV_{SS0}$				–1	μA
	I_{LIL2}	P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
	I_{LIL4}	P20 to P27, P150 to P154	$V_I = AV_{SS}$				–1	μA
On-chip pull-up resistance	R_U	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	$V_I = EV_{SS0}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 32 MHz[Note 3]	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.6	7.0	mA
				f_{IH} = 24 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		3.7	5.5	mA
				f_{IH} = 16 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		2.7	4.0	mA
			LS (low-speed main) mode[Note 5]	f_{IH} = 8 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			LV (Low-voltage main) mode[Note 5]	f_{IH} = 4 MHz[Note 3]	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	
			HS (high-speed main) mode[Note 5]	f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (low-speed main) mode[Note 5]	f_{MX} = 8 MHz[Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 2], V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
			Subsystem clock mode	f_{SUB} = 32.768 kHz[Note 4] T_A = –40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +25°C	Normal operation	Square wave input		4.2	4.9	μA
						Resonator connection		4.3	5.0	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +50°C	Normal operation	Square wave input		4.3	5.5	μA
						Resonator connection		4.4	5.6	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +70°C	Normal operation	Square wave input		4.5	6.3	μA
						Resonator connection		4.6	6.4	
				f_{SUB} = 32.768 kHz[Note 4] T_A = +85°C	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: V_{DD} = 2.7 V to 3.6 V@1 MHz to 32 MHz
V_{DD} = 2.4 V to 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: V_{DD} = 1.8 V to 3.6 V@1 MHz to 8 MHz
LV (Low-voltage main) mode: V_{DD} = 1.6 V to 3.6 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(2/3)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 3.0 V		0.54	1.63	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 3.0 V		0.44	1.28	mA
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V		0.40	1.00	mA
			LS (low-speed main) mode[Note 7]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		270	530	μA
					V_{DD} = 2.0 V		270	530	
			LV (Low-voltage main) mode[Note 7]	f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		435	640	μA
					V_{DD} = 2.0 V		435	640	
			HS (high-speed main) mode[Note 7]	f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	
			LS (low-speed main) mode[Note 7]	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f_{MX} = 8 MHz[Note 3], V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
			Subsystem clock mode	f_{SUB} = 32.768 kHz[Note 5] T_A = –40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +50°C	Square wave input		0.38	1.17	μA
					Resonator connection		0.57	1.36	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +70°C	Square wave input		0.52	1.97	μA
					Resonator connection		0.71	2.16	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +85°C	Square wave input		0.97	3.37	μA
					Resonator connection		1.16	3.56	
	I_{DD3}[Note 6]	STOP mode[Note 8]	T_A = –40°C				0.16	0.50	μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.34	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). Including the current flowing into the RTC. However, not including the current flowing into the 12-bit interval timer, and watchdog timer.

6. When subsystem clock is stopped. Not including the current flowing into the RTC, 12-bit interval timer, watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} < 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

<R> **(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)** **(3/3)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} [Note 1]				0.20		μA
RTC operating current	I_{RTC} [Notes 1, 2, 3]				0.02		μA
12-bit interval timer operating current	I_{IT} [Notes 1, 2, 4]				0.02		μA
Watchdog timer operating current	I_{WDT} [Notes 1, 2, 5]	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} [Notes 6, 7]	AV_{DD} = 3.0 V, When conversion at maximum speed			420	720	μA
$AV_{REF(+)}$ current	I_{AVREF} [Note 8]	AV_{DD} = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 [Note 7]			14.0	25.0	μA
		AV_{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 [Note 10]			14.0	25.0	μA
		ADREFP1 = 1, ADREFP0 = 0 [Note 1]			14.0	25.0	μA
A/D converter reference voltage current	I_{ADREF} [Notes 1, 9]	V_{DD} = 3.0 V			75.0		μA
Temperature sensor operating current	I_{TMP} [Note 1]	V_{DD} = 3.0 V			75.0		μA
LVD operating current	I_{LVD} [Notes 1, 11]				0.08		μA
BGO operating current	I_{BGO} [Notes 1, 12]				2.5	12.2	mA
Self-programming operating current	I_{FSP} [Notes 1, 13]				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ}	A/D converter operation (AV_{DD} = 3.0 V)	The mode is performed [Notes 1, 14]		0.50	0.60	mA
			During A/D conversion [Note 1]		0.60	0.75	mA
			During A/D conversion [Note 7]		420	720	μA
		CSI/UART operation [Note 1]			0.70	0.84	mA

(**Notes** and **Remarks** are listed on the next page.)

<R> **Notes** **1.** Current flowing to V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing to the AV_{DD}.

8. Current flowing from the reference voltage source of A/D converter.

9. Operation current flowing to the internal reference voltage.

10. Current flowing to the AV_{REFP}.

11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

12. Current flowing only during data flash rewrite.

13. Current flowing only during self programming.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

(T_A = –40 to +85°C, AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns$^{\text{Note}}$
TO00, TO01, TO03 to TO07 output frequency	f_{TO}	HS (high-speed main) mode	2.7 V ≤ EV_{DD0} ≤ 3.6 V				8	MHz
			1.8 V ≤ EV_{DD0} < 2.7 V				4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V				2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD0} ≤ 3.6 V				4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V				2	MHz
		LV (low-voltage main) mode	1.6 V ≤ EV_{DD0} ≤ 3.6 V				2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	2.7 V ≤ EV_{DD0} ≤ 3.6 V				8	MHz
			1.8 V ≤ EV_{DD0} < 2.7 V				4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V				2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD0} ≤ 3.6 V				4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V				2	MHz
		LV (low-voltage main) mode	1.8 V ≤ EV_{DD0} ≤ 3.6 V				4	MHz
			1.6 V ≤ EV_{DD0} < 1.8 V				2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	1.6 V ≤ V_{DD} ≤ 3.6 V		1			μs
		INTP1 to INTP11	1.6 V ≤ EV_{DD0} ≤ 3.6 V		1			μs
Key interrupt input high-level width, low-level width	t_{KR}	KR0 to KR9	1.8 V ≤ EV_{DD0} ≤ 3.6 V, 1.8 V ≤ AV_{DD0} ≤ 3.6 V		250			ns
			1.6 V ≤ EV_{DD0} < 1.8 V, 1.6 V ≤ AV_{DD0} < 1.8 V		1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

(**Note** and **Remark** are listed on the next page.)

Note The following conditions are required for low-voltage interface when $EV_{DD0} < V_{DD}$.

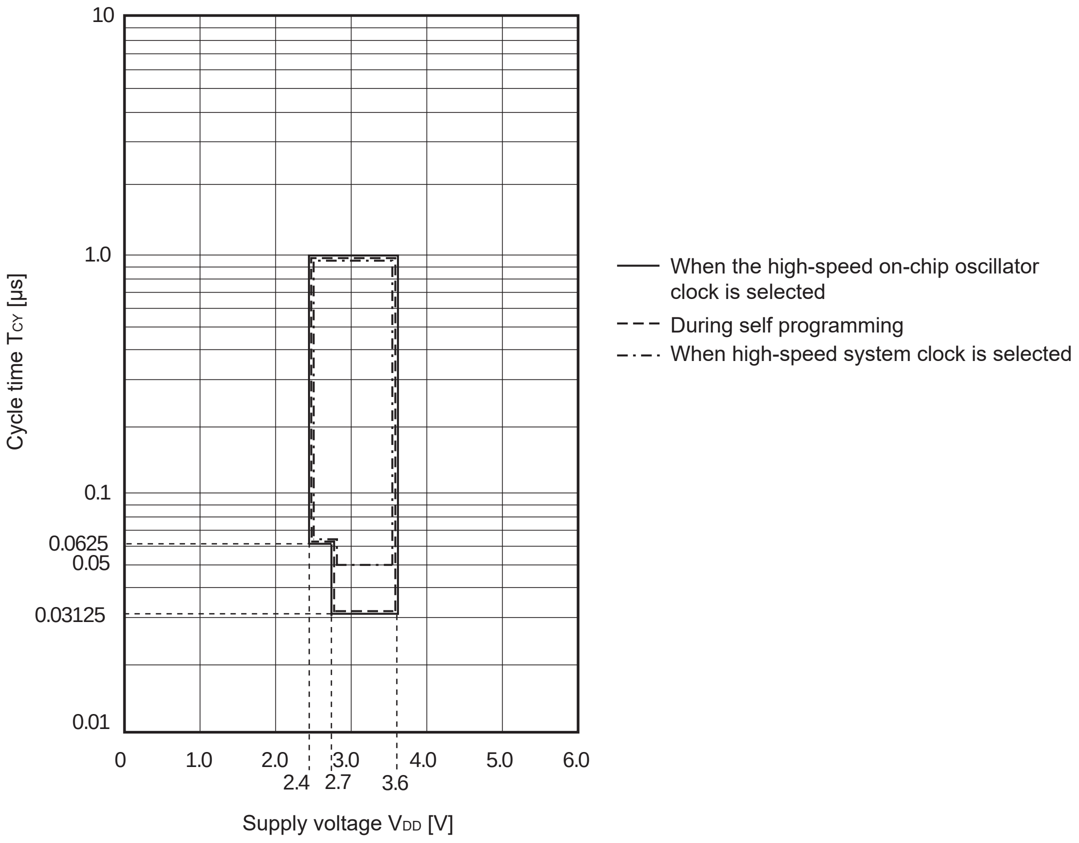
$1.8 V \leq EV_{DD0} < 2.7 V$: MIN. 125 ns

$1.6 V \leq EV_{DD0} < 1.8 V$: MIN. 250 ns

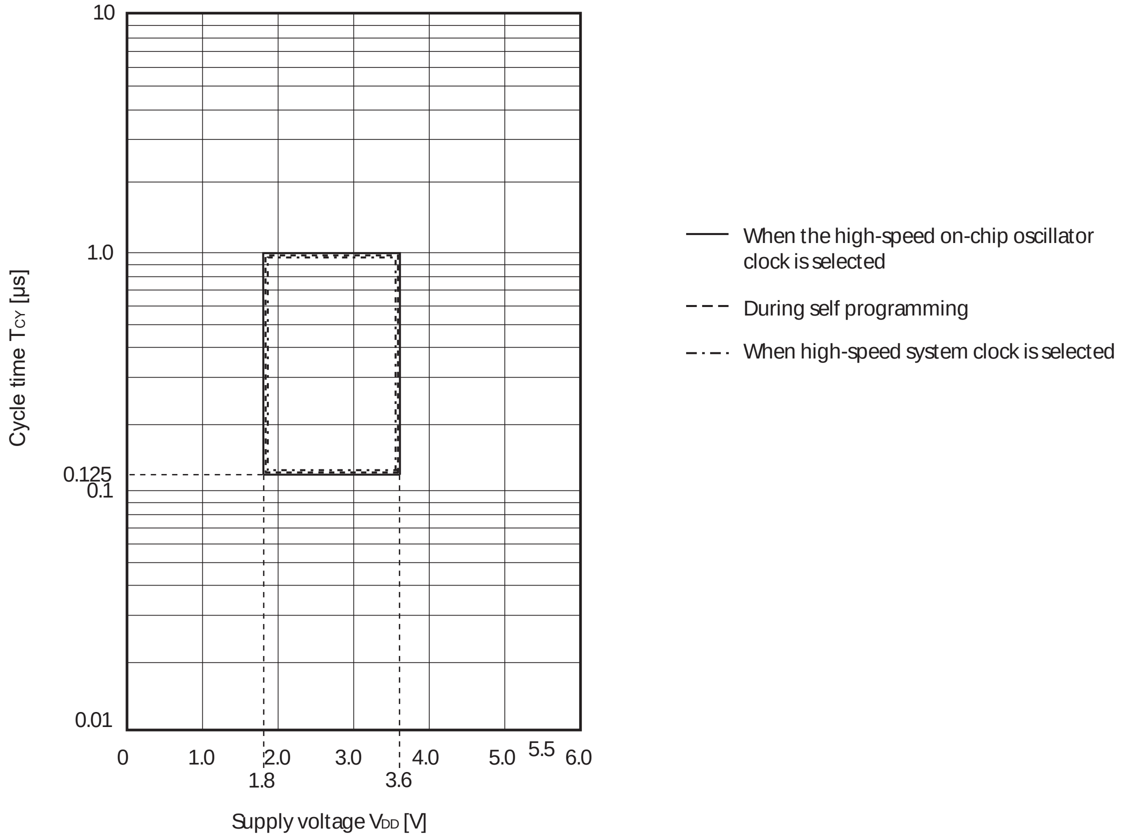
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer clock select register 0 (TPS0) and timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

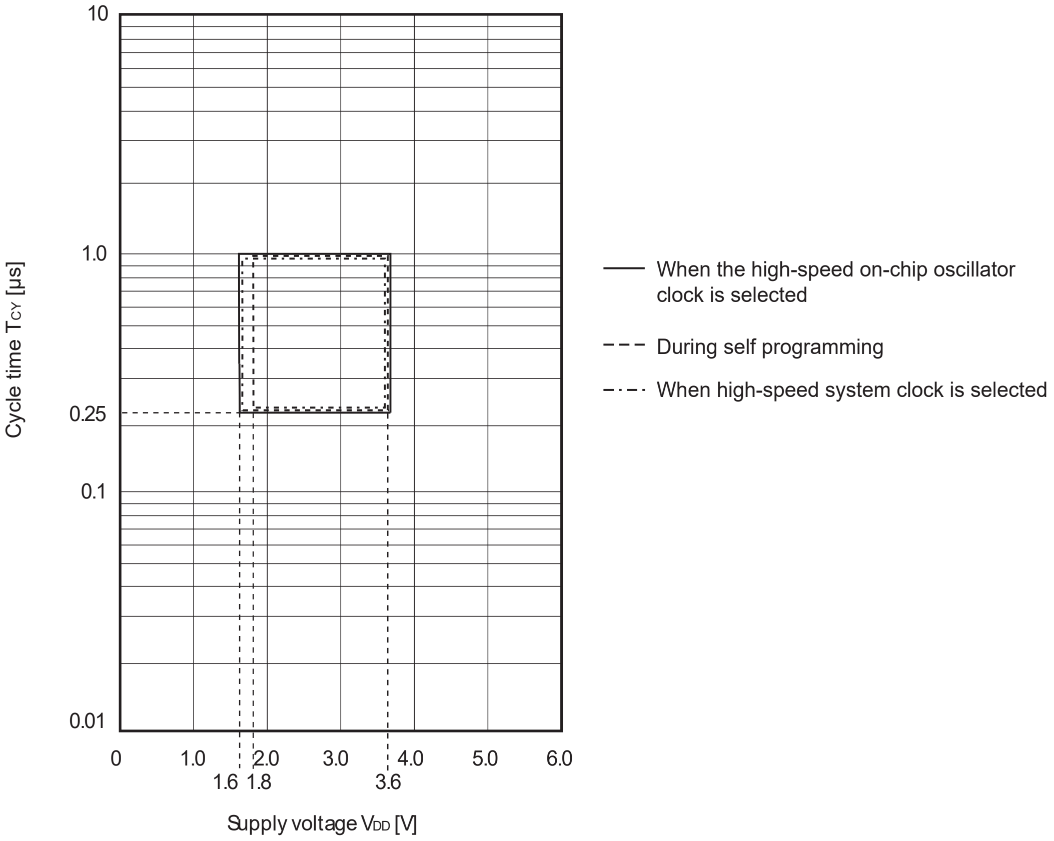
<R> T_{CY} vs V_{DD} (HS (high-speed main) mode)



<R> T_{CY} vs V_{DD} (LS (low-speed main) mode)

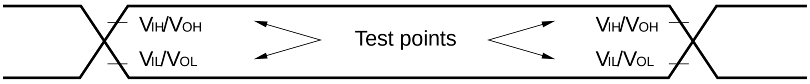


<R> T_{CY} vs V_{DD} (LV (low-voltage main) mode)

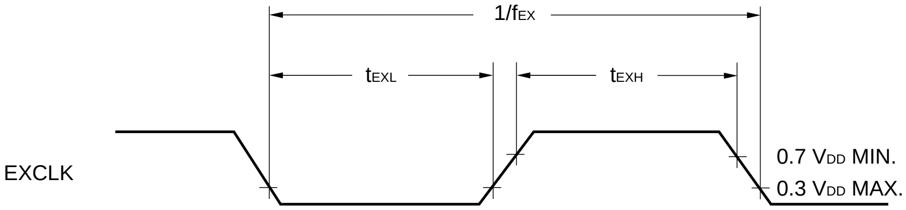


AC Timing Test Points

<R>

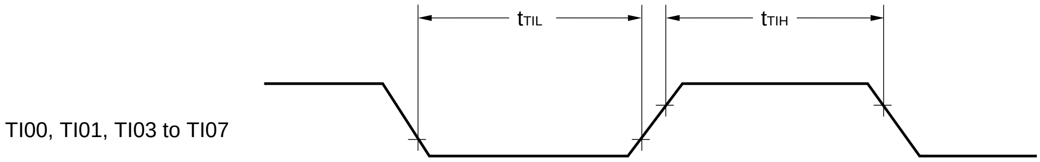


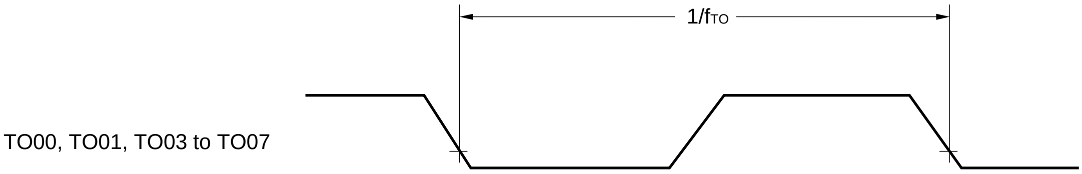
External System Clock Timing



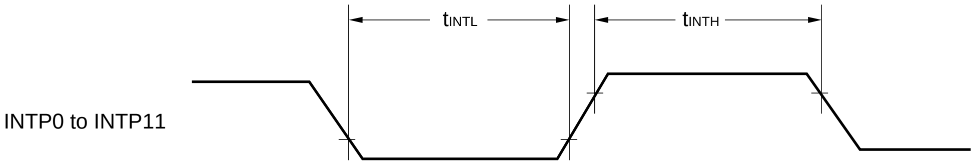
<R>

TI/TO Timing

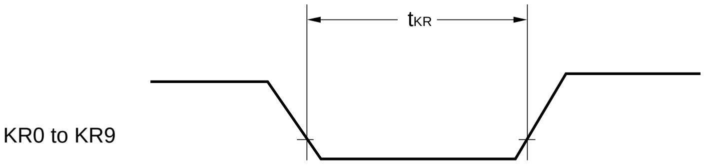




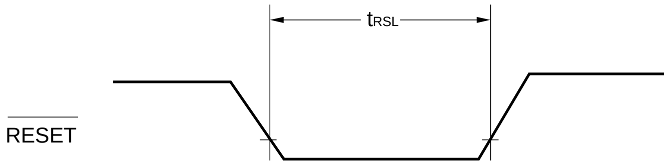
Interrupt Request Input Timing



Key Interrupt Input Timing



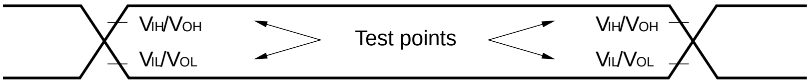
$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points

<R>



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate[Note 4]		2.4 V ≤ EV_{DD} ≤ 3.6 V		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$[Note 6]		5.3[Note 5]		1.3		0.6	Mbps
		1.8 V ≤ EV_{DD} ≤ 3.6 V		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$[Note 6]		5.3[Note 5]		1.3		0.6	Mbps
		1.7 V ≤ EV_{DD} ≤ 3.6 V		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$[Note 6]		5.3[Note 5]		1.3[Note 5]		0.6	Mbps
		1.6 V ≤ EV_{DD} ≤ 3.6 V		–		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$[Note 6]		–		1.3[Note 5]		0.6	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

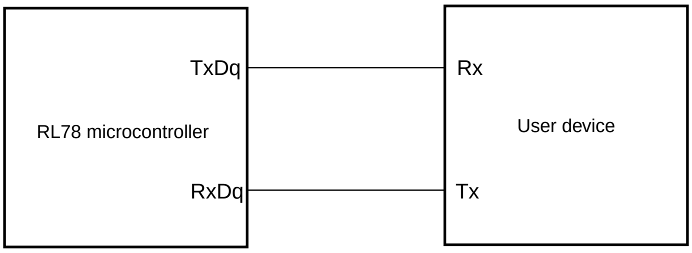
4. Transfer rate in the SNOOZE mode is 4800 bps.

5. The following conditions are required for low-voltage interface when $EV_{DD0} < V_{DD}$.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps
1.6 V ≤ EV_{DD0} < 1.8 V : MAX. 0.6 Mbps

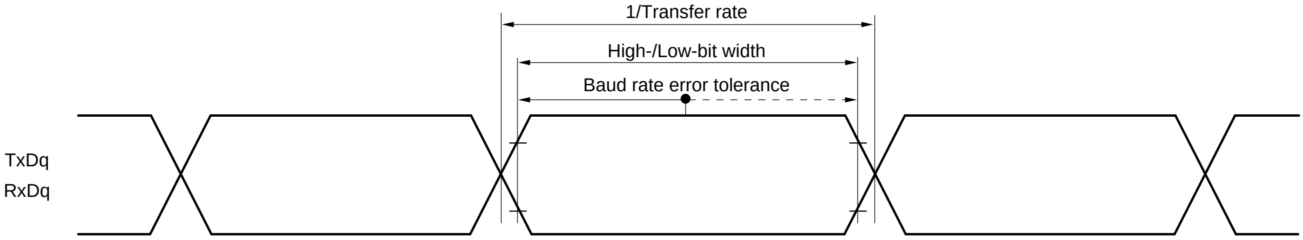
6. f_{CLK} in each operating mode is as below.
HS (high-speed main) mode: f_{CLK} = 32 MHz
LS (low-speed main) mode: f_{CLK} = 8 MHz
LV (low-voltage main) mode: f_{CLK} = 4 MHz

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)
(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 3.6 V	t_{KCY1} ≥ 2/f_{CLK}	83.3		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD} ≤ 3.6 V		t_{KCY1}/2 –10		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 3.6 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	2.7 V ≤ EV_{DD} ≤ 3.6 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO1}	C = 20 pF Note 6			10		10		10	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output) (T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ $4/f_{CLK}$	125		500		1000		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ $4/f_{CLK}$	250		500		1000		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ $4/f_{CLK}$	500		500		1000		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ $4/f_{CLK}$	1000		1000		1000		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1} ≥ $4/f_{CLK}$	–		1000		1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY2}/2$ –18		$t_{KCY2}/2$ –50		$t_{KCY2}/2$ –50		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY2}/2$ –38		$t_{KCY2}/2$ –50		$t_{KCY2}/2$ –50		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY2}/2$ –50		$t_{KCY2}/2$ –50		$t_{KCY2}/2$ –50		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY2}/2$ –100		$t_{KCY2}/2$ –100		$t_{KCY2}/2$ –100		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		$t_{KCY2}/2$ –100		$t_{KCY2}/2$ –100		ns
SIp setup time (to SCKp↑)[Note 4]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		110		110		110		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		220		220		220		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		220		220		ns
SIp hold time (from SCKp↑)[Note 4]	t_{KSI2}	1.7 V ≤ EV_{DD} ≤ 3.6 V		19		19		19		ns
		1.6 V ≤ EV_{DD} ≤ 3.6 V		–		19		19		ns
Delay time from SCKp↓ to SOp output[Note 5]	t_{KSO2}	1.7 V ≤ EV_{DD} ≤ 3.6 V	C = 30 pF[Note 6]		25		25		25	ns
		1.6 V ≤ EV_{DD} ≤ 3.6 V	C = 30 pF[Note 6]		–		25		25	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time[Note 4]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	16 MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD} ≤ 3.6 V		$t_{KCY2}/2 - 8$		$t_{KCY2}/2 - 8$		$t_{KCY2}/2 - 8$		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY2}/2 - 18$		$t_{KCY2}/2 - 18$		$t_{KCY2}/2 - 18$		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY2}/2 - 66$		$t_{KCY2}/2 - 66$		$t_{KCY2}/2 - 66$		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		$t_{KCY2}/2 - 66$		$t_{KCY2}/2 - 66$		ns
SIp setup time (to SCKp↑)[Note 5]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +40		1/f_{MCK} +40		1/f_{MCK} +40		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		1/f_{MCK} +40		1/f_{MCK} +40		ns
SIp hold time (from SCKp↑)[Note 5]	t_{KSI2}	1.8 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK}+ 250		1/f_{MCK}+ 250		1/f_{MCK}+ 250		ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		1/f_{MCK}+ 250		1/f_{MCK}+ 250		ns
Delay time from SCKp↓ to SOp output[Note 6]	t_{KSO2}	C = 30 pF[Note 7]	2.7 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.4 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +75		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.8 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +110		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.7 V ≤ EV_{DD0} ≤ 3.6 V		2/f_{MCK} +220		2/f_{MCK} +220		2/f_{MCK} +220	ns
			1.6 V ≤ EV_{DD0} ≤ 3.6 V		–		2/f_{MCK} +220		2/f_{MCK} +220	ns

(**Note, Caution** and **Remark** are listed on the next page.)

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. C is the load capacitance of the SOp output lines.

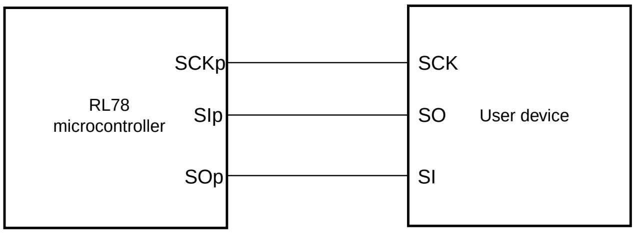
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1)

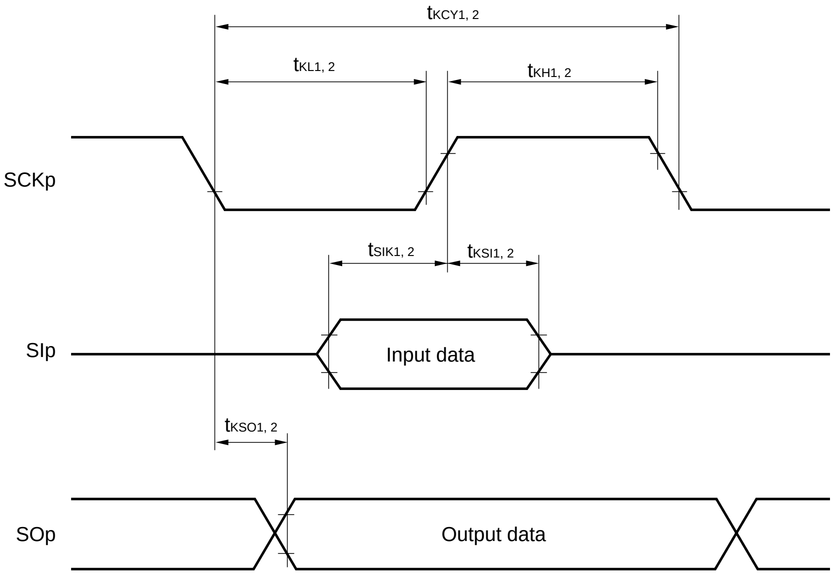
2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

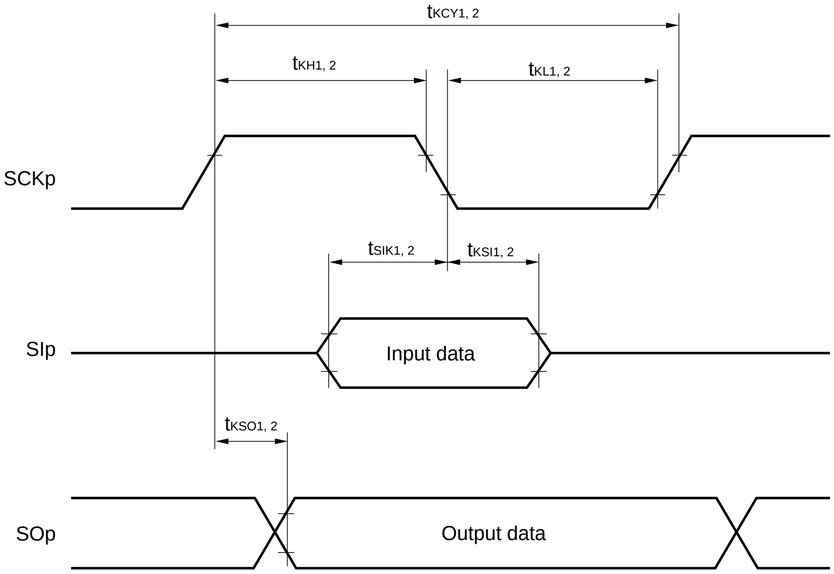
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) During communication at same potential (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS$^{\text{Note 1}}$		LS$^{\text{Note 2}}$		LV$^{\text{Note 3}}$		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		1000$^{\text{Note 4}}$		400$^{\text{Note 4}}$		400$^{\text{Note 4}}$	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		400$^{\text{Note 4}}$		400$^{\text{Note 4}}$		400$^{\text{Note 4}}$	kHz
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300$^{\text{Note 4}}$		300$^{\text{Note 4}}$		300$^{\text{Note 4}}$	kHz
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250$^{\text{Note 4}}$		250$^{\text{Note 4}}$		250$^{\text{Note 4}}$	kHz
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		–		250$^{\text{Note 4}}$		250$^{\text{Note 4}}$	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		1850		1850		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		1850		1850		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85$^{\text{Note 5}}$		1/f_{MCK} + 145$^{\text{Note 5}}$		1/f_{MCK} + 145$^{\text{Note 5}}$		ns
		1.8 V ≤ EV_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145$^{\text{Note 5}}$		1/f_{MCK} + 145$^{\text{Note 5}}$		1/f_{MCK} + 145$^{\text{Note 5}}$		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK}+ 230$^{\text{Note 5}}$		1/f_{MCK}+ 230$^{\text{Note 5}}$		1/f_{MCK}+ 230$^{\text{Note 5}}$		ns
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290$^{\text{Note 5}}$		1/f_{MCK} + 290$^{\text{Note 5}}$		1/f_{MCK} + 290$^{\text{Note 5}}$		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		1/f_{MCK} + 290$^{\text{Note 5}}$		1/f_{MCK} + 290$^{\text{Note 5}}$		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(5) During communication at same potential (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV_{DD0} ≤ 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–	–	0	405	0	405	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

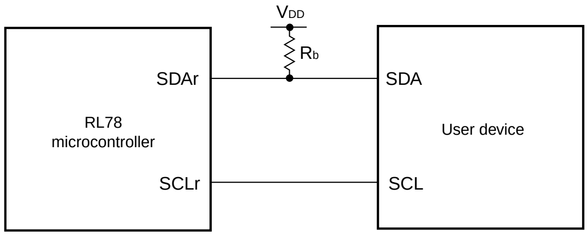
3. LV is condition of LV (low-voltage main) mode.

4. The value must also be f_{CLK}/4 or lower.

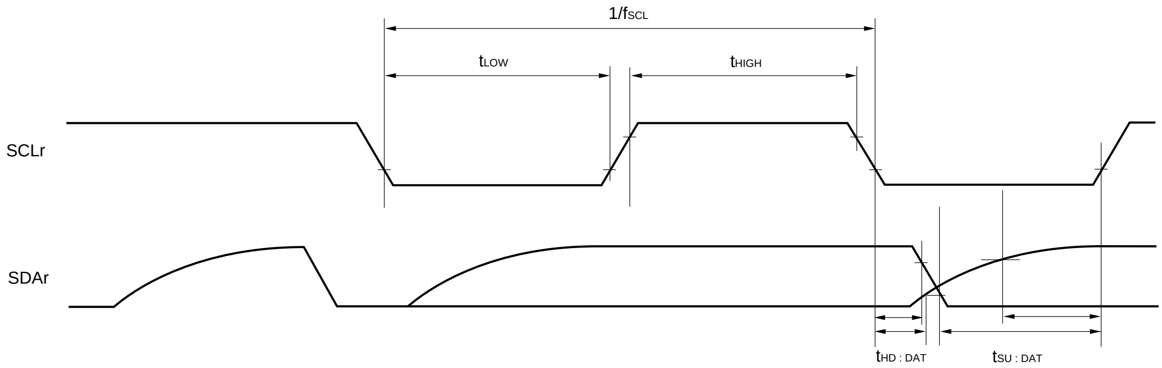
5. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I^2C mode mode connection diagram (during communication at same potential)



Simplified I^2C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			HS Note 1		LS Note 2		LV Note 3		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 4		Reception	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 7		5.3		1.3		0.6	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 5			$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 7		5.3 Note 6		1.3		0.6	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode is 4800 bps.

5. Use it with $EV_{DD0} \geq V_b$.

6. The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.

2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps

7. f_{CLK} in each operating mode is as below.

HS (high-speed main) mode: f_{CLK} = 32 MHz
LS (low-speed main) mode: f_{CLK} = 8 MHz
LV (low-voltage main) mode: f_{CLK} = 4 MHz

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			HS$^{\text{Note 1}}$		LS$^{\text{Note 2}}$		LV$^{\text{Note 3}}$		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 4**		**Note 4**		**Note 4**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 5		1.2 Note 5		1.2 Note 5	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V$^{\text{Note 6}}$			**Note 7**		**Note 7**		**Note 7**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 8		0.43 Note 8		0.43 Note 8	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} ≤ 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. Use it with EV_{DD0} ≥ V_b.

7. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

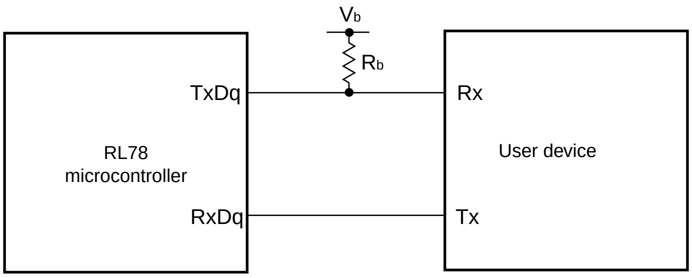
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

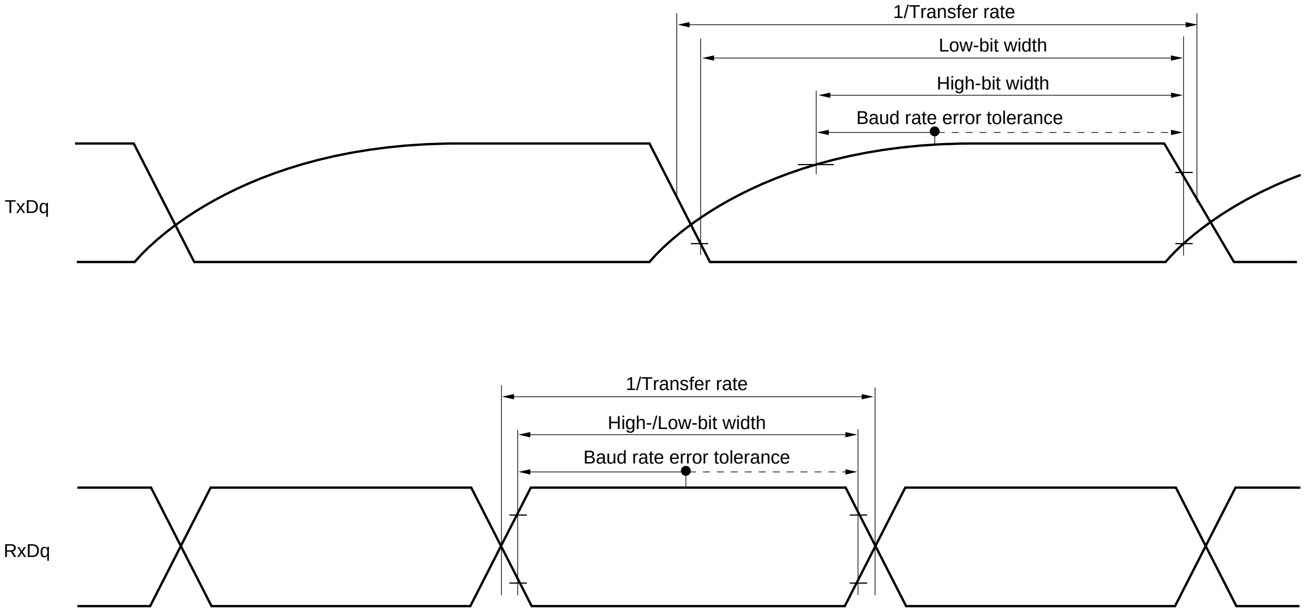
8. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

<R> **Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1} ≥ $2/f_{CLK}$	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 120		$t_{KCY1}/2$ – 120		$t_{KCY1}/2$ – 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 10		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
SIp setup time (to SCKp↑)[Note 4]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑)[Note 4]	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output[Note 4]	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns
SIp setup time (to SCKp↓)[Note 5]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33		110		110		ns
SIp hold time (from SCKp↓)[Note 5]	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output[Note 5]	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10		10		10	ns

Notes **1.** HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

5. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

<R> **Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)

(8) Communication at different potential (1.8V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		$\text{HS}^{\text{Note 1}}$		$\text{LS}^{\text{Note 2}}$		$\text{LV}^{\text{Note 3}}$		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	$t_{KCY1} \geq 4/f_{CLK}$	500		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 $V^{\text{Note 4}}$, C_b = 30 pF, R_b = 5.5 kΩ	$t_{KCY1} \geq 4/f_{CLK}$	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 170		$t_{KCY1}/2$ – 170		$t_{KCY1}/2$ – 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 $V^{\text{Note 4}}$, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ – 458		$t_{KCY1}/2$ – 458		$t_{KCY1}/2$ – 458		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 18		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 $V^{\text{Note 4}}$, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Use it with $EV_{DD0} \geq V_b$.

<R>

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑)[Note 4]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 6], C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑)[Note 4]	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 6], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output[Note 4]	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 6], C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns
SIp setup time (to SCKp↓)[Note 5]	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 6], C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓)[Note 5]	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 6], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output[Note 5]	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 6], C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

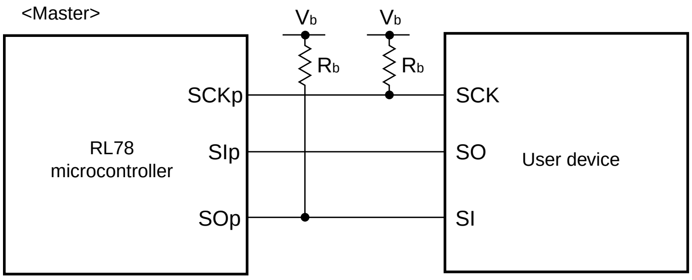
5. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. Use it with EV_{DD0} ≥ V_b.

<R> **Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

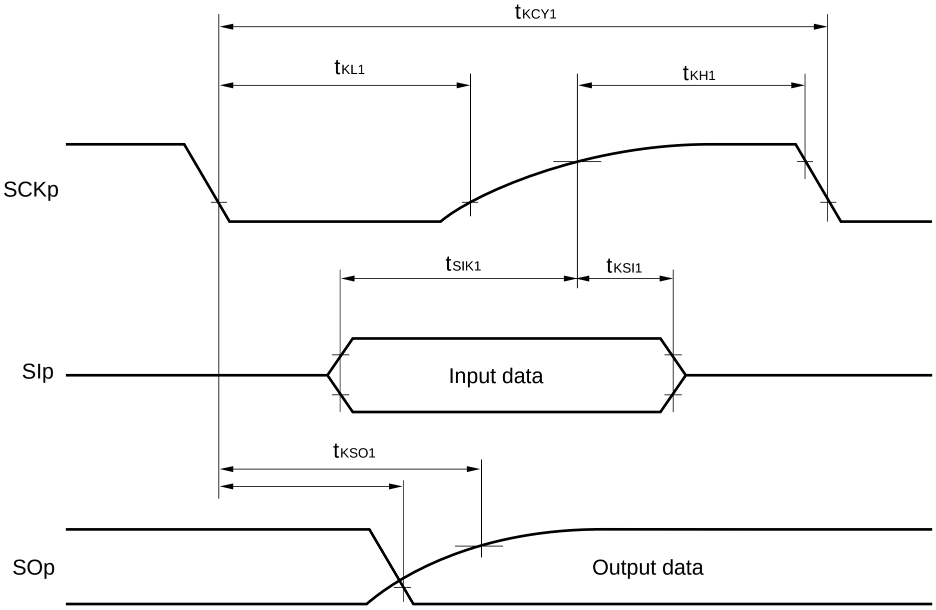


Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

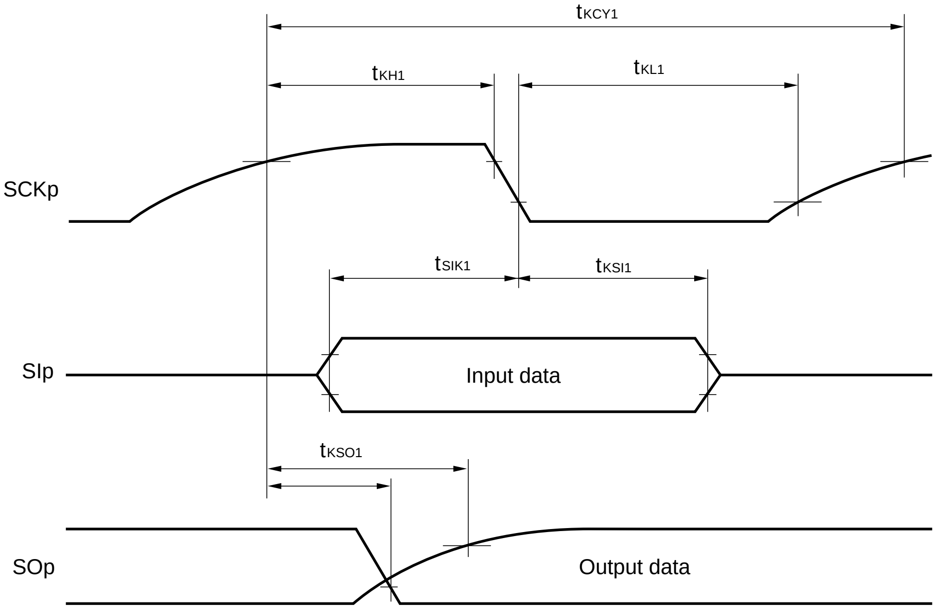
2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input) (T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS[Note 1]		LS[Note 2]		LV[Note 3]		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time[Note 4]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		–		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 5]	24 MHz < f_{MCK}	48/f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		–		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 5]		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to SCKp↑)[Note 6]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 5]		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑)[Note 6]	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output[Note 7]	t_{KSO2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 5], C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

5. Use it with EV_{DD0} ≥ V_b.

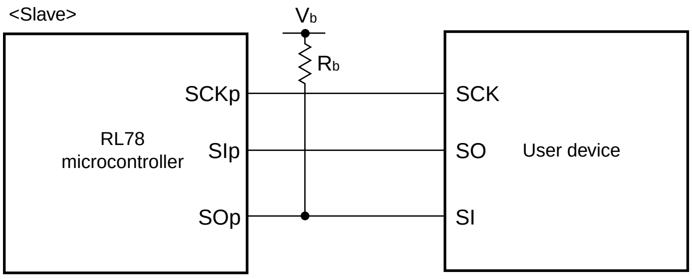
6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓“ when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑“ when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

<R> **Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



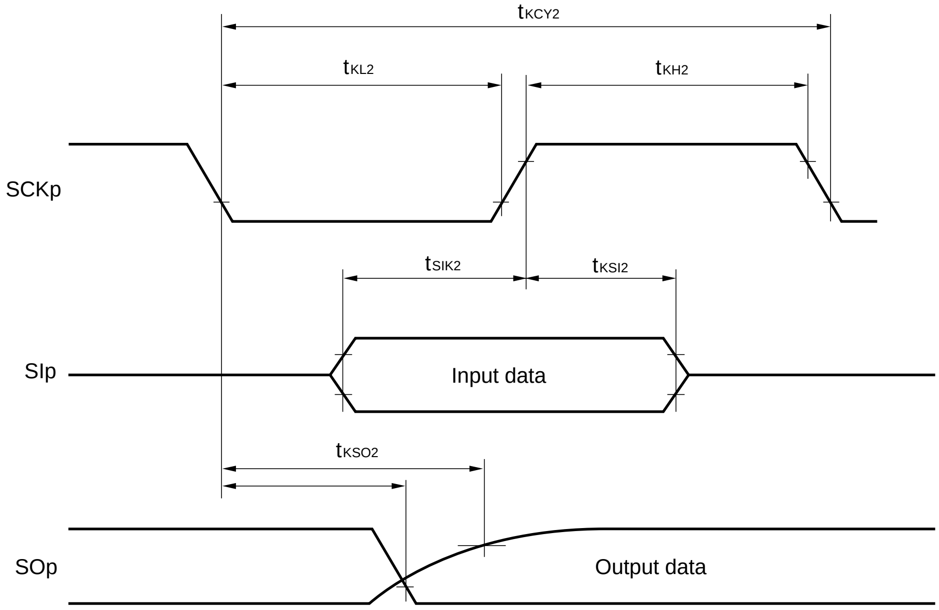
Remarks 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)

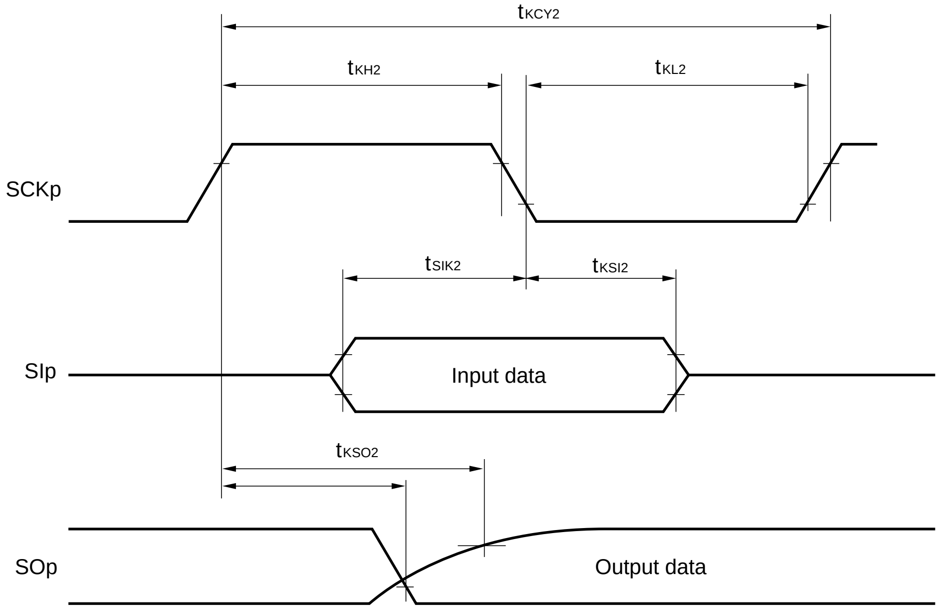
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

4. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	$HS^{\text{Note 1}}$		$LS^{\text{Note 2}}$		$LV^{\text{Note 3}}$		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		$1000^{\text{Note 4}}$		$300^{\text{Note 4}}$		$300^{\text{Note 4}}$	kHz
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		$400^{\text{Note 4}}$		$300^{\text{Note 4}}$		$300^{\text{Note 4}}$	kHz
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 $V^{\text{Note 5}}$, C_b = 100 pF, R_b = 5.5 kΩ		$300^{\text{Note 4}}$		$300^{\text{Note 4}}$		$300^{\text{Note 4}}$	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 $V^{\text{Note 5}}$, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		610		610		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 $V^{\text{Note 5}}$, C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(10) Communication at different potential (1.8 V, 2.5 V) (simplified I^2C mode) (2/2)
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	HS$^{\text{Note 1}}$		LS$^{\text{Note 2}}$		LV$^{\text{Note 3}}$		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK} + 135^{\text{Note 6}}$		$1/f_{MCK} + 190^{\text{Note 6}}$		$1/f_{MCK} + 190^{\text{Note 6}}$		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK} + 190^{\text{Note 6}}$		$1/f_{MCK} + 190^{\text{Note 6}}$		$1/f_{MCK} + 190^{\text{Note 6}}$		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V$^{\text{Note 5}}$, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK} + 190^{\text{Note 6}}$		$1/f_{MCK} + 190^{\text{Note 6}}$		$1/f_{MCK} + 190^{\text{Note 6}}$		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V$^{\text{Note 5}}$, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The value must also be f_{CLK}/4 or lower.

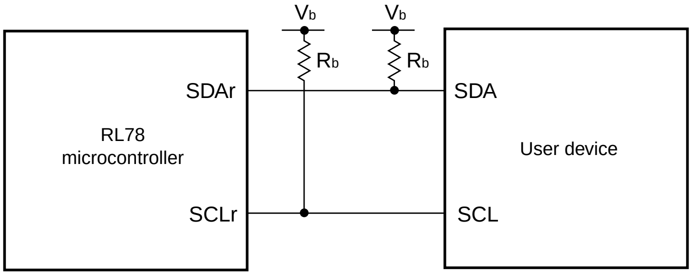
5. Use it with EV_{DD0} ≥ V_b.

6. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

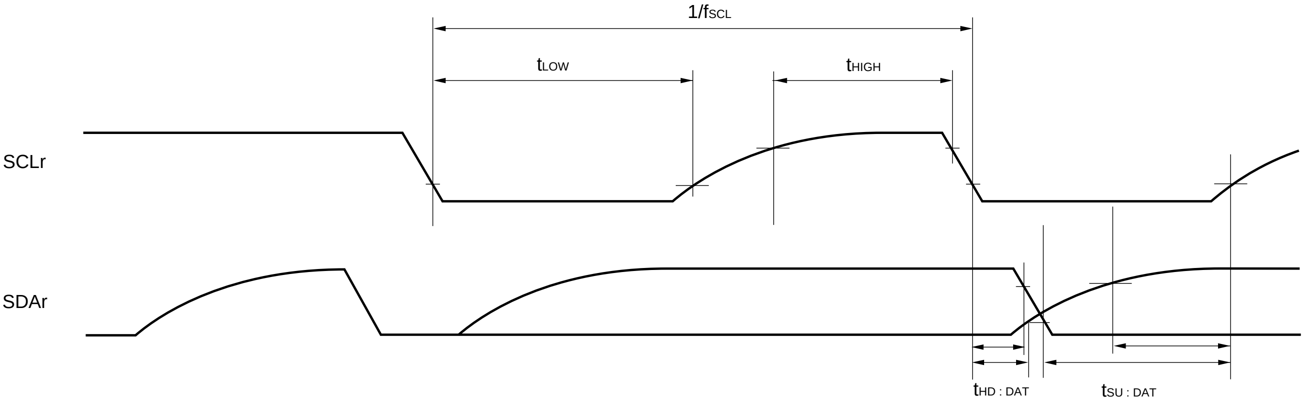
<R> **Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

Simplified I^2C mode connection diagram (during communication at different potential)



Simplified I^2C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10)

4. IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	Standard Mode[Note 1]						Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	100	0	100	0	100	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		0	100	0	100	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	250		250		250		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		250		250		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	0	3.45	0	3.45	0	3.45	
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–	–	0	3.45	0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.0		4.0		4.0		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.0		4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.7 V ≤ EV_{DD0} ≤ 3.6 V	4.7		4.7		4.7		
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	–		4.7		4.7		

(**Note** and **Remark** are listed on the next page.)

(2) I^{2}C fast mode, fast mode plus
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

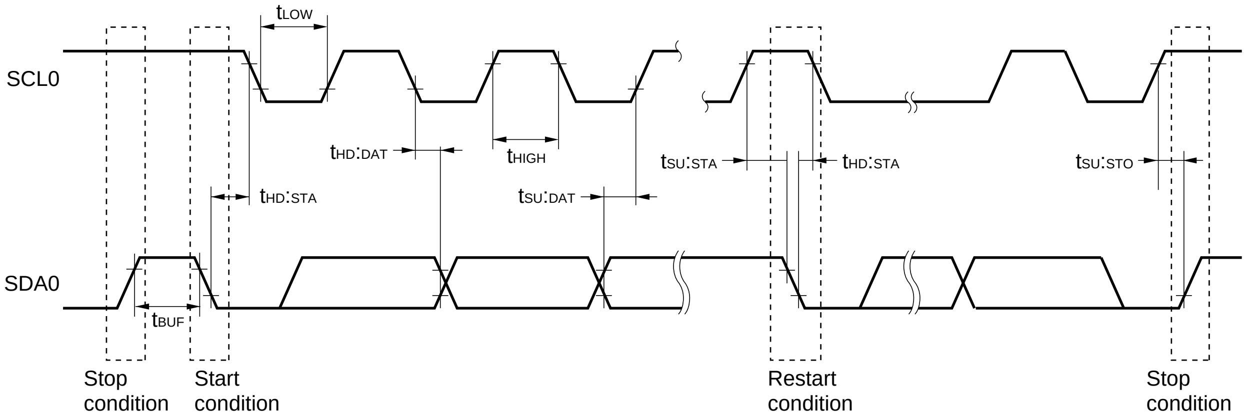
Parameter	Symbol	Conditions	Fast Mode[Note 7]						Fast Mode Plus[Note 8]		Unit
			HS[Note 2]		LS[Note 3]		LV[Note 4]		HS[Note 2]		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	0	1000	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	400	0	400	0	400	–		
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time[Note 5]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		50		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	100		100		100		–		
Data hold time (transmission)[Note 6]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	0	450	µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0	0.9	0	0.9	0	0.9	–		
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		0.26		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	0.6		0.6		0.6		–		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		0.5		µs
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	1.3		1.3		1.3		–		

Notes
1. In normal mode, use it with f_{CLK} ≥ 1 MHz, 1.6 V ≤ EV_{DD} ≤ 3.6 V.
2. HS is condition of HS (high-speed main) mode.
3. LS is condition of LS (low-speed main) mode.
4. LV is condition of LV (low-voltage main) mode.
5. The first clock pulse is generated after this period when the start/restart condition is detected.
6. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
7. In fast mode, use it with f_{CLK}≥ 3.5 MHz, 1.8 V ≤ EV_{DD} ≤ 3.6 V.
8. In fast mode plus, use it with f_{CLK}≥ 10 MHz, 2.7 V ≤ EV_{DD} ≤ 3.6 V.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Division of A/D Converter Characteristics

Reference voltag Input channel	Reference voltage (+) = AV$_{REFP}$ Reference voltage (–) = AV$_{REFM}$	Reference voltage (+) = AV$_{DD}$ Reference voltage (–) = AV$_{SS}$	Reference voltage (+) = Internal refrence voltage Reference voltage (–) = AV$_{SS}$
High-accuracy channel; ANI0 to ANI12 (input buffer power supply: AV$_{DD}$)	See **2.6.1 (1)** See **2.6.1 (2)**	See **2.6.1 (3)**	See **2.6.1 (6)**
Standard channel; ANI16 to ANI30 (input buffer power supply: V$_{DD}$ or EV$_{DD0}$)	See **2.6.1 (4)**	See **2.6.1 (5)**	
Temperature sensor, internal reference voltage output	See **2.6.1 (4)**	See **2.6.1 (5)**	–

<R> **(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12**

<R> **(T_A = –40 to +85°C, 2.4 V ≤ AV$_{REFP}$ ≤ AV$_{DD}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = 0 V, AV$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (–) = AV$_{REFM}$ = 0 V, HALT mode)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$				12	bit
Overall error Notes 1, 2, 3	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t$_{CONV}$	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error Notes 1, 2, 3	E$_{ZS}$	12-bit resolution		±1.3	±3.2	LSB
Full-scale error Notes 1, 2, 3	E$_{FS}$	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error Notes 1, 2, 3	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error Notes 1, 2, 3	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V$_{AIN}$		0		AV$_{REFP}$	V

Notes 1. TYP. Value is the average value at AV$_{DD}$ = AV$_{REFP}$ = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV$_{REFP}$ from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

<R> (2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		10[Note 1]	
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8[Note 2]			
Overall error[Note 3]	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution[Note 1]	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution[Note 2]	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	10.25			
Zero-scale error[Note 3]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
Full-scale error[Note 3]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
Integral linearity error[Note 3]	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.0	
Differential linearity error[Note 3]	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.0	
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error (±1/2 LSB).

<R> **(3) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI12**

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10[Note 1]	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8[Note 2]			
Overall error[Note 3]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution[Note 1]	1.8 V ≤ AV_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution[Note 2]	1.6 V ≤ AV_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	10.25			
Zero-scale error[Note 3]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error[Note 3]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error[Note 3]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error[Note 3]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
<R> Analog input voltage	V_{AIN}			0		AV_{DD}	V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error (±1/2 LSB).

<R> **(4) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		10$^{\text{Note 1}}$	
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V		8$^{\text{Note 2}}$		
Overall error$^{\text{Note 3}}$	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±7.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution$^{\text{Note 1}}$	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution$^{\text{Note 2}}$	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error$^{\text{Note 3}}$	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error$^{\text{Note 3}}$	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error$^{\text{Note 3}}$	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error$^{\text{Note 3}}$	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)			$V_{BGR}$$^{\text{Note 4}}$		V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)			$V_{TMPS25}$$^{\text{Note 4}}$		V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error (±1/2 LSB).

4. See **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R>

(5) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD0} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10[Note 1]	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8[Note 2]			
Overall error[Note 3]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution[Note 1]	1.8 V ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution[Note 2]	1.6 V ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.3125			μs
			1.8 V ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error[Note 3]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Full-scale error[Note 3]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Integral linearity error[Note 3]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error[Note 3]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
Analog input voltage	V_{AIN}			0		AV_{DD} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR}[Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25}[Note 4]			V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error (±1/2 LSB).

4. See **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R> **(6) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV$_{SS}$ (ADREFM = 0), target ANI pin: ANI0 to ANI12, ANI16 to ANI30**

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD} ≤ V_{DD}, 1.6 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (–) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		bit
Conversion time	t_{CONV}	8-bit resolution	16			μs
Zero-scale error^{Note}	E_{ZS}	8-bit resolution			±4.0	LSB
Integral linearity error^{Note}	ILE	8-bit resolution			±2.0	LSB
Differential linearity error^{Note}	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	1.38	1.45	1.5	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

2.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, HS (high-speed main) mode)

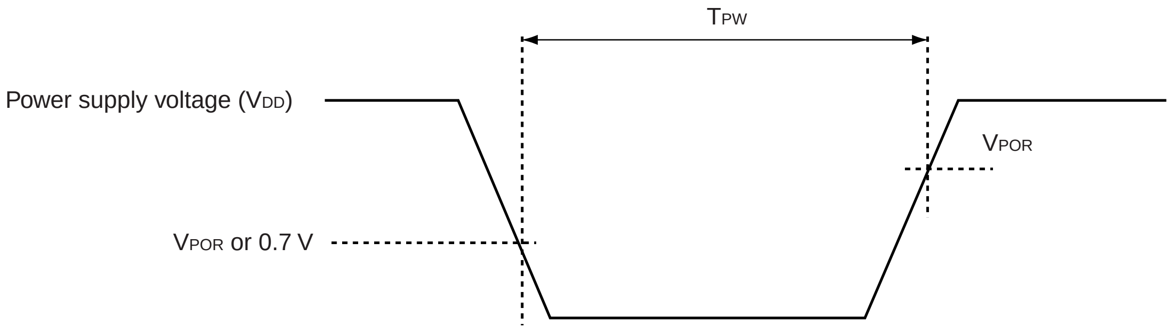
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width^{Note}	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V@1 MHz to 32 MHz

V_{DD} = 2.4 to 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 3.6 V@1 MHz to 8 MHz

LV (low-voltage main) mode: V_{DD} = 1.6 to 3.6 V@1 MHz to 4 MHz

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt & reset mode	V_{LVD13}	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V_{LVD12}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVD11}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVD4}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD11}	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVD10}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVD9}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVD2}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVD8}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVD7}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVD6}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVD4}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD3}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V@1 MHz to 32 MHz
V_{DD} = 2.4 to 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: V_{DD} = 1.8 to 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: V_{DD} = 1.6 to 3.6 V@1 MHz to 4 MHz

2.6.5 Supply voltage rise slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage rise	SV_{DD}				54	V/ms

Caution Be sure to maintain the internal reset state until V_{DD} reaches the operating voltage range specified in 2.4 AC Characteristics, by using the LVD circuit or external reset pin.

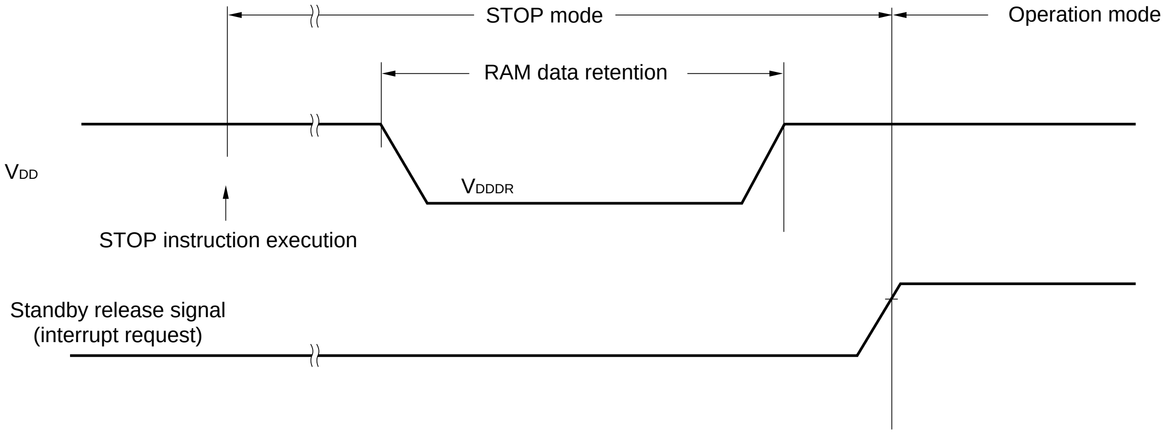
<R> 2.7 RAM Data Retention Characteristics

<R> **(T_A = –40 to +85°C, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46^{Note}		3.6	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>



<R> 2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites[Notes 1, 2]	C_{erwr}	Retained for 20 years T_A = 85°C[Note 3]	1,000			Times
Number of data flash rewrites[Notes 1, 2]		Retained for 1 years T_A = 25°C[Note 3]		1,000,000		
		Retained for 5 years T_A = 85°C[Note 3]	100,000			
		Retained for 20 years T_A = 85°C[Note 3]	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

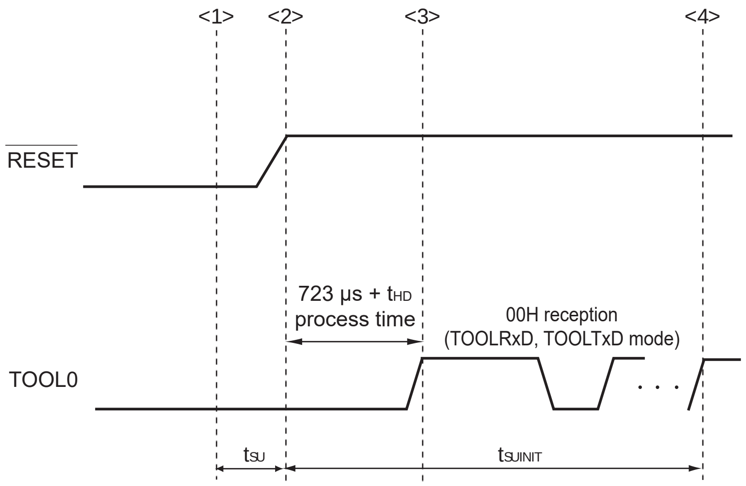
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115.2 k		1 M	bps

2.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
<R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

<R>



<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications T_A = –40 to +105°C
R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB
R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA
R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

Cautions

1. **The RL78/G1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**
2. **With products not provided with an EV_{DD0} or EV_{SS0} pin, replace EV_{DD0} with V_{DD}, or replace EV_{SS0} with V_{SS}.**
3. **Please contact Renesas Electronics sales office for derating of operation under T_A = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

Remark When RL78/G1A is used in the range of T_A = –40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS (T_A = –40 to +85°C)**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD0}		−0.5 to +6.5	V
	AV_{DD}		−0.5 to +4.6	V
	AV_{REFP}		−0.3 to AV_{DD} +0.3[Note 3]	V
	EV_{SS0}		−0.5 to +0.3	V
	AV_{SS}		−0.5 to +0.3	V
	AV_{REFM}		−0.3 to AV_{DD} +0.3[Note 3] and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3[Note 2]	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3[Note 2]	V
	V_{I4}	P20 to P27, P150 to P154	−0.3 to AV_{DD} +0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	−0.3 to EV_{DD0} +0.3[Note 2]	V
	V_{O2}	P20 to P27, P150 to P154	−0.3 to AV_{DD} +0.3[Note 2]	V
Analog input voltage	V_{AI1}	ANI16 to ANI30	−0.3 to EV_{DD0} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3[Notes 2, 4]	V
	V_{AI2}	ANI0 to ANI12	−0.3 to AV_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3[Notes 2, 4]	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Must be 4.6 V or lower.

4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS}: Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	–40	mA
		Total of all pins –170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	–70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	–100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P154	–0.1	mA
		Total of all pins		–1.3	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_X)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. See AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

<R> **Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation frequency[Notes 1, 2]	f_{IH}			1		32	MHz
High-speed on-chip oscillator oscillation frequency accuracy		+85 to +105 °C	2.4 V ≤ V_{DD} ≤ 3.6 V	–2		+2	%
		–20 to +85 °C	2.4 V ≤ V_{DD} ≤ 3.6 V	–1		+1	%
		–40 to –20 °C	2.4 V ≤ V_{DD} ≤ 3.6 V	–1.5		+1.5	%
Low-speed on-chip oscillator oscillation frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator oscillation frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

<R> **(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)** **(1/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.4 V ≤ EV_{DD0} ≤ 3.6 V			–3.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			–10.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			–5.0	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			–19.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			–10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4 V ≤ EV_{DD0} ≤ 3.6 V			–29.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P154	2.4 V ≤ AV_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4 V ≤ AV_{DD} ≤ 3.6 V			–1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I_{OH} = –10.0 mA
  Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution **P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> **(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)** **(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141				8.5[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			15.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty ≤ 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			35.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				50.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P154				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4 V ≤ AV_{DD} ≤ 3.6 V			5.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the dury factor > 70% the duty ratio can can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	$0.8EV_{DD0}$		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} ≤ 3.6 V	2.0		EV_{DD0}	V
			TTL input buffer 2.4 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P154		$0.7AV_{DD}$		AV_{DD}	V
	V_{IH4}	P60 to P63		$0.7EV_{DD0}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0		$0.2EV_{DD0}$	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} ≤ 3.6 V	0		0.5	V
			TTL input buffer 2.4 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P154		0		$0.3AV_{DD}$	V
	V_{IL4}	P60 to P63		0		$0.3EV_{DD0}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –2.0 mA	EV_{DD0} – 0.6			V
			2.4 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = –1.5 mA	EV_{DD0} – 0.5			V
	V_{OH2}	P20 to P27, P150 to P154	2.4 V ≤ AV_{DD} ≤ 3.6 V, I_{OH2} = –100 μA	AV_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P154	2.4 V ≤ AV_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 3.0 mA			0.4	V
			2.4 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 2.0 mA			0.4	V

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (5/5)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141	V_I = EV_{DD0}				1	μA
	I_{LIH2}	P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P20 to P27, P150 to P154	V_I = AV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141	V_I = EV_{SS0}				–1	μA
	I_{LIL2}	P137, $\overline{\text{RESET}}$	V_I = V_{SS}				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
	I_{LIL4}	P20 to P27, P150 to P154	V_I = AV_{SS}				–1	μA
On-chip pull-up resistance	R_U	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	V_I = EV_{SS0}, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} [Note 1]	Operating mode	HS (high-speed main) mode [Note 5]	f_{IH} = 32 MHz [Note 3]	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.6	7.5	mA
				f_{IH} = 24 MHz [Note 3]	Normal operation	V_{DD} = 3.0 V		3.7	5.8	mA
				f_{IH} = 16 MHz [Note 3]	Normal operation	V_{DD} = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode [Note 5]	f_{MX} = 20 MHz [Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 10 MHz [Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
			Subsystem clock mode	f_{SUB} = 32.768 kHz [Note 4] T_A = –40°C	Normal operation	Square wave input		4.1	4.9	µA
						Resonator connection		4.2	5.0	
				f_{SUB} = 32.768 kHz [Note 4] T_A = +25°C	Normal operation	Square wave input		4.2	4.9	µA
						Resonator connection		4.3	5.0	
				f_{SUB} = 32.768 kHz [Note 4] T_A = +50°C	Normal operation	Square wave input		4.3	5.5	µA
						Resonator connection		4.4	5.6	
				f_{SUB} = 32.768 kHz [Note 4] T_A = +70°C	Normal operation	Square wave input		4.5	6.3	µA
						Resonator connection		4.6	6.4	
				f_{SUB} = 32.768 kHz [Note 4] T_A = +85°C	Normal operation	Square wave input		4.8	7.7	µA
						Resonator connection		4.9	7.8	
				f_{SUB} = 32.768 kHz [Note 4] T_A = +105°C	Normal operation	Square wave input		6.9	19.7	µA
						Resonator connection		7.0	19.8	

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer and watchdog timer

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: V_{DD} = 2.7 V to 3.6 V@1 MHz to 32 MHz
V_{DD} = 2.4 V to 3.6 V@1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(2/3)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 3.0 V		0.54	2.90	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 3.0 V		0.44	2.30	mA
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V		0.40	1.70	mA
			HS (high-speed main) mode[Note 7]	f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	
			Subsystem clock mode	f_{SUB} = 32.768 kHz[Note 5] T_A = –40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +50°C	Square wave input		0.38	1.17	μA
					Resonator connection		0.57	1.36	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +70°C	Square wave input		0.52	1.97	μA
					Resonator connection		0.71	2.16	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +85°C	Square wave input		0.97	3.37	μA
					Resonator connection		1.16	3.56	
				f_{SUB} = 32.768 kHz[Note 5] T_A = +105°C	Square wave input		3.01	15.37	μA
					Resonator connection		3.20	15.56	
	I_{DD3}[Note 6]	STOP mode[Note 8]	T_A = –40°C				0.16	0.50	μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.34	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	
			T_A = +105°C				2.94	15.30	

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and data flash rewriting.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). Including the current flowing into the RTC. However, not including the current flowing into the 12-bit interval timer, and watchdog timer.

6. When subsystem clock is stopped. Not including the current flowing into the RTC, 12-bit interval timer, watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) **(3/3)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} [Note 1]				0.20		μA
RTC operating current	I_{RTC} [Notes 1, 2, 3]				0.02		μA
12-bit interval timer operating current	I_{IT} [Notes 1, 2, 4]				0.02		μA
Watchdog timer operating current	I_{WDT} [Notes 1, 2, 5]	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} [Notes 6, 7]	AV_{DD} = 3.0 V, When conversion at maximum speed			420	720	μA
$AV_{REF(+)}$ current	I_{AVREF} [Note 8]	AV_{DD} = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 [Note 7]			14.0	25.0	μA
		AV_{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 [Note 10]			14.0	25.0	μA
		ADREFP1 = 1, ADREFP0 = 0 [Note 1]			14.0	25.0	μA
A/D converter reference voltage current	I_{ADREF} [Notes 1, 9]	V_{DD} = 3.0 V			75.0		μA
Temperature sensor operating current	I_{TMPS} [Note 1]	V_{DD} = 3.0 V			75.0		μA
LVD operating current	I_{LVD} [Notes 1, 11]				0.08		μA
BGO operating current	I_{BGO} [Notes 1, 12]				2.5	12.2	mA
Self-programming operating current	I_{FSP} [Notes 1, 13]				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ}	A/D converter operation (AV_{DD} = 3.0 V)	The mode is performed [Notes 1, 14]		0.50	1.10	mA
			During A/D conversion [Note 1]		0.60	1.34	mA
			During A/D conversion [Note 7]		420	720	μA
		CSI/UART operation [Note 1]			0.70	1.54	mA

(**Notes** and **Remarks** are listed on the next page.)

<R> **Notes**

1. Current flowing to V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing to the AV_{DD}.

8. Current flowing from the reference voltage source of A/D converter.

9. Operation current flowing to the internal reference voltage.

10. Current flowing to the AV_{REFP}.

11. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

12. Current flowing only during data flash rewrite.

13. Current flowing only during self programming.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

3.4 AC Characteristics

(T_A = –40 to +105°C, AV_{DD} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

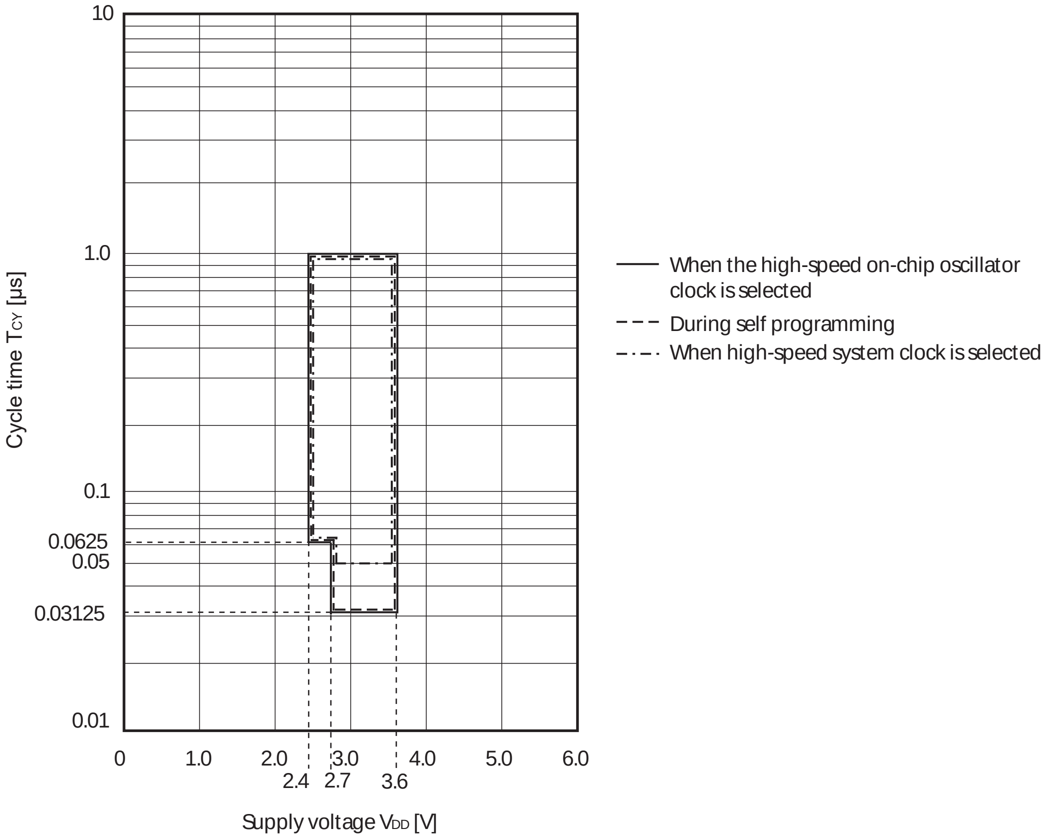
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation		2.4 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				$1/f_{MCK}+10$			ns$^{\text{Note}}$
TO00, TO01, TO03 to TO07 output frequency	f_{TO}	HS (high-speed main) mode	2.7 V ≤ EV_{DD0} ≤ 3.6 V				8	MHz
			2.4 V ≤ EV_{DD0} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	2.7 V ≤ EV_{DD0} ≤ 3.6 V				8	MHz
			2.4 V ≤ EV_{DD0} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	2.4 V ≤ V_{DD} ≤ 3.6 V		1			μs
		INTP1 to INTP11	2.4 V ≤ EV_{DD0} ≤ 3.6 V		1			μs
Key interrupt input high-level width, low-level width	t_{KR}	KR0 to KR9	2.4 V ≤ EV_{DD0} ≤ 3.6 V, 2.4 V ≤ AV_{DD0} ≤ 3.6 V		250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Note The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer clock select register 0 (TPS0) and timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

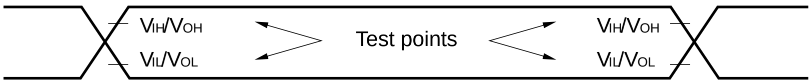
Minimum Instruction Execution Time during Main System Clock Operation

<R> T_{CY} vs V_{DD} (HS (high-speed main) mode)

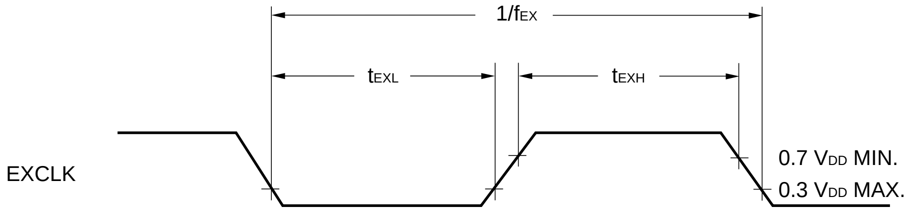


AC Timing Test Points

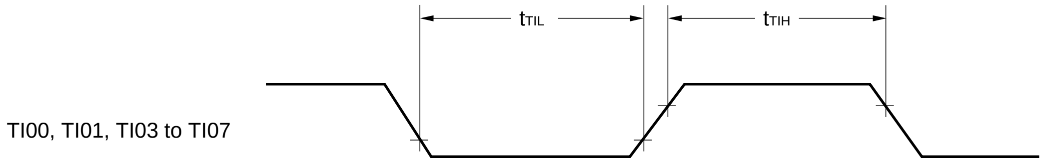
<R>

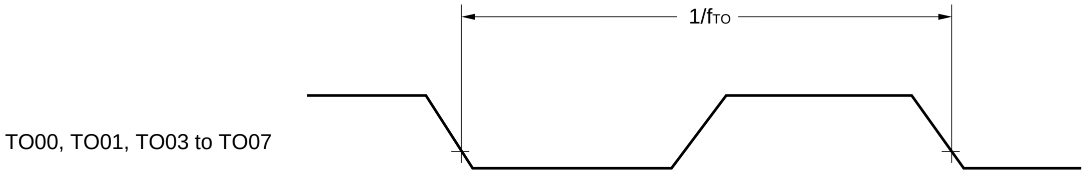


External System Clock Timing

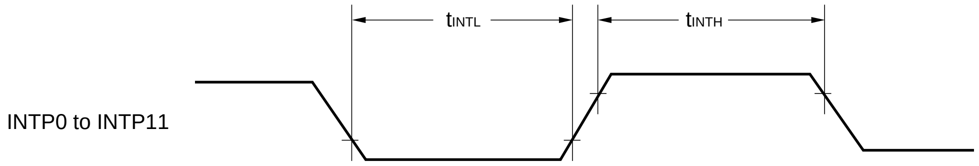


<R> TI/TO Timing

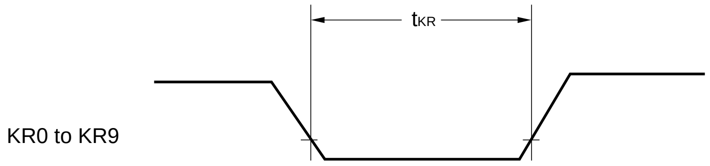




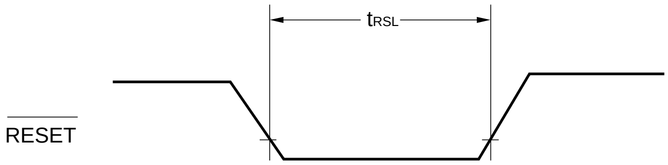
Interrupt Request Input Timing



Key Interrupt Input Timing



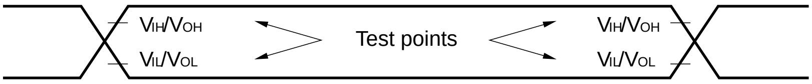
$\overline{\text{RESET}}$ Input Timing



3.5 Peripheral Functions Characteristics

AC Timing Test Points

<R>



3.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

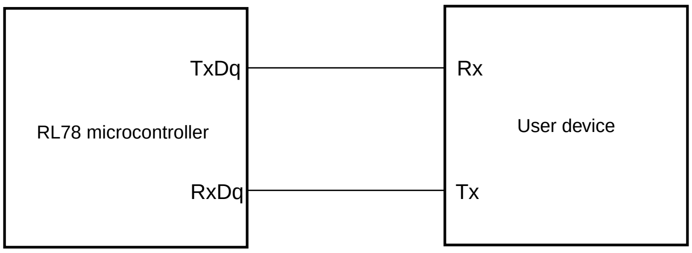
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate[Note 1]						$f_{MCK}/12$	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6[Note 2]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps.

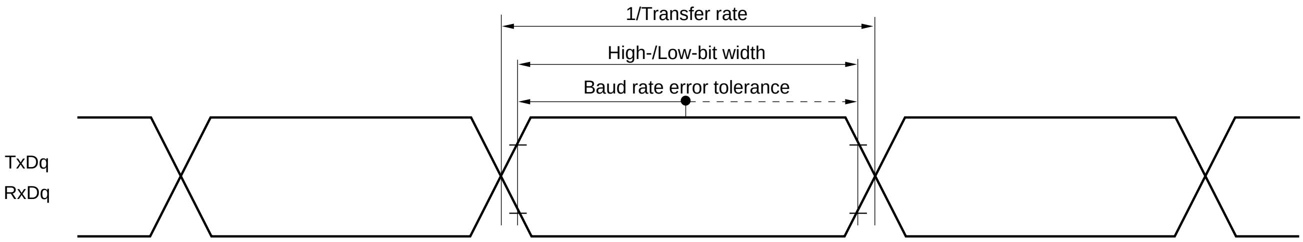
2. The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	$t_{KCY1} \geq 4/f_{CLK}$	250			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	$t_{KCY1} \geq 4/f_{CLK}$	500			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY1}/2 - 36$			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		$t_{KCY1}/2 - 76$			ns
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		66			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		113			ns
SIp hold time (from SCKp↑)Note 1	t_{KSI1}			38			ns
Delay time from SCKp↓ to SOp outputNote 2	t_{KSO1}	C = 30 pNote 3				50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1)

<R> **(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time[Note 1]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	16 MHz < f_{MCK}	16/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		12/f_{MCK} and 1000			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2–14			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		t_{KCY2}/2–16			ns
SIp setup time (to SCKp↑)[Note 2]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} + 40			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK} + 60			ns
SIp hold time (from SCKp↑)[Note 2]	t_{KSI2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK}+62			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK}+62			ns
Delay time from SCKp↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]	2.7 V ≤ EV_{DD0} ≤ 3.6 V			2/f_{MCK}+66	ns
			2.4 V ≤ EV_{DD0} ≤ 3.6 V			2/f_{MCK}+113	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

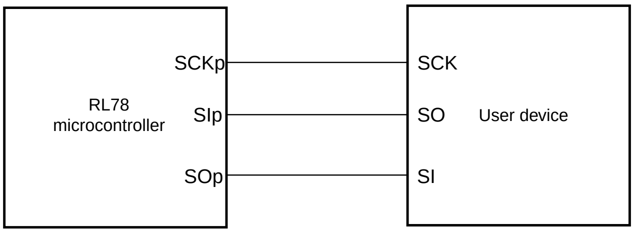
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1)

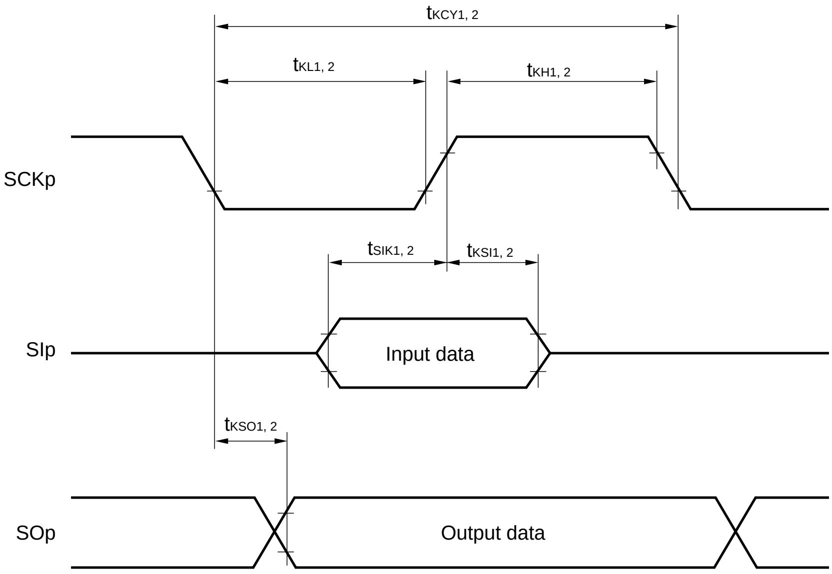
2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

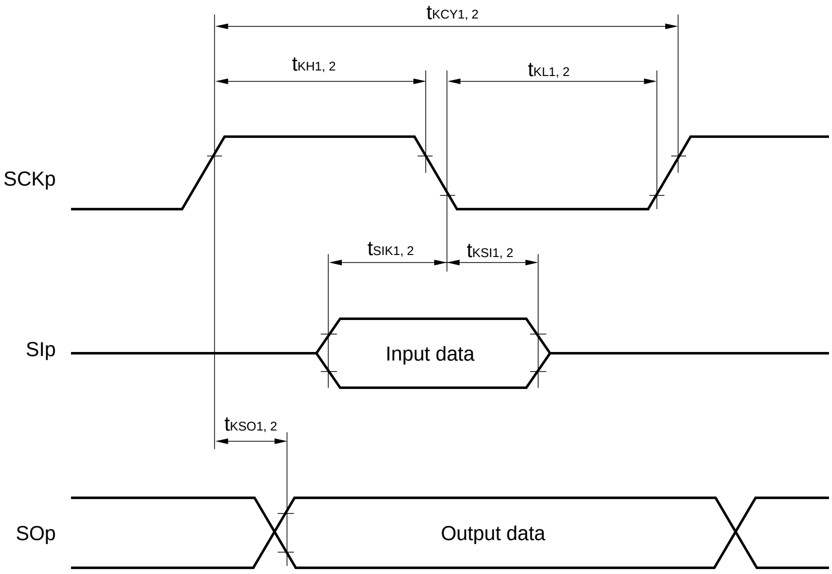
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(4) During communication at same potential (simplified I^{2}C mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

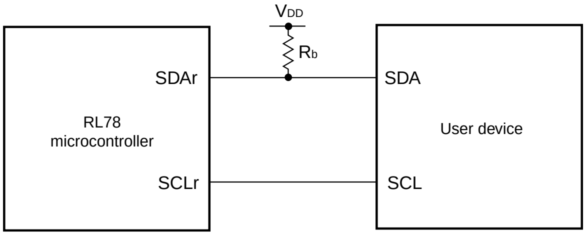
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		400$^{\text{Note 1}}$	kHz
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		100$^{\text{Note 1}}$	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220$^{\text{Note 2}}$		ns
		2.4 V ≤ EV_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580$^{\text{Note 2}}$		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes 1. The value must also be f_{CLK}/4 or lower.

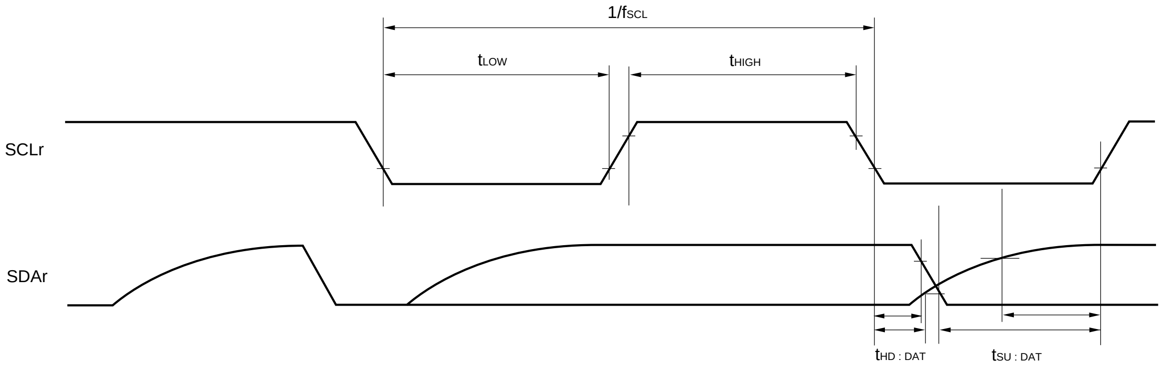
2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I^{2}C mode mode connection diagram (during communication at same potential)



Simplified I^{2}C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate[Note 1]		Reception	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				$f_{MCK}/12$	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				$f_{MCK}/12$	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			2.6[Note 2]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps.

2. The following conditions are required for low-voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.** <R>

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		Transmission	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2[Note 2]	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V			0.43[Note 4]	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} ≤ 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

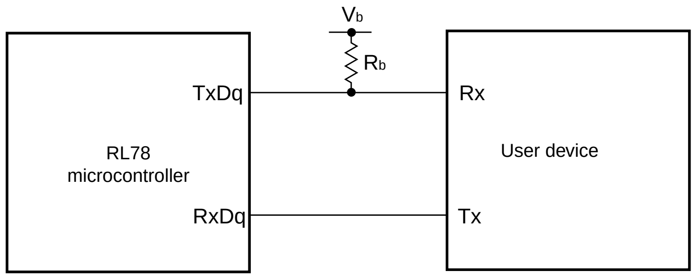
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

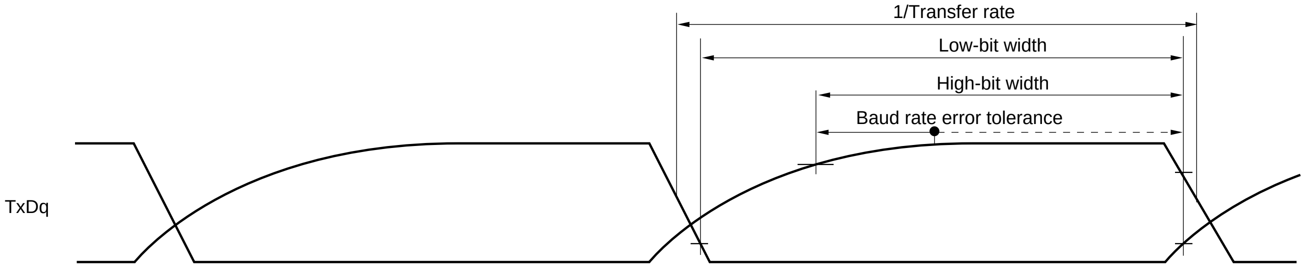
4. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

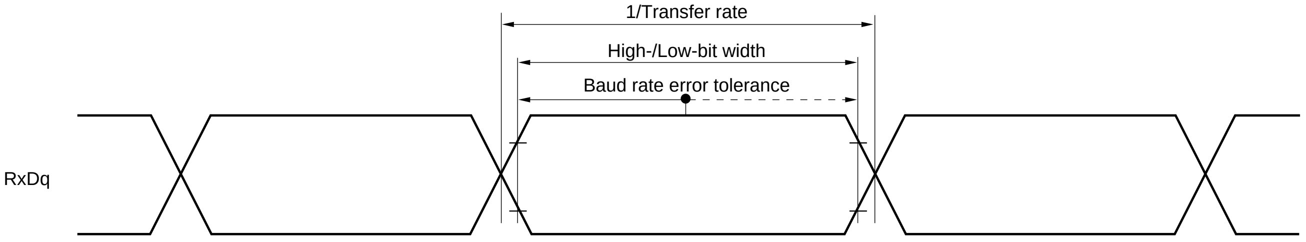
<R> **Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)





Remarks 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)
($T_A = -40$ to $+105°C$, $2.4\ V \le EV_{DD0} \le V_{DD} \le 3.6\ V$, $V_{SS} = EV_{SS0} = 0\ V$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$2.7\ V \le EV_{DD0} \le 3.6\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 30\ pF$, $R_b = 2.7\ k\Omega$	$t_{KCY1} \ge 4/f_{CLK}$	1000			ns
		$2.4\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$, $C_b = 30\ pF$, $R_b = 5.5\ k\Omega$	$t_{KCY1} \ge 4/f_{CLK}$	2300			ns
SCKp high-level width	t_{KH1}	$2.7\ V \le EV_{DD0} \le 3.6\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 30\ pF$, $R_b = 2.7\ k\Omega$		$t_{KCY1}/2 - 340$			ns
		$2.4\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$, $C_b = 30\ pF$, $R_b = 5.5\ k\Omega$		$t_{KCY1}/2 - 916$			ns
SCKp low-level width	t_{KL1}	$2.7\ V \le EV_{DD0} \le 3.6\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 30\ pF$, $R_b = 2.7\ k\Omega$		$t_{KCY1}/2 - 36$			ns
		$2.4\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$, $C_b = 30\ pF$, $R_b = 5.5\ k\Omega$		$t_{KCY1}/2 - 100$			ns

<R> **Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2) (T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

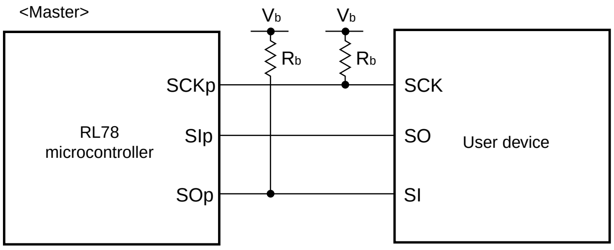
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958			ns
SIp hold time (from SCKp↑)Note 1	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38			ns
Delay time from SCKp↓ to SOp outputNote 1	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			390	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			966	ns
SIp setup time (to SCKp↓)Note 2	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	220			ns
SIp hold time (from SCKp↓)Note 2	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38			ns
Delay time from SCKp↑ to SOp outputNote 2	t_{KSO1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			50	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected. <R>

CSI mode connection diagram (during communication at different potential)

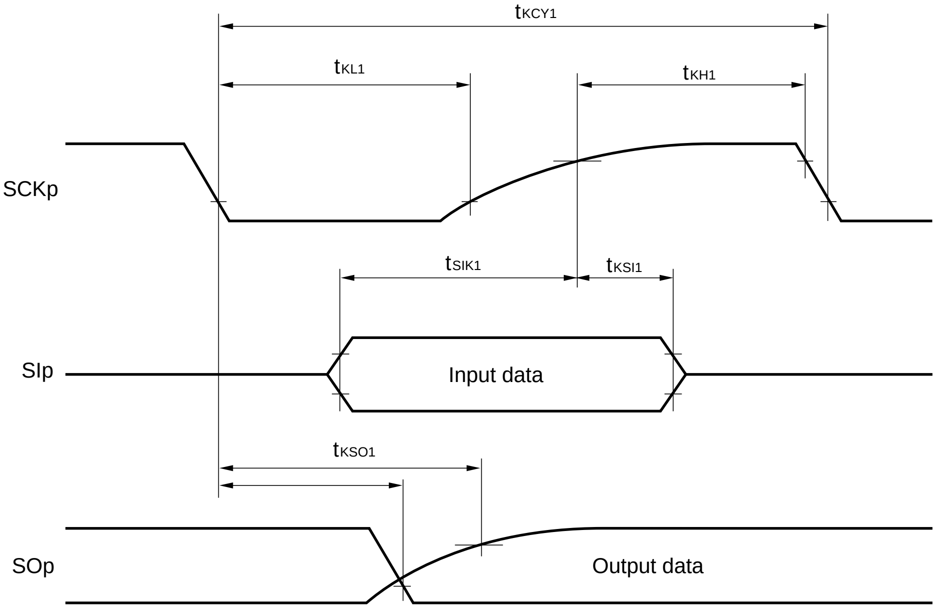


Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

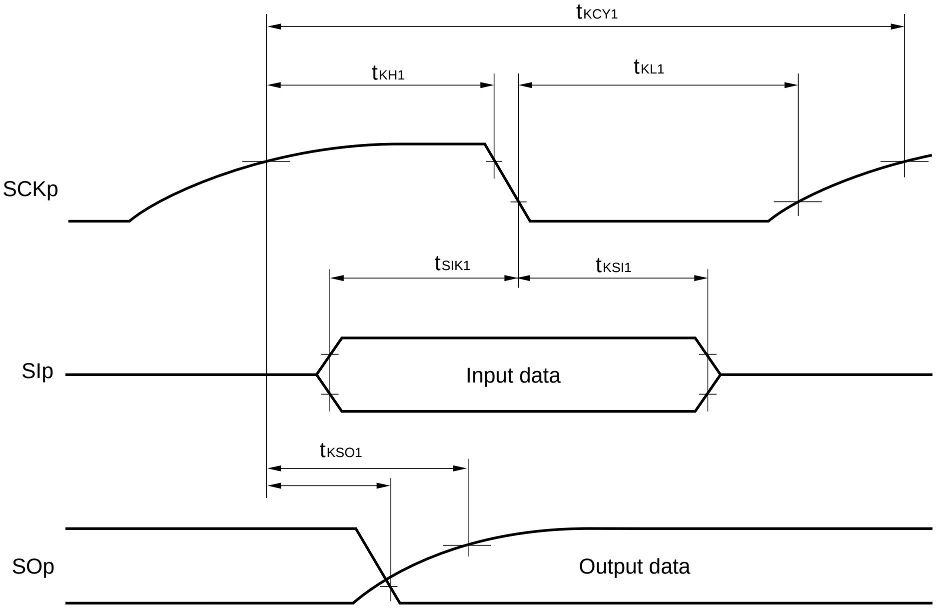
2. p: CSI number (p = 00, 10, 20), m: Unit number , n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input) (T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time[Note 1]	t_{KCY2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	40/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	96/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 36			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 – 100			ns
SIp setup time (to SCKp↑)[Note 2]	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40			ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60			
SIp hold time (from SCKp↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 62			ns
Delay time from SCKp↓ to SOp output[Note 3]	t_{KSO2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ				2/f_{MCK} + 1146	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

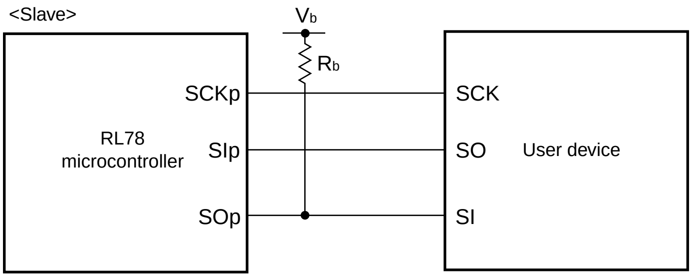
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time becomes “from SCKp↓“ when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑“ when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

<R> **Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



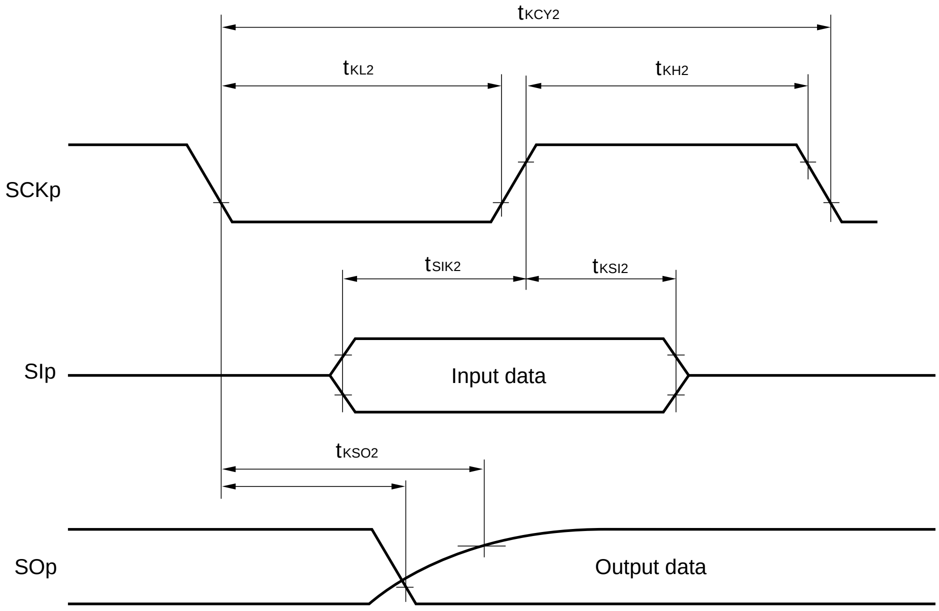
Remarks 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 02, 10), g: PIM and POM number (g = 0, 1)

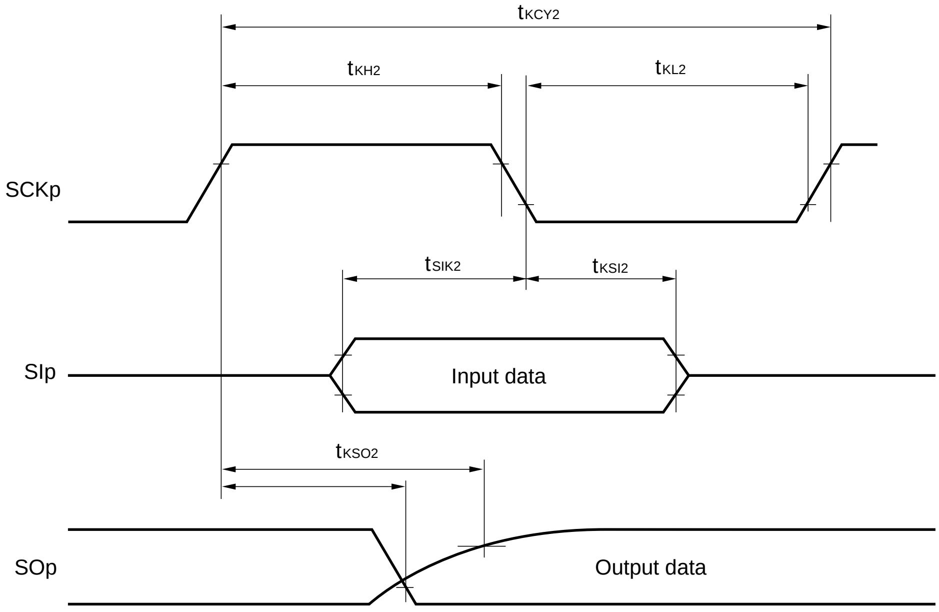
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

4. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11, and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400^{Note 1}	kHz
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100^{Note 1}	kHz
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ		100^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340**Note 2**		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760**Note 2**		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570**Note 2**		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

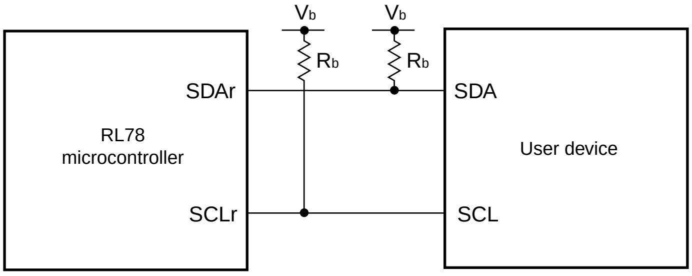
Notes 1. The value must also be f_{CLK}/4 or lower.

2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

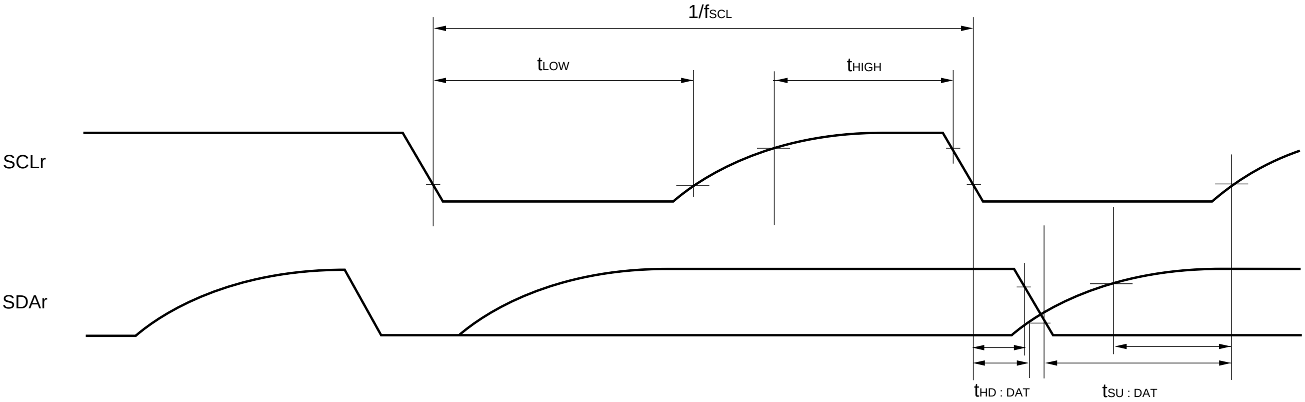
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected. <R>

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10)

4. IIC01, IIC11, and IIC21 cannot communicate at different potential. Use IIC00, IIC10, or IIC20 for communication at different potential.

3.5.2 Serial interface IICA

(1) I^2C standard mode, fast mode

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		Standard Mode		Fast Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.4 V ≤ EV_{DD0} ≤ 3.6 V			0	400	kHz
		Normal mode: f_{CLK} ≥ 1 MHz	2.4 V ≤ EV_{DD0} ≤ 3.6 V	0	100			kHz
Setup time of restart condition	$t_{SU:STA}$			4.7		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$			4.0		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}			4.7		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}			4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$			250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$			0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$			4.0		0.6		μs
Bus-free time	t_{BUF}			4.7		1.3		μs

Notes **1.** The first clock pulse is generated after this period when the start/restart condition is detected.

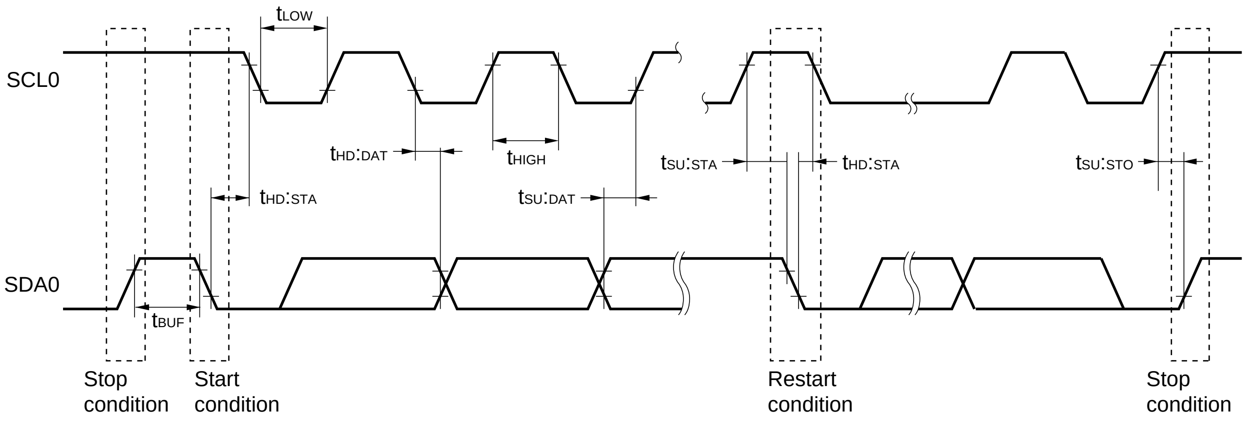
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Division of A/D Converter Characteristics

Reference voltag Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = AV_{DD} Reference voltage (–) = AV_{SS}	Reference voltage (+) = Internal refrence voltage Reference voltage (–) = AV_{SS}
High-accuracy channel; ANI0 to ANI12 (input buffer power supply: AV_{DD})	See **3.6.1 (1)**	See **3.6.1 (2)**	See **3.6.1 (5)**
Standard channel; ANI16 to ANI30 (input buffer power supply: V_{DD} or EV_{DD0})	See **3.6.1 (3)**	See **3.6.1 (4)**	
Temperature sensor, internal reference voltage output	See **3.6.1 (3)**	See **3.6.1 (4)**	–

<R> (1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8.		12.	bit
Overall error[Note]	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.375			μs
Zero-scale error[Note]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
Full-scale error[Note]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
Integral linearity error[Note]	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Differential linearity error[Note]	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note Excludes quantization error (±1/2 LSB).

<R> **(2) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI12**

(T_A = –40 to +105°C, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
Zero-scale error[Note]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Full-scale error[Note]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
Integral linearity error[Note]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
Differential linearity error [Note]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Analog input voltage	V_{AIN}			0		AV_{DD}	V

Note Excludes quantization error (±1/2 LSB).

<R> **(3) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note 1]	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±7.0	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	4.125			μs
Zero-scale error[Note 1]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
Full-scale error[Note 1]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
Integral linearity error[Note 1]	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
Analog input voltage	V_{AIN}			0.		AV_{REFP} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR}[Note 2]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25}[Note 2]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. See **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R> **(4) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI30, interanal reference voltage, temperature sensor output voltage**

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD0} ≤ 3.6 V, 2.4 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error[Note 1]	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
Zero-scale error[Note 1]	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
Full-scale error[Note 1]	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
Integral linearity error[Note 1]	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{DD} and EV_{DD0}	V
		Interanal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR}[Note 2]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMPS25}[Note 2]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. See **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

<R> **(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI12, ANI16 to ANI30**

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ EV_{DD} ≤ V_{DD}, 2.4 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (–) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		8			bit
Conversion time	t_{CONV}	8-bit resolution	16.0			μs
Zero-scale error[Note]	E_{ZS}	8-bit resolution			±4.0	LSB
Integral linearity error[Note]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error[Note]	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	1.38	1.45	1.50	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

3.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, HS (high-speed main) mode)

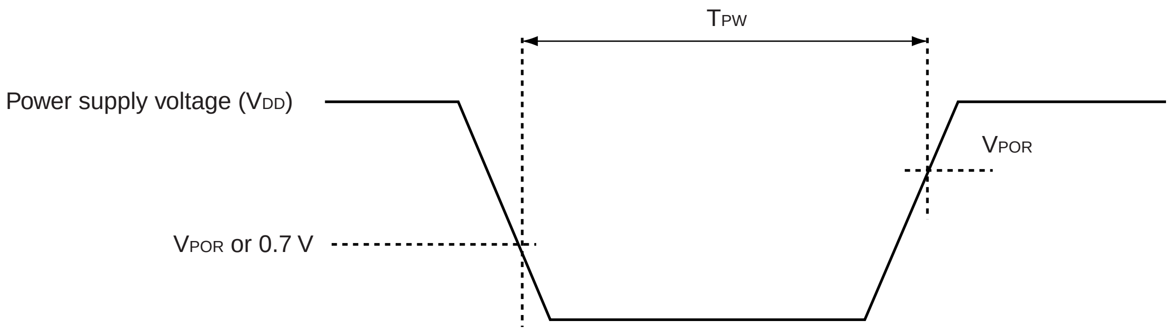
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

3.6.3 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

Remark $V_{LVD\,(n-1)} > V_{LVDn}$: n = 3 to 7

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq 3.6$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt & reset mode	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVD4}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVD3}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V@1 MHz to 32 MHz

V_{DD} = 2.4 to 3.6 V@1 MHz to 16 MHz

3.6.5 Supply voltage rise slope characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage rise	SV_{DD}				54	V/ms

Caution Be sure to maintain the internal reset state until V_{DD} reaches the operating voltage range specified in 3.4 AC Characteristics, by using the LVD circuit or external reset pin.

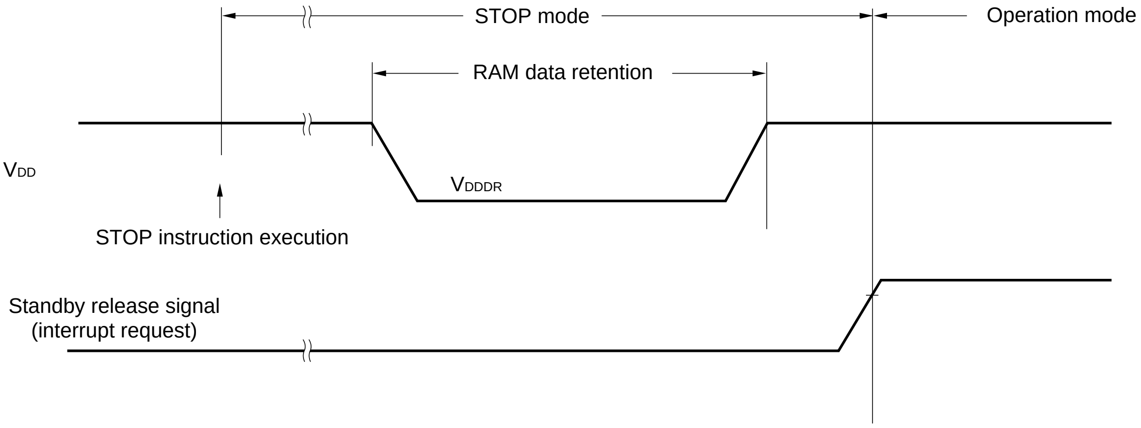
<R> 3.7 RAM Data Retention Characteristics

<R> **(T_A = –40 to +105°C, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		3.6	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R>



3.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 3.6 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **4.** This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

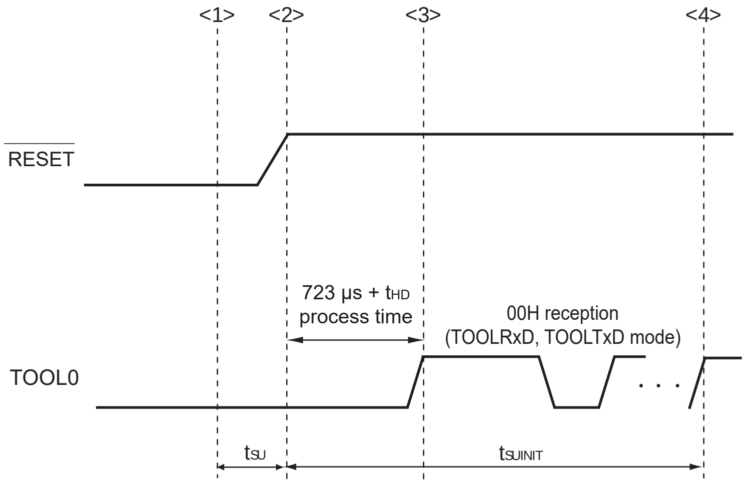
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During flash memory programming	115.2 k		1 M	bps

3.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
<R> How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash firmware processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

<R>



<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends

<R> t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (except flash firmware processing time)

4. PACKAGE DRAWINGS

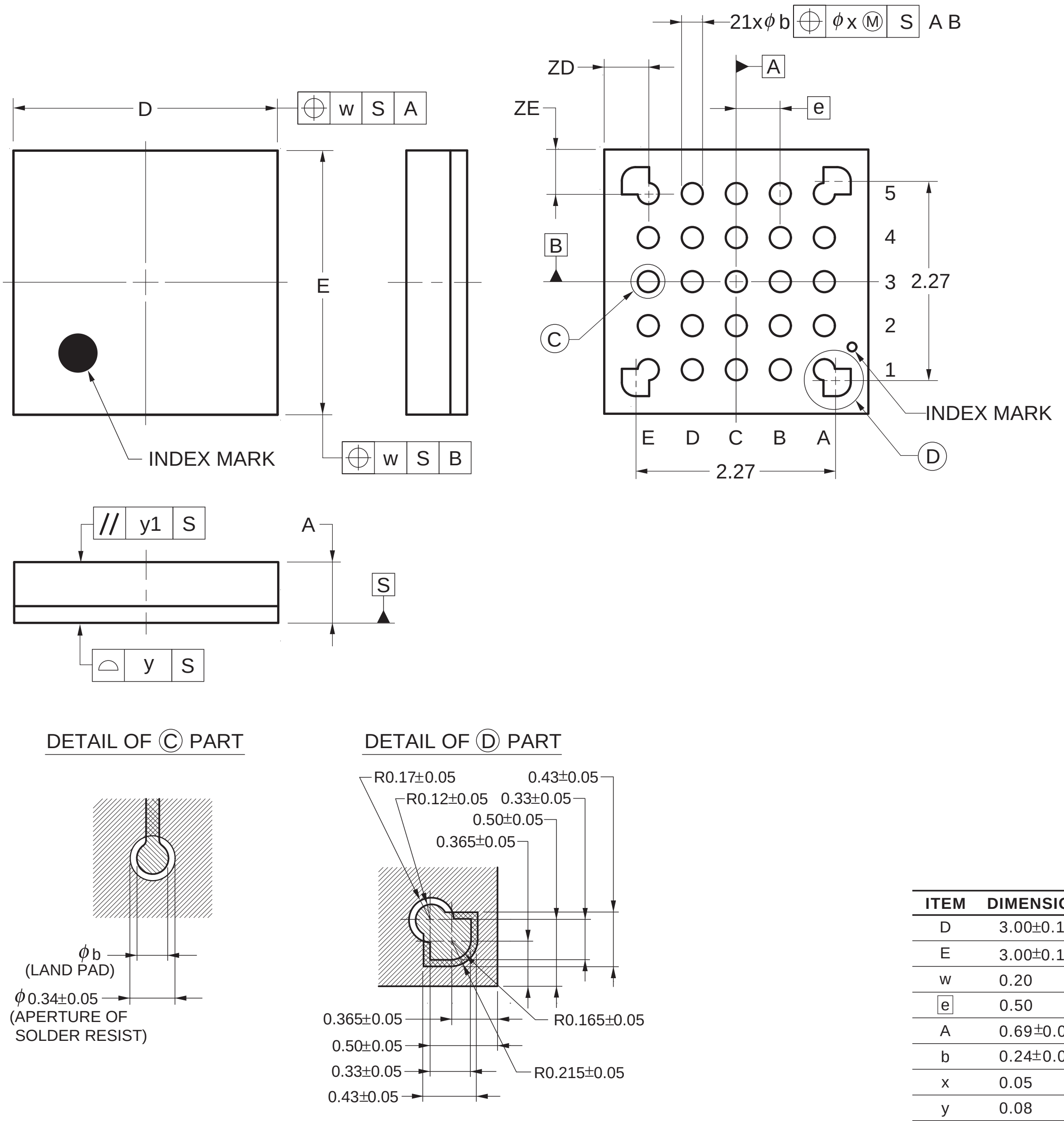
4.1 25-pin products

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-3	0.01

Unit: mm

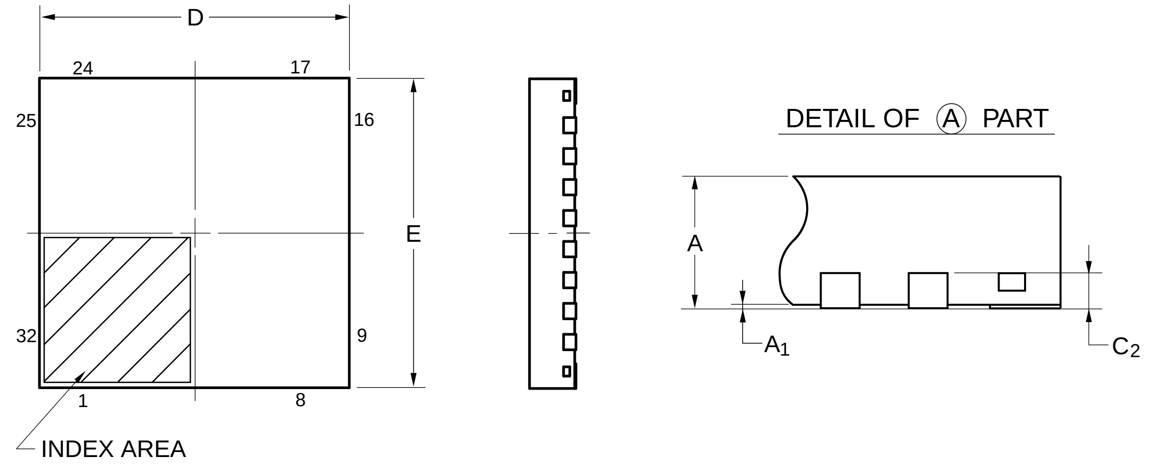


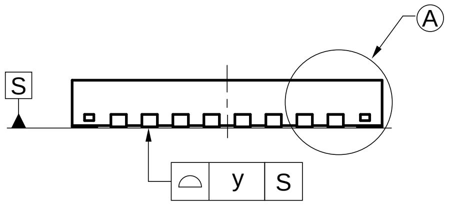
ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

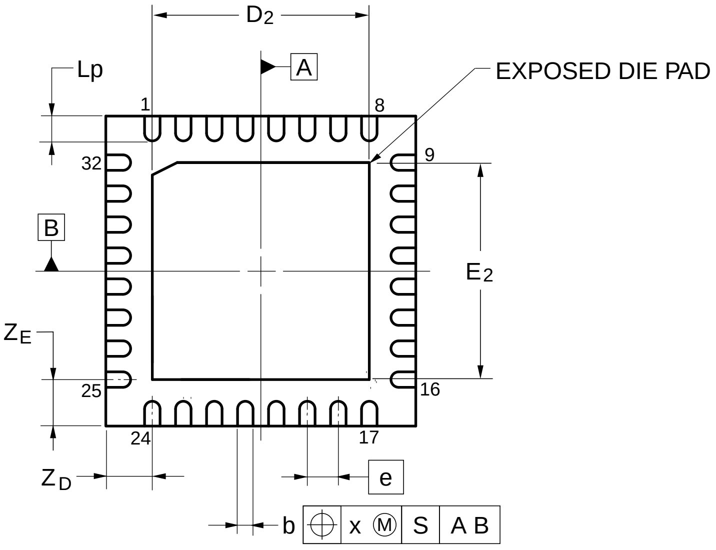
4.2 32-pin products

R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA
R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06





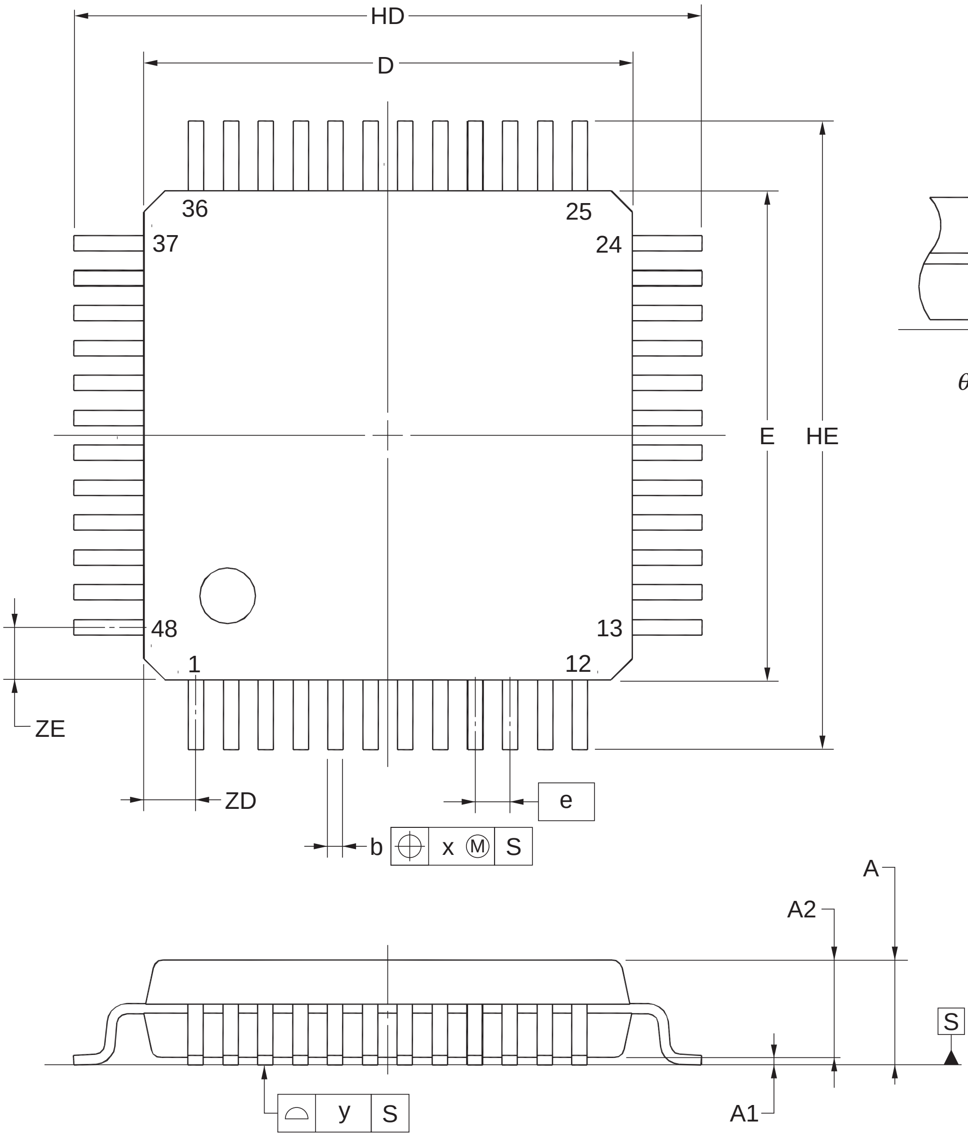


Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	3.50	—
E_2	—	3.50	—

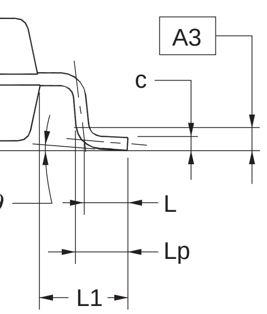
4.3 48-pin products

R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
$\boxed{\text{e}}$	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

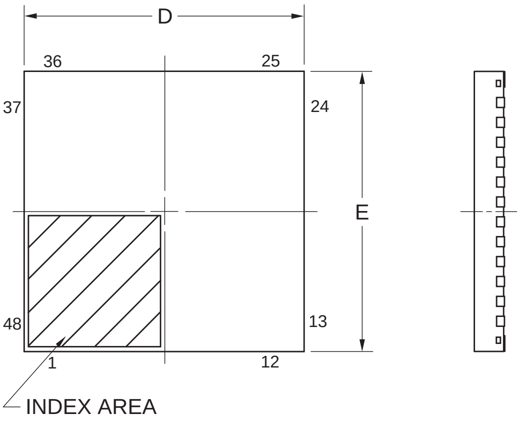
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

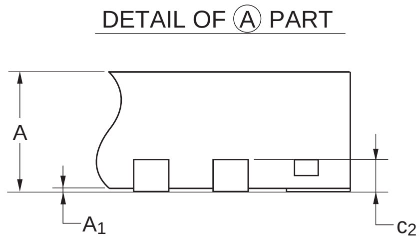
R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA
R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA

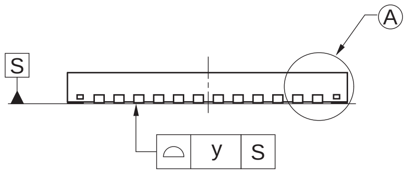
<R>

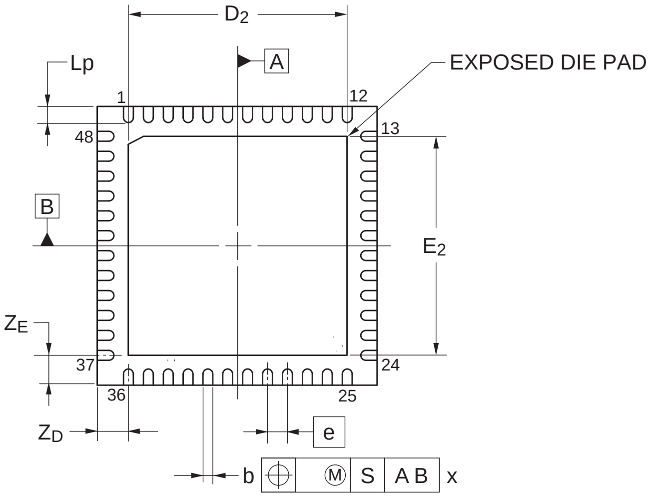
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13

Unit: mm







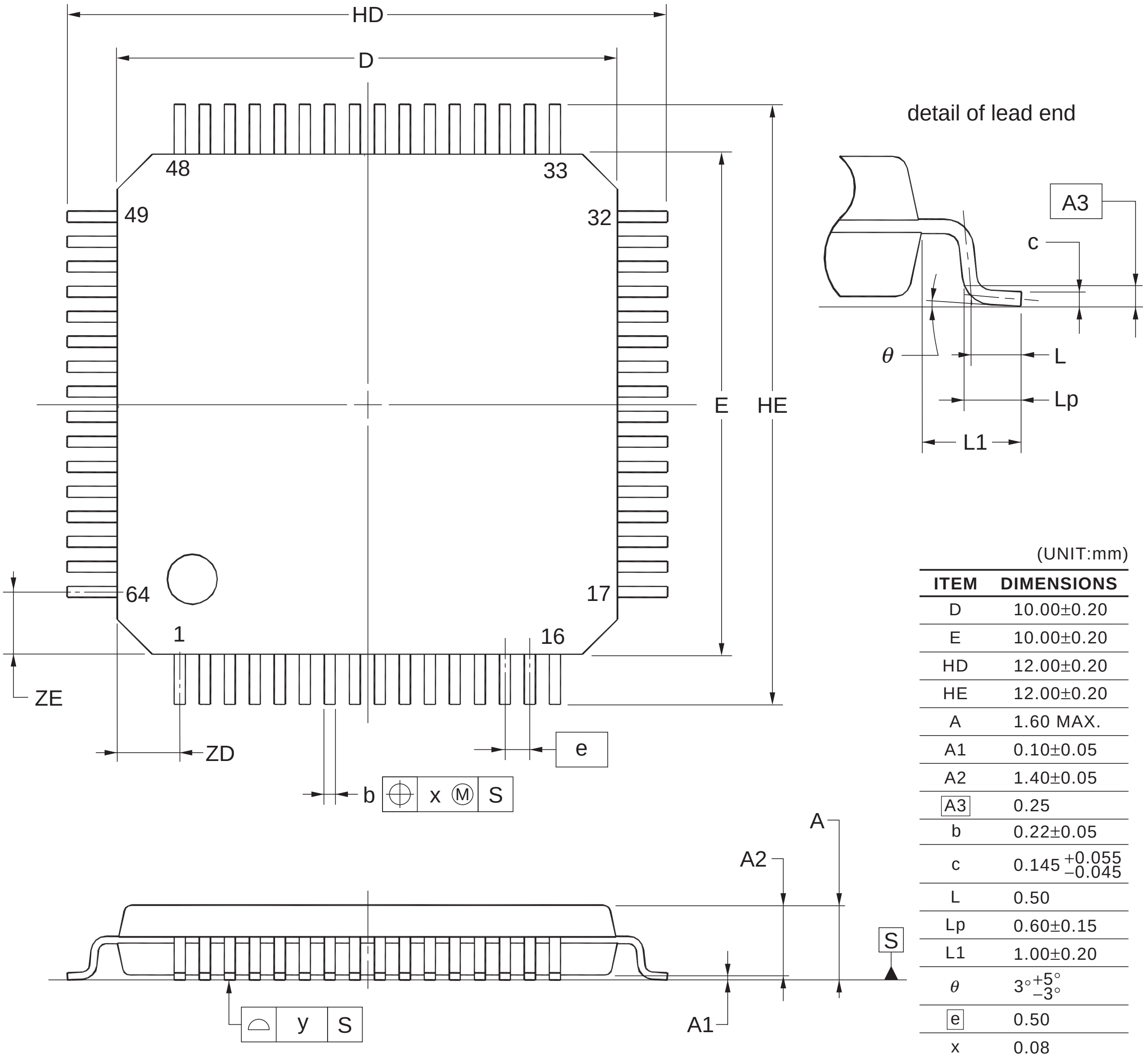


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

4.4 64-pin products

R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB
R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



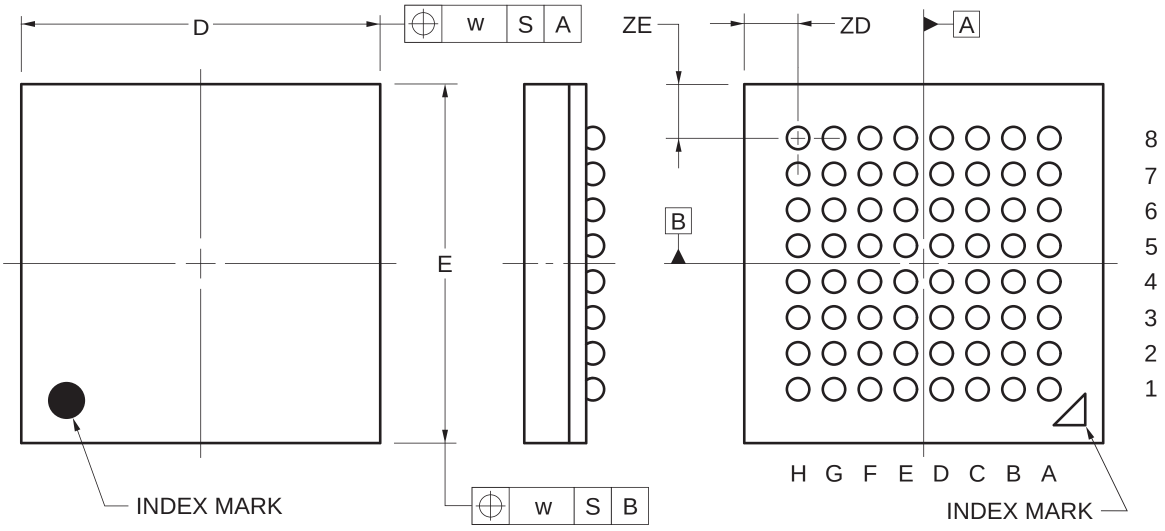
(UNIT:mm)

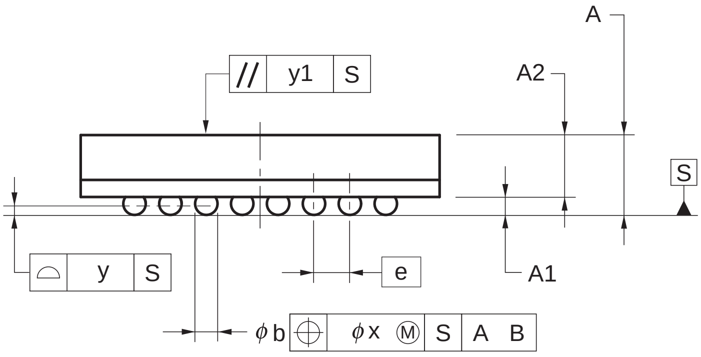
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
$\boxed{\text{e}}$	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

Rev.	**Date**	**Description**	
		Page	**Summary**
0.01	Dec 26, 2011	-	First Edition issued
1.00	Sep 25, 2013	p.1	Modification of 1.1 Features
		p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.6	Modification of Remark 3 to 1.3.2 32-pin products.
		p.13	Modification of 1.5.2 32-pin products.
		p.14	Modification of 1.5.3 48-pin products.
		p.16	Modification of 1.6 Outline of Functions
		p.21	Modification of 2.2.1 X1, XT1 oscillator characteristics
		p.31, 32	Modification of Note 1 in 2.3.2 Supply current characteristics
		p.34, 35	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.37	Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics
		p.46 to 58	Modification of Caution to 2.5.1 Serial array unit.
		p.63 to 68	Modification of 2.6.1 A/D converter characteristics
		p.71	Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		p.71	Modification of 2.8 Flash Memory Programming Characteristics
		p.72	Modification of 2.10 Timing Specs for Switching Flash Memory Programming Modes
		p.73 to 117	Addition of 3 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C)
		p.118 to 123	Modification of 4. PACKAGE DRAWINGS
2.10	Nov 30, 2016	p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.5 to 10	Modification of the position of the index mark in 1.3.1 25-pin products to 1.3.4 64-pin products
		p.6	Modification of Remark 3
		p.13	Modification of 1.5.2 32-pin products
		p.14	Modification of 1.5.3 48-pin products
		p.16	Modification of description in 1.6 Outline of Functions
		p.21	Modification of 2.2.1 X1, XT1 oscillator characteristics
		p.31, 32	Modification of Note 1 in 2.3.2 Supply current characteristics
		p.34, 35	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.36	Modification of AC Timing Test Points and TI/TO Timing
		p.38	Modification of AC Timing Test Points in 2.5 Peripheral Functions Characteristics
		p.48, 50 to 52, 55, 59	Modification of Caution in 2.5.1 Serial array unit
		p.64 to 69	Modification of conditions of 2.6.1 A/D converter characteristics
		p.72	Renamed to 2.7 RAM Data Retention Characteristics, and modification of note and figure
		p.72	Modification of 2.8 Flash Memory Programming Characteristics

Rev.	Date	Description	
		Page	Summary
2.10	Nov 30, 2016	p.73	Modification of 2.10 Timing Specs for Switching Flash Memory Programming Modes
		p.77	Modification of 3.2.1 X1, XT1 oscillator characteristics
		p.78, 79	Modification of 3.3.1 Pin characteristics
		p.88	Modification of 3.3.2 Supply current characteristics
		p.90	Modification of Minimum Instruction Execution Time during Main System Clock Operation
		p.91	Modification of AC Timing Test Points and TI/TO Timing
		p.93	Modification of AC Timing Test Points in 3.5 Peripheral Functions Characteristics
		p.95	Modification of 3.5.1 Serial array unit
		p.99, 100, 102, 103, 105, 109	Modification of Caution in 2.5.1 Serial array unit
		p.112 to 116	Modification of 3.6.1 (1) to (5)
		p.118	Renamed to 3.7 RAM Data Retention Characteristics, and modification of note and figure
		p.118	Addition of note 4 to 3.8 Flash Memory Programming Characteristics
		p.119	Modification of 3.10 Timing Specs for Switching Flash Memory Programming Modes
		p.120	Modification of 4.1 25-pin products
		p.123	Modification of 4.3 48-pin products

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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