APS11000 and APS11060





Vertical and Planar Hall-Effect Switches

FEATURES AND BENEFITS

- ASIL A functional safety compliance (pending confirmation)
- Planar and vertical Hall-effect sensor ICs
- 3.3 to 24 V operation
- Automotive-grade ruggedness and fault tolerance
 Extended AEC-Q100 qualification
 - □ Internal protection circuits enable 40 V load dump compliance
 - \square Reverse-battery protection
 - □ Output short-circuit and overvoltage protection
 - □ Operation from -40°C to 165°C junction temperature □ High EMC immunity
- Omnipolar and unipolar switch threshold options
- Choice of output polarity
- Open-drain output
- Solid-state reliability

PACKAGES

Not to scale



³⁻pin SOT23W (suffix LH)

DESCRIPTION

The APS11000 and APS11060 families of Hall-effect switches are AEC-Q100 qualified for 24 V automotive applications and compliant with ISO 26262:2011 ASIL A (pending confirmation). These sensors are temperature-stable and suited for operation over extended junction temperature ranges up to 165°C. The APS11000 and APS11060 families are available in several different magnetic sensitivities and polarities to offer flexible options for system design. They are available in active high and active low variants for ease of integration into electronic subsystems.

The APS11000 features a Hall-effect element that is sensitive to magnetic flux perpendicular to the face of the IC package. The APS11060 features a vertical Hall-effect sensing element sensitive to magnetic flux parallel to the face of the IC package.

Continued on next page ...

TYPICAL APPLICATIONS

- Gear shift selectors and driver controls (PRNDL)
- Human-machine interfaces (HMI) and driver controls
- Open/close sensor for LCD screens/doors/lids/trunks
- Clutch/brake position sensor
- Magnetically actuated lighting
- Wiper home/end position sensor
- End of travel and index sensors



Figure 1: Functional Block Diagram

³⁻pin SIP (suffix UA)

DESCRIPTION (continued)

The devices include on-board reverse-battery and overvoltage protection for operating directly from an automobile battery, as well as protection from shorts to ground by limiting the output current until the short is removed. The device is especially suited for operation from unregulated supplies. Two package styles provide a choice of through-hole or surface mounting. Package type LH is a modified 3-pin SOT23W surface mount package, while package type UA is a 3-pin ultra-mini SIP for through-hole mounting. Both packages are lead (Pb) free, with 100% matte-tin-plated leadframes.





SELECTION GUIDE

Part Number ^[1]	Packing ^[2]	Mounting	Output State for B > B _{OP}	Sensing Orientation	Operating Mode	
APS11000LLHALT-0SL	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	Low			
APS11000LLHALX-0SL	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	Low			
APS11000LUAA-0SL	Bulk, 500 pieces/bag	3-pin SIP through-hole	Low	Z-Axis	Unipolar	
APS11000LLHALT-0SH	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	High	Z-AXIS	South	
APS11000LLHALX-0SH	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	High			
APS11000LUAA-0SH	Bulk, 500 pieces/bag	3-pin SIP through-hole	High			
APS11000LLHALT-0PL	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	Low			
APS11000LLHALX-0PL	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	Low	Z-Axis	Omnipolar	
APS11000LUAA-0PL	Bulk, 500 pieces/bag	3-pin SIP through-hole Low				
APS11060LLHALT-0SL	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	Low	X-Axis		
APS11060LLHALX-0SL	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	Low	X-Axis		
APS11060LUAA-0SL	Bulk, 500 pieces/bag	3-pin SIP through-hole	Low	Y-Axis	Unipolar	
APS11060LLHALT-0SH	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	High	X-Axis	South	
APS11060LLHALX-0SH	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	High	X-Axis		
APS11060LUAA-0SH	Bulk, 500 pieces/bag	3-pin SIP through-hole	High	Y-Axis		
APS11060LLHALT-0PL	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	Low	X-Axis		
APS11060LLHALX-0PL	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	Low	X-Axis	Omnipolar	
APS11060LUAA-0PL	Bulk, 500 pieces/bag	3-pin SIP through-hole	Low	Y-Axis		

^[1] Contact Allegro MicroSystems for options not listed in the selection guide.

^[2] Contact Allegro MicroSystems for additional packing options.



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage ^[1]	V _{CC}		40	V
Reverse Supply Voltage [1]	V _{RCC}		-18	V
Output Voltage ^[1]	V _{OUT}		-0.3 to 32	V
Output Current [2]	I _{OUT}		40	mA
Reverse Output Current	I _{ROUT}		-50	mA
Magnetic Flux Density ^[3]	В		Unlimited	G
Operating Ambient Temperature	T _A	Range L	–40 to 150	°C
Maximum Junction Temperature	T _{J(max)}		165	°C
Storage Temperature	T _{stg}		–65 to 170	°C

^[1] This rating does not apply to extremely short voltage transients. Transient events such as Load Dump and/or ESD have individual, specific ratings. ^[2] Through short-circuit current limiting device.

[3] Guaranteed by design.

ESD PERFORMANCE^[4]

Characteristic	stic Symbol Notes		Rating	Units
ESD Voltage	V _{ESD(HBM)}	Human Body Model according to AEC-Q100-002	±11	kV
ESD Voltage	V _{ESD(CDM)}	Charged Device Model according to AEC-Q100-011	±1	kV

^[4] ESD ratings provided are based on qualification per AEC-Q100 as an expected level of ESD robustness.



PINOUT DIAGRAMS AND TERMINAL LIST

(View from branded face)



Terminal List

Name	Description	Number		
Name	Description	LH	UA	
VCC	Connects power supply to chip	1	1	
VOUT	Output from circuit	2	3	
GND	Terminal for ground connection 3		2	



APS11000 and APS11060

Vertical and Planar Hall-Effect Switches

ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_{J(max)}$ and

 $C_{BVP} = 0.1 \,\mu$ F, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. ^[1]	Max.	Unit
SUPPLY AND STARTUP	·			· · · · · · · · · · · · · · · · · · ·		
Supply Voltage	V _{CC}		3.3	_	24	V
Summer Current		APS11000	1	2.2	4	mA
Supply Current	I _{CC}	APS11060	1	2.5	5	mA
Power-On Time ^[2]	t _{PO}	$V_{CC} \ge V_{CC}(min)$	-	180	350	μs
Power-On State ^[5]	POS	$V_{CC} \ge V_{CC}(min), t < t_{PO}$		High		_
Linderveltage Leekeut [3]	V _{CC(UV)EN}	$V_{CC} \ge V_{CC}(min) \rightarrow V_{CC} < V_{CC}(min)$	_	2	-	V
Undervoltage Lockout [3]	V _{CC(UV)DIS}	$V_{CC} < V_{CC}(min) \rightarrow V_{CC} \ge V_{CC}(min)$	_	2.3	-	V
UVLO Reset Time ^[3]	t _{POR}		_	100	_	μs
CHOPPER STABILIZATION AND OUT	PUT MOSF	ET CHARACTERISTICS		^^		
Chopping Frequency	f _C		-	800	-	kHz
Output Leakage Current ^[4]	IOUTOFF	$V_{OUT(OFF)}$ = 12 V, T _A = -40°C to 85°C, output off, V _{CC} ≥ V _{CC(min)} , t > t _{PO}	_	-	0.1	μA
Output Leakage Current	IOUTOFF	$V_{OUT(OFF)}$ = 24 V, output off, $V_{CC} \ge V_{CC(min)}$, t > t _{PO}	_	-	1	μA
Output Leakage Current, Power-On [4][5]	I _{OUTOFF(PO)}	$V_{CC} \ge V_{CC(min)}, t < t_{PO}$	_	-	95	μA
Output Saturation Voltage	V _{OUT(SAT)}	Output on, I _{OUT} = 5 mA	_	100	500	mV
Output Off Voltage	V _{OUT(OFF)}		-	-	24	V
Output Rise Time [6][7]	t _r	C_L = 20 pF, $R_{PULL-UP}$ = 4.8 k Ω	-	0.2	2	μs
Output Fall Time ^{[6][7]}	t _f	C _L = 20 pF, R _{PULL-UP} = 4.8 kΩ	_	0.1	2	μs
ON-BOARD PROTECTION		· · · · · ·				
Output Short-Circuit Current Limit	I _{OM}	Output on	15	_	40	mA
Output Zener Clamp Voltage	V _{Z(OUT)}	I _{OUT} = 1.5 mA, T _A = 25°C	32	_	_	V
Supply Zener Clamp Voltage	Vz	$I_{CC} = I_{CC}(max) + 3 \text{ mA}, T_A = 25^{\circ}C$	40	-	-	V
Reverse Battery Zener Clamp Voltage	V _{RZ}	$I_{CC} = -5 \text{ mA}, T_A = 25^{\circ}\text{C}$	_	-	-18	V
Reverse Battery Current	I _{RCC}	V _{CC} = -18 V, T _A = 25°C	-5	_	_	mA

^[1] Typical data is at $T_A = 25^{\circ}C$ and $V_{CC} = 12 V$ unless otherwise noted. ^[2] Measured from $V_{CC} \ge 3.3 V$ to valid output. ^[3] See Undervoltage Lockout section for operational characteristics.

^[4] Guaranteed by device design and characterization.

^[5] See Power-On Behavior section and Figure 4.

^[6] C_L = oscilloscope probe capacitance.

[7] See Figure 2 - Definition of Output Rise and Fall Time.



Figure 2: Definition of Output Rise and Fall Time



APS11000 and APS11060

Vertical and Planar Hall-Effect Switches

MAGNETIC CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_{J(max)}$ and

 $C_{BYP} = 0.1 \ \mu F$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Тур. [1]	Max.	Unit ^[2]
-0Px OPTION						
Operate Baint	B _{OPS}	-0Px Option	-	35	70	G
Operate Point	B _{OPN}	-0Px Option	-70	-35	_	G
Release Point	B _{RPS}	-0Px Option	5	25	_	G
	B _{RPN}	-0Px Option	-	-25	-5	G
Hysteresis	B _{HYS}	-0Px Option	5	15	25	G
-0Sx OPTION	·		·			
Operate Point	B _{OPS}	-0Sx Option	-	35	70	G
Release Point	B _{RPS}	-0Sx Option	5	25	_	G
Hysteresis	B _{HYS}	-0Sx Option	5	15	25	G
-0Nx OPTION	, , , , , , , , , , , , , , , , , , ,		, ,			
Operate Point	B _{OPN}	-0Nx Option	-70	-35	_	G
Release Point	B _{RPN}	-0Nx Option	-	-25	-5	G
Hysteresis	B _{HYS}	-0Nx Option	5	15	25	G

^[1] Typical data are at $T_A = 25^{\circ}$ C and $V_{CC} = 12$ V unless otherwise noted. ^[2] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and a positive value for south-polarity magnetic fields.



Figure 3: Hall Switch Output State vs. Magnetic Field

B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.



APS11000 and APS11060

Vertical and Planar Hall-Effect Switches

MAGNETIC CHARACTERISTICS (continued): Valid over full operating voltage and ambient temperature ranges for T_J < T_{J(max)}

and $C_{PVP} = 0.1 \ \mu F$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. ^[1]	Max.	Unit ^[2]
-1Px OPTION ^[3]		·				<u>.</u>
Or events Delint	B _{OPS}	-1Px Option	50	95	135	G
Operate Point	B _{OPN}	-1Px Option	-135	-95	-50	G
Deleges Deint	B _{RPS}	-1Px Option	40	70	110	G
Release Point	B _{RPN}	-1Px Option	-110	-70	-40	G
Hysteresis	B _{HYS}	-1Px Option	10	25	42	G
-1Sx OPTION ^[3]		·	· ·			
Operate Point	B _{OPS}	-1Sx Option	50	95	135	G
Release Point	B _{RPS}	-1Sx Option	40	70	110	G
Hysteresis	B _{HYS}	-1Sx Option	10	25	42	G
-1Nx OPTION [3]			, , , , , , , , , , , , , , , , , , ,		~	
Operate Point	B _{OPN}	-1Nx Option	-135	-95	-50	G
Release Point	B _{RPN}	-1Nx Option	-110	-70	-40	G
Hysteresis	B _{HYS}	-1Nx Option	10	25	42	G
-2Px OPTION ^[3]						·
	B _{OPS}	-2Px Option	120	150	200	G
Operate Point	B _{OPN}	-2Px Option	-200	-150	-120	G
Delesse Delet	B _{RPS}	-2Px Option	110	125	190	G
Release Point	B _{RPN}	-2Px Option	-190	-125	-110	G
Hysteresis	B _{HYS}	-2Px Option	10	25	42	G
-2Sx OPTION ^[3]		·	· ·			
Operate Point	B _{OPS}	-2Sx Option	120	150	200	G
Release Point	B _{RPS}	-2Sx Option	110	125	190	G
Hysteresis	B _{HYS}	-2Sx Option	10	25	42	G
-2Nx OPTION [3]		•	,			
Operate Point	B _{OPN}	-2Nx Option	-200	-150	-120	G
Release Point	B _{RPN}	-2Nx Option	-190	-125	-110	G
Hysteresis	B _{HYS}	-2Nx Option	10	25	42	G

^[1] Typical data are at $T_A = 25^{\circ}$ C and $V_{CC} = 12$ V unless otherwise noted. ^[2] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and a positive value for south-polarity magnetic fields. ^[3] Contact Allegro MicroSystems for availability.



APS11000 and APS11060

Vertical and Planar Hall-Effect Switches

PACKAGE THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information.

Characteristic	Symbol	Test Conditions	Value	Units
		Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 2-layer PCB with 0.463 in ² of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

2543221098765432 222221918765432 V_{CC(max)} Package LH, 2-layer PCB (R_{8JA} = 110°C/W) Maximum Allowable V_{cc} (V) Package UA, 1-lay (R_{8JA} = 165°C/W) РСВ Package LH, 1-layer PCB (R_{BJA} = 228°C/W) $V_{CC(min)}$ 45 65 85 105 125 145 165 185 25 T_J(max) Temperature (°C)

Power Derating Curve $T_{J(max)} = 165^{\circ}C; I_{CC} = I_{CC(max)}, I_{OUT} = 0 \text{ mA (Output Off)}$







CHARACTERISTIC PERFORMANCE DATA **Electrical Characteristics**





(Output Off) 5 V_{CC} (V) 4.5 APS11000 4 3.3 3.5 22222222222 I_{cc} (mA) 12 3 2.5 - 24 2 APS11060 1.5 --- 3.3 1 --- 12 0.5 **---** 24 0 -60 -40 -20 0 20 40 60 80 100 120 140 160 Т_А (°С)



Supply Current versus Ambient Temperature



CHARACTERISTIC PERFORMANCE DATA Magnetic Characteristics















FUNCTIONAL DESCRIPTION

Power-On Behavior

Device power-on begins when the supply voltage reaches $V_{CC}(min)$. During the power-on time, t_{PO} , the device output is off with the exception of the leakage current, I_{OUTOFF(PO)}. Use of a large pull-up resistor, R_{PULL-UP} (see Figure 6), can influence the Power-On State (POS) voltage level on the output pin during t_{ON}. The output voltage level during the POS is a function of the pullup resistor and pull-up voltage. The level can be determined by subtracting the voltage drop created by R_{PULL-UP} and I_{OUTOFF(PO)} from the pull-up voltage. To retain a power-on output voltage level above V_{PULL-UP}/2, a pull-up resistor less than or equal to 20 k Ω is recommended. After power-on is complete and the power-on time has elapsed, the device output will correspond with the applied magnetic field for $B > B_{OP}$ and $B < B_{RP}$. Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will cause the device output to remain off. A valid output state is attained after the first excursion beyond B_{OP} or B_{RP}.

Undervoltage Lockout Operation

The APS11000 and APS11060 have an internal diagnostic to check the voltage supply (an undervoltage lockout regulator). When the supply voltage falls below the undervoltage lockout voltage threshold, $V_{CC(UV)EN}$, the device enters reset, where the output state returns to the Power-On State (POS) until V_{CC} is increased to $V_{CC(UV)DIS}$. Once the $V_{CC(UV)DIS}$ threshold is reached, the power-on sequence begins and the output will correspond with the applied magnetic field for $B > B_{OP}$ and $B < B_{RP}$ after t_{POR} has elapsed. In the case the supply voltage does not return to these operational levels, or if the applied magnetic field is within the hysteresis range, the output will remain in the power-on state. See Figure 4 for an example of the undervoltage lockout behavior.



Figure 4: Power-On and Undervoltage Lockout Behavior



Functional Safety



The APS11000 and APS11060 were designed accordance with the international standard for automotive functional safety, ISO 26262:2011.

These products achieve an ASIL (Automotive Safety Integrity Level) rating of ASIL A (pending confirmation) according to the standard. The APS11000 and APS11060 are both classified as a SEooC (Safety Element out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. For further information, contact your local FAE for A²-SILTM documentation: www.allegromicro.com/ASIL.

Operation

The APS11000 and APS11060 are integrated Hall-effect sensor ICs with an open-drain output. Table 1 offers a guide for selecting the output polarity configuration, further explained in the configuration sections below. The open-drain output is an NMOS transistor that actuates in response to a magnetic field. The direction of the applied magnetic field is perpendicular to the branded face for the APS11000, and parallel with the branded face for the APS11060; see Figure 5 for an illustration. The devices are offered in two packages: the UA package, a 3-pin through-hole mounting configuration, or in the LH package, a 3-pin surface-mount configuration. See the Selection Guide for a complete list of available options.

Configurations xSL and xSH. The unipolar output of these devices is actuated when a south-polarity magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OPS} . When B_{OPS} is exceeded, the xSL output turns on (goes low). The xSH is complementary, in that for this device the output turns off (goes high) when B_{OPS} is exceeded. When the magnetic field is removed or reduced below the release point, B_{RPS} , the device outputs return to their original state—off for the xSL and on for the xSH. See Figure 3 for unipolar south switching behavior.

Configurations xNL and xNH. The unipolar output of these devices is actuated when a north-polarity magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OPN} . When B_{OPN} is exceeded, the xNL output turns on (goes low). The xNH is complementary, in that for this device the output turns off (goes high) when B_{OPN} is exceeded. When the magnetic field is removed or reduced below the release point, B_{RPN} , the device outputs return to their original state—off for the xNL and on for the xNH. See Figure 3 for unipolar north switching behavior.

Part Number Suffix	Operating Mode	Output State for B > B _{OP}	Output State for B = 0 G	Power-On State, t < t _{PO}
xSL	Unipolar South	Low	High	High
xSH	Unipolar South	High	Low	High
XNL	Unipolar North	Low	High	High
xNH	Unipolar North	High	Low	High
xPL	Omnipolar	Low	High	High
xPH	Omnipolar	High	Low	High

Table 1: Switch Polarity Configuration Options

Configurations xPL and xPH. The omnipolar operation of these devices allows actuation with either a north or a south polarity field. The xPL operates using the standard output polarity convention. Fields exceeding the operating points, B_{OPS} or B_{OPN} , will turn the output on (low). When the magnetic field is removed or reduced below the release point, B_{RPN} or B_{RPS} , the device output turns off (goes high). The xPH is complementary, in that for the device, a north or south polarity field exceeding the operate points, B_{OPS} or B_{OPN} , will turn the output off (high). Removal of the field, or reduction below the release point threshold, B_{RPS} or B_{RPN} , will turn the output on (low). See Figure 3 for omnipolar switching behavior.

After turn-on, the output transistor is capable of sinking current up to the short circuit current limit, I_{OM} , which is a minimum of 15 mA. The difference in the magnetic operate and release points is the hysteresis, B_{HYS} , of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.



Figure 5: Magnetic Sensing Orientations APS11000 LH (Panel A), APS11000 UA (Panel B), APS11060 LH (Panel C), and APS11060 UA (Panel D)



Applications

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to guarantee correct performance under harsh environmental conditions and to reduce noise from internal circuitry. As is shown in Figure 6: Typical and Enhanced Protection Application Circuits, a 0.1 μ F capacitor is required.

In applications where the APS11000 or APS11060 receives its power from an unregulated source such as a car battery, or where greater immunity is required, additional measures may be employed. Specifications for such transients will vary, so protection circuit design should be optimized for each application. For example, the circuit shown in Figure 6 includes an optional series resistor and output capacitor which improves performance during Powered ESD testing (ISO 10605) and Bulk Current Injection testing (ISO 11452-4).

Typical Applications Circuit



Enhanced Protection Circuit



Figure 6: Typical and Enhanced Protection Application Circuits

Recommended $R_{PULL-UP} \le 20 \text{ k}\Omega$. See Power-On Behavior section. Extensive applications information for Hall-effect devices is available in:

- Hall-Effect IC Applications Guide, AN27701,
- Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices AN27703.1
- Soldering Methods for Allegro's Products SMD and Through-Hole, AN26009

All are provided on the Allegro website:

www.allegromicro.com

Vertical Hall-Effect Sensor Linear Tools

System design and magnetic sensor evaluation often require an in-depth look at the overall strength and profile generated by a magnetic field input. To aid in this evaluation, Allegro MicroSystems, LLC provides a high-accuracy linear output tool capable of reporting the nonperpendicular magnetic field by means of an vertical Hall-effect sensor IC equipped with a calibrated analog output. For further information, contact your local Allegro field applications engineer or sales representative.



APS11000 and APS11060

Vertical and Planar Hall-Effect Switches

CHOPPER STABILIZATION

A limiting factor for switchpoint accuracy when using Hall-effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 7: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation) illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro's innovative chopper-stabilization technique uses a high-frequency clock.

The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS11000 and APS11060 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.



Figure 7: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)



POWER DERATING

The device must be operated below the maximum junction temperature, $T_{J(max)}$. Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance, $R_{\theta JA}$ (junction to ambient), is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. $R_{\theta JA}$ is dominated by the Effective Thermal Conductivity, K, of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A , and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions:

$$P_D = V_{IN} \times I_{IN} (1)$$
$$\Delta T = P_D \times R_{\theta JA} (2)$$
$$T_J = T_A + \Delta T (3)$$

Determining Junction Temperature

For example, given common conditions: $T_A = 25^{\circ}C$, $V_{CC} = 12 \text{ V}$, $I_{CC} = 2.5 \text{ mA}$, $V_{OUT(SAT)} = 100 \text{ mV}$, $I_{OUT} = 5 \text{ mA}$, and $R_{\theta JA} = 165^{\circ}C/W$, then:

$$\begin{split} P_D &= (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OUT}) = \\ &(12 \ V \times 2.5 \ mA) + (100 \ mV \times 5 \ mA) = \\ &30 \ mW + 0.5 \ mW = 30.5 \ mW \\ &\Delta T = P_D \times R_{\theta JA} = 30.5 \ mW \times 165^{\circ} C/W = 5^{\circ} C \\ &T_J = T_A + \Delta T = 25^{\circ} C + 5^{\circ} C = 30^{\circ} C \end{split}$$

Determining Maximum V_{CC}

For a given ambient temperature (T_A), the maximum allowable power dissipation as a function of V_{CC} can be calculated. P_{D(max)}, represents the maximum allowable power level without exceeding T_{J(max)}, at a selected R_{0JA} and T_A.

Example: V_{CC} estimation using the conditions $R_{\theta JA} = 228$ °C/W, $T_{A(max)} = 150$ °C, $T_{J(max)} = 165$ °C, $V_{CC(max)} = 24$ V, $I_{CC(max)} = 5$ mA, $V_{OUT} = 500$ mV, and $I_{OUT} = 20$ mA (output on), calculate the maximum allowable power level, $P_D(max)$, first using equation 3:

$$\Delta T_{(max)} = T_{J(max)} - T_A = 165^{\circ}C - 150^{\circ}C = 15^{\circ}C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, using equation 2 first for the output as shown below:

$$P_{D(VOUT)} = V_{OUT} \times I_{OUT} = 500 \text{ mV} \times 20 \text{ mA} = 10 \text{ mW}$$

Then, for the V_{CC} supply:

$$P_{D(VCC)} = V_{CC} \times I_{CC} = 24 \ V \times 5 \ mA = 120 \ mW$$

Combine the power dissipated by the device pins:

$$P_{D(total)} = (P_{D(VOUT)} + P_{D(VCC)})$$

$$P_{D(total)} = (10 \text{ mW} + 120 \text{ mW}) = 130 \text{ mW}$$

Next, solve for the maximum allowable $\rm V_{\rm CC}$ for the given conditions using equation 1:

$$V_{CC(est)} = P_{D(total)} \div (I_{CC} + I_{OUT})$$

$$I30 mW \div (5 mA + 20 mA)$$

$$V_{CC(est)} = I30 mW \div 25 mA = 5.2 V$$

The result indicates that, at T_A , the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

If the application requires $V_{CC} > V_{CC(est)}$ then $R_{\theta JA}$ must by improved. This can be accomplished by adjusting the layout, PCB materials, or by controlling the ambient temperature.

Determining Maximum T_A

In cases where the $V_{CC(max)}$ level is known, and the system designer would like to determine the maximum allowable ambient temperature, $T_{A(max)}$, the calculations can be reversed.

For example, in a worst-case scenario with conditions $V_{CC(max)} = 24 \text{ V}$, $I_{CC(max)} = 5 \text{ mA}$, $V_{OUT} = 500 \text{ mV}$, $I_{OUT(max)} = 15 \text{ mA}$, and $R_{0JA} = 228^{\circ}\text{C/W}$, for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = P_{D(VOUT)} + P_{D(VCC)} = 500 \text{ mV} \times 15 \text{ mA} + 24 \text{ V} \times 5 \text{ mA}$$

$$P_D = 7.5 \text{ mW} + 120 \text{ mW} = 127.5 \text{ mW}$$

Then, by rearranging equation 3:

$$T_{A(max)} = T_{J(max)} - \Delta T$$

$$T_{A(max)} = 165^{\circ}C - (127.5 \text{ mW} \times 228^{\circ}C/W)$$

$$T_{A(max)} = 165^{\circ}C - 29.1^{\circ}C = 135.9^{\circ}C$$

Finally, note that the $T_{A(max)}$ rating of the device is 150°C and performance is not guaranteed above this temperature for any power level.



Package LH, 3-Pin SMD (SOT23W) APS11000



Reference land pattern layout All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

- Branding scale and appearance at supplier discretion
- A Hall element, not to scale



Package LH, 3-Pin SMD (SOT23W) APS11060



All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

- Branding scale and appearance at supplier discretion
- A Hall element, not to scale



Package UA, 3-Pin SIP APS11000





Package UA, 3-Pin SIP APS11060





Revision History

Number	Date	Description
_	March 15, 2018	Initial release
1	July 16, 2018	Added APS11000 part option; updated Magnetic Characteristics tables; other minor editorial updates
2	October 22, 2018	Updated T _{J(max)} to 165°C, Selection Guide (page 3), Absolute Maximum Ratings footnotes (page 4), Power- On State (page 6), Magnetic Characteristics table (page 8), Package Thermal Characteristics (page 9), Magnetic Characteristic Performance chart labels (page 11), and Power Derating section (page 16).
3	February 7, 2020	Minor editorial updates
4	May 12, 2020	Added "(pending confirmation)" to ASIL references.

Copyright 2020, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website: www.allegromicro.com

